MOS INTEGRATED CIRCUIT

μPD754144, 754244

4-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD754244 is a 4-bit single-chip microcontroller which incorporates the EEPROM™ for key-less entry application.

It incorporates a 16 × 8-bit EEPROM, a 4-Kbyte mask ROM to store software, a 128 × 4-bit RAM to store the processing data, a processing CPU, and a carrier generator which easily outputs waveforms for infrared remote controller.

The details of functions are described in the following user's manual. Be sure to read it before designing.

μPD754144, 754244 User's Manual: U10676E

FEATURES

- On-chip EEPROM: 16 × 8 bits (mapped to the data memory)
- On-chip key return reset function for key-less entry
- System clock oscillation circuit
  - μPD754144: RC oscillator (external resistor and capacitor)
  - μPD754244: Crystal/ceramic oscillator
- Low-voltage operation: V_{DD} = 1.8 to 6.0 V
- Timer function (4 channels)
  - Basic interval timer/watchdog timer: 1 channel
  - 8-bit timer counter : 3 channels
- On-chip memory
  - Program memory (ROM)
    4096 × 8 bits
  - Data memory (static RAM)
    128 × 4 bits
- Instruction execution time variable function suited for power saving.
  - μPD754144:
    4, 8, 16, 64 μs (at f_{CC} = 1.0-MHz operation)
  - μPD754244:
    0.95, 1.91, 3.81, 15.3 μs (at f_X = 4.19-MHz operation)
    0.67, 1.33, 2.67, 10.7 μs (at f_X = 6.0-MHz operation)

APPLICATIONS

Automotive appliances such as key-less entry, compact data carrier, etc.

Unless contextually excluded, references in this data sheet to the μPD754244 (crystal/ceramic oscillation: f_X) mean the μPD754144.

The μPD754144 and μPD754244 differ in the notation of their RC oscillation: whenever f_X (RC oscillation notation for μPD754244) is described, f_{CC} should be substituted for the μPD754144.

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Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD754144GS-xxx-BA5	20-pin plastic SOP (300 mil, 1.27-mm pitch)
μPD754144GS-xxx-GJG	20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)
μPD754244GS-xxx-BA5	20-pin plastic SOP (300 mil, 1.27-mm pitch)
μPD754244GS-xxx-GJG	20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)

Remark xxx indicates ROM code suffix.

Functional Outline

<table>
<tr><th colspan="2">Parameter</th><th colspan="2">μPD754144</th><th>μPD754244</th></tr>
<tr><td colspan="2">Instruction execution time</td><td colspan="2">• 4, 8, 16, 64 μs
(at fcc = 1.0-MHz operation)</td><td>• 0.95, 1.91, 3.81, 15.3 μs
(at fx = 4.19-MHz operation)
• 0.67, 1.33, 2.67, 10.7 μs
(at fx = 6.0-MHz operation)</td></tr>
<tr><td rowspan="3">On-chip memory</td><td>Mask ROM</td><td colspan="3">4096 × 8 bits (0000H-0FFFH)</td></tr>
<tr><td>RAM</td><td colspan="3">128 × 4 bits (000H-07FH)</td></tr>
<tr><td>EEPROM</td><td colspan="3">16 × 8 bits (400H-41FH)</td></tr>
<tr><td colspan="2">System clock oscillator</td><td colspan="2">RC oscillator
(External resistor and capacitor)</td><td>Crystal/ceramic oscillator</td></tr>
<tr><td colspan="2">General-purpose register</td><td colspan="3">• 4-bit operation: 8 × 4 banks
• 8-bit operation: 4 × 4 banks</td></tr>
<tr><td rowspan="3">Input/output port</td><td>CMOS input</td><td>4</td><td colspan="2">On-chip pull-up resistor can be specified by mask option.</td></tr>
<tr><td>CMOS input/output</td><td>9</td><td colspan="2">On-chip pull-up resistor connection can be specified by means of software.</td></tr>
<tr><td>Total</td><td colspan="3">13</td></tr>
<tr><td colspan="2">Start-up time after reset</td><td colspan="2">56/fcc</td><td>2¹⁷/fx, 2¹⁵/fx (selected by mask option)</td></tr>
<tr><td colspan="2">Stand-by mode release time</td><td colspan="2">2⁹/fcc</td><td>2²⁰/fx, 2¹⁷/fx, 2¹⁵/fx, 2¹³/fx
(selected by the setting of BTM)</td></tr>
<tr><td colspan="2">Timer</td><td colspan="3">4 channels
• 8-bit timer counter
(can be used as 16-bit timer counter) : 3 channels
• Basic interval/watchdog timer : 1 channel</td></tr>
<tr><td colspan="2">Bit sequential buffer</td><td colspan="3">16 bits</td></tr>
<tr><td colspan="2">Vectored interrupt</td><td colspan="3">External: 1, Internal: 5</td></tr>
<tr><td colspan="2">Test input</td><td colspan="3">External: 1 (key return reset function available)</td></tr>
<tr><td colspan="2">Standby function</td><td colspan="3">STOP/HALT mode</td></tr>
<tr><td colspan="2">Operating ambient temperature</td><td colspan="3">TA = –40 to +85 °C</td></tr>
<tr><td colspan="2">Operating supply voltage</td><td colspan="3">VDD = 1.8 to 6.0 V</td></tr>
<tr><td colspan="2">Package</td><td colspan="3">• 20-pin plastic SOP (300 mil, 1.27-mm pitch)
• 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)</td></tr>
</table>

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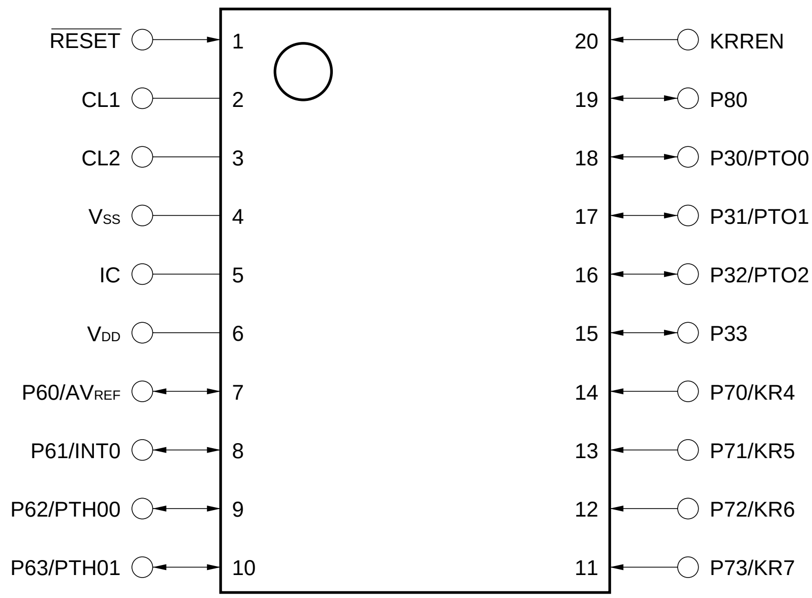
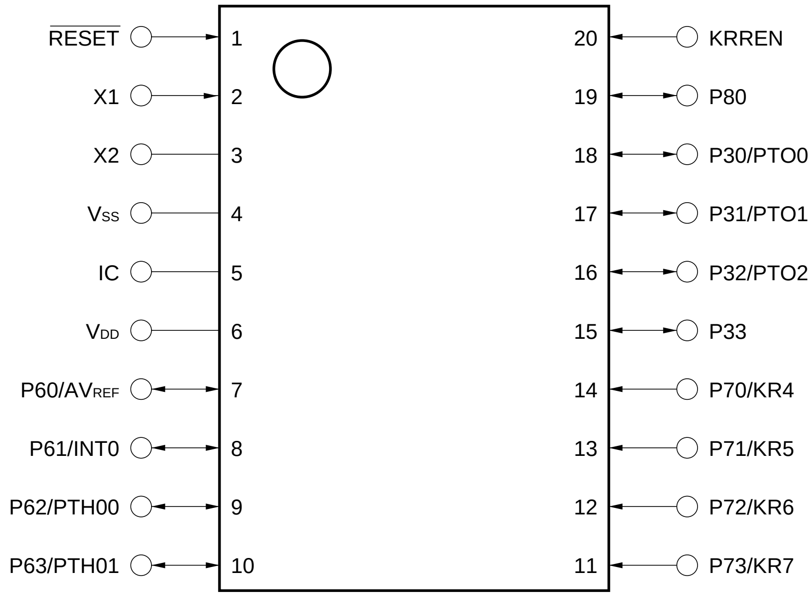
1. PIN CONFIGURATION (TOP VIEW)

- μPD754144
  - 20-pin Plastic SOP (300 mil, 1.27-mm pitch)
    μPD754144GS-×××-BA5
  - 20-pin Plastic Shrink SOP (300 mil, 0.65-mm pitch)
    μPD754144GS-×××-GJG



IC: Internally Connected (Connect to V_{DD} directly)

- μPD754244
  - 20-pin Plastic SOP (300 mil, 1.27-mm pitch)
    μPD754244GS-×××-BA5
  - 20-pin Plastic Shrink SOP (300 mil, 0.65-mm pitch)
    μPD754244GS-×××-GJG

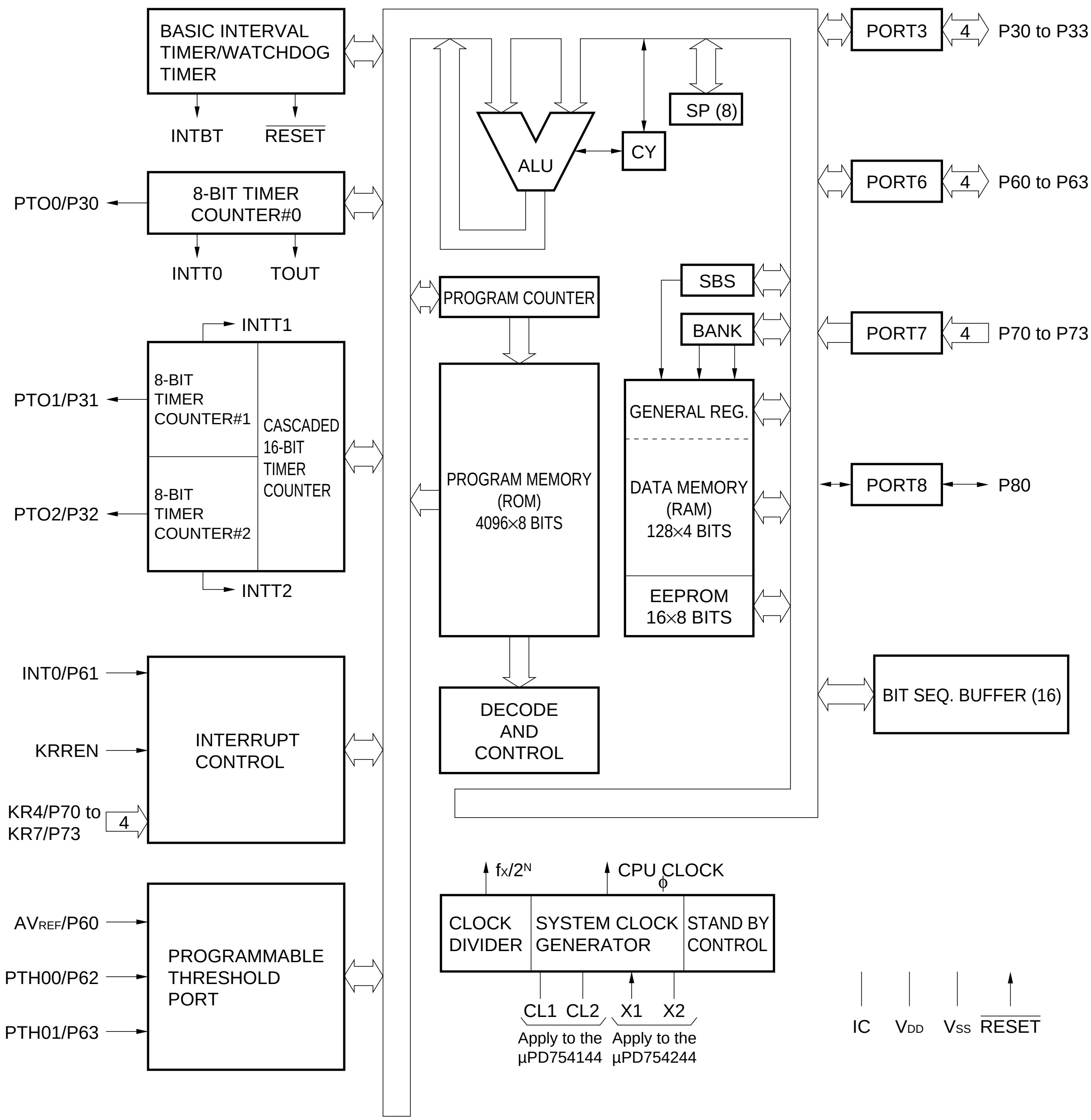


IC: Internally Connected (Connect to V_{DD} directly)

Pin Identification

AV_{REF}	: Analog reference	P70 to P73	: Port 7
CL1 and CL2	: System clock (RC)	P80	: Port 8
IC	: Internally connected	PTH00 and PTH01	: Programmable threshold port analog inputs 0 and 1
INT0	: External vectored interrupt 0	PTO0 to PTO2	: Programmable timer outputs 0 to 2
KR4 to KR7	: Key returns 4 to 7	$\overline{\text{RESET}}$	: Reset
KRREN	: Key return reset enable	V_{DD}	: Positive power supply
P30 to P33	: Port 3	V_{SS}	: Ground
P60 to P63	: Port 6	X1 and X2	: System clock (crystal/ceramic)

2. BLOCK DIAGRAM



3. PIN FUNCTION

3.1 Port Pins

Pin Name	Input/Output	Alternate Function	Function	8-bit I/O	After Reset	I/O Circuit TYPE Note 1
P30	Input/Output	PTO0	Programmable 4-bit input/output port (PORT3). This port can be specified input/output bit-wise. On-chip pull-up resistor connection can be specified by software in 4-bit units.	–	Input	E-B
P31		PTO1				
P32		PTO2				
P33		–				
P60	Input/Output	AV_{REF}	Programmable 4-bit input/output port (PORT6). This port can be specified input/output bit-wise. On-chip pull-up resistor can be specified by software in 4-bit units Note2. Noise eliminator can be selected with P61/INT0.	–	Input	F-A
P61		INT0				
P62		PTH00				
P63		PTH01				
P70	Input	KR4	4-bit input port (PORT7). On-chip pull-up resistor can be specified by software bit-wise.	–	Input	B-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	Input/Output	–	1-bit input/output port (PORT8). On-chip pull-up resistor connection can be specified by software.	–	Input	F-A

Notes 1. Circled characters indicate the Schmitt-trigger input.

2. Do not specify an on-chip pull-up resistor connection when using the programmable threshold port.

3.2 Non-port Pins

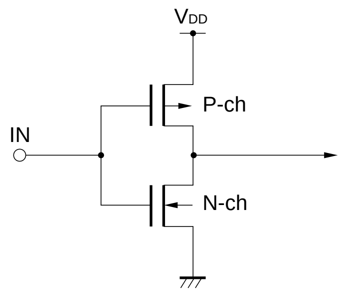
Pin Name	Input/Output	Alternate Function	Function		After Reset	I/O Circuit TYPE[Note]
PTO0	Output	P30	Timer counter output pins		Input	E-B
PTO1		P31				
PTO2		P32				
INT0	Input	P61	Edge detection vectored interrupt input pin (detected edge can be selected) Noise elimination circuit can be selected.	Noise elimination circuit can be selected. Asynchronous input	Input	F-A
KR4 to KR7	Input	P70 to P73	Falling edge detection testable input pins		Input	B-A
PTH00	Input	P62	Threshold voltage-variable 2-bit analog input pins		Input	F-A
PTH01		P63				
KRREN	Input	–	Key return reset enable pin The reset signal is generated at the falling edge of KRn while KRREN is high in STOP mode.		Input	B
AV_{REF}	Input	P60	Reference voltage input pin		Input	F-A
CL1	–	–	Incorporated in the μPD754144 only RC (for system clock oscillation) connection pin External clock cannot be input.		–	–
CL2	–					
X1	Input	–	Incorporated in the μPD754244 only Crystal/ceramic resonator (for system clock oscillation) connection pin When inputting the external clock, input the external clock to pin X1 and input the inverted phase of the external clock to pin X2.		–	–
X2	–					
$\overline{\text{RESET}}$	Input	–	System reset input pin (low-level active) Pull-up resistor can be incorporated (mask option).		–	B-A
IC	–	–	Internally Connected Connect directly to V_{DD}.		–	–
V_{DD}	–	–	Positive supply pin		–	–
V_{SS}	–	–	Ground potential		–	–

Note Circled characters indicate the Schmitt-trigger input.

3.3 Pin Input/Output Circuits

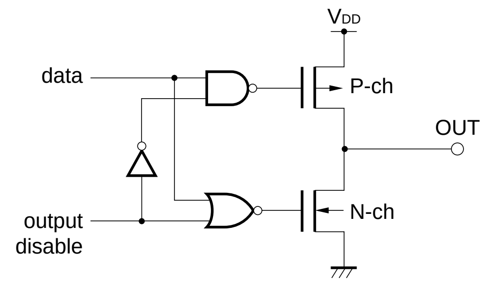
The μPD754244 pin input/output circuits are shown schematically.

TYPE A



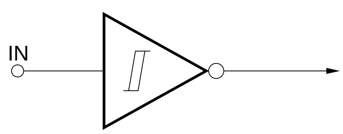
CMOS specification input buffer.

TYPE D



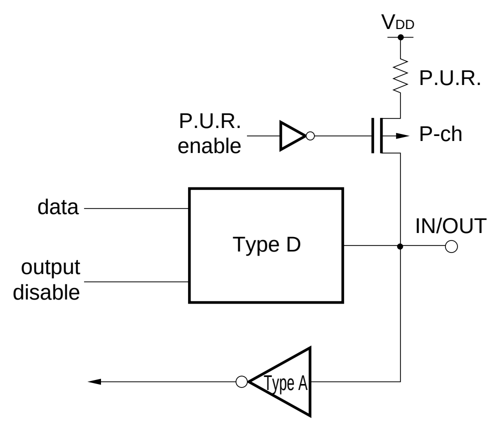
Push-pull output that can be placed in output high-impedance (both P-ch, N-ch off).

TYPE B



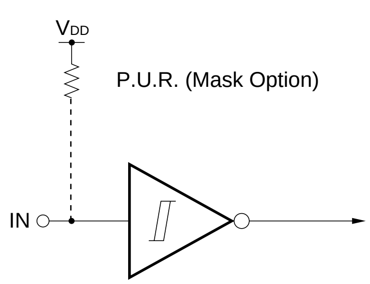
Schmitt-trigger input having hysteresis characteristic.

TYPE E-B



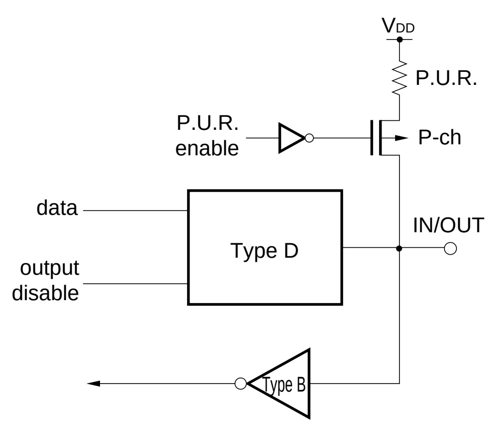
P.U.R. : Pull-Up Resistor

TYPE B-A



P.U.R. : Pull-Up Resistor

TYPE F-A



P.U.R. : Pull-Up Resistor

3.4 Recommended Connection of Unused Pins

Table 3-1. List of Recommended Connection of Unused Pins

Pin	Recommended Connecting Method
P30/PTO0	Input state : Independently connect to V_{SS} or V_{DD} via a resistor. Output state: Leave open.
P31/PTO1	
P32/PTO2	
P33	
P60/AV_{REF}	
P61/INT0	
P62/PTH00	
P63/PTH01	
P70/KR4	Connect to V_{DD}.
P71/KR5	
P72/KR6	
P73/KR7	
P80	Input state : Independently connect to V_{SS} or V_{DD} via a resistor. Output state: Leave open.
KRREN	When this pin is connected to V_{DD}, internal reset signal is generated at the falling edge of the KRn pin in the STOP mode. When this pin is connected to V_{SS}, internal reset signal is not generated even if the falling edge of KRn pin is detected in the STOP mode.
IC	Connect directly to V_{DD}.

4. SWITCHING FUNCTION BETWEEN MK I MODE AND MK II MODE

4.1 Difference between Mk I and Mk II Modes

The μPD754244 75XL CPU has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by the bit 3 of the Stack Bank Select register (SBS).

- Mk I mode: Instructions are compatible with the 75X series. Can be used in the 75XL CPU with a ROM capacity of up to 16 Kbytes.
- Mk II mode: Incompatible with 75X series. Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16 Kbytes.

Table 4-1. Differences between Mk I Mode and Mk II Mode

	Mk I Mode	Mk II Mode
Number of stack bytes for subroutine instructions	2 bytes	3 bytes
BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
CALL !addr instruction	3 machine cycles	4 machine cycles
CALLF !faddr instruction	2 machine cycles	3 machine cycles

Caution The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 Kbytes.

With regard to the number of stack bytes during execution of subroutine call instructions, the usable area increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected.

However, when the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.

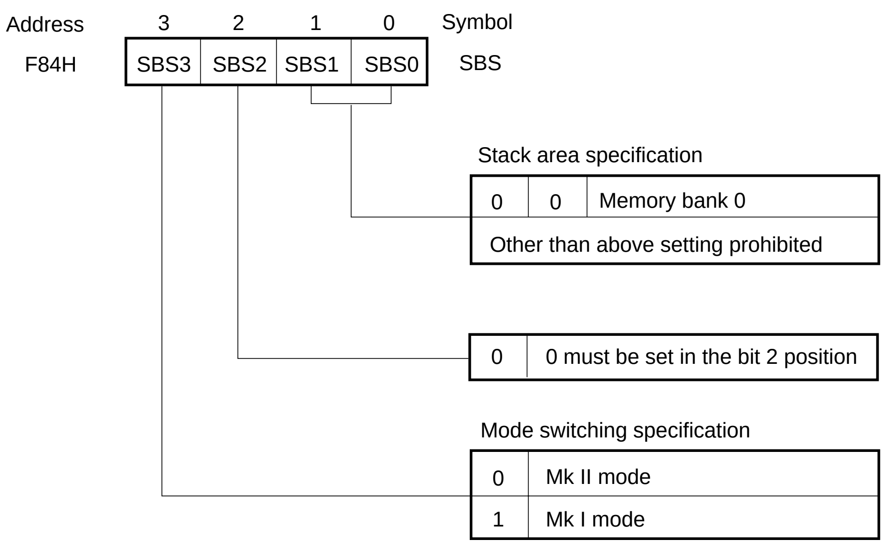
4.2 Setting Method of Stack Bank Select Register (SBS)

Switching between the Mk I mode and Mk II mode can be done by the SBS. Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction.

When using the Mk I mode, the SBS must be initialized to 1000B at the beginning of a program. When using the Mk II mode, it must be initialized to 0000B.

Figure 4-1. Stack Bank Select Register Format



Caution Because SBS. 3 is set to "1" after a $\overline{\text{RESET}}$ signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to "0" to select the Mk II mode.

5. MEMORY CONFIGURATION

- **Program memory (ROM)** ··· 4096 x 8 bits
  - Addresses 0000H and 0001H
    Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset and start are possible at an arbitrary address.

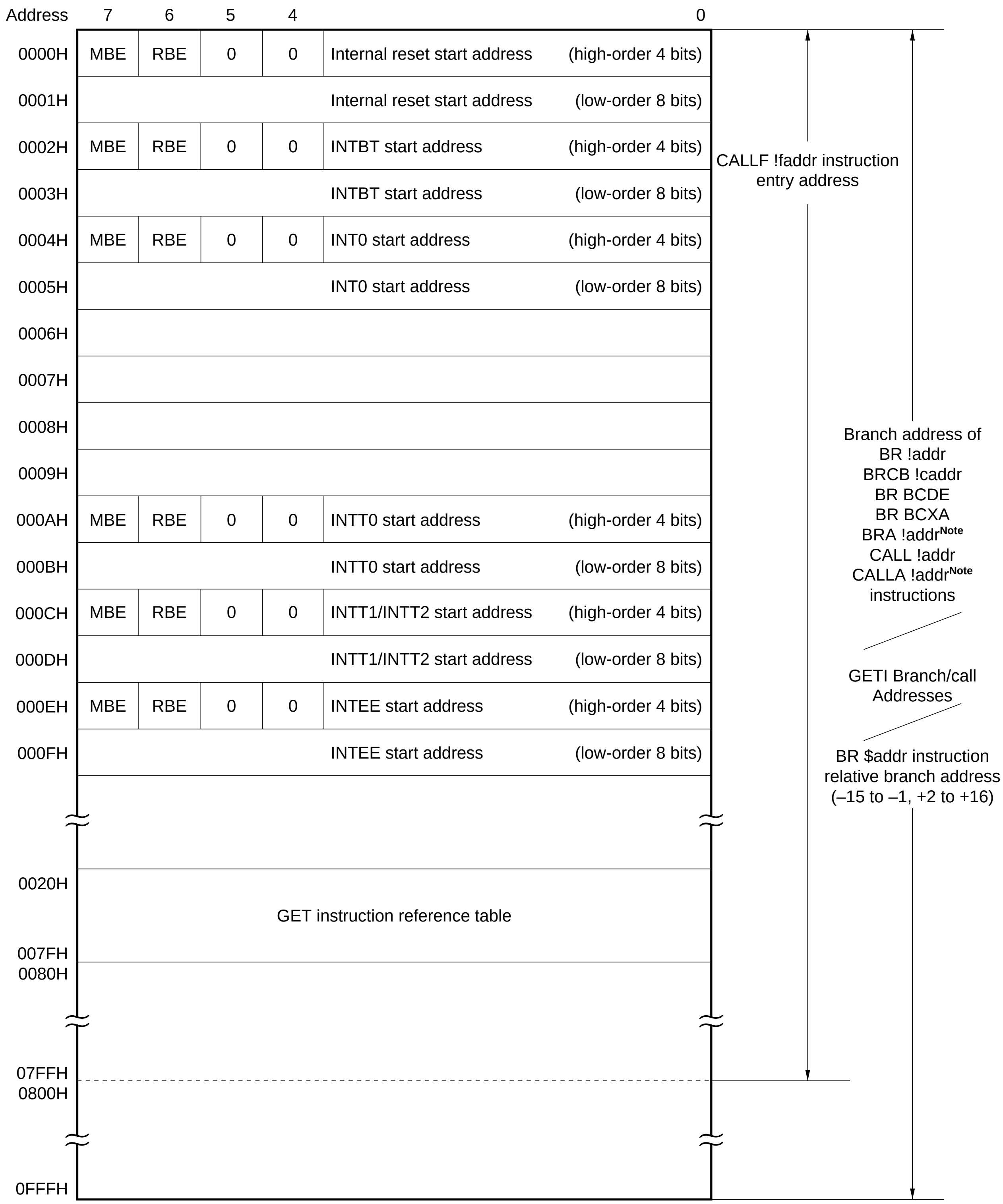
  - Addresses 0002H to 000FH
    Vector table wherein the program start address and values set for the RBE and MBE by the vectored interrupts are written. Interrupt service can be started at an arbitrary address.

  - Addresses 0020H to 007FH
    Table area referenced by the GETI instruction[Note].

Note The GETI instruction realizes a 1-byte instruction on behalf of an arbitrary 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the program steps.

- **Data memory**
  - Data area
    Static RAM ··· 128 words x 4 bits (000H to 07FH)
    EEPROM ··· 16 words x 8 bits (400H to 41FH)
  - Peripheral hardware area ··· 128 words x 4 bits (F80H to FFFH)

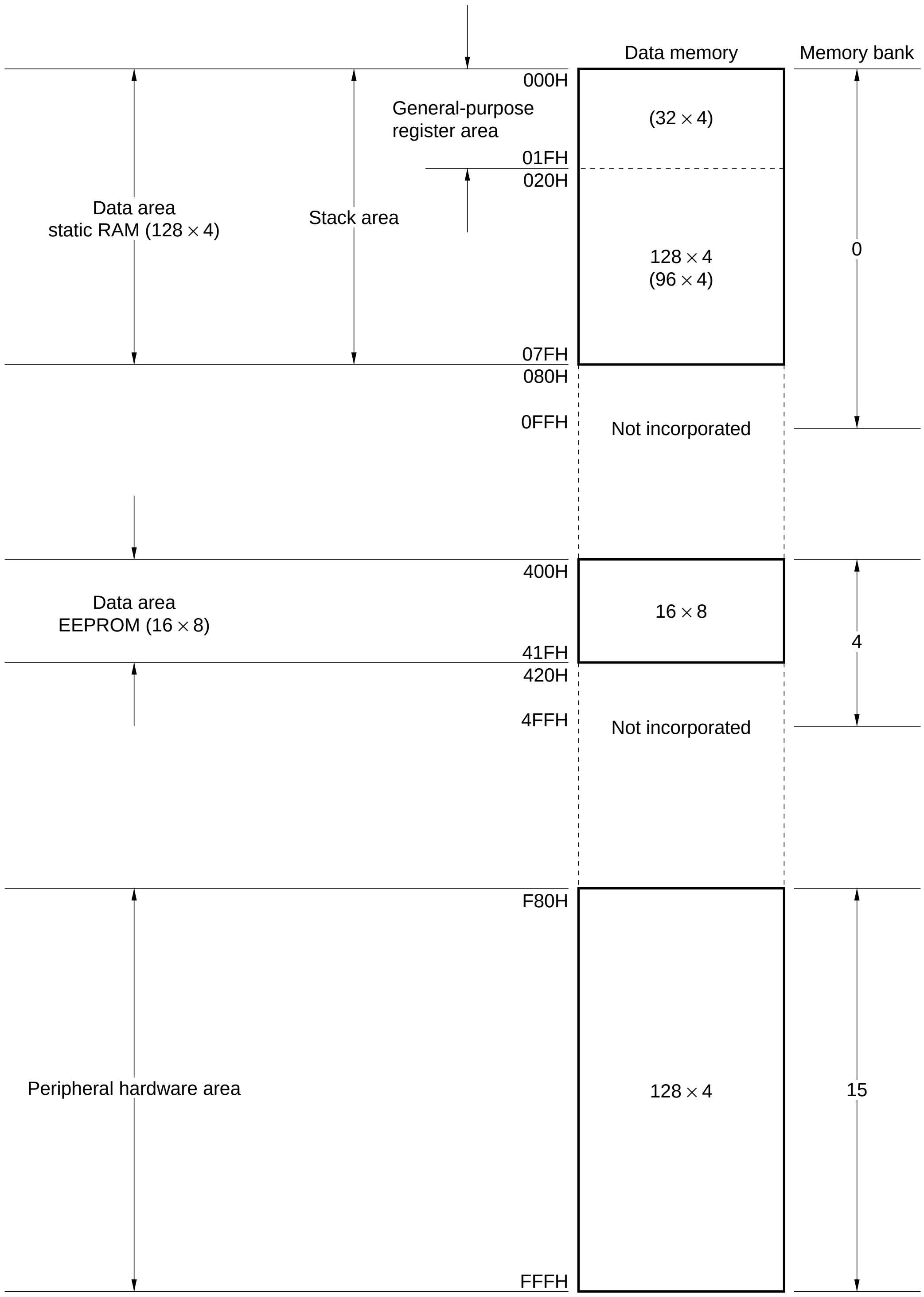
Figure 5-1. Program Memory Map



Note Can be used in the MkII mode only.

Remark In addition to the above, a branch can be made to an address with the low-order 8-bits only of the PC changed by means of a BR PCDE or BR PCXA instruction.

Figure 5-2. Data Memory Map



6. EEPROM

The μPD754244 incorporates 16 words × 8 bit EEPROM (Electrically Erasable PROM) as well as static RAM (128 words × 4 bit) as a data memory.

The EEPROM incorporated into the μPD754244 has the following features.

(1) Written data is retained if power is turned off.
(2) 8-bit data manipulation (auto-erase/auto-write) is available by memory manipulation instruction as well as for static RAM. However available instructions are restricted.
(3) It can reduce loads of software because the auto-erase and/or auto-write operation is performed by hardware.
(4) Write operation control using the interrupt request
The interrupt request is generated under following conditions.
• Terminates write operation
• Write status flag
It is possible to check whether enables or disables write operation by bit manipulation instructions.

7. PERIPHERAL HARDWARE FUNCTIONS

7.1 Digital Input/Output Ports

The following two types of I/O ports are provided.

- CMOS input (Port 7) : 4
- CMOS I/O (Ports 3, 6, 8) : 9

Total : 13

Table 7-1. Types and Features of Digital Ports

Port Name	Function	Operation and Features	Remarks
PORT3	4-bit I/O	Can be set to input or output mode bit-wise.	Also used as PTO0 to PTO2 pins.
PORT6			Also used as AV_{REF}, INT0, PTH00, and PTH01 pins.
PORT7	4-bit input	4-bit input only port On-chip pull-up resistor connection can be specified by mask option bit-wise.	Also used as KR4 to KR7 pins.
PORT8	1-bit I/O	Can be set to input or output mode bit wise.	–

7.2 Clock Generator

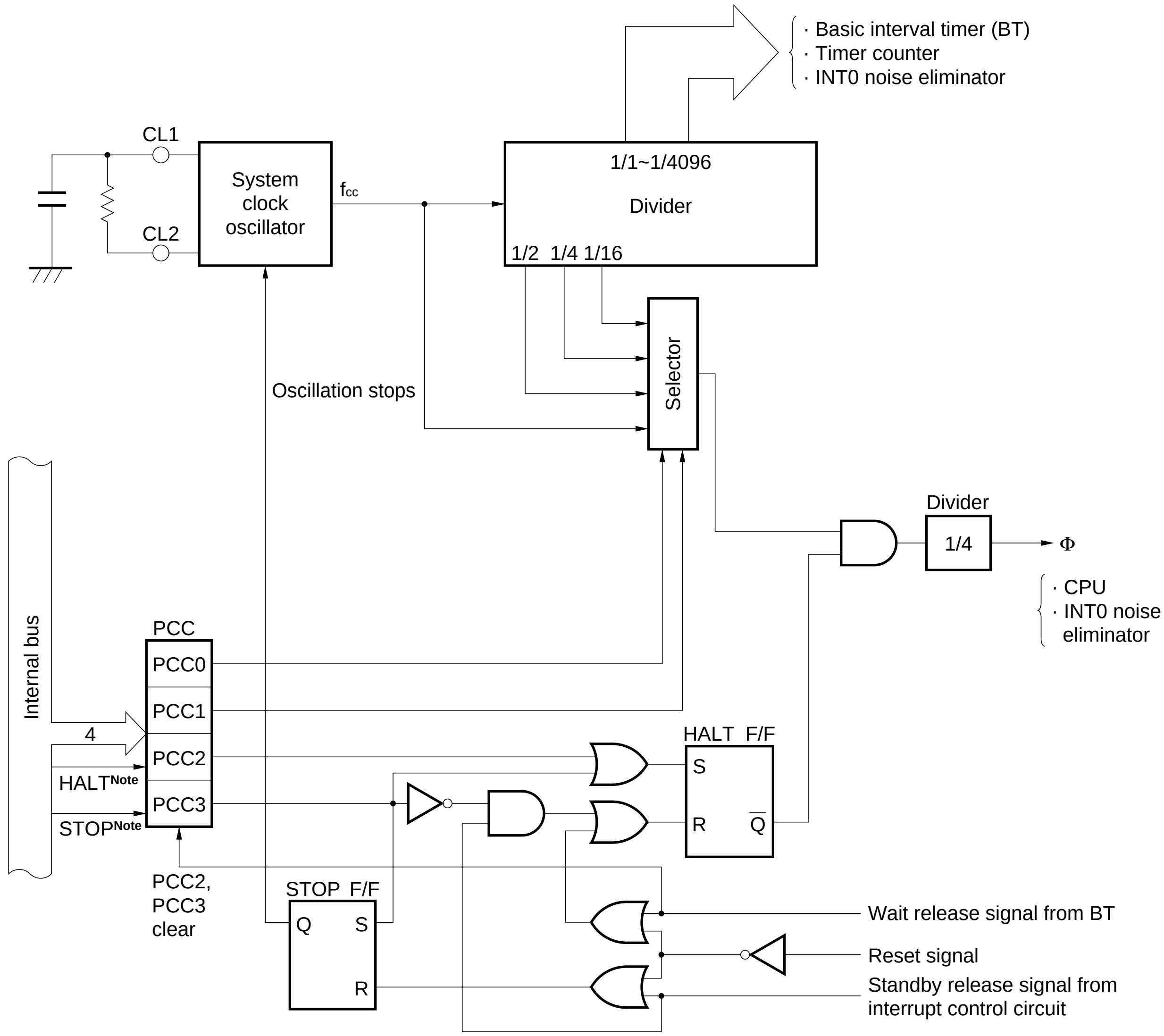
The clock generator provides the clock signals to the CPU and peripheral hardware. Its configuration is shown in Figures 7-1 and 7-2.

The operation of the clock generator is set with the processor clock control register (PCC).

The instruction execution time can be changed.

- μPD754144
  - 4, 8, 16, 64 μs (when the system clock f_{CC} operates at 1.0 MHz)
- μPD754244
  - 0.95, 1.91, 3.81, 15.3 μs (when the system clock f_X operates at 4.19 MHz)
  - 0.67, 1.33, 2.67, 10.7 μs (when the system clock f_X operates at 6.0 MHz)

Figure 7-1. μPD754144 (RC Oscillation) Clock Generator Block Diagram



Note Instruction execution

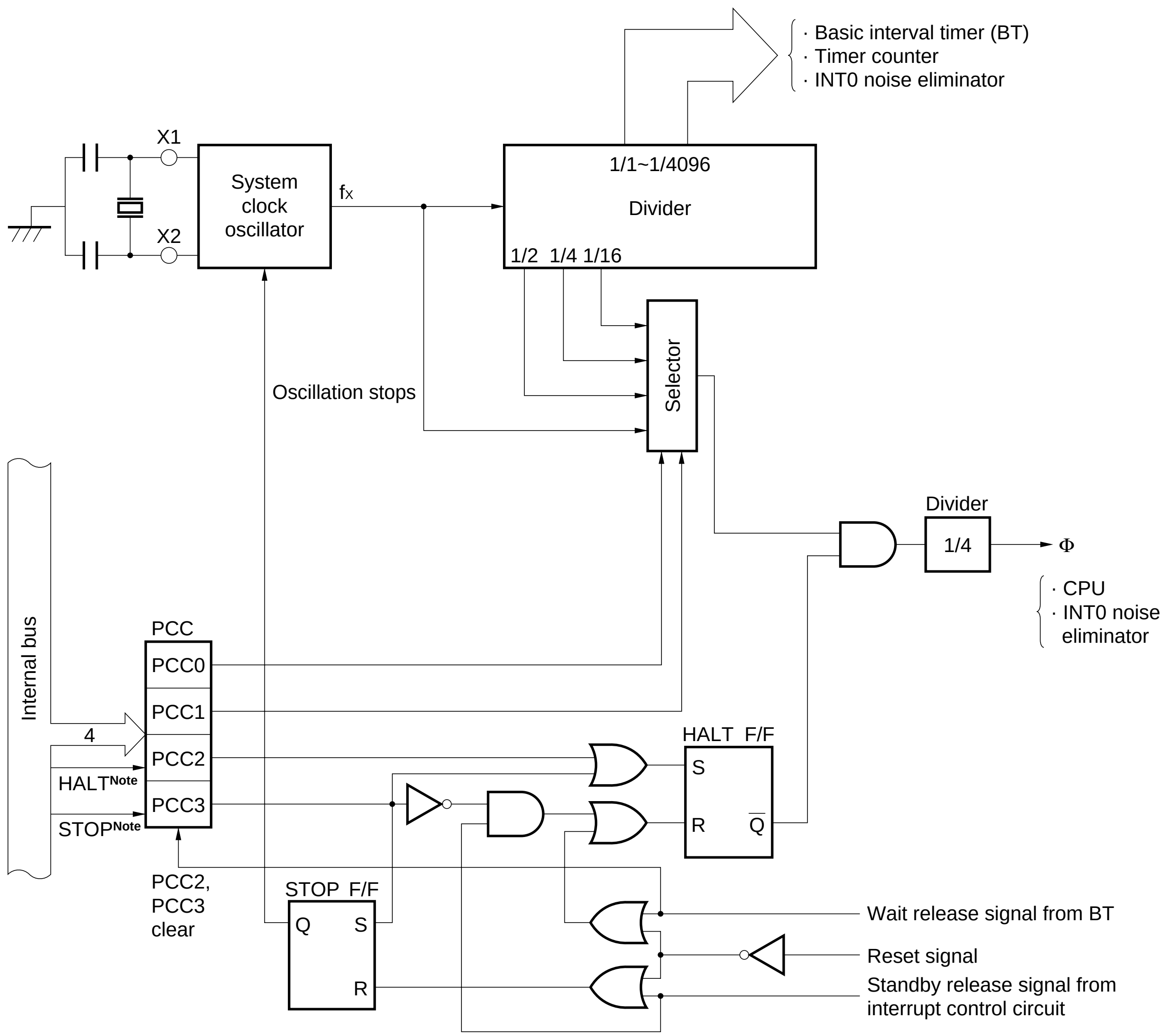
Remarks 1. f_{CC}: System clock frequency

2. Φ = CPU clock

3. PCC: Processor Clock Control Register

4. One clock cycle (t_{CY}) of the CPU clock is equal to one machine cycle of the instruction.

Figure 7-2. μPD754244 (Crystal/Ceramic Oscillation) Clock Generator Block Diagram



Note Instruction execution

Remarks 1. f_X: System clock frequency

2. Φ = CPU clock

3. PCC: Processor Clock Control Register

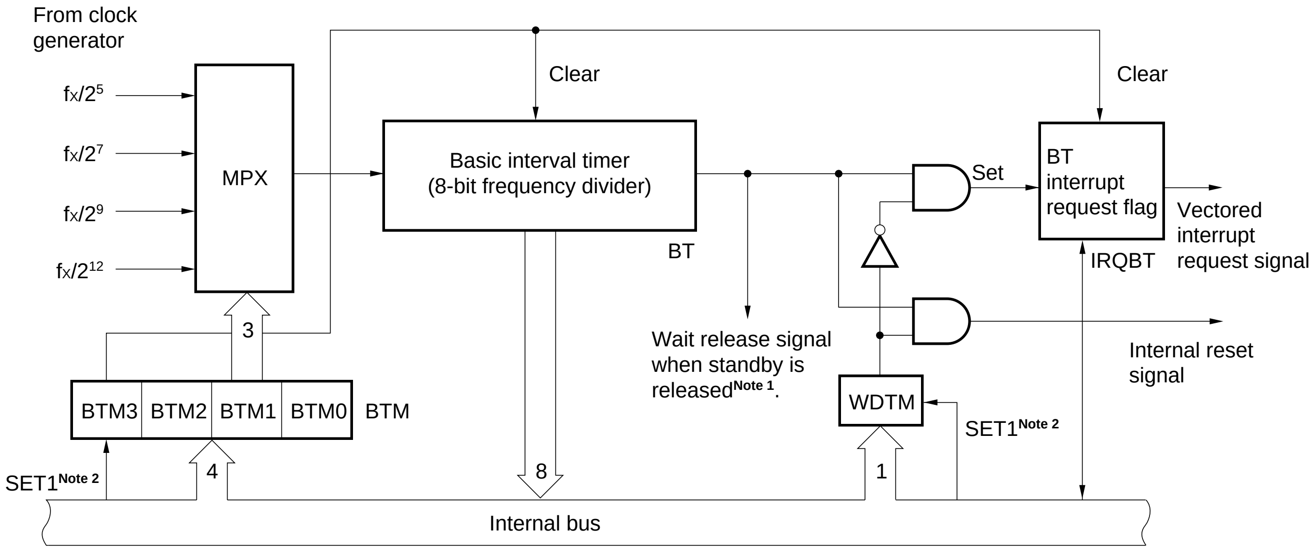
4. One clock cycle (t_{CY}) of the CPU clock is equal to one machine cycle of the instruction.

7.3 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

(a) Interval timer operation to generate a reference time interrupt
(b) Watchdog timer operation to detect a runaway of program and reset the CPU
(c) Selects and counts the wait time when the standby mode is released (μPD754244 only)[Note 1]
(d) Reads the contents of counting

Figure 7-3. Basic Interval Timer/Watchdog Timer Block Diagram



Notes 1. In the μPD754144 (RC oscillation), the wait time cannot be specified when the standby mode is released. The oscillation stabilization wait time is negligible in the μPD754144 and this device returns to the normal operation mode after counting $2^9/f_{CC}$ (512 μs: @ f_{CC} = 1.0-MHz operation). In the μPD754244 (crystal/ceramic oscillation), on the other hand, the wait time can be specified when the standby mode is released.

2. Instruction execution.

7.4 Timer Counter

The μPD754244 incorporates three channels of timer counters. Its configuration is shown in Figures 7-4 to 7-6.

The timer counter has the following functions.

(a) Programmable interval timer operation
(b) Square wave output of any frequency to PTO0-PTO2 pins
(c) Count value read function

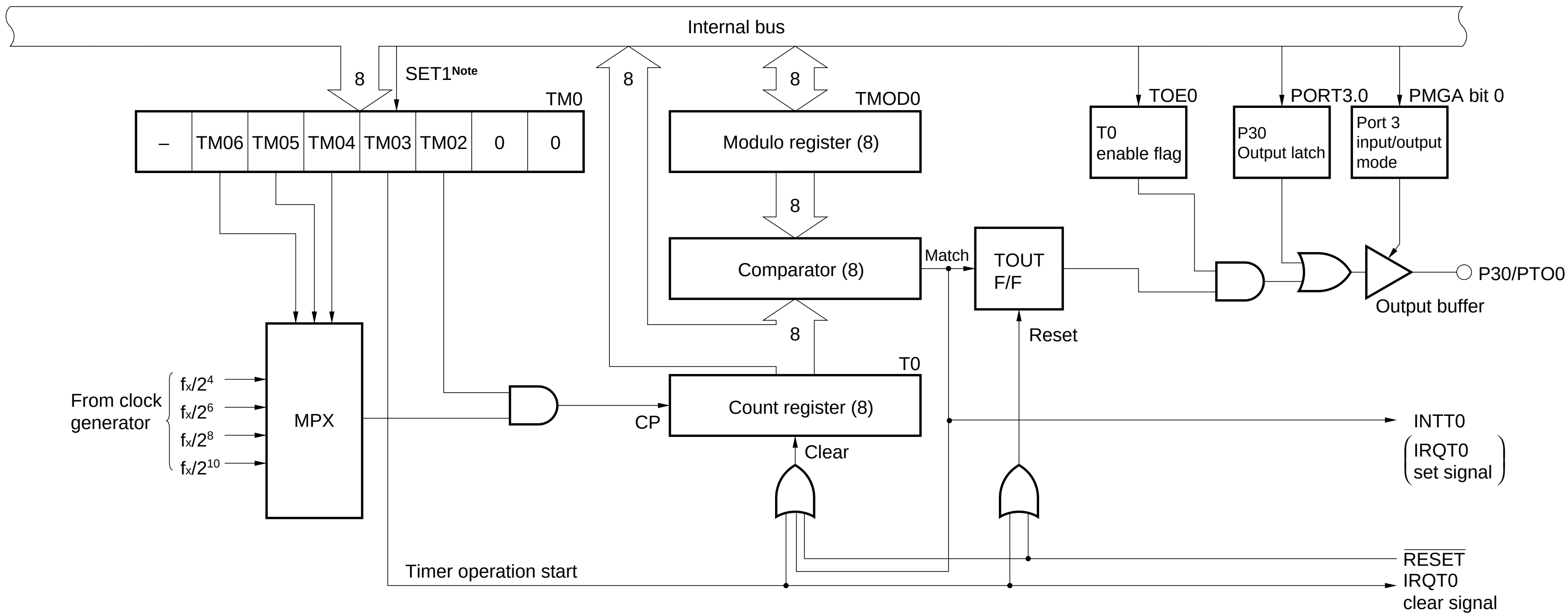
The timer counter can operate in the following four modes as set by the mode register.

Table 7-2. Mode List

Mode \ Channel	Channel 0	Channel 1	Channel 2	TM11	TM10	TM21	TM20
8-bit timer counter mode	○	○	○	0	0	0	0
PWM pulse generator mode	×	×	○	0	0	0	1
16-bit timer counter mode	×	○		1	0	1	0
Carrier generator mode	×	○		0	0	1	1

Remark ○ : Available
× : Not available

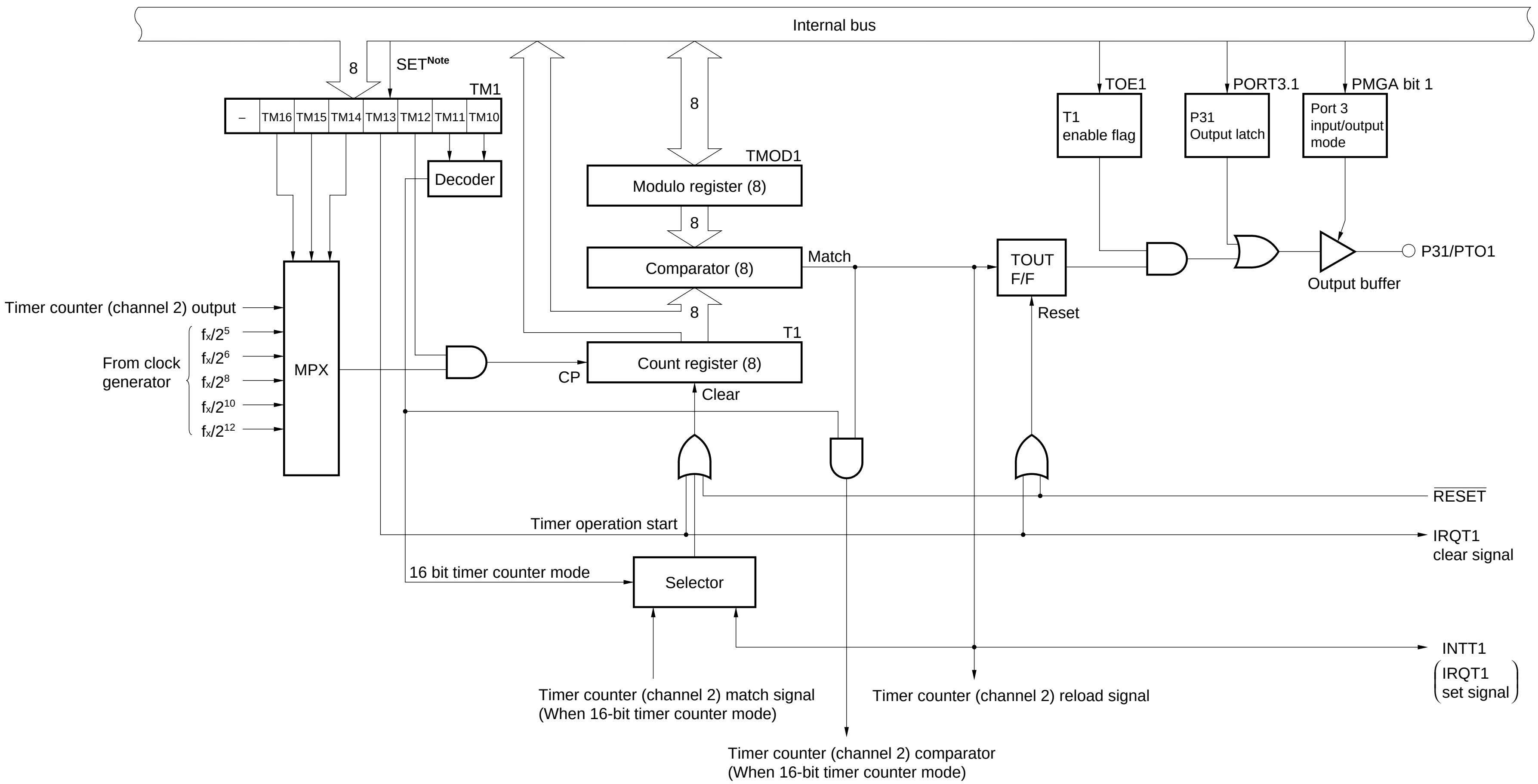
Figure 7-4. Timer Counter (Channel 0) Block Diagram



Note Instruction execution

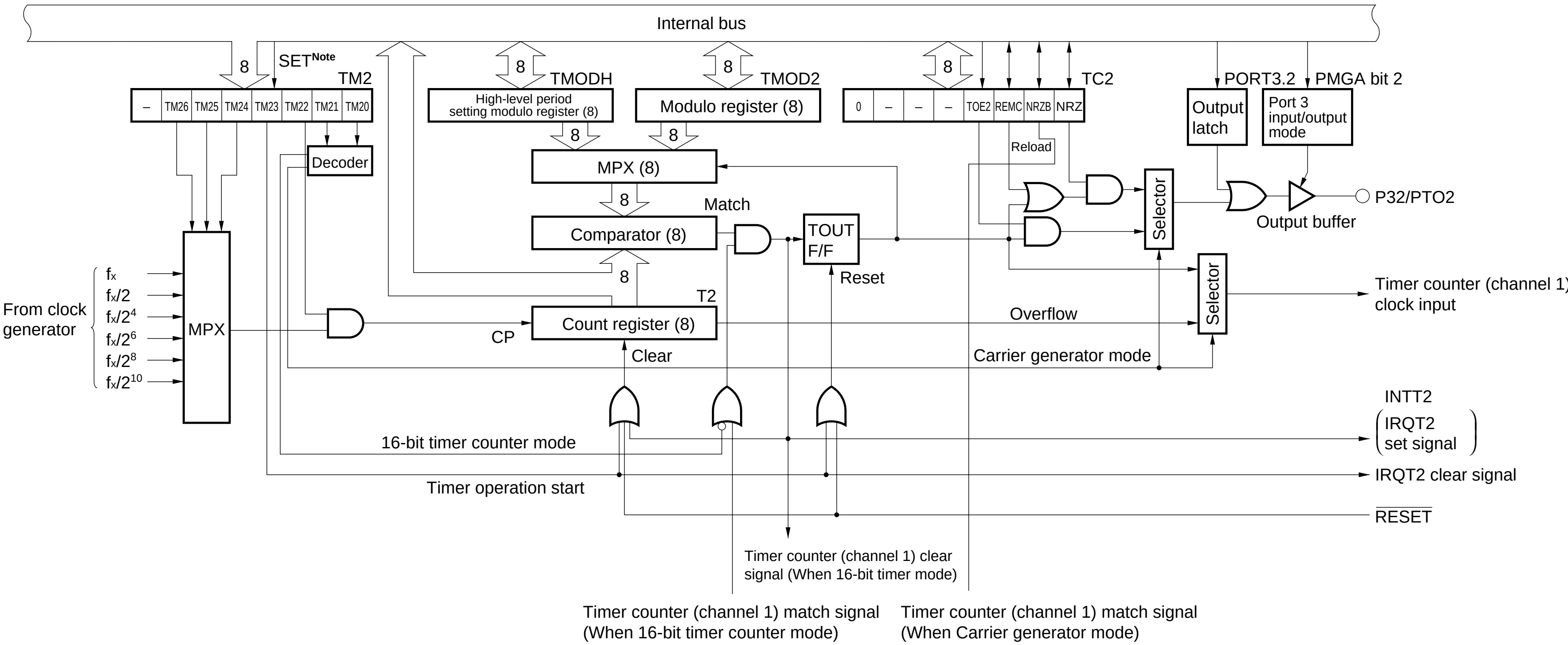
Caution When setting data to TM0, be sure to set bits 0 and 1 to 0.

Figure 7-5. Timer Counter (Channel 1) Block Diagram



Note Instruction execution

Figure 7-6. Timer Counter (Channel 2) Block Diagram



Note Instruction execution

Caution When setting data to TC2, be sure to set bit 7 to 0.

7.5 Programmable Threshold Port (Analog Input Port)

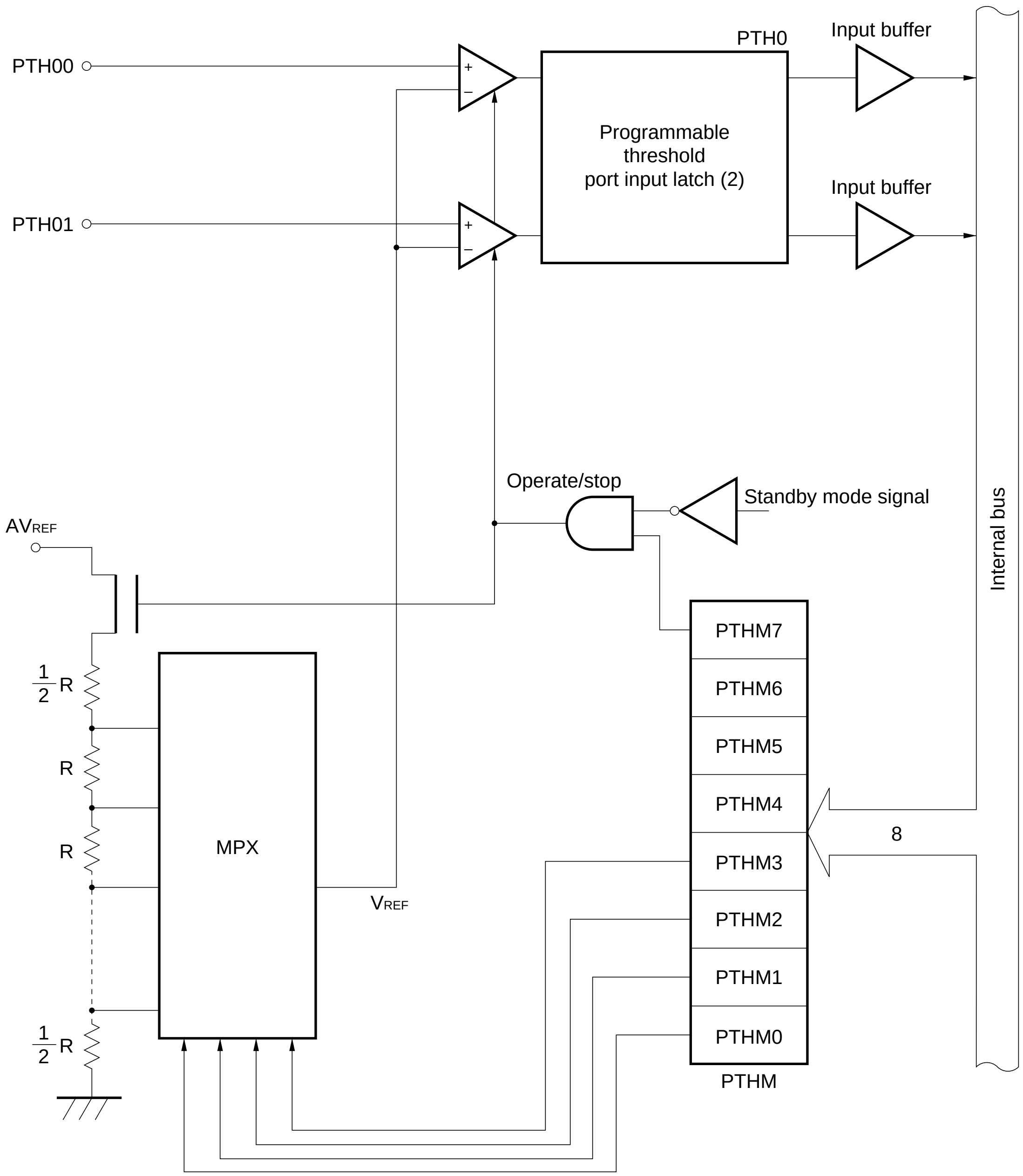
The μPD754244 provides analog input pins (PTH00, PTH01) whose threshold voltage (reference voltage) is selectable within sixteen steps. The following operations can be performed with these analog input pins.

(1) Comparator operation

(2) 4-bit resolution A/D converter operation (controlled by software)

Caution Do not specify an on-chip pull-up resistor connection for Port 6 when using the programmable threshold port.

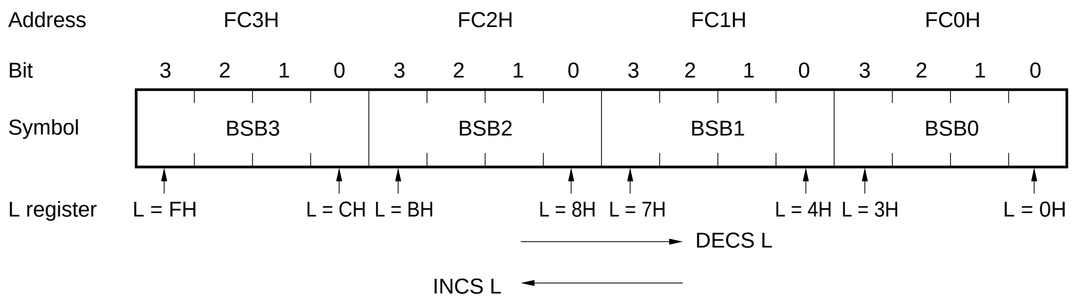
Figure 7-7. Programmable Threshold Port Block Diagram



7.6 Bit Sequential Buffer .... 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing large data bit-wise.

Figure 7-8. Bit Sequential Buffer Format



Remarks 1. In the pmem.@L addressing, the specified bit moves corresponding to the L register.

2. In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MSB specification.

8. INTERRUPT FUNCTION AND TEST FUNCTION

Figure 8-1 shows the interrupt control circuit. Each hardware device is mapped in the data memory space.

The interrupt control circuit of the μPD754244 has the following functions.

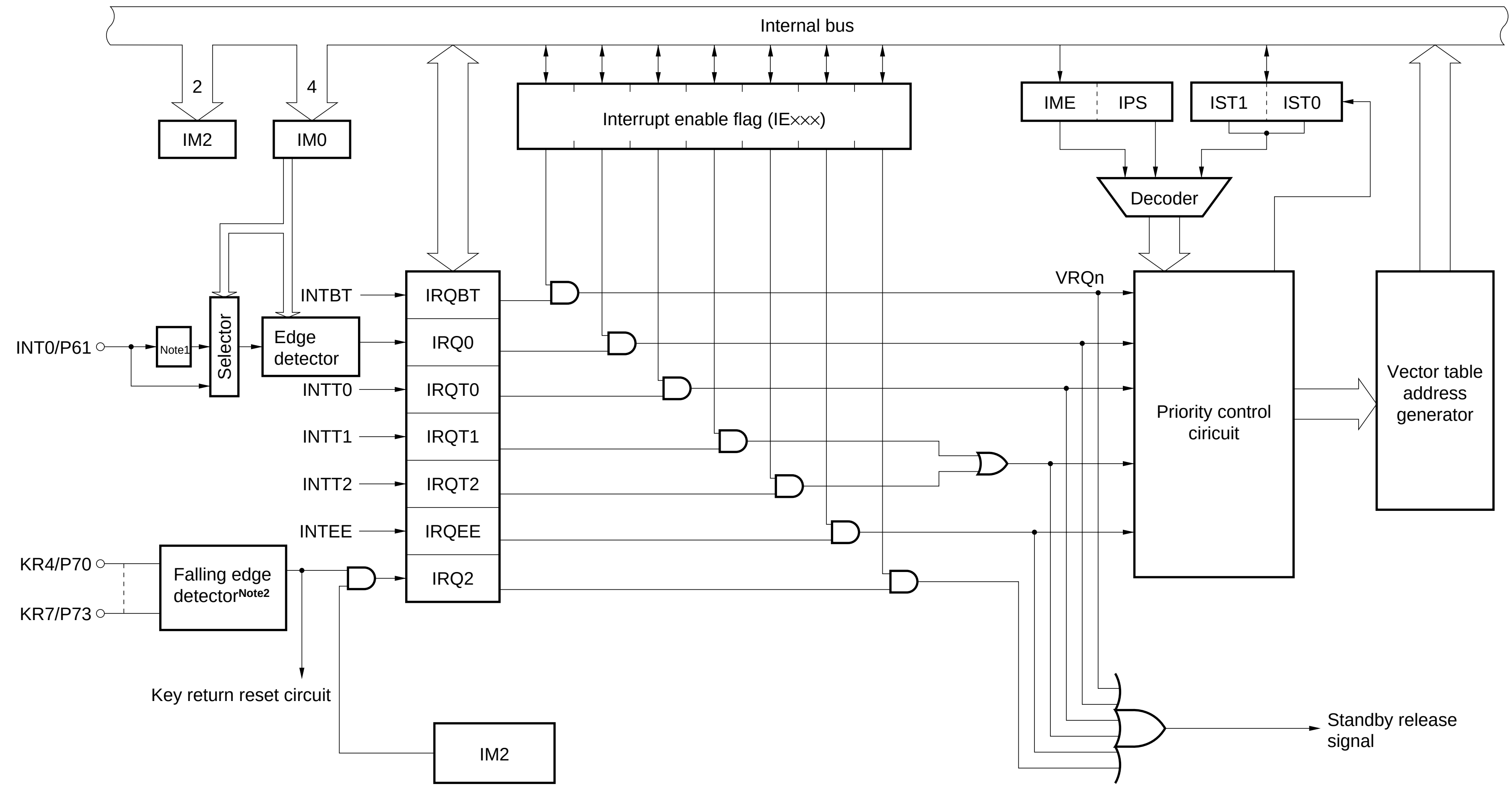
(1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acknowledgement by the interrupt enable flag (IE×××) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQ×××). An interrupt generated can be checked by software.
- Release the standby mode. A release interrupt can be selected by the interrupt enable flag.

(2) Test function

- Test request flag (IRQ2) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

Figure 8-1. Interrupt Control Circuit Block Diagram



Notes 1. Noise eliminator (Standby release is disable when noise eliminator is selected.)

2. The INT2 pin is not provided. Interrupt request flag (IRQ2) is set at the KRn pin falling edge when IM20 = 1 and IM21 = 0.

9. STANDBY FUNCTION

In order to reduce power dissipation while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD754244.

Table 9-1. Operation Status in Standby Mode

Mode Item		STOP Mode	HALT Mode
Set instruction		STOP instruction	HALT instruction
Operation status	Clock generator	Operation stops.	Only the CPU clock Φ halts (oscillation continues).
	Basic interval timer/ watchdog timer	Operation stops.	Operable BT mode: The IRQBT is set in the basic time interval. WT mode: Reset is generated by the BT overflow.
	Timer	Operation stops.	Operable.
	External interrupt	INT0 is not operable.[Note] INT2 is operable during KRn falling period only.	
	CPU	The operation stops.	
Release signal		• Reset signal • Interrupt request signal sent from interrupt enabled peripheral hardware • System reset signal (key return reset) generated by KRn falling edge when the KRREN pin = 1	• Reset signal • Interrupt request signal sent from interrupt enabled peripheral hardware

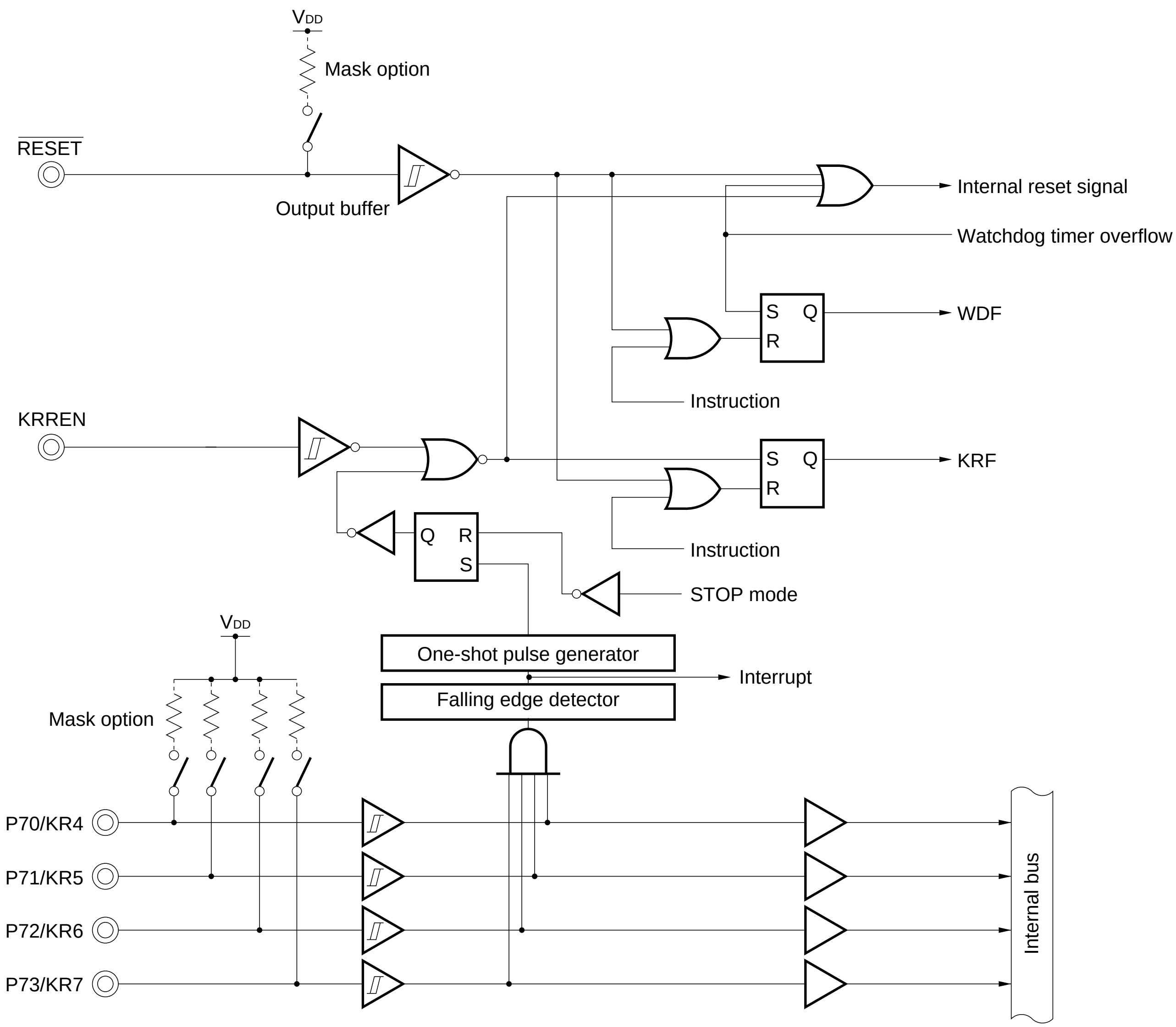
Note Can operate only when the noise eliminator is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

10. RESET FUNCTION

10.1 Configuration and Operation Status of RESET Function

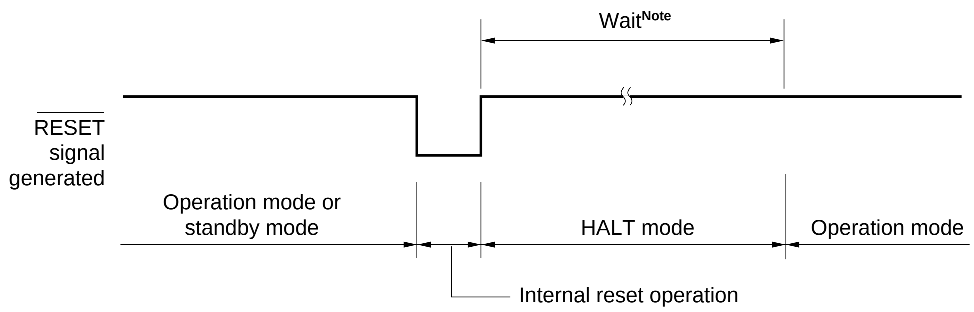
There are three kinds of reset input: the external reset signal ($\overline{\text{RESET}}$), the reset signal sent from the basic interval/watchdog timer, and the reset signal generated by a falling edge signal from KRn in the STOP mode. When any of these reset signals is input, an internal reset signal is generated. The configuration is shown in Figure 10-1.

Figure 10-1. Configuration of Reset Function



Each hardware is initialized by the $\overline{\text{RESET}}$ signal generation as listed in Table 10-1. Figure 10-2 shows the timing chart of the reset operation.

Figure 10-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation



Note In the μPD754144, the wait time is fixed to 56/fcc (56μs: @ 1.0-MHz operation).
In the μPD754244, the wait time can be selected from the following two time settings by means of the mask option.

2^{17}/fx (21.8 ms : @ 6.0-MHz operation, 31.3 ms: @ 4.19-MHz operation)

2^{15}/fx (5.46 ms : @ 6.0-MHz operation, 7.81 ms: @ 4.19-MHz operation)

Table 10-1. Hardware Status After Reset (1/3)

Hardware		RESET signal generation in the standby mode	RESET signal generation in operation
Program counter (PC)		Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.	Sets the low-order 4 bits of program memory's address 0000H to the PC11-PC8 and the contents of address 0001H to the PC7-PC0.
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to SK2)	0	0
	Interrupt status flag (IST0, IST1)	0	0
	Bank enable flag (MBE, RBE)	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.	Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.
Stack pointer (SP)		Undefined	Undefined
Stack bank select register (SBS)		1000B	1000B
Data memory (RAM)		Held	Undefined
Data memory (EEPROM)		Held[Note 1]	Held[Note 2]
EEPROM write control register (EWC)		0	0
General-purpose register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank select register (MBS, RBS)		0, 0	0, 0
Basic interval timer/watchdog timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
	Watchdog timer enable flag (WDTM)	0	0
Timer counter (channel 0)	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Timer counter (channel 1)	Counter (T1)	0	0
	Modulo register (TMOD1)	FFH	FFH
	Mode register (TM1)	0	0
	TOE1, TOUT F/F	0, 0	0, 0
Timer counter (channel 2)	Counter (T2)	0	0
	Modulo register (TMOD2)	FFH	FFH
	High-level period setting modulo register (TMOD2H)	FFH	FFH
	Mode register (TM2)	0	0
	TOE2, TOUT F/F	0, 0	0, 0
	REMC, NRZ, NRZB	0, 0, 0	0, 0, 0

Notes 1. Undefined if STOP mode is entered during an EEPROM write operation. Also undefined if HALT mode is entered during a write operation and a RESET signal is input during a write operation.

2. If a RESET signal is input during an EEPROM write operation, the data at that address is undefined.

Table 10-1. Hardware Status After Reset (2/3)

Hardware		RESET signal generation in the standby mode	RESET signal generation in operation
Programmable threshold port mode register (PTHM)		00H	00H
Clock generator	Processor clock control register (PCC)	0	0
Interrupt function	Interrupt request flag (IRQ×××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE×××)	0	0
	Interrupt priority selection register (IPS)	0	0
	INT0, 2 mode registers (IM0, IM2)	0, 0	0, 0
Digital port	Output buffer	Off	Off
	Output latch	Cleared (0)	Cleared (0)
	I/O mode registers (PMGA, C)	0	0
	Pull-up resistor setting register (POGA, B)	0	0
Bit sequential buffer (BSB0-BSB3)		Held	Undefined

Table 10-1. Hardware Status After Reset (3/3)

Hardware	RESET signal generation by key return reset	RESET signal generation in the standby mode	RESET signal generation by WDT during operation	RESET signal generation during operation
Watchdog flag (WDF)	Hold the previous status	0	1	0
Key return flag (KRF)	1	0	Hold the previous status	0

10.2 Watchdog Flag (WDF), Key Return Flag (KRF)

The WDF is cleared by a watchdog timer overflow signal, and the KRF is set by a reset signal generated by the KRn pins. As a result, by checking the contents of WDF and KRF, it is possible to know what kind of reset signal is generated.

As the WDF and KRF are cleared only by external signal or instruction execution, if once these flags are set, they are not cleared until an external signal is generated or a clear instruction is executed. Check and clear the contents of WDF and KRF after reset start operation by executing SKTCLR instruction and so on.

Table 10-2 lists the contents of WDF and KRF corresponding to each signal. Figure 10-3 shows the WDF operation in generating each signal, and Figure 10-4 shows the KRF operation in generating each signal.

Table 10-2. WDF and KRF Contents Correspond to Each Signal

Hardware	External $\overline{\text{RESET}}$ signal generation	Reset signal generation by watch-dog timer overflow	Reset signal generation by the KRn input	WDF clear instruction execution	KRF clear instruction execution
Watchdog flag (WDF)	0	1	Hold	0	Hold
Key return flag (KRF)	0	Hold	1	Hold	0

Figure 10-3. WDF Operation in Generating Each Signal

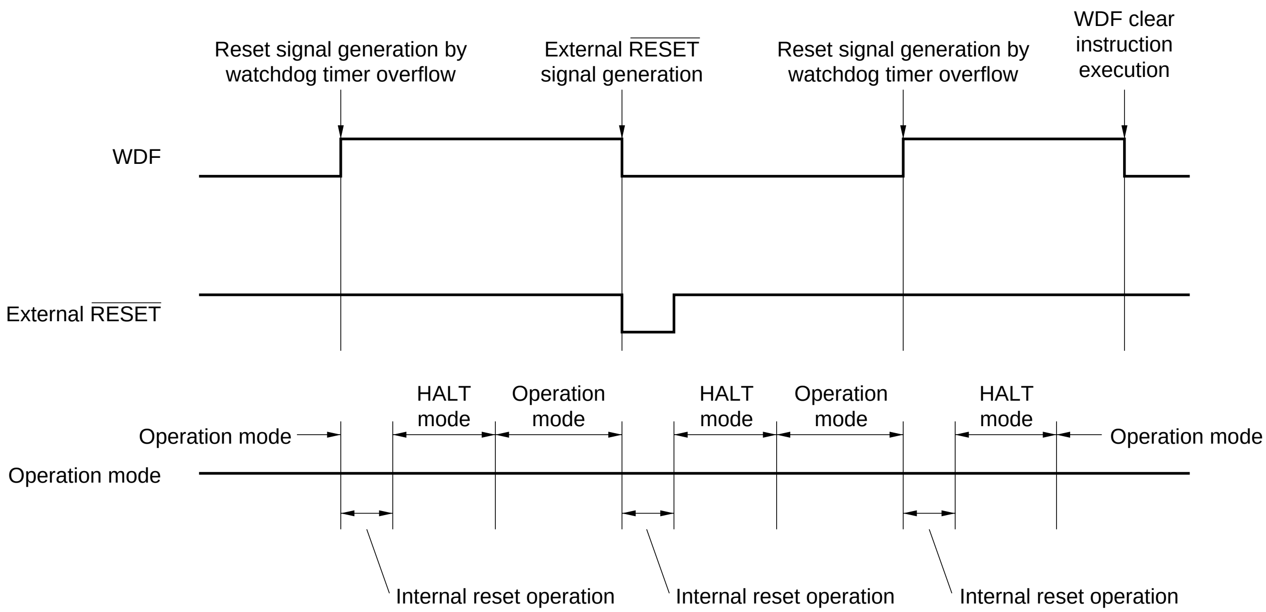
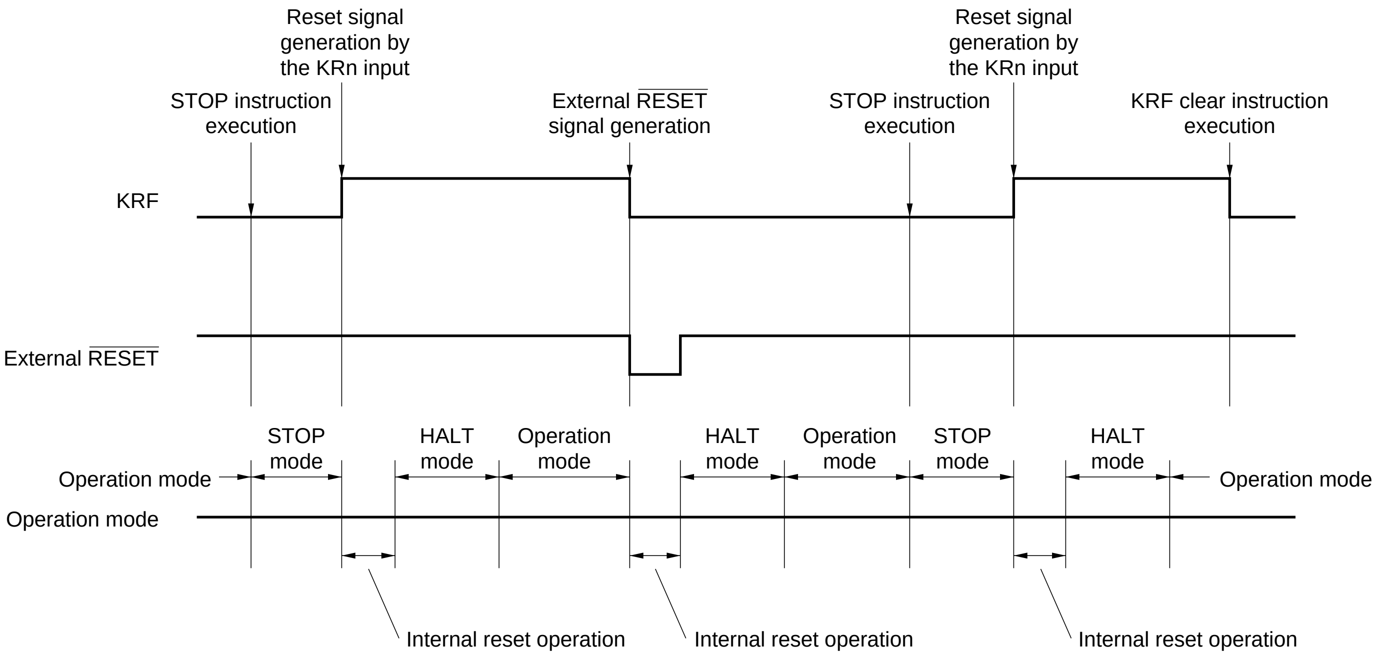


Figure 10-4. KRF Operation in Generating Each Signal



11. MASK OPTION

The μPD754244 has the following mask options:

- Mask option of P70/KR4 to P73/KR7
  On-chip pull-up resistor connection can be specified for these pins.
  (1) Do not connect an on-chip pull-up resistor
  (2) Connect the 100-kΩ (typ.) pull-up resistor bit-wise

- Mask option of $\overline{\text{RESET}}$ pin
  On-chip pull-up resistor connection can be specified for this pin.
  (1) Do not connect an on-chip pull-up resistor
  (2) Connect the 100-kΩ (typ.) pull-up resistor

- Standby function mask option (μPD754244 only) [Note]
  The wait time when the $\overline{\text{RESET}}$ signal is input can be selected.
  (1) $2^{17}/f_X$ (21.8 ms: @ f_X = 6.0-MHz operation, 31.3 ms: @ f_X = 4.19-MHz operation)
  (2) $2^{15}/f_X$ (5.46 ms: @ f_X = 6.0-MHz operation, 7.81 ms: @ f_X = 4.19-MHz operation)

Note This mask option is not provided for the μPD754144, and its wait time is fixed to 56/f_{CC} (56 μs: @ f_{CC} = 1.0-MHz operation).

12. INSTRUCTION SETS

(1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to "**RA75X ASSEMBLER PACKAGE USERS' MANUAL — LANGUAGE (EEU-1367)**". If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the registers can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, refer to **"μPD754144, 754244 user's manual (U10676E)"**.

Expression format	Description method
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label[Note] 2-bit immediate data or label
fmem pmem	FB0H-FBFH, FF0H-FFFH immediate data or label FC0H-FFFH immediate data or label
addr addr1 caddr faddr	000H-FFFH immediate data or label 000H-FFFH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H-7FH immediate data (where bit 0 = 0) or label
PORTn IE×× RBn MBn	PORT3, 6, 7, 8 IEBT, IET0-IET2, IE0, IE2, IEEE RB0-RB3 MB0, MB4, MB15

Note mem can be only used for even address in 8-bit data processing.

(2) Legend in explanation of operation

A	: A register, 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: XA register pair; 8-bit accumulator
BC	: BC register pair
DE	: DE register pair
HL	: HL register pair
XA’	: XA’ extended register pair
BC’	: BC’ extended register pair
DE’	: DE’ extended register pair
HL’	: HL’ extended register pair
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag, bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 3, 6, 7, 8)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IE×××	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Separation between address and bit
(××)	: The contents addressed by ××
××H	: Hexadecimal data

(3) Explanation of symbols under addressing area column

*1	MB = MBE•MBS (MBS = 0, 4, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS (MBS = 0, 4, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 000H to FFFH	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
	addr1 = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 000H to FFFH	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 000H to FFFH	

Remarks 1. MB indicates memory bank that can be accessed.

2. In *2, MB = 0 independently of how MBE and MBS are set.

3. In *4 and *5, MB = 15 independently of how MBE and MBS are set.

4. *6 to *11 indicate the areas that can be addressed.

(4) Explanation of number of machine cycles column

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction[Note]: S = 2

Note 3-byte instruction: BR !addr, BRA !addr1, CALL !addr, or CALLA !addr1 instruction

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of CPU clock (= t_{CY}); time can be selected from among four types by setting PCC.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Transfer instruction	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2+S	A ← (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ← (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2+S	A ↔ (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ↔ (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table reference instructions	MOVT	XA, @PCDE	1	3	XA ← $(PC_{11-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{11-8}+XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ Note	*6	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ Note	*6	

Note Set “0” in register B.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Bit transfer instructions	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← (H+mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit, CY	2	2	(H+mem_{3-0}.bit) ← CY	*1	
Operation instructions	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		XA, #n8	2	2+S	XA ← XA+n8		carry
		A, @HL	1	1+S	A ← A+(HL)	*1	carry
		XA, rp'	2	2+S	XA ← XA+rp'		carry
		rp'1, XA	2	2+S	rp'1 ← rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY ← XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1+XA+CY		
	SUBS	A, @HL	1	1+S	A ← A–(HL)	*1	borrow
		XA, rp'	2	2+S	XA ← XA–rp'		borrow
		rp'1, XA	2	2+S	rp'1 ← rp'1–XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A–(HL)–CY	*1	
		XA, rp'	2	2	XA, CY ← XA–rp'–CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1–XA–CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∀ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∀ XA		
Accumulator manipulation instructions	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Increment and Decrement instructions	INCS	reg	1	1+S	reg ← reg+1		reg=0
		rp1	1	1+S	rp1 ← rp1+1		rp1=00H
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL)=0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem)=0
	DECS	reg	1	1+S	reg ← reg–1		reg=FH
		rp'	2	2+S	rp' ← rp'–1		rp'=FFH
Comparison instruction	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg=n4
		@HL, #n4	1	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	2	1+S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2+S	Skip if A = reg		A=reg
		XA, rp'	2	2+S	Skip if XA = rp'		XA=rp'
Carry flag manipulation instruction	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY=1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory bit manipulation instructions	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if (fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if (mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if (fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if (H+mem$_{3-0}$.bit)=0	*1	(@H+mem.bit)=0

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Memory bit manipulation instructions	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=1 and clear	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if (H+mem_{3-0}.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∧ (H+mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H+mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∀ (H+mem_{3-0}.bit)	*1	
Branch instructions	BR[Note 1]	addr	–	–	PC_{11-0} ← addr (Select appropriate instruction among BR !addr BRCB !caddr, and BR $addr according to the assembler being used.)	*6	
		addr1	–	–	PC_{11-0} ← addr (Select appropriate instruction among BR !addr BRA !addr1, BRCB !caddr and BR $addr1 according to the assembler being used.)	*11	
		! addr	3	3	PC_{11-0} ← addr	*6	
		$addr	1	2	PC_{11-0} ← addr	*7	
		$addr1	1	2	PC_{11-0} ← addr1		
		PCDE	2	3	PC_{11-0} ← PC_{11-8}+DE		
		PCXA	2	3	PC_{11-0} ← PC_{11-8}+XA		
		BCDE	2	3	PC_{11-0} ← BCDE[Note 2]	*6	
		BCXA	2	3	PC_{11-0} ← BCXA[Note 2]	*6	
	BRA[Note 1]	!addr1	3	3	PC_{11-0} ← addr1	*11	
	BRCB	!caddr	2	2	PC_{11-0} ← $caddr_{11-0}$	*8	

Notes 1. The above operations in the double boxes can be performed only in the Mk II mode.

2. "0" must be set to B register.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Subroutine stack control instructions	CALLA Note	!addr1	3	3	(SP–2) ← ×, ×, MBE, RBE (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 PC_{11-0} ← addr1, SP ← SP–6	*11	
	CALL Note	!addr	3	3	(SP–3) ← MBE, RBE, 0, 0 (SP–4) (SP–1) (SP–2) ← PC_{11-0} PC_{11-0} ← addr, SP ← SP–4	*6	
				4	(SP–2) ← ×, ×, MBE, RBE (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 PC_{11-0} ← addr, SP ← SP–6		
	CALLF Note	!faddr	2	2	(SP–3) ← MBE, RBE, 0, 0 (SP–4) (SP–1) (SP–2) ← PC_{11-0} PC_{11-0} ← 0+faddr, SP ← SP–4	*9	
				3	(SP–2) ← ×, ×, MBE, RBE (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 PC_{11-0} ← 0+faddr, SP ← SP–6		
	RET Note		1	3	PC_{11-0} ← (SP) (SP+3) (SP+2) MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4		
					×, ×, MBE, RBE ← (SP+4) 0, 0, 0, 0, ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2), SP ← SP+6		
	RETS Note		1	3+S	MBE, RBE, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) SP ← SP+4 then skip unconditionally		Unconditional
					0, 0, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) ×, ×, MBE, RBE ← (SP+4) SP ← SP+6 then skip unconditionally		
	RETI Note		1	3	MBE, RBE, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6		
					0, 0, 0, 0 ← (SP+1) PC_{11-0} ← (SP) (SP+3) (SP+2) PSW ← (SP+4) (SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP–1) (SP–2) ← rp, SP ← SP–2		
		BS	2	2	(SP–1) ← MBS, (SP–2) ← RBS, SP ← SP–2		
	POP	rp	1	1	rp ← (SP+1) (SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP+2		

Note The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

Instruction group	Mnemonic	Operand	Number of bytes	Number of machine cycles	Operation	Addressing area	Skip condition
Interrupt control instructions	EI		2	2	IME (IPS.3) ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IE×××	2	2	IE××× ← 0		
Input/output instructions	IN[Note 1]	A, PORTn	2	2	A ← PORTn (n = 3, 6, 7, 8)		
	OUT[Note 1]	PORTn, A	2	2	PORTn ← A (n = 3, 6, 8)		
CPU control instructions	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special instructions	SEL	RBn	2	2	RBS ← n (n = 0-3)		
		MBn	2	2	MBS ← n (n = 0, 4, 15)		
	GETI[Notes 2, 3]	taddr	1	3	• When TBR instruction PC_{11-0} ← $(taddr)_{3-0}$ + (taddr+1)	*10	
					• When TCALL instruction (SP–4) (SP–1) (SP–2) ← PC_{11-0} (SP–3) ← MBE, RBE, 0, 0 PC_{11-0} ← $(taddr)_{3-0}$ + (taddr+1) SP ← SP–4		
					• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.		Depending on the reference instruction
				3	• When TBR instruction PC_{11-0} ← $(taddr)_{3-0}$ + (taddr+1)	*10	
				4	• When TCALL instruction (SP–6) (SP–3) (SP–4) ← PC_{11-0} (SP–5) ← 0, 0, 0, 0 (SP–2) ← ×, ×, MBE, RBE PC_{11-0} ← $(taddr)_{3-0}$ + (taddr+1) SP ← SP–6		
				3	• When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.		Depending on the reference instruction

Notes 1. While the IN instruction and OUT instruction are being executed, MBE must be set to 0, or MBE must be set to 1 and MBS must be set to 15.

2. The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.

3. The above operations in the double boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

13. ELECTRICAL SPECIFICATIONS

13.1 μPD754144

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Power supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	P30, P31, P33, P60 to P63, P80	–10	mA
			P32	–20	mA
		For all pins		–30	mA
Output current, low	I_{OL}	Per pin		20	mA
		For all pins		90	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

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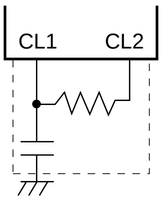
System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 6.0 V)

Resonator	Recommended Constant	Parameter	Testing Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillation frequency (f_{CC}) **Note**		0.4		2.0	MHz

Note Only the oscillator characteristics are shown. For the instruction execution time and oscillation frequency characteristics, refer to **AC Characteristics**.

Caution When using the oscillation circuit of the system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:
- **Keep the wire length as short as possible.**
- **Do not cross other signal lines.**
- **Do not route the wiring in the vicinity of lines though which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit as the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}	Per pin	P30, P31, P33, P60 to P63, P80			–5	mA
			P32, V_{DD} = 3.0 V, V_{OH} = V_{DD} – 2.0 V		–7	–15	mA
		Total of all pins				–20	mA
Low-level output current	I_{OL}	Per pin				15	mA
		Total of all pins				45	mA
High-level input voltage	V_{IH1}	Port 3	2.7 V ≤ V_{DD} ≤ 6.0 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 6 to 8, KRREN, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	Port 3	2.7 V ≤ V_{DD} ≤ 6.0 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 6 to 8, KRREN, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 6.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1.0 mA		V_{DD} – 1.0			V
		V_{DD} = 1.8 to 6.0 V, I_{OH} = –100 μA		V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	V_{DD} = 4.5 to 6.0 V	Port 3, I_{OL} = 15 mA		0.6	2.0	V
			Ports 6, 8, I_{OL} = 1.6 mA			0.4	V
		V_{DD} = 1.8 to 6.0 V, I_{OH} = 400 μA				0.5	V
High-level input leakage current	I_{LIH}	VIN = V_{DD}				3.0	μA
Low-level input leakage current	I_{LIL}	V_{IN} = 0 V				–3.0	μA
High-level output leakage current	I_{LOH}	V_{OUT} = V_{DD}				3.0	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3.0	μA
On-chip pull-up resistance	R_{L1}	V_{IN} = 0 V	Ports 3, 6, 8	50	100	200	kΩ
	R_{L2}		Port 7, $\overline{\text{RESET}}$ (mask option)	50	100	200	kΩ

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	1.0-MHz RC oscillation R = 22 kΩ C = 22 pF	V_{DD} = 5.0 V ± 10% Note 2			0.7	2.1	mA
			V_{DD} = 3.0 V ± 10% Note 3			0.3	1.0	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		0.5	1.8	mA
				V_{DD} = 3.0 V ± 10%		0.25	0.9	mA
	I_{DD1}	1.0-MHz RC oscillation R = 5.1 kΩ C = 120 pF	V_{DD} = 5.0 V ± 10% Note 2			1.15	3.5	mA
			V_{DD} = 3.0 V ± 10% Note 3			0.55	1.6	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		0.95	2.8	mA
				V_{DD} = 3.0 V ± 10%		0.5	1.5	mA
	I_{DD3}	STOP mode	V_{DD} = 1.8 to 6.0 V				5	μA
				T_A = 25°C			1	μA
			V_{DD} = 3.0 V ±10%			0.1	3	μA
				T_A = –40 to +40°C		0.1	1	μA

Notes 1. The current flowing through the on-chip pull-up resistor, the current during EEPROM writing time, and the current when the program threshold port (PTH) is operating are not included.

2. When the device is operated in the high-speed mode by setting the processor clock control register (PCC) to 0011H.

3. When the device is operated in the low-speed mode by setting PCC to 0000H.

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AC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note1 (Minimum instruction execution time = 1 machine cycle)	t_{CY}			2.0	4.0	128	μs
RC oscillation frequency	f_{CC}	R = 22 kΩ, C = 22 pF	V_{DD} = 3.6 to 6.0 V	0.9	1.0 Note 2	1.2	MHz
			V_{DD} = 2.2 to 3.6 V	0.75	1.0 Note 2	1.15	MHz
			V_{DD} = 1.8 to 3.6 V	0.5	1.0 Note 2	1.15	MHz
			V_{DD} = 1.8 to 6.0 V	0.5	1.0 Note 2	1.2	MHz
		R = 5.1 kΩ, C = 120 pF	V_{DD} = 3.6 to 6.0 V	0.91	1.0 Note 2	1.1	MHz
			V_{DD} = 2.2 to 3.6 V	0.76	1.0 Note 2	1.05	MHz
			V_{DD} = 1.8 to 3.6 V	0.51	1.0 Note 2	1.05	MHz
			V_{DD} = 1.8 to 6.0 V	0.51	1.0 Note 2	1.1	MHz
Interrupt input high- and low-level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 3**			μs
			IM02 = 1	10			μs
		KR4 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

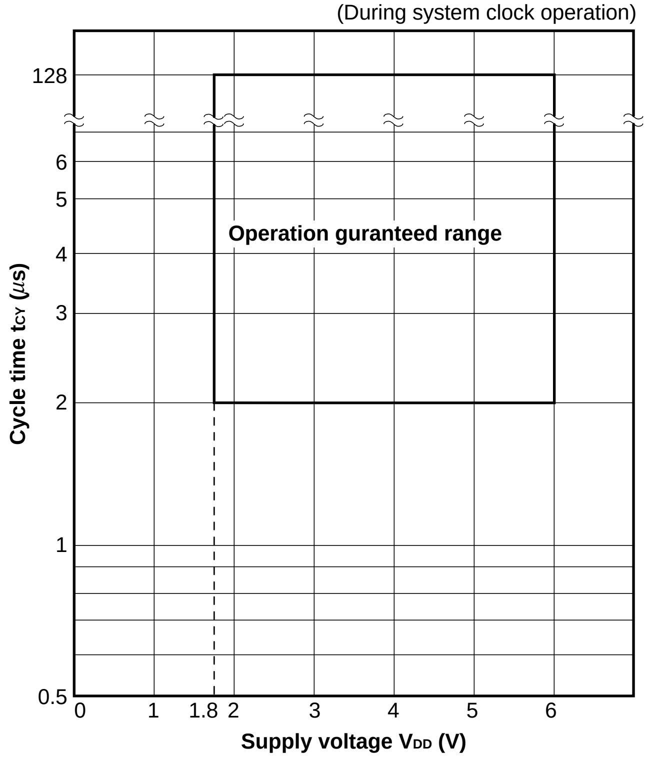
Notes 1. The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the time constants of the connected resistor (R) and capacitor (d) and the processor clock control register (PCC). The figure on the right shows the cycle time t_{CY} characteristics against the supply voltage V_{DD} when the system clock is used.

2. This is the typical value when V_{DD} = 3.6 V.

3. $2t_{CY}$ or $128/f_{CC}$ depending on the setting of the interrupt mode register (IM0).

t_{CY} vs. V_{DD}

(During system clock operation)



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EEPROM Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
EEPROM write current	I_{EEW}	1.0 MHz, RC oscillation	V_{DD} = 5.0 V ± 10%		4.0	12	mA
			V_{DD} = 3.0 V ± 10%		2.0	6	mA
EEPROM write time	t_{EEW}	1.0 MHz, RC oscillation **Note**		3.8	4.6	10.0	ms
EEPROM write times	EEWT	T_A = –40 to +70°C		100000			times/byte
		T_A = –40 to +85°C		80000			times/byte

Note Set EWTC 4 to 6 so as to be 18 x $2^8/f_{CC}$ (4.6 ms: @ f_{CC} = 1.0-MHz operation), considering the variation of the RC oscillation.

Comparator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		**Note**		**Note**	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
AV_{REF} input voltage	V_{IAVREF}		1.8		V_{DD}	V
Comparator circuit current consumption	I_{DD5}	When bit 7 of PTHM is set to 1		1		mA

Note The threshold voltage becomes as follows by settings bits 0 to 3 of PTHM.
$V_{TH} = V_{IAVREF}$ x (n + 0.5)/16 (n = 0 to 15)

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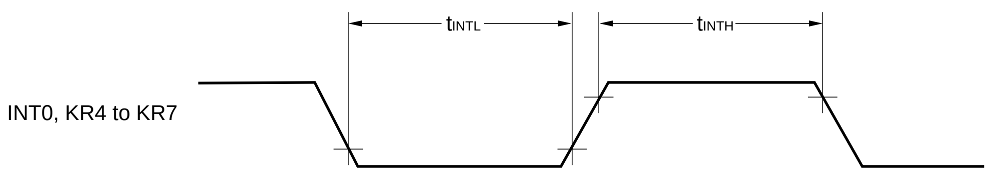
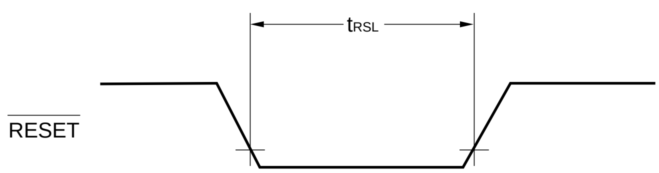
AC Timing Test Points

Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data Memory STOP Mode Low-Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$56/f_{CC}$		μs
		Release by interrupt request		$512/f_{CC}$		μs

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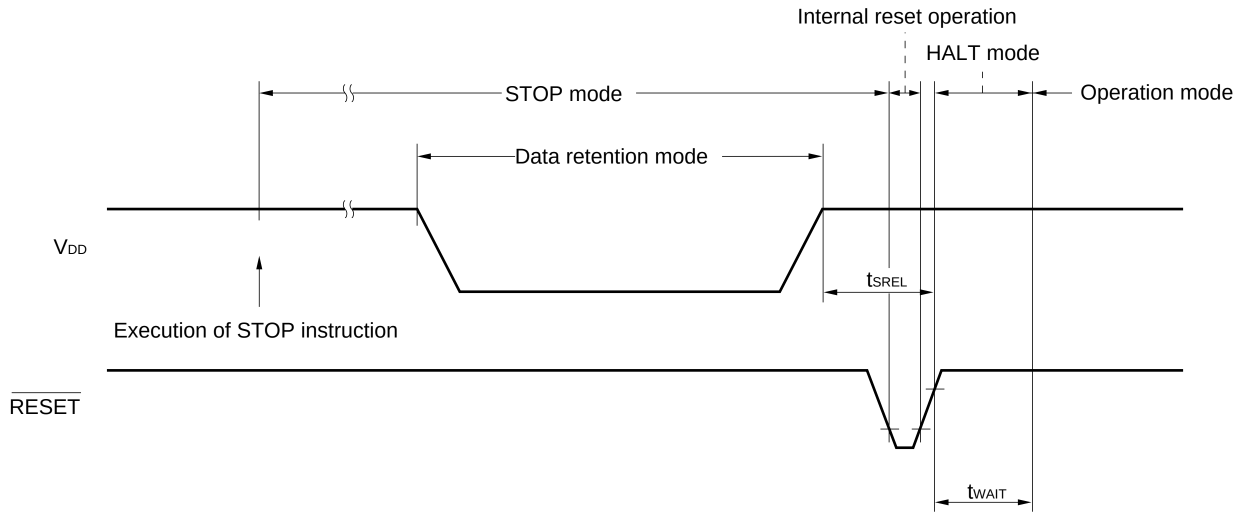
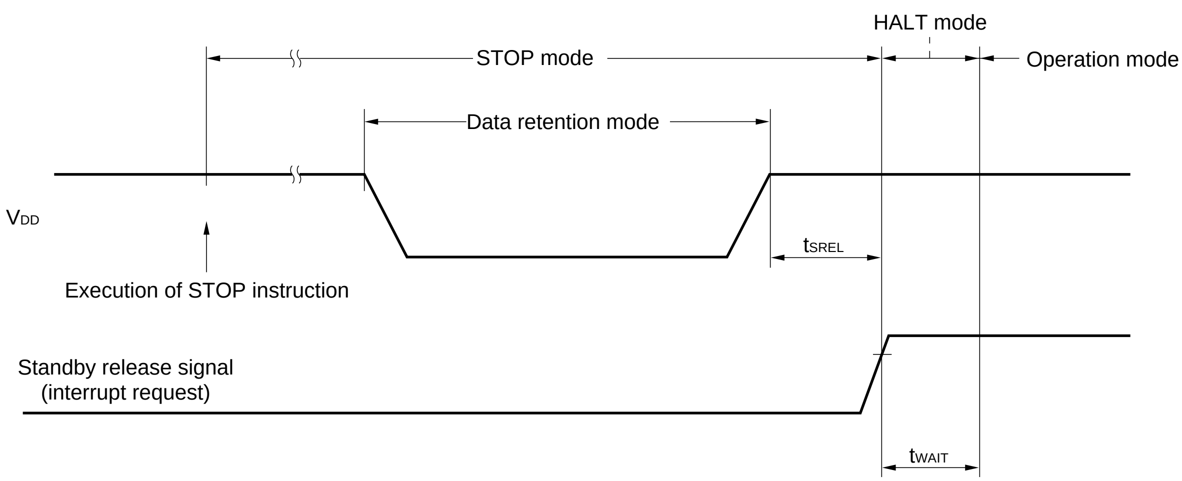
Data Retention Timing (on releasing STOP mode by $\overline{\text{RESET}}$)



Data Retention Timing (Standby release signal: on releasing STOP mode by interrupt signal)



13.2 μPD754244

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Power supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	P30, P31, P33, P60 to P63, P80	–10	mA
			P32	–20	mA
		For all pins		–30	mA
Output current, low	I_{OL} Note	Per pin		20	mA
		For all pins		90	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V			15	pF
I/O capacitance	C_{IO}				15	pF

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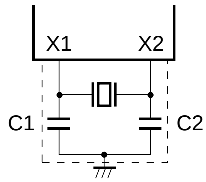
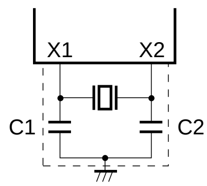
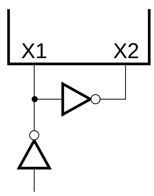
System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Resonator	Recommended Constant	Parameter	Testing Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note1		1.0		6.0 Notes2, 3, 4	MHz
		Oscillation stabilization time Note 5	After V_{DD} reaches MIN. value of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency(f_X) Note1		1.0		6.0 Notes2, 3, 4	MHz
		Oscillation stabilization time Note3	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) Note1		1.0		6.0 Notes2, 3, 4	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

2. If the oscillation frequency is 2.1 MHz < f_X ≤ 4.19 MHz at 1.8 V ≤ V_{DD} < 2.0 V, set the processor control register (PCC) to a value other than 0011. If the PCC is set to 0011, the rated machine cycle time of 1.9 μs is not satisfied.

3. If the oscillation frequency is 4.19 MHz < f_X ≤ 6.0 MHz at 1.8 V≤ V_{DD} < 2.0 V, set the processor control register (PCC) to a value other than 0011 or 0010. If the PCC is set to 0011 or 0010, the rated machine cycle time of 1.9 μs is not satisfied.

4. If the oscillation frequency is 4.19 MHz < f_X ≤ 6.0 MHz at 2.0 V≤ V_{DD} < 2.7 V, set the processor control register (PCC) to a value other than 0011. If the PCC is set to 0011, the rated machine cycle time of 0.95 μs is not satisfied.

5. Oscillation stabilization time is a time required for oscillation to stabilize after application of V_{DD}, or after the STOP mode has been released.

Caution When using the oscillation circuit of the system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wire length as short as possible.**
- **Do not cross other signal lines.**
- **Do not route the wiring in the vicinity of lines though which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit as the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

• **μPD754244**

Recommended Oscillator Constants

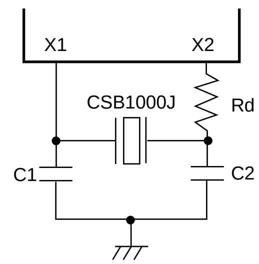
Ceramic resonator (T_A = –20 to +80°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MN. (V)	MAX. (V)	
Kyocera	KBR-1000F/Y	1.0	100	100	1.8	6.0	—
	KBR-2.0MS	2.0	47	47			
	KBR-4.19MSB	4.19	33	33			
	KBR-4.19MKC		—	—			Model with capacitor
	PBRC4.19A		33	33			—
	PBRC4.19B		—	—			Model with capacitor
	KBR-6.0MSB	6.0	33	33			—
	KBR-6.0MKC		—	—			Model with capacitor
	PBRC6.00A		33	33			—
	PBRC6.00B		—	—			Model with capacitor

Ceramic resonator (T_A = –40 to +80°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J Note	1.0	100	100	2.0	6.0	Rd = 2.2 kΩ
	CSA2.00MG040	2.0					—
	CST2.00MG040		—	—			Model with capacitor
	CSA4.19MG	4.19	30	30	1.9		—
	CST4.19MGW		—	—			Model with capacitor
	CSA4.19MGU		30	30	1.8		—
	CST4.19MGWU		—	—			Model with capacitor
	CSA6.00MG	6.0	30	30	2.5		—
	CST6.00MGW		—	—			Model with capacitor
	CSA6.00MGU		30	30	1.8		—
	CST6.00MGWU		—	—			Model with capacitor
TDK	CCR1000K2	1.0	100	100	2.0		—
	CCR4.19MC3	4.19	—	—			Model with capacitor
	FCR4.19MC5						
	CCR6.0MC3	6.0					
	FCR6.0MC5						

Note When using the CSB1000J (1.0 MHz) made by Murata Mfg. Co., Ltd. as a ceramic resonator, a limiting resistor (Rd = 2.2 kΩ) is necessary (refer to the figure below). This resistor is not necessary when using the other recommended resonators.



Caution **The oscillator constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the oscillator in the actual circuit. Please contact directly the manufacturer of the resonator to be used.**

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DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output current	I_{OH}	Per pin	P30, P31, P33, P60 to P63, P80			–5	mA
			P32, V_{DD} = 3.0 V, V_{OH} = V_{DD} – 2.0 V		–7	–15	mA
		Total of all pins				–20	mA
Low-level output current	I_{OL}	Per pin				15	mA
		Total of all pins				45	mA
High-level input voltage	V_{IH1}	Port 3	2.7 V ≤ V_{DD} ≤ 6.0 V	0.7V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 6 to 8, KRREN, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	X1		V_{DD} – 0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Port 3	2.7 V ≤ V_{DD} ≤ 6.0 V	0		0.3V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 6 to 8, KRREN, $\overline{\text{RESET}}$	2.7 V ≤ V_{DD} ≤ 6.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IH3}	X1		0		0.1	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1.0 mA		V_{DD} – 1.0			V
		V_{DD} = 1.8 to 6.0 V, I_{OH} = –100 μA		V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	V_{DD} = 4.5 to 6.0 V	Port 3, I_{OL} = 15 mA		0.6	2.0	V
			Ports 6, 8, I_{OL} = 1.6 mA			0.4	V
		V_{DD} = 1.8 to 6.0 V, I_{OH} = 400 μA				0.5	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1			3.0	μA
	I_{LIH2}		X1			20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Pins other than X1			–3.0	μA
	I_{LIH2}		X1			–20	μA
High-level output leakage current	I_{LOH}	V_{OUT} = V_{DD}				3.0	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3.0	μA
On-chip pull-up resistance	R_{L1}	V_{IN} = 0 V	Port 3, 6, 8	50	100	200	kΩ
	R_{L2}		Port 7, $\overline{\text{RESET}}$ (mask option)	50	100	200	kΩ

• **μPD754244**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="4">Conditions</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th></tr>
<tr><td rowspan="8">Power supply current Note 1</td><td rowspan="2">I_{DD1}</td><td rowspan="4">4.19-MHz crystal oscillation C1 = C2 = 22 pF</td><td colspan="3">V_{DD} = 5.0 V ± 10% Note 2</td><td></td><td>1.5</td><td>5.0</td><td>mA</td></tr>
<tr><td colspan="3">V_{DD} = 3.0 V ± 10% Note 3</td><td></td><td>0.23</td><td>1.0</td><td>mA</td></tr>
<tr><td rowspan="2">I_{DD2}</td><td rowspan="2">HALT mode</td><td colspan="2">V_{DD} = 5.0 V ± 10%</td><td></td><td>0.64</td><td>3.0</td><td>mA</td></tr>
<tr><td colspan="2">V_{DD} = 3.0 V ± 10%</td><td></td><td>0.20</td><td>0.9</td><td>mA</td></tr>
<tr><td rowspan="4">I_{DD3}</td><td rowspan="4">X1 = 0 V STOP mode</td><td colspan="2" rowspan="2">V_{DD} = 1.8 to 6.0 V</td><td></td><td></td><td></td><td>5</td><td>μA</td></tr>
<tr><td>T_A = 25°C</td><td></td><td></td><td>1</td><td>μA</td></tr>
<tr><td colspan="2" rowspan="2">V_{DD} = 3.0 V ± 10%</td><td></td><td></td><td>0.1</td><td>3</td><td>μA</td></tr>
<tr><td>T_A = –40 to +40°C</td><td></td><td>0.1</td><td>1</td><td>μA</td></tr>
</table>

★

Notes 1. The current flowing through the on-chip pull-up resistor, the current during EEPROM writing time, and the current during the program threshold port (PTH) operation are not included.

2. When the device is operated in the high-speed mode by setting the processor clock control register (PCC) to 0011H

3. When the device is operated in the low-speed mode by setting PCC to 0000H

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AC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

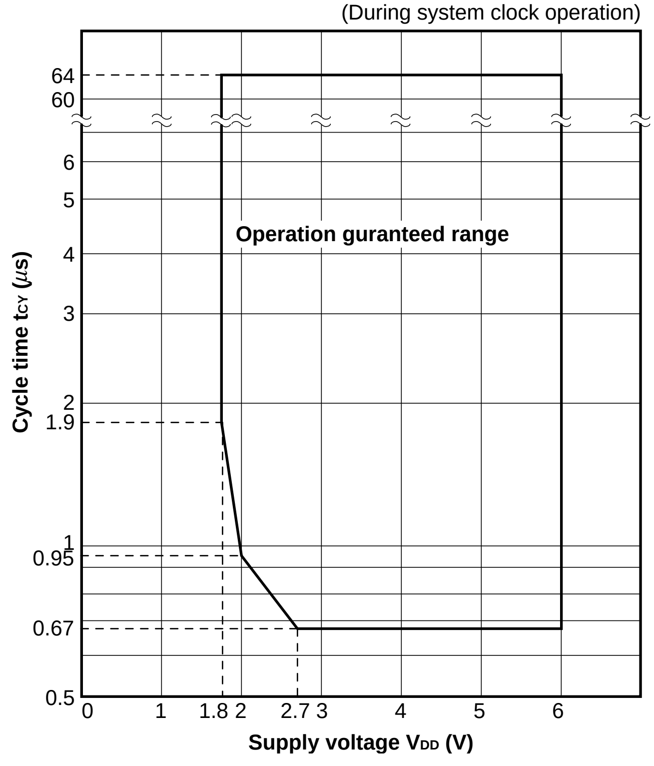
Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note 1 (Minimum instruction execution time = 1 machine cycle)	t_{CY}	V_{DD} = 1.8 to 2.0 V		1.9		64.0	μs
		V_{DD} = 2.0 to 2.7 V		0.95		64.0	μs
		V_{DD} = 2.7 to 6.0 V		0.67		64.0	μs
Interrupt input high- and low-level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		KR4 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator (or external clock) and the processor clock control register (PCC). The figure on the right shows the cycle time t_{CY} characteristics against the supply voltage V_{DD} when the system clock is used.

2. $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).

t_{CY} vs. V_{DD}

(During system clock operation)



- μ**PD754244**

EEPROM Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
EEPROM write current	I_{EEW}	4.19 MHz, crystal oscillation	V_{DD} = 5.0 V ± 10%		4.5	15	mA
			V_{DD} = 3.0 V ± 10%		2.0	6	mA
EEPROM write time	t_{EEW}			3.8		10.0	ms
EEPROM write times	EEWT	T_A = –40 to +70°C		100000			times/byte
		T_A = –40 to +85°C		80000			times/byte

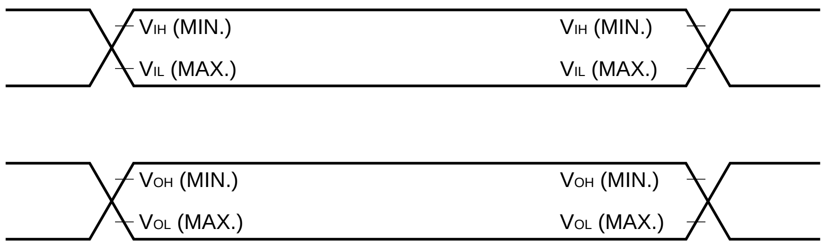
Comparator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 6.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		**Note**		**Note**	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
AV_{REF} input voltage	V_{IAVREF}		1.8		V_{DD}	V
Comparator circuit current consumption	I_{DD5}	When bit 7 of PTHM is set to 1		1		mA

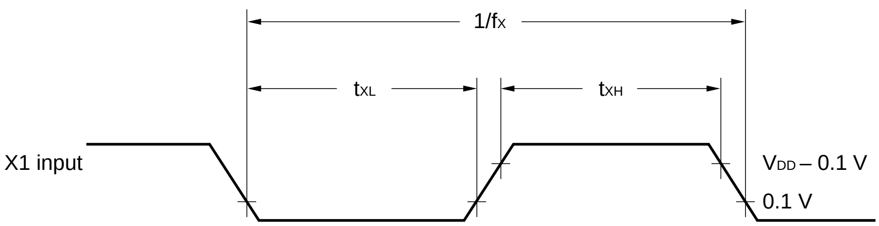
Note The threshold voltage becomes as follows by settings bits 0 to 3 of PTHM.
$V_{TH} = V_{IAVREF}$ x (n + 0.5)/16 (n = 0 to 15)

• μPD754244

AC Timing Test Points (Excluding X1 Input)

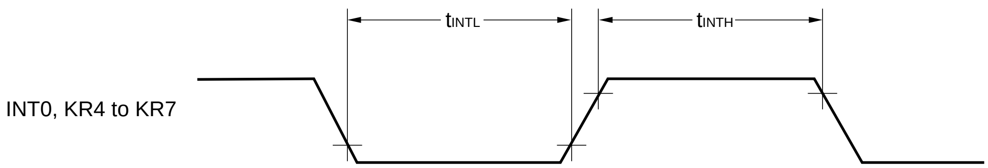


Clock Timing

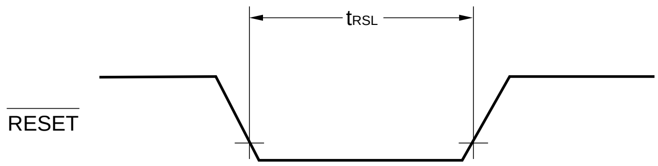


• μPD754244

Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Data Memory STOP Mode Low-Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Release by $\overline{\text{RESET}}$		**Note 2**		ms
		Release by interrupt request		**Note 3**		ms

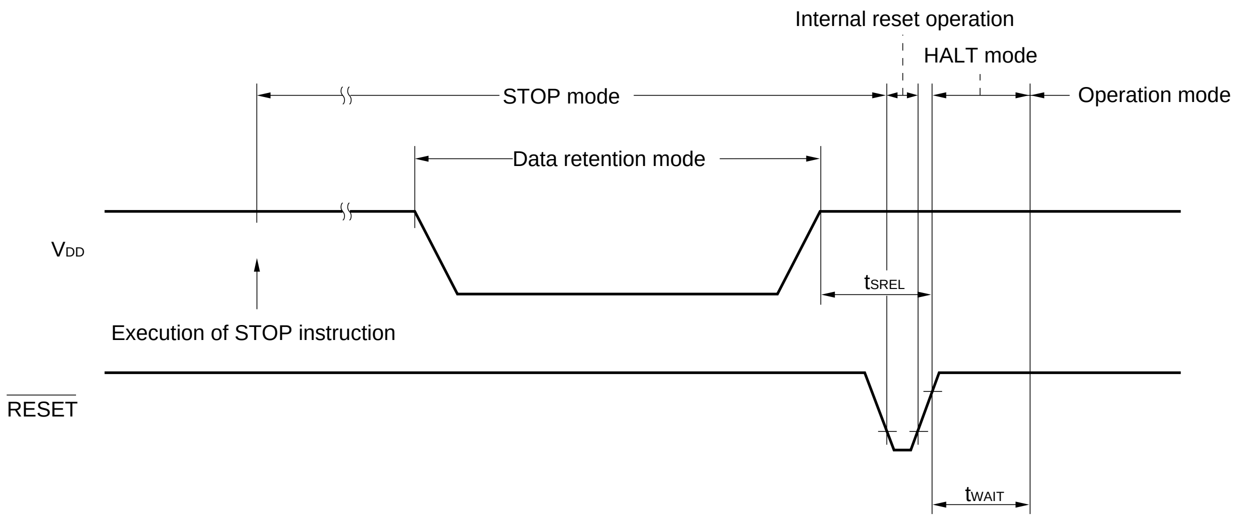
Notes 1. The oscillation stabilization wait time is the time during which the CPU operation is stopped to avoid unstable operation at oscillation start.

2. 2^{17}/fx and 2^{15}/fx can be selected with mask option.

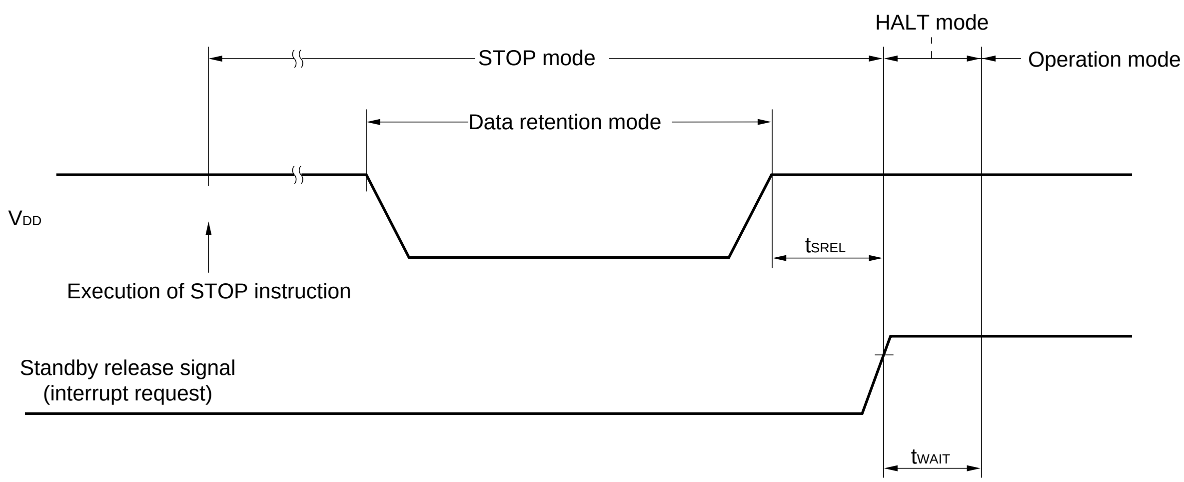
3. Depends on setting of basic interval timer mode register (BTM) (see table below).

BTM3	BTM2	BTM1	BTM0	Wait Time	
				When f_X = 4.19 MHz	When f_X = 6.0 MHz
–	0	0	0	$2^{20}/f_X$ (Approx. 250 ms)	$2^{20}/f_X$ (Approx. 175 ms)
–	0	1	1	$2^{17}/f_X$ (Approx. 31.3 ms)	$2^{17}/f_X$ (Approx. 21.8 ms)
–	1	0	1	$2^{15}/f_X$ (Approx. 7.81 ms)	$2^{15}/f_X$ (Approx. 5.46 ms)
–	1	1	1	$2^{13}/f_X$ (Approx. 1.95 ms)	$2^{13}/f_X$ (Approx. 1.37 ms)

Data Retention Timing (on releasing STOP mode by $\overline{\text{RESET}}$)

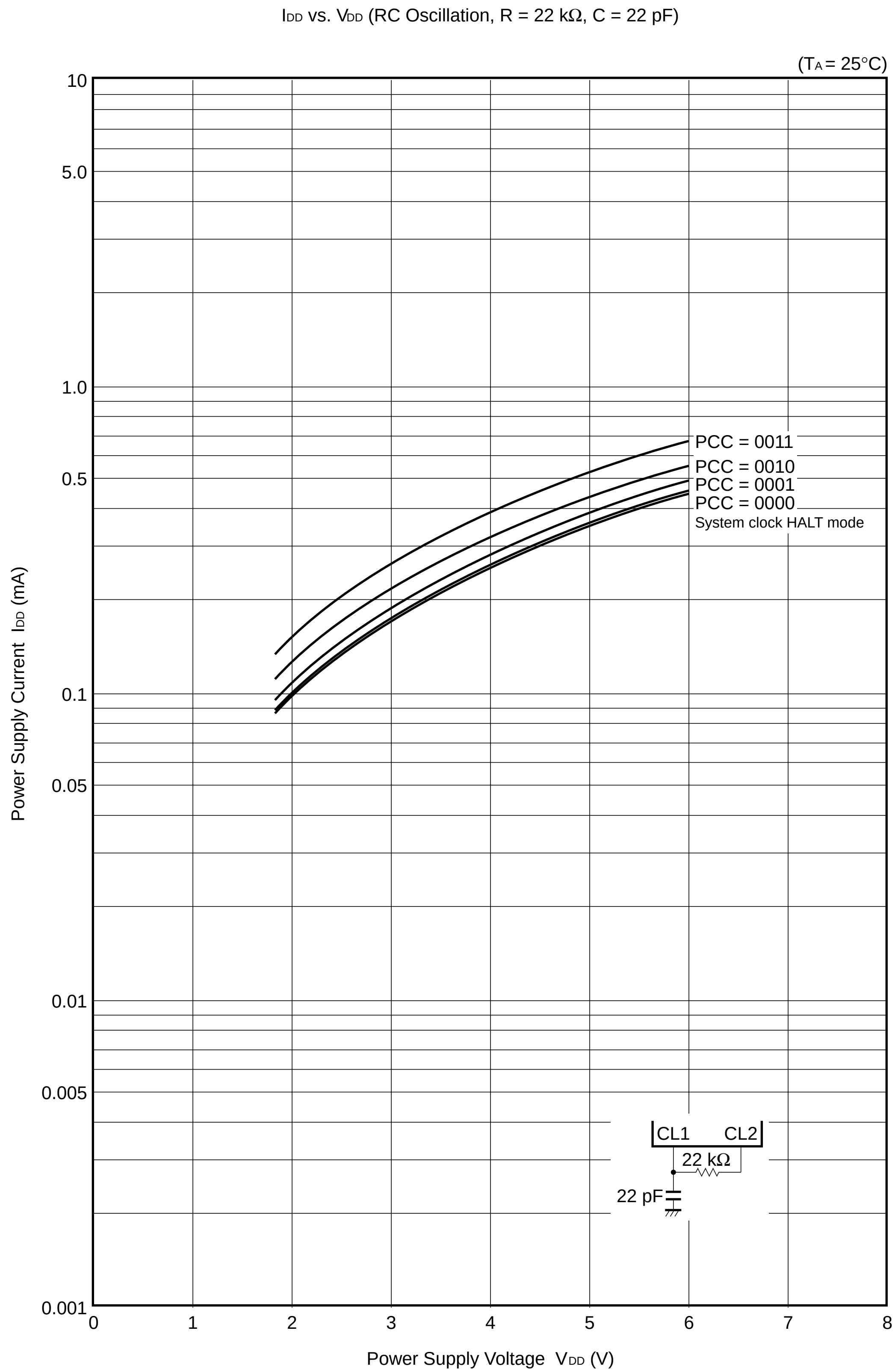


Data Retention Timing (Standby release signal: on releasing STOP mode by interrupt signal)

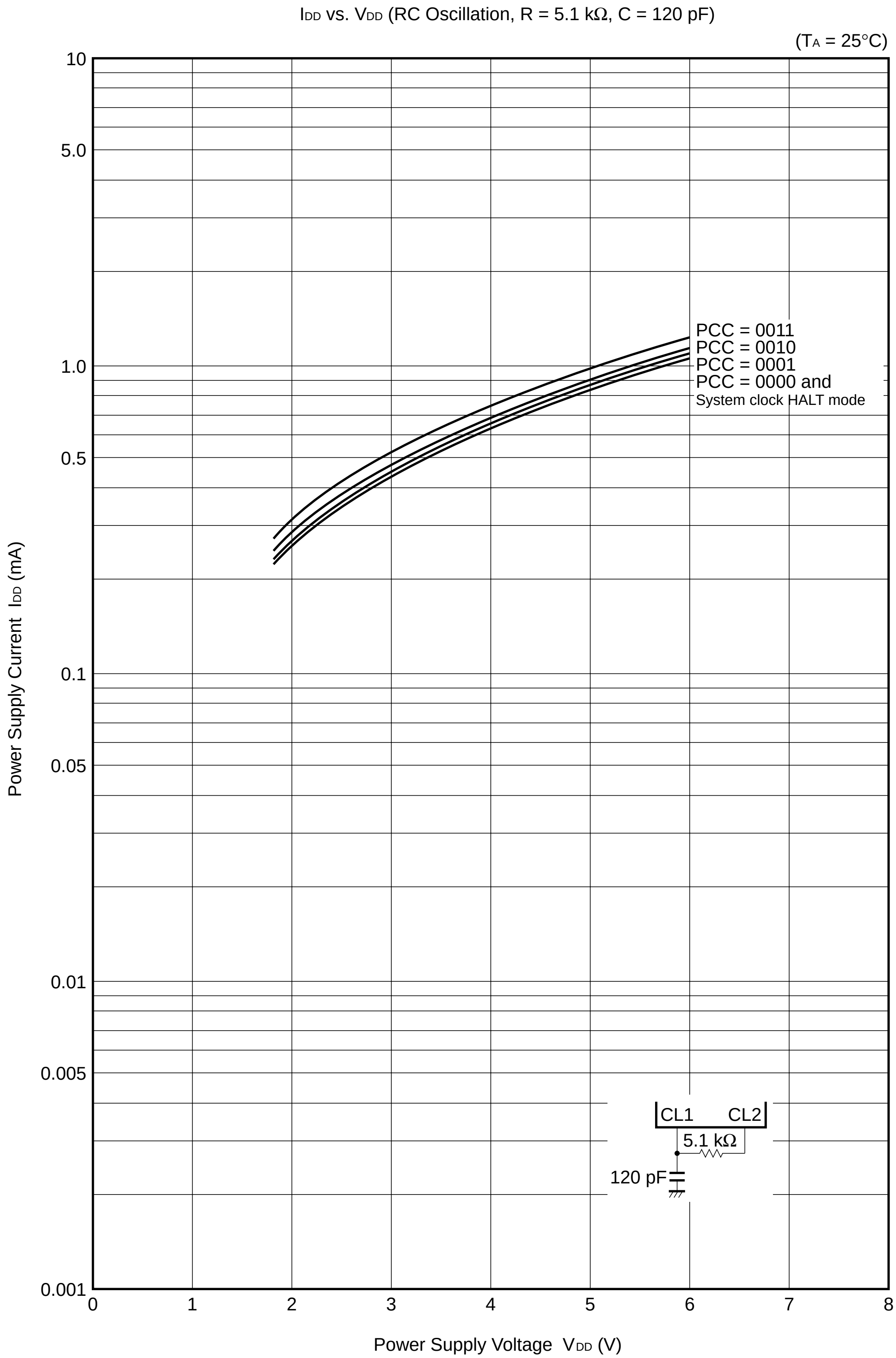


14. CHARACTERISTICS CURVES (REFERENCE VALUES)

14.1 μPD754144

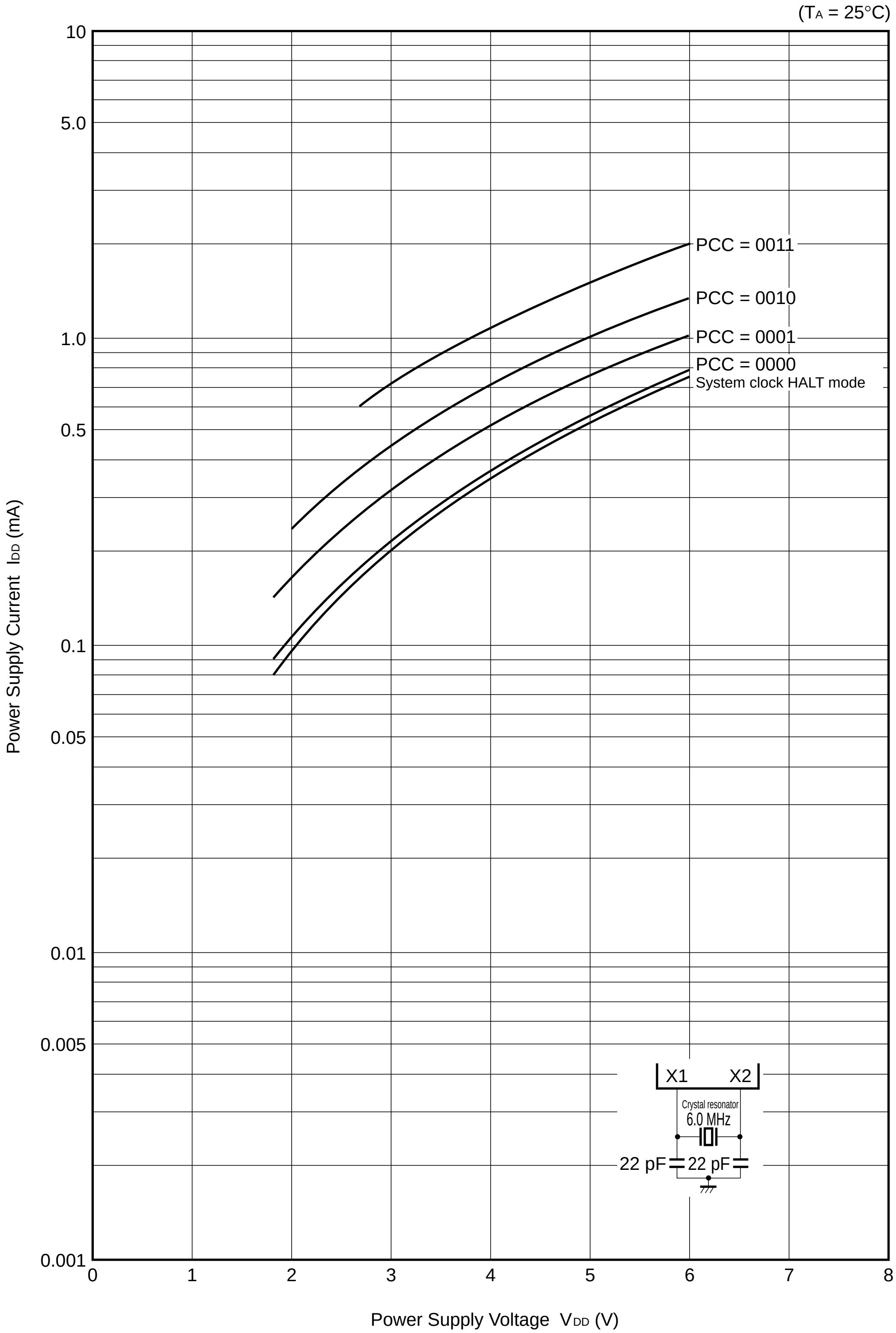


• μPD754144

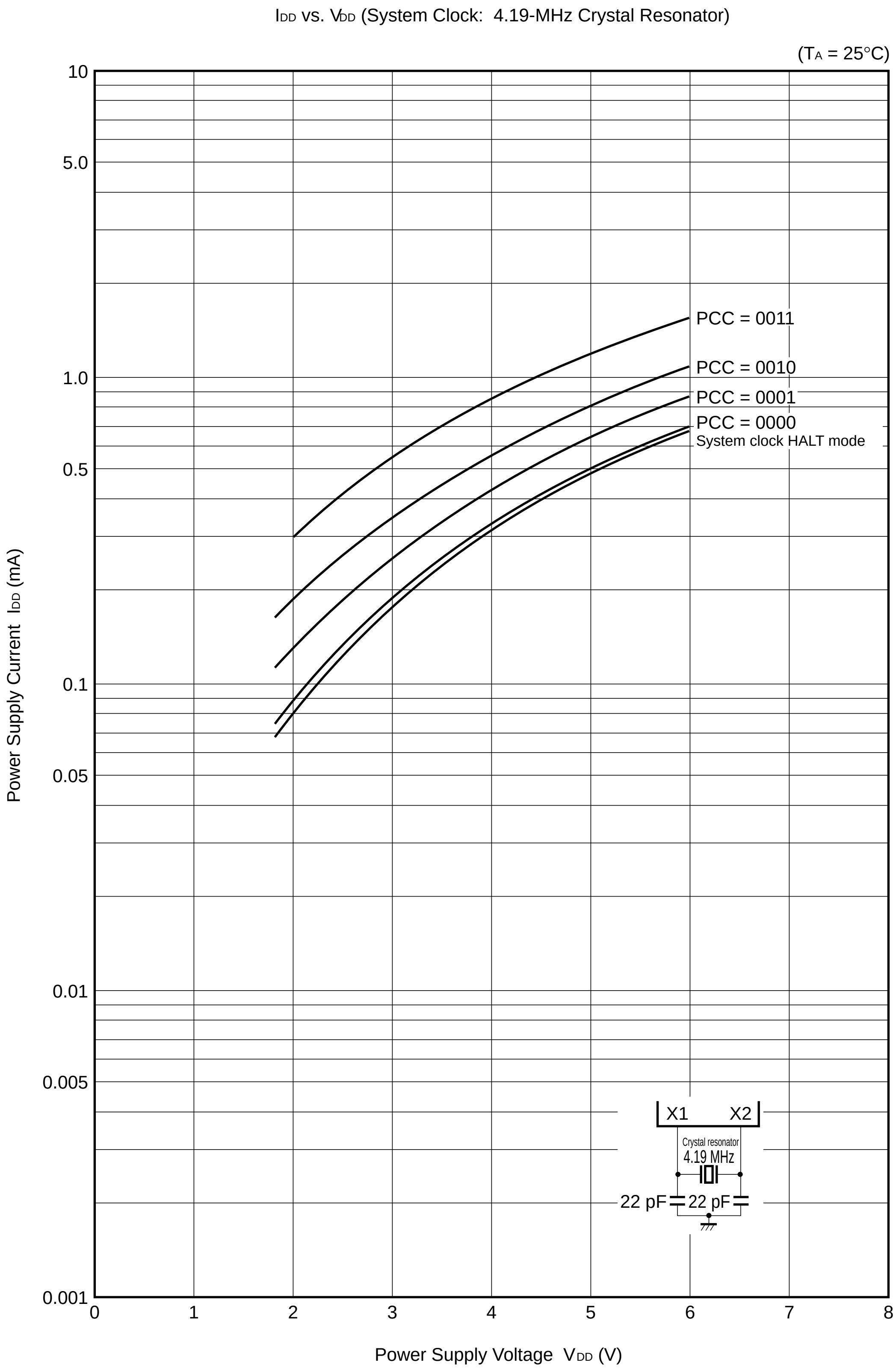

IDD vs. VDD (RC Oscillation, R = 5.1 kΩ, C = 120 pF)
(TA = 25°C)
10
5.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
PCC = 0011
PCC = 0010
PCC = 0001
PCC = 0000 and
System clock HALT mode
CL1
CL2
5.1 kΩ
120 pF
Power Supply Current IDD (mA)
Power Supply Voltage VDD (V)

14.2 μPD754244

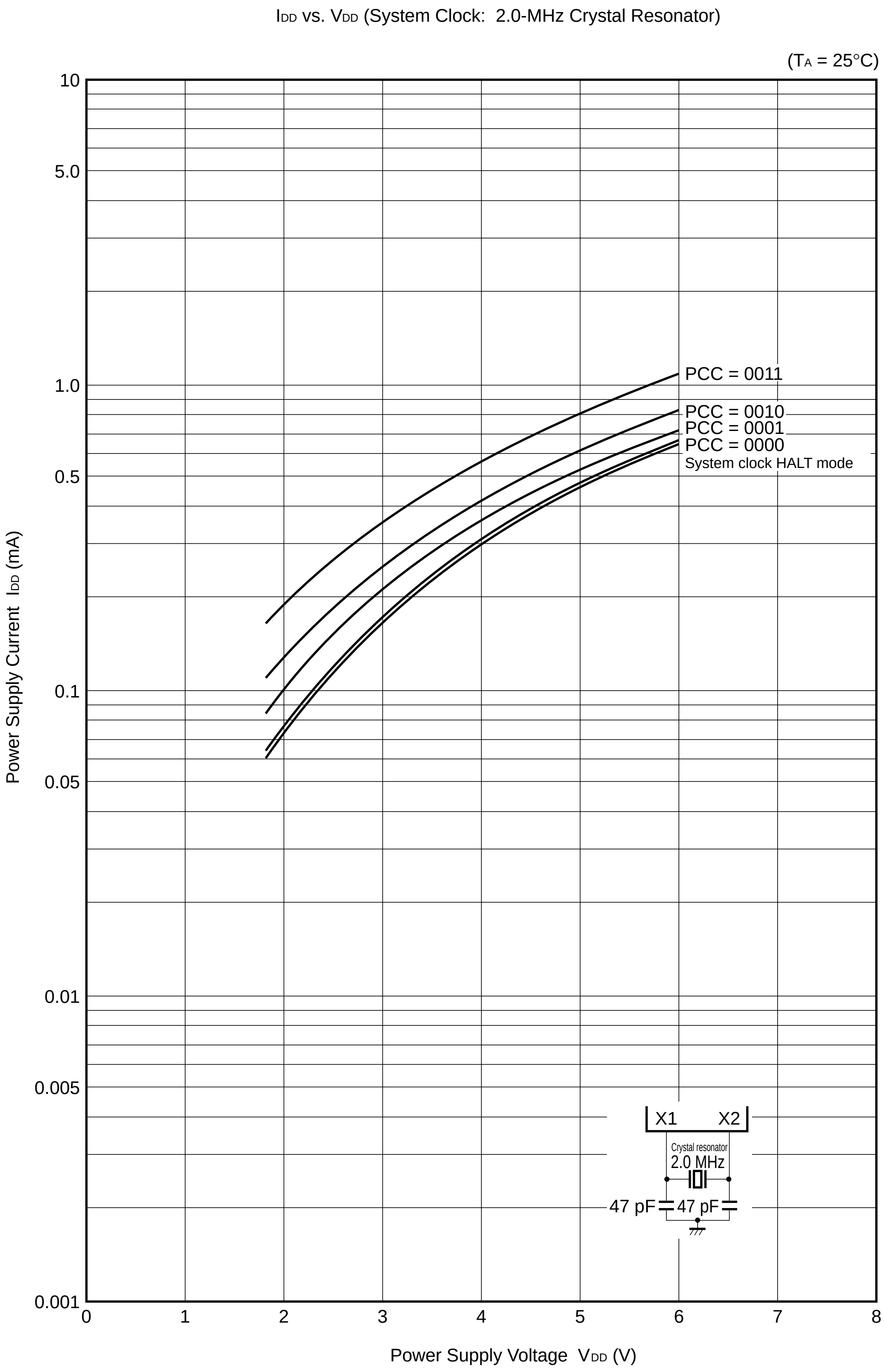
I_{DD} vs. V_{DD} (System Clock: 6.0-MHz Crystal Resonator)



• μPD754244

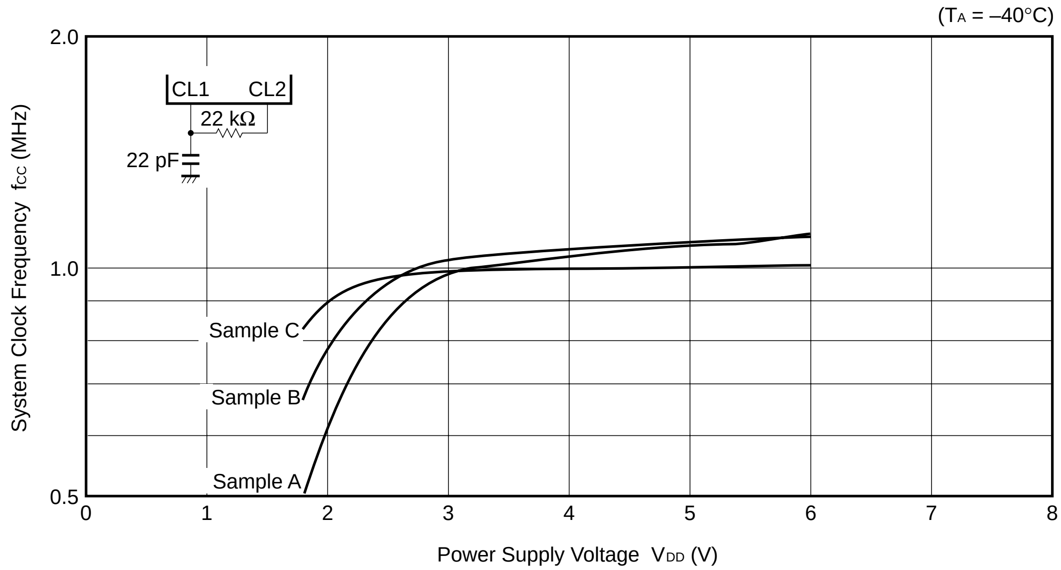

IDD vs. VDD (System Clock: 4.19-MHz Crystal Resonator)
(TA = 25°C)
10
5.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
PCC = 0011
PCC = 0010
PCC = 0001
PCC = 0000
System clock HALT mode
X1
X2
Crystal resonator
4.19 MHz
22 pF
22 pF
Power Supply Current IDD (mA)
Power Supply Voltage VDD (V)

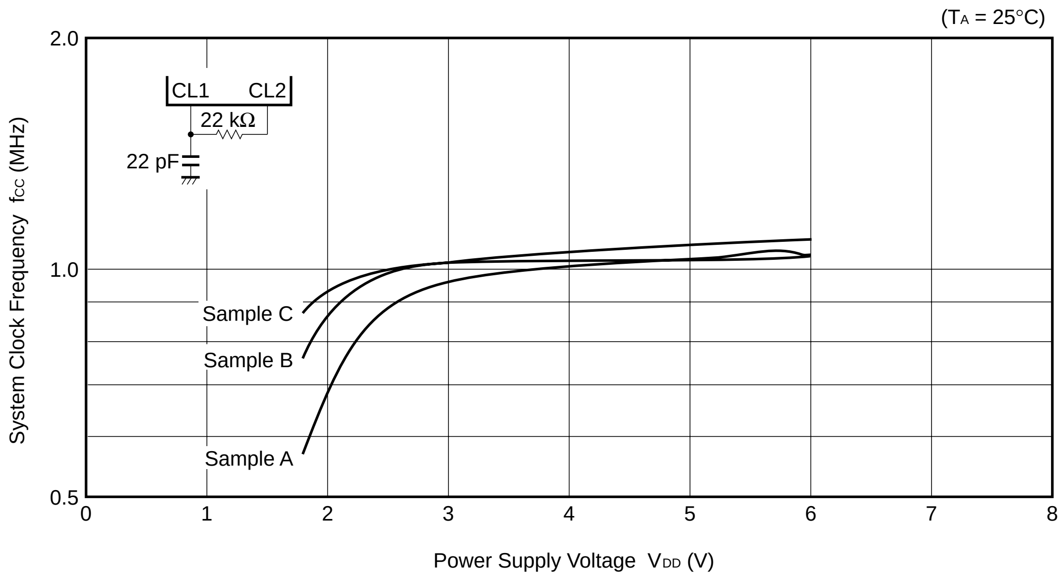
• μPD754244

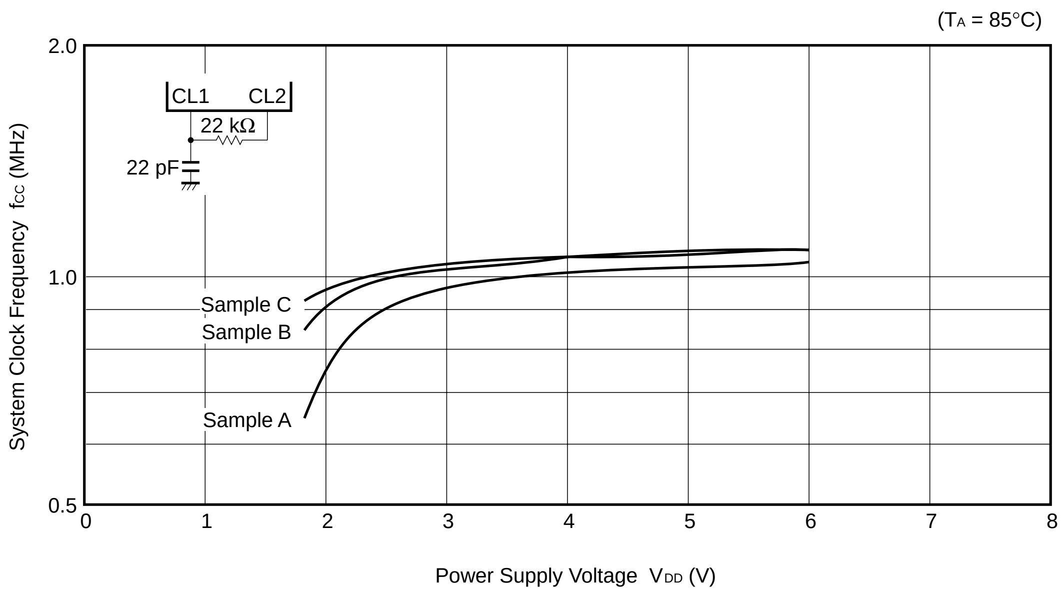

IDD vs. VDD (System Clock: 2.0-MHz Crystal Resonator)
(TA = 25°C)
10
5.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Power Supply Current IDD (mA)
Power Supply Voltage VDD (V)
PCC = 0011
PCC = 0010
PCC = 0001
PCC = 0000
System clock HALT mode
X1
X2
Crystal resonator
2.0 MHz
47 pF
47 pF

15. RC OSCILLATION FREQUENCY CHARACTERISTICS EXAMPLES (REFERENCE VALUES)

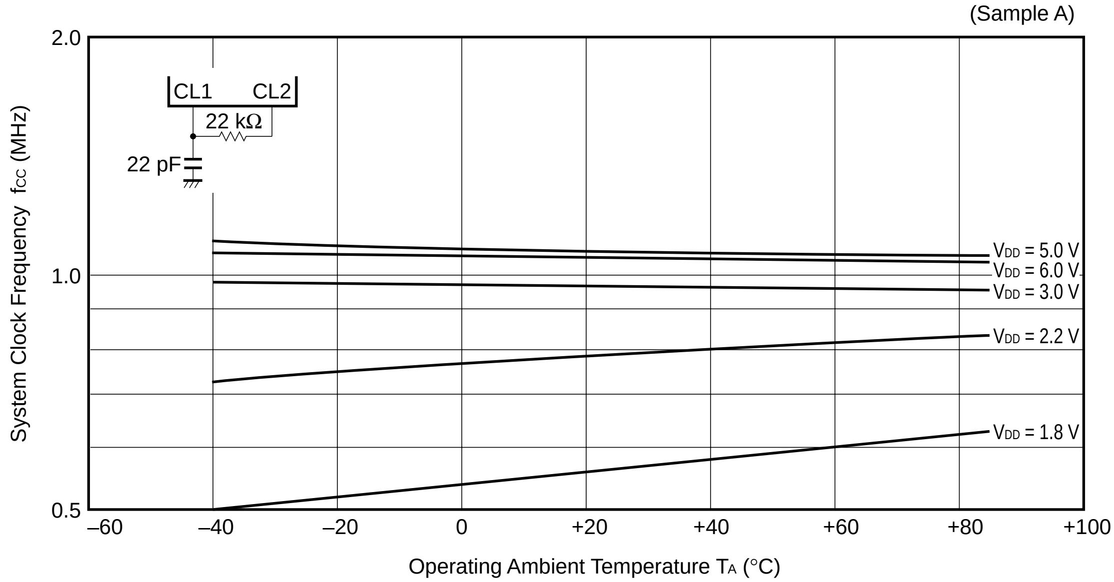
f_{CC} vs. V_{DD} (RC Oscillation, R = 22 kΩ, C = 22 pF)

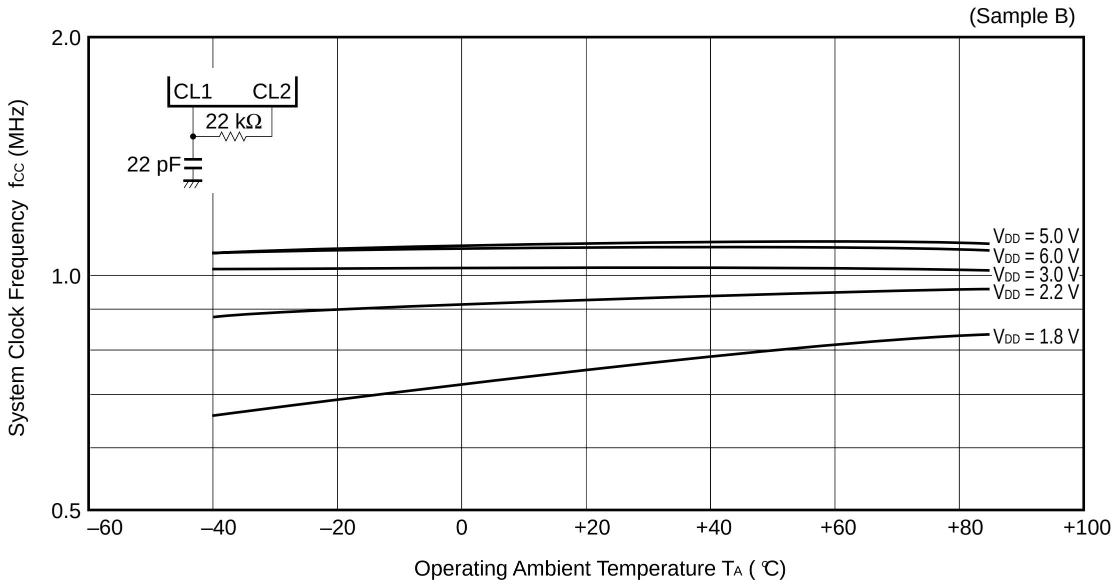


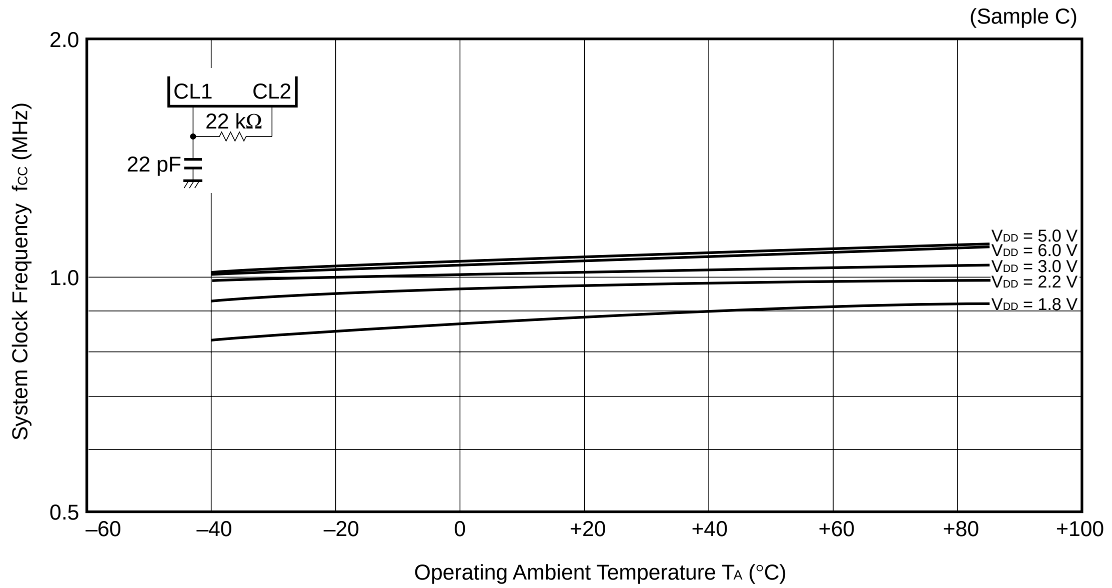




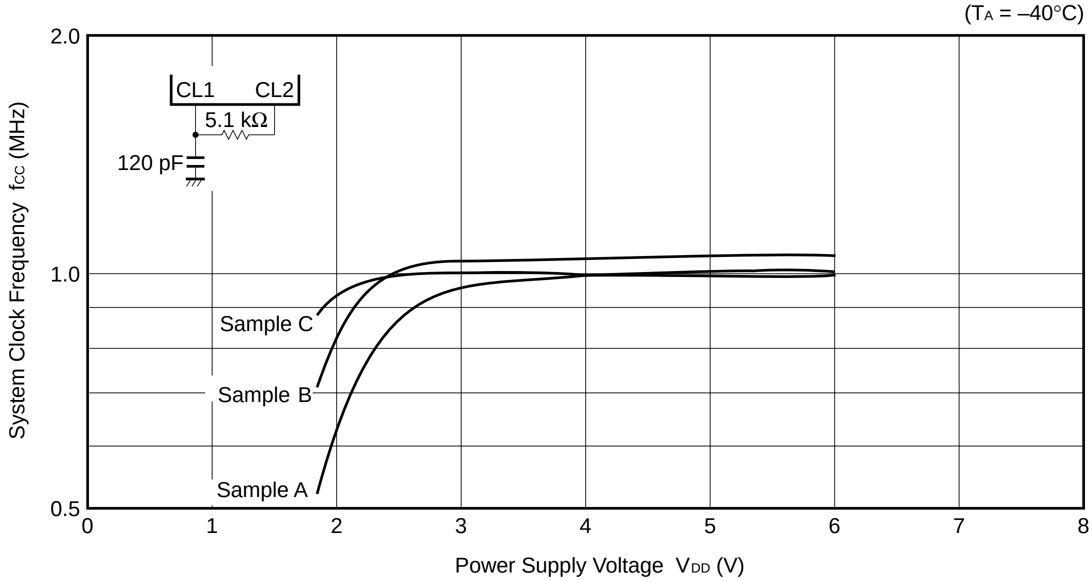
f_{CC} vs. T_A (RC Oscillation, R = 22 kΩ, C = 22 pF)

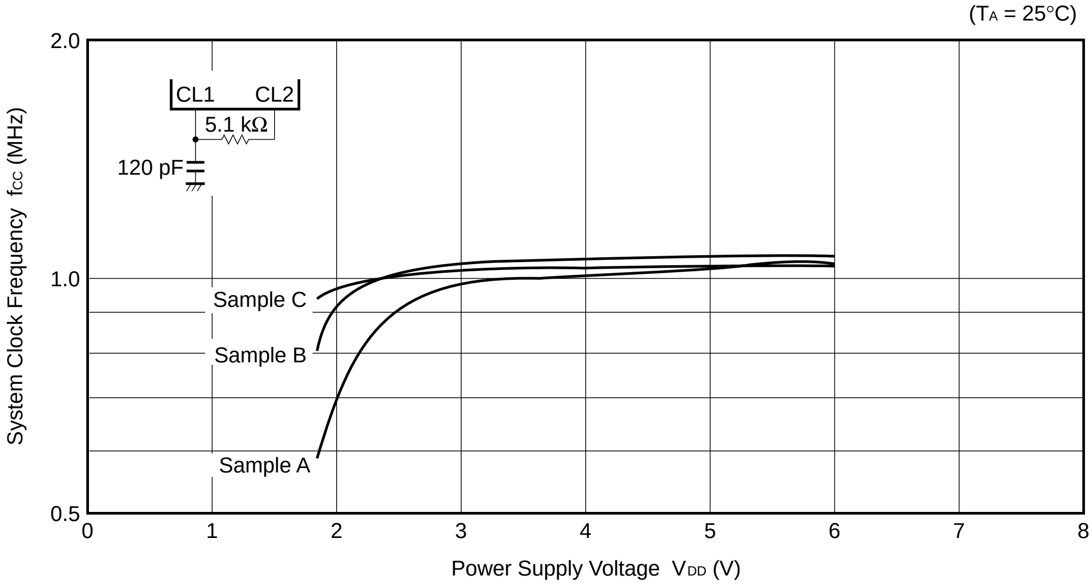


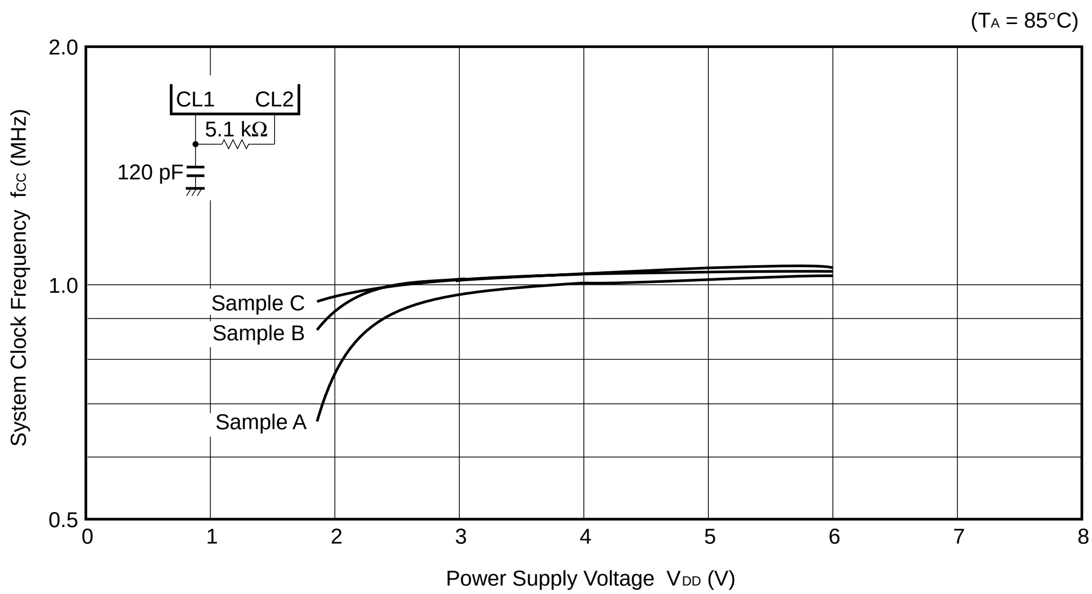




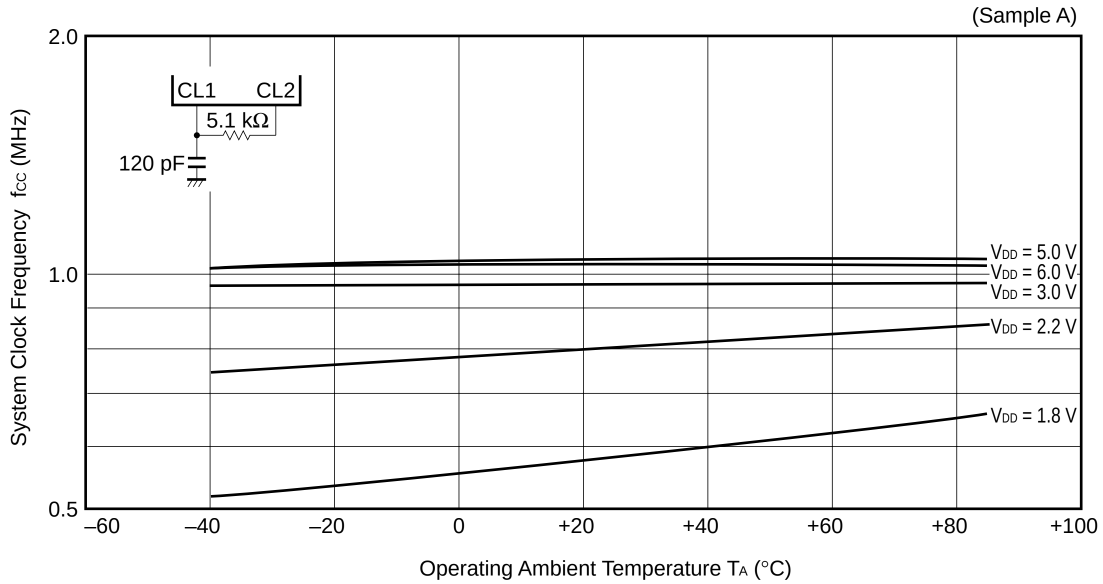
f_{CC} vs. V_{DD} (RC Oscillation, R = 5.1 kΩ, C = 120 pF)

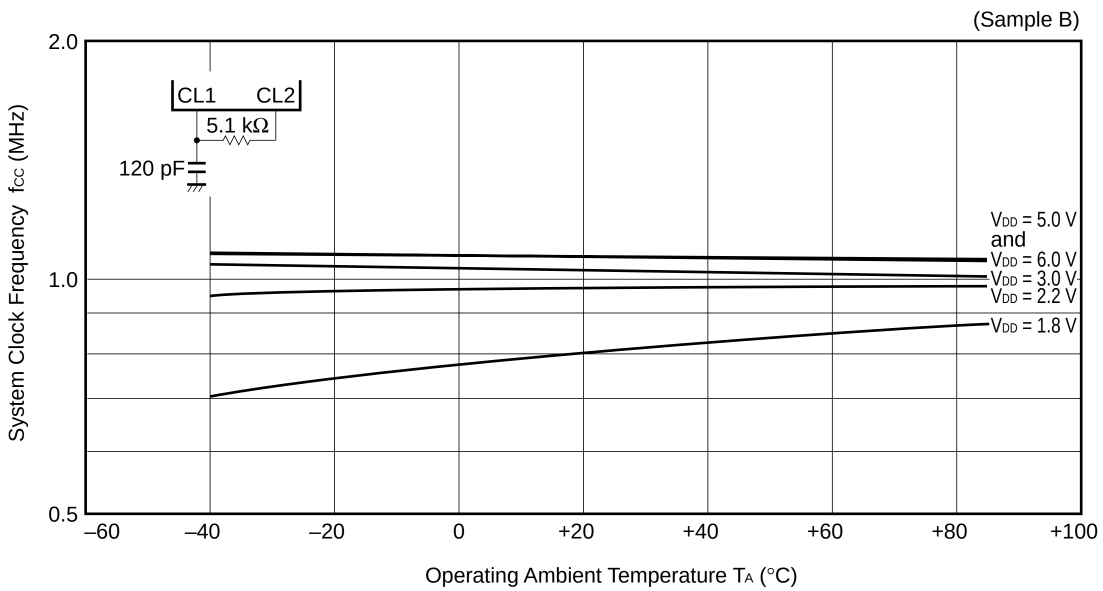


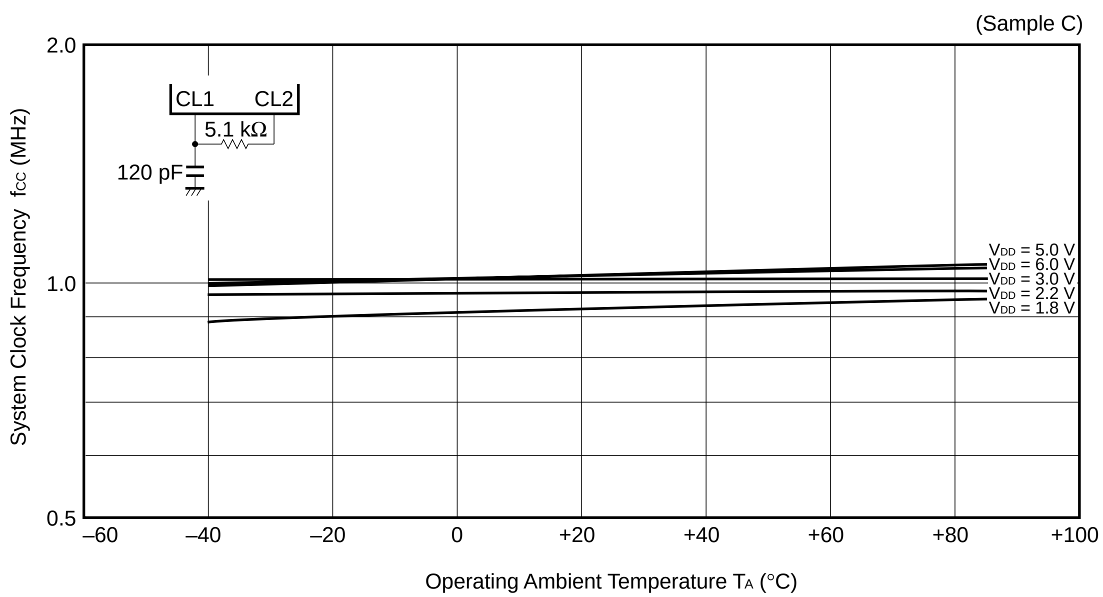




f_{CC} vs. T_A (RC Oscillation, R = 5.1 kΩ, C = 120 pF)

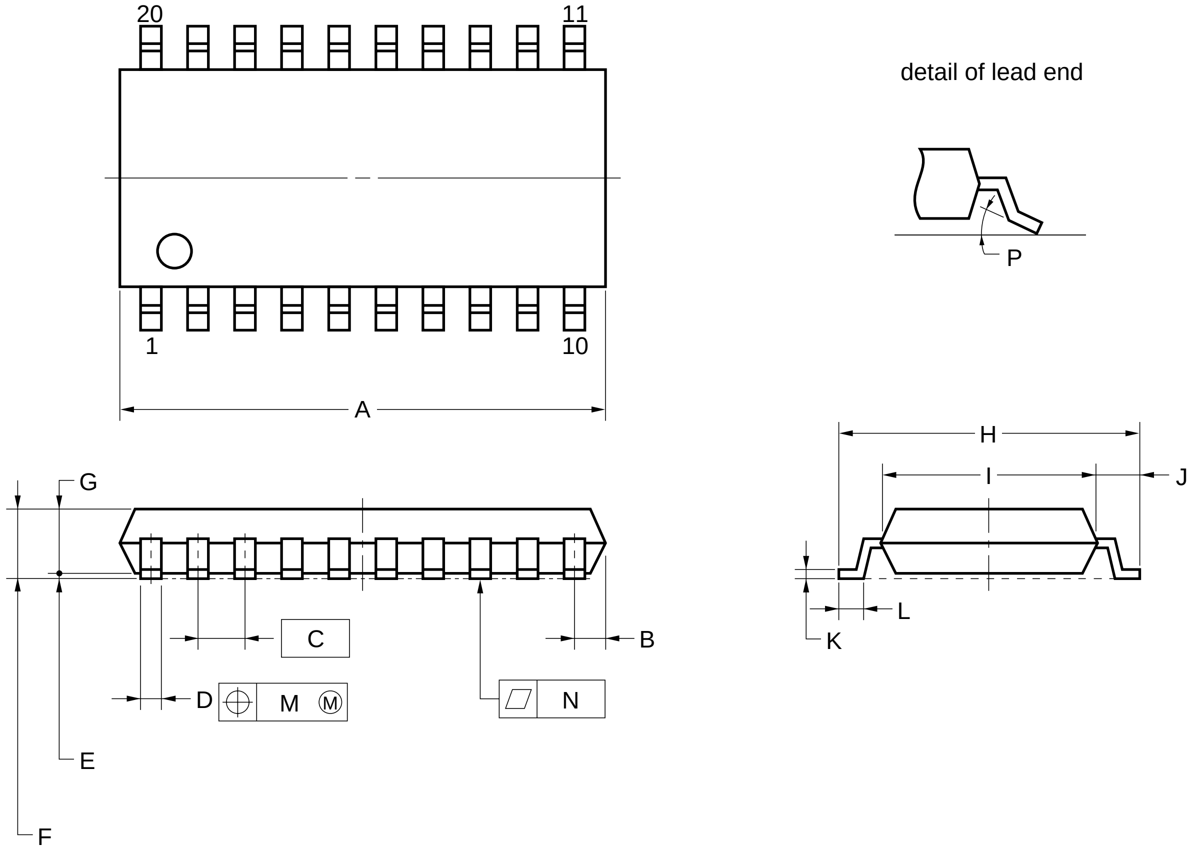






16. PACKAGE DRAWINGS

20-pin Plastic SOP (300 mils)



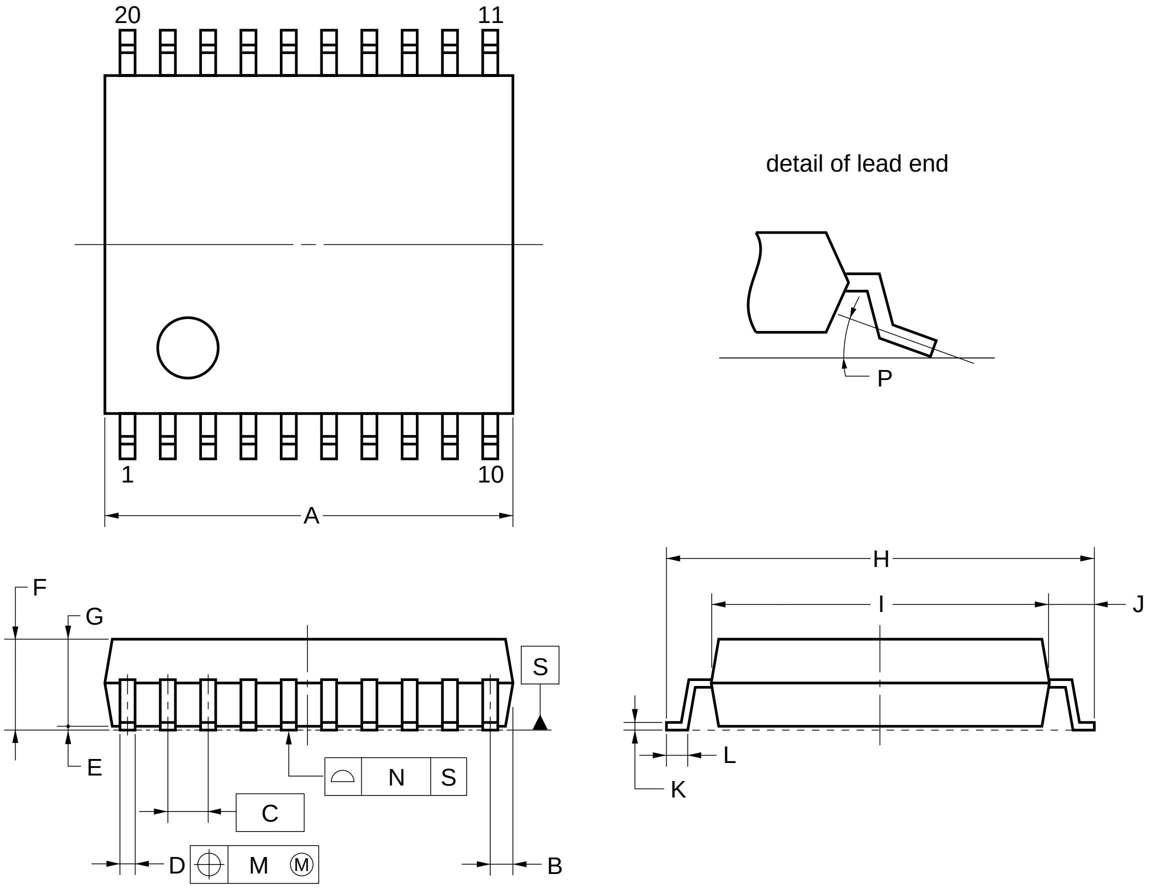
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	12.7±0.3	0.500±0.012
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	$0.017^{+0.003}_{-0.004}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55±0.05	0.061±0.002
H	7.7±0.3	0.303±0.012
I	5.6±0.2	$0.220^{+0.009}_{-0.008}$
J	1.1	0.043
K	$0.22^{+0.08}_{-0.07}$	$0.009^{+0.003}_{-0.004}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P20GM-50-300B, C-5

20-pin Plastic shrink SOP (300 mils)



NOTE

1. Controlling dimension —— millimeter.
2. Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	6.7±0.3	$0.264^{+0.012}_{-0.013}$
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	$0.013^{+0.003}_{-0.004}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	$0.067^{+0.004}_{-0.005}$
H	8.1±0.3	0.319±0.012
I	6.1±0.2	0.240±0.008
J	1.0±0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P20GM-65-300B-3

17. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD754244 under the following recommended conditions.

For the details on the recommended soldering conditions, refer to Information Document **“Semiconductor Device Mounting Technology Manual (C10535E)”**.

For the soldering method and conditions other than those recommended, consult an NEC representative.

Table 17-1. Soldering Conditions of Surface Mount Type (1/2)

(1) μPD754244GS-xxx-GJG: 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds max. (210°C min.), Number of reflow process: 2 max.	IR35-00-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds max. (200°C min.), Number of reflow process: 2 max.	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Flow time: 10 seconds max., Number of flow process: 1 Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	–

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD754144GS-xxx-GJG: 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds max. (210°C min.), Number of reflow process: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds max. (200°C min.), Number of reflow process: 3 max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Flow time: 10 seconds max., Number of flow process: 1 Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 17-1. Soldering Conditions of Surface Mount Type (2/2)

(3) μPD754144GS-xxx-BA5: 20-pin plastic SOP (300 mil, 1.27-mm pitch)
μPD754244GS-xxx-BA5: 20-pin plastic SOP (300 mil, 1.27-mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds max. (210°C min.), Number of reflow process: 2 max. Exposure limit: 7 days[Note] (afterward, 10-hour pre-baking at 125°C is required)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds max. (200°C min.), Number of reflow process: 2 max. Exposure limit: 7 days[Note] (afterward, 10-hour pre-baking at 125°C is required)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Flow time: 10 seconds max., Number of flow process: 1 Preheating temperature: 120°C max. (package surface temperature) Exposure limit: 7 days[Note] (afterward, 10-hour pre-baking at 125°C is required)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	–

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. COMPARISON OF FUNCTIONS AMONG μPD754144, 754244, AND 75F4264

Item		μPD754144	μPD754244	μPD75F4264 Note
Program memory		Mask ROM 0000H to 0FFFH (4096 x 8 bits)		Flash memory 0000H to 0FFFH (4096 x 8 bits)
Data memory	Static RAM	000H to 07FH (128 x 4 bits)		
	EEPROM	400H to 41FH (16 x 8 bits)		400H to 43FH (32 x 8 bits)
CPU		75XL CPU		
General-purpose register		(4 bits x 8 or 8 bits x 4) x 4 banks		
Instruction execution time		• 4, 8, 16, 64 μs (@ f_{CC} = 1.0-MHz operation)	• 0.67, 1.33, 2.67, 10.7 μs (@ f_X = 6.0-MHz operation) • 0.95, 1.91, 3.81, 15.3 μs (@ f_X = 4.19-MHz operation)	
I/O port	CMOS input	4 (on-chip pull-up resistor can be connected by mask option)		
	CMOS I/O	9 (on-chip pull-up resistor connection can be specified by means of software)		
	Total	13		
System clock oscillator		RC oscillator (resistor and capacitor are connected externally)	Ceramic/crystal oscillator	
Start-up time after reset		$56/f_{CC}$	$2^{17}/f_X$, $2^{15}/f_X$ (can be selected by mask option)	$2^{15}/f_X$
Standby mode release time		$2^9/f_{CC}$	$2^{20}/f_X$, $2^{17}/f_X$, $2^{15}/f_X$, $2^{13}/f_X$ (can be selected by the setting of BTM)	
Timer		4 channels • 8-bit timer counter: 3 channels (can be used as 16-bit timer counter) • Basic interval timer/watchdog timer: 1 channel		
A/D converter		None		• 8-bit resolution x 2 channels (successive approximation, hardware control) • Can be operated from V_{DD} = 1.8 V
Programmable threshold port		2 channels		
Vectored interrupt		External: 1, internal: 5		
Test input		External: 1 (key return reset function available)		
Power supply voltage		V_{DD} = 1.8 to 6.0 V		
Operating ambient temperature		T_A = –40 to +85°C		
Package		• 20-pin plastic SOP (300 mil, 1.27-mm pitch) • 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)		• 20-pin plastic SOP (300 mil, 1.27-mm pitch)

Note Under development

APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD754244.

In the 75XL series, the relocatable assembler which is common to the series is used in combination with the device file of each product.

Language processor

RA75X relocatable assembler	Host machine	OS	Distribution media	Part number (product name)
	PC-9800 series	MS-DOS™ (Ver. 3.30 to Ver. 6.2Note)	3.5-inch 2HD	μS5A13RA75X
			5-inch 2HD	μS5A10RA75X
	IBM PC/AT™ and compatible machines	Refer to "**OS for IBM PC**"	3.5-inch 2HC	μS7B13RA75X
			5-inch 2HC	μS7B10RA75X

Device file	Host machine	OS	Distribution media	Part number (product name)
	PC-9800 series	MS-DOS (Ver. 3.30 to Ver. 6,2Note)	3.5-inch 2HD	μS5A13DF754244
			5-inch 2HD	μS5A10DF754244
	IBM PC/AT and compatible machines	Refer to "**OS for IBM PC**"	3.5-inch 2HC	μS7B13DF754244
			5-inch 2HC	μS7B10DF754244

Note Ver.5.00 or later have the task swap function, but it cannot be used for this software.

Remark Operation of the assembler and device file are guaranteed only on the above host machine and OSs.

Debugging tool

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD754244.

The system configurations are described as follows.

<table>
<tr><td rowspan="5">Hardware</td><td>IE-75000-R [Note 1]</td><td colspan="4">In-circuit emulator for debugging the hardware and software when developing application systems that use the 75X series and 75XL series. When developing the μPD754244, the emulation board IE-75300-R-EM and emulation probe EP-754144GS-R that are sold separately must be used with the IE-75000-R.
By connecting with the host machine, efficient debugging can be made.
It contains the emulation board IE-75000-R-EM which is connected.</td></tr>
<tr><td>IE-75001-R</td><td colspan="4">In-circuit emulator for debugging the hardware and software when developing application systems that use the 75X series and 75XL series. When developing the μPD754244, the emulation board IE-75300-R-EM and emulation probe EP-754144GS-R which are sold separately must be used with the IE-75001-R.
By connecting the host machine, efficient debugging can be made.</td></tr>
<tr><td>IE-75300-R-EM</td><td colspan="4">Emulation board for evaluating the application systems that use the μPD754244.
It must be used with the IE-75000-R or IE-75001-R.</td></tr>
<tr><td>EP-754144GS-R</td><td colspan="4" rowspan="2">Emulation probe for the μPD754244GS.
It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM.
It is supplied with the flexible boards EV-9500GS-20 (supporting 20-pin plastic shrink SOPs) and EV-9501GS-20 (supporting 20-pin plastic SOPs) which facillitate connection to a target system.</td></tr>
<tr><td>EV-9500GS-20
EV-950IGS-20</td></tr>
<tr><td rowspan="7">Software</td><td rowspan="7">IE control program</td><td colspan="4">Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the above hardware on a host machine.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2"></td><td rowspan="2">Part No.
(product name)</td></tr>
<tr><td>OS</td><td>Distribution media</td></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS
(Ver. 3.30 to Ver. 6.2 [Note 2])</td><td>3.5-inch 2HD</td><td>μS5A13IE75X</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10IE75X</td></tr>
<tr><td rowspan="2">IBM PC/AT and its compatible machine</td><td rowspan="2">Refer to "OS for IBM PC"</td><td>3.5-inch 2HC</td><td>μS7B13IE75X</td></tr>
<tr><td>5-inch 2HC</td><td>μS7B10IE75X</td></tr>
</table>

Notes 1. Maintenance parts

2. Ver.5.00 or later have the task swap function, but it cannot be used for this software.

Remark Operation of the IE control program is guaranteed only on the above host machines and OSs.

OS for IBM PC

The following IBM PC OS's are supported.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.3 J6.1/V[Note] to J6.3/V[Note]
MS-DOS	Ver. 5.0 to Ver. 6.22 5.0/V[Note] to J6.2/V[Note]
IBM DOS™	J5.02/V[Note]

Note Supported only English mode.

Caution Ver. 5.0 and later have the task swap function, but it cannot be used for operating systems above.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device related documents

Document Name	Document Number	
	Japanese	English
μPD754144, 754244 Data Sheet	U10040J	This document
μPD754144, 754244 User's Manual	U10676J	U10676E
75XL Series Selection Guide	U10453J	U10453E

Development tool related documents

Document Name			Document Number	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		U11354J	U11354E
	EP-754144GS-R User's Manual		U10695J	U10695E
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363

Other related documents

Document Name	Document Number	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Static Electricity Discharge (ESD) Test	MEM-539	–
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Microcomputer Related Product Guide - Other Manufacturers	U11416J	–

Caution These documents are subject to change without notice. Be sure to read the latest documents.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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[MEMO]

The μPD754244 is manufactured and sold based on a licence contract with CP8 Transac regarding the EEPROM microcomputer patent.
This product cannot be used for an IC card (SMART CARD).