μPD7507/08
4-Bit, Single-Chip CMOS Microcomputers

Description

The μPD7507 and μPD7508 4-bit, single-chip CMOS microcomputers have the μPD7500 series architecture. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Thirty-two I/O lines are organized into eight 4-bit ports: input port/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, 6, and 7.

The μPD7507 and μPD7508 execute 92 instructions of the μPD7500 series A instruction set with a 5-μs instruction cycle time.

Maximum power consumption is 900 μA at 5 V, less in the HALT and STOP low-power modes.

The μPD75CG08E is a piggyback EPROM prototyping chip that is pin-compatible with μPD7507 and μPD7508. A 2716 inserted into the top of the μPD75CG08E emulates the μPD7507's ROM. A 2732 emulates the μPD7508's ROM. When emulating the μPD7507, the user must take care to use only the first 128 RAM locations. Although the μPD7507 and μPD7508 can operate over a range of 2.5 to 6.0 V, μPD75CG08E operation is limited to 5 V ±10%.

Table 1 summarizes the differences among μPD7507, μPD7508 and μPD75CG08E.

Table 1. Features Comparison

	μPD75CG08E	μPD7507/7508
Program memory	2K x 8 EPROM (2716) 4K x 8 EPROM (2732)	2K x 8 masked ROM (7507) 4K x 8 masked ROM (7508)
Data memory	224 x 4	128 x 4 (7507) 224 x 4 (7508)
Data retention mode	No	Yes
Power supply	5 V ±10%	2.7 to 6.0 V
Package types	40-pin ceramic piggyback DIP	40-pin plastic DIP 40-pin plastic shrink DIP 52-pin plastic QFP

Features

- ☐ Single chip microcomputer
- ☐ Program ROM
  - — μPD7507: 2048 x 8-bit
  - — μPD7508: 4096 x 8-bit
  - — μPD75CG08: piggyback EPROM
- ☐ Data RAM
  - — μPD7507: 128 x 4-bit
  - — μPD7508: 224 x 4-bit
  - — μPD75CG08: 224 x 4-bit
- ☐ 8-bit timer/event counter
- ☐ Four 4-bit general purpose registers
- ☐ Four vectored, prioritized interrupts
- ☐ Executes 92 instructions of μPD7500 series A instruction set
- ☐ 5 μs instruction cycle/400 kHz external clock
- ☐ Two standby modes
- ☐ 32 I/O lines
- ☐ Low-power HALT and STOP modes

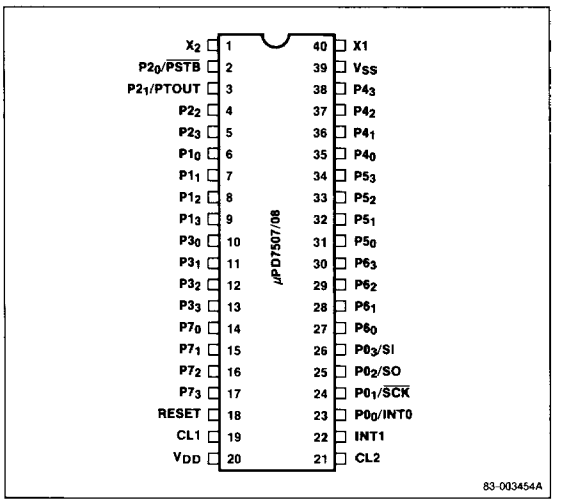
Ordering Information

*Part Number	Package Type	Max Frequency of Operation
μPD7507C	40-pin plastic DIP	410 kHz
μPD7507CU	40-pin plastic shrink DIP	410 kHz
μPD7507GC-00	52-pin plastic QFP	410 kHz
μPD7508C	40-pin plastic DIP	410 kHz
μPD7508CU	40-pin plastic shrink DIP	410 kHz
μPD7508GC-00	52-pin plastic QFP	410 kHz
μPD75CG08E	40-pin ceramic piggyback DIP	410 kHz

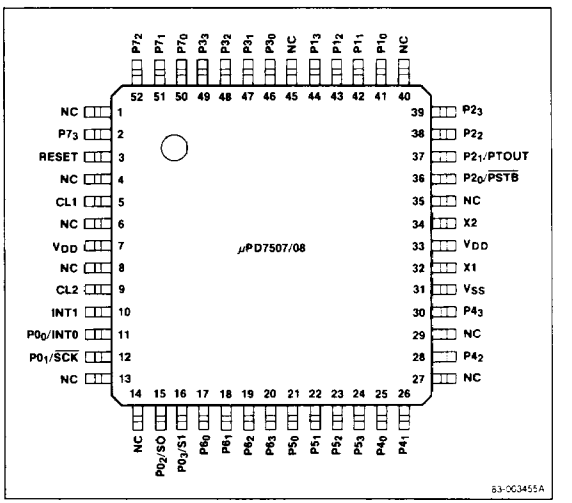
* A 3-digit mask identification code is added to the part number by NEC at the time of code verification.

Pin Configurations

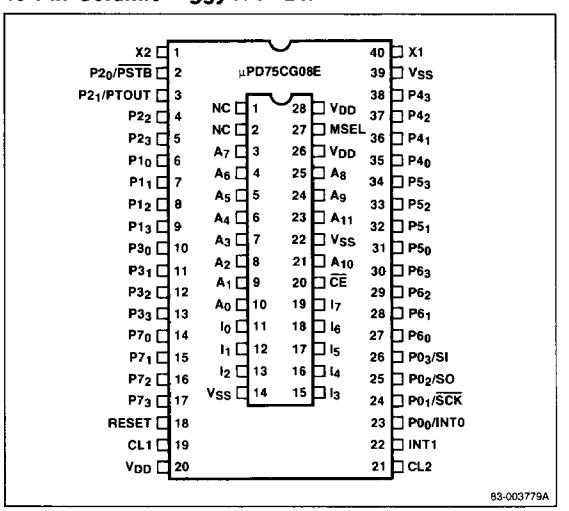
40-Pin Plastic DIP and Plastic Shrink DIP



52-Pin Plastic QFP



40-Pin Ceramic Piggyback DIP



Pin Identification

40-Pin DIP, Shrink DIP and Piggyback DIP

No.	Symbol	Function
1, 40	X2, X1	Crystal clock/external event input port
2-5	$P2_0$/PSTB, $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/output strobe pulse, timer out F/F signal
6-9	$P1_0$-$P1_3$	I/O port 1
10-13	$P3_0$-$P3_3$	Output port 3
14-17	$P7_0$-$P7_3$	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	V_{DD}	Positive power supply
22	INT1	External interrupt
23-26	$P0_0$/INT0, $P0_1$/SCK, $P0_2$/SO, $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
27-30	$P6_0$-$P6_3$	I/O port 6
31-34	$P5_0$-$P5_3$	I/O port 5
35-38	$P4_3$-$P4_0$	I/O port 4
39	V_{SS}	Ground

Pin Identification (cont)

28-Pin EPROM Socket on Piggyback DIP

No.	Symbol	Function
1, 2	NC	Not connected
3-10	A_7-A_0	Address bits 7-0
11-13	I_0-I_2	Data bits 0-2
14, 22	V_{SS}	Ground
15-19	I_3-I_7	Data bits 3-7
20	$\overline{CE}$	Chip enable
21, 23	A_{10}-A_{11}	Address bits 10, 11
24, 25	A_9, A_8	Address bits 9, 8
26, 28	V_{DD}	Positive power supply
27	MSEL	Memory select

52-Pin QFP

No.	Symbol	Function
1, 4, 6, 8, 13, 14, 27, 29, 35, 40, 45	NC	Not connected
2, 50-52	$P7_0$-$P7_3$	I/O port 7
3	RESET	RESET input
5, 9	CL1, CL2	System clock inputs
7	V_{DD}	Positive power supply
10	INT1	External interrupt
11, 12, 15, 16	$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
17-20	$P6_0$-$P6_3$	I/O port 6
21-24	$P5_0$-$P5_3$	I/O port 5
25, 26 28, 30	$P4_3$-$P4_0$	I/O port 4
31	V_{SS}	Ground
32, 34	X1, X2	Crystal clock/external event input
33	V_{DD}	Positive power supply
36-39	$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$	4-bit output port 2/output strobe pulse, timer out F/F signal
41-44	$P1_0$-$P1_3$	I/O port 1
46-49	$P3_0$-$P3_3$	Output port 3

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI [Port 0/ External Interrupt, Serial Interface]

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO (active low), and the serial clock $\overline{SCK}$ (active low), used for synchronizing data transfer, make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising edge-triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to V_{SS}. If $P0_1$/$\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a $P2_0$/$\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

$P3_0$-$P3_3$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_0$-$P4_3$ [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{DD} or GND. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

3

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three state output port. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

Connect a crystal oscillator circuit to input X1 and output X2 for crystal clock operation. Alternatively, connect external event pulses to input X1 and leave output X2 open for external event counting. If X1 is not used, connect it to ground. If X2 is not used, leave it open.

CL1, CL2 [System Clock Input]

Connect a 82 kΩ resistor across CL1 and CL2, and connect a 33 pF capacitor from CL1 to V_{SS}. Alternatively, connect an external clock source to CL1 and leave CL2 open.

RESET [Reset]

A high level input to this pin initializes the μPD7507/08 after power up.

INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V_{SS} if unused.

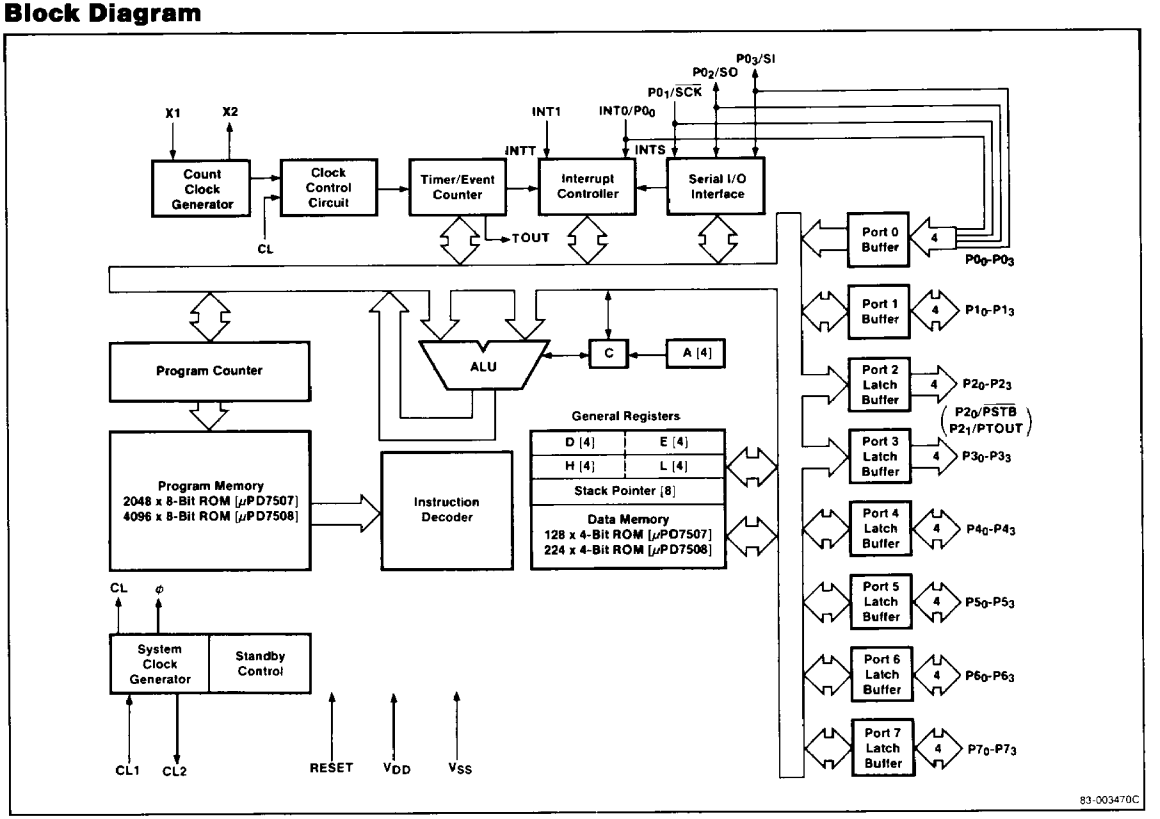
V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

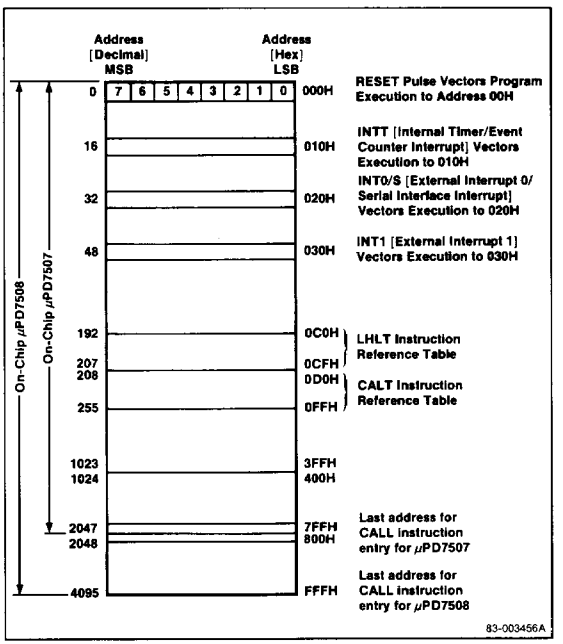
Block Diagram



Memory Map

Figure 1 shows the ROM memory map of the μPD7507/08.

Figure 1. ROM Map



Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (bits CM_1 and CM_2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and count clock generator circuit (X). It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter. Figure 2 shows the clock control circuit.

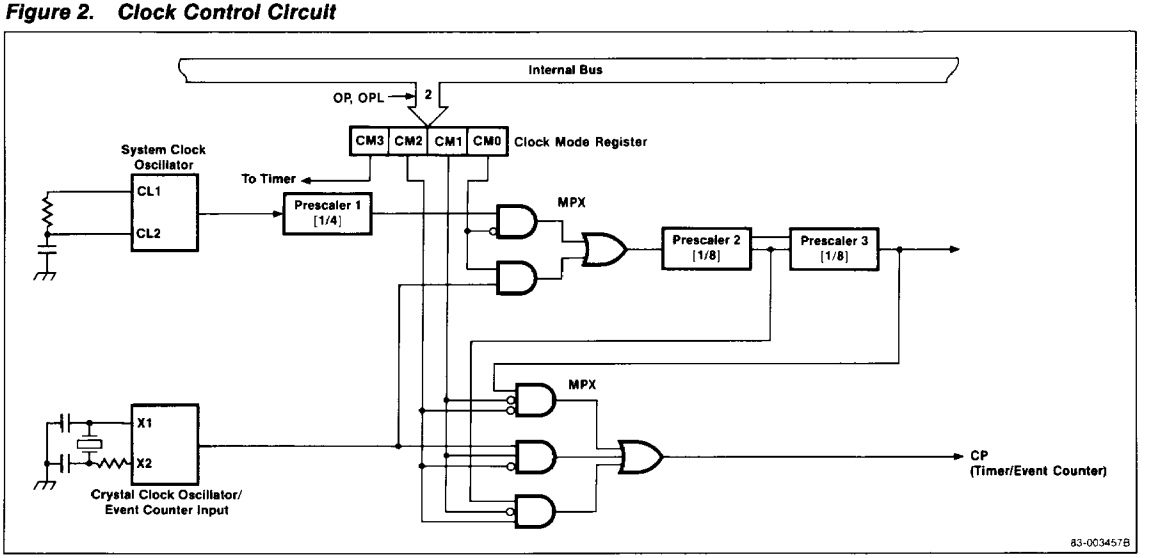
Table 2 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency.

Table 2. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	CL/256
0	0	1	X/64
0	1	0	X
0	1	1	X
1	0	0	CL/32
1	0	1	X/8
1	1	0	Not used
1	1	1	Not used

CM3	TOUT Signal
0	Disabled
1	Enabled

Figure 2. Clock Control Circuit



Timer/Event Counter

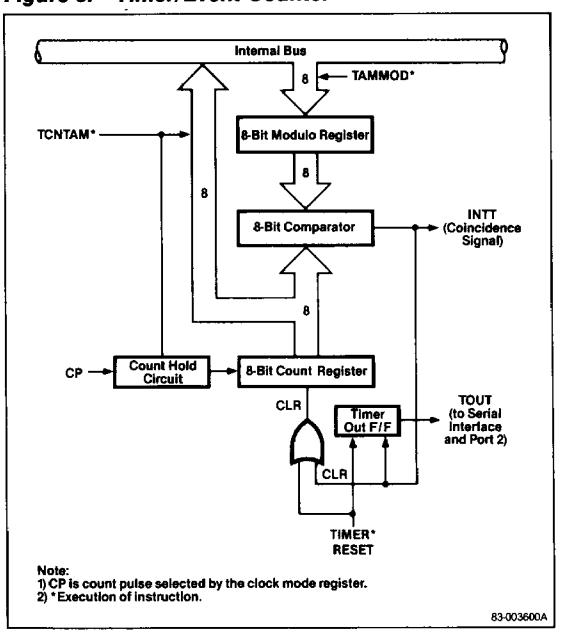
The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip-flop as shown in figure 3.

The 8-bit count register is a binary 8-bit up-counter which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and the modulo register and outputs an INTT when they are equal.

Figure 3. Timer/Event Counter

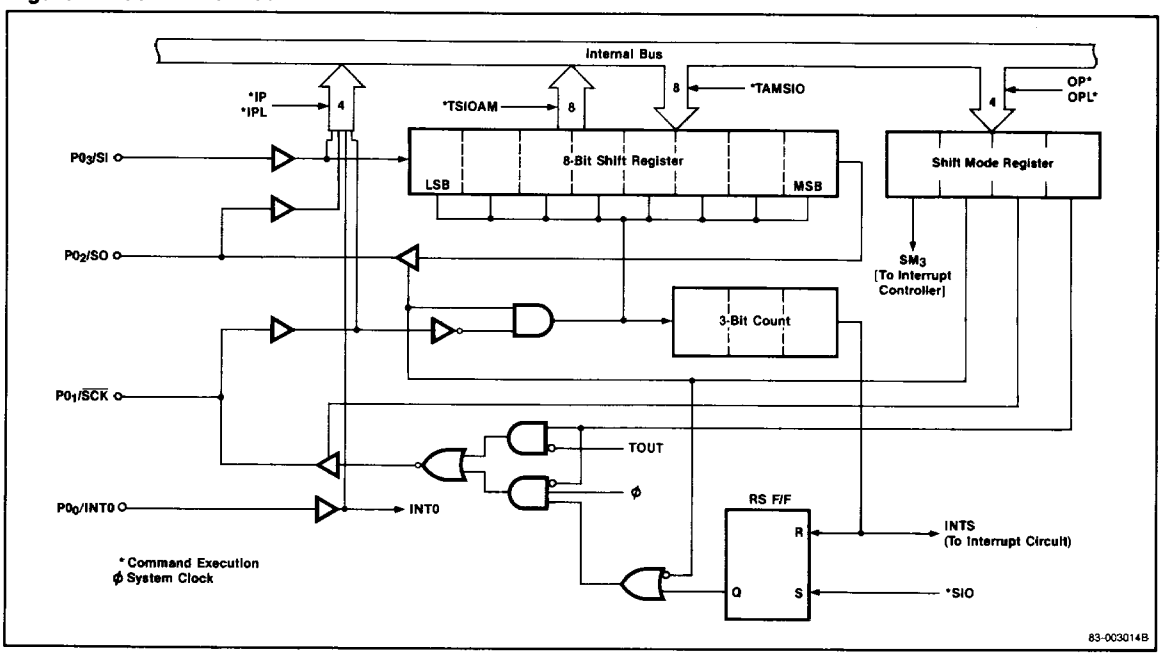


Serial Interface

The 8-bit serial interface allows the μPD7507/08 to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers. Figure 4 shows the serial interface.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Figure 4. Serial Interface



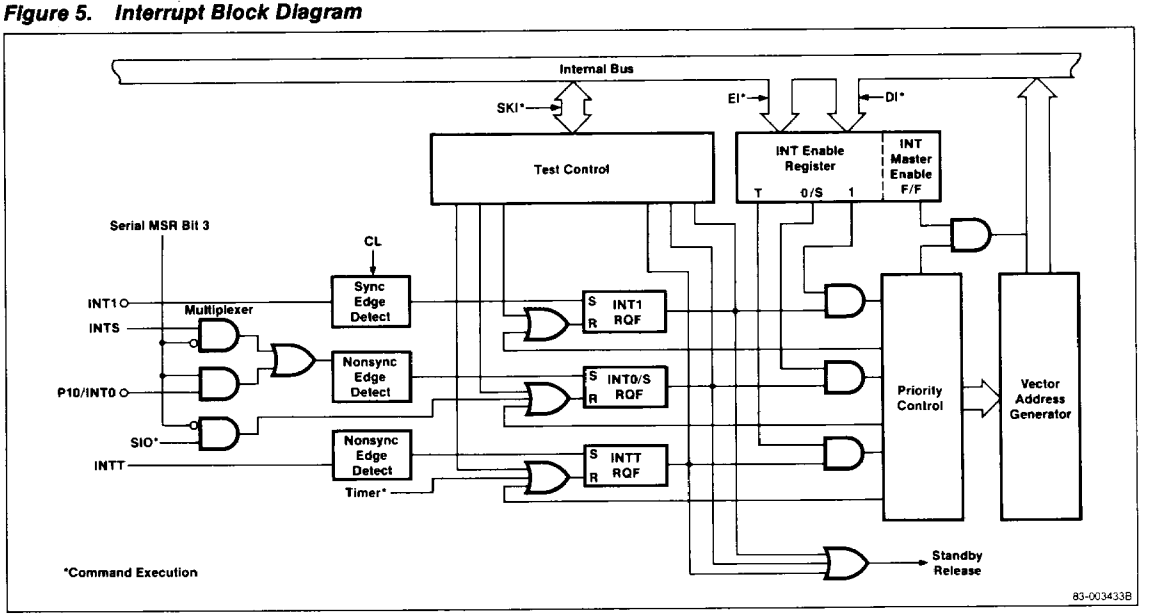
Interrupts

The μPD7507/08 has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 3 is a summary of the four interrupts. Figure 5 is the block diagram.

Table 3. μPD7507/08 Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 5. Interrupt Block Diagram



System Clock and Timing Circuitry

Timing for the μPD7507/08 is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase shift required for oscillation. Figure 6 shows the connection for an RC circuit. Figure 7 shows the connection for an external clock source.

The internal oscillator generates a frequency in the range 60 kHz to 300 kHz depending on the frequency reference. For example, at $V_{DD} = 5$ V, an 82-kΩ resistor and a 33-pF capacitor generate a frequency of 200 kHz. The oscillation frequency is fed to the clock control circuit. It is divided by two and the resulting signal is fed to the CPU and serial interface as shown in figure 8.

Table 4 shows the operating status of the various logic blocks under the three power down-modes.

Figure 6. RC Circuit Connection

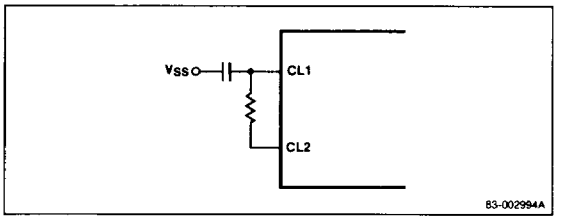


Figure 7. External Clock Source Connection

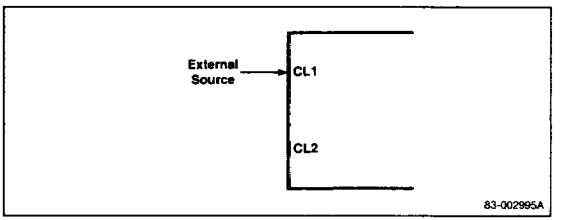


Figure 8. System Clock Circuitry

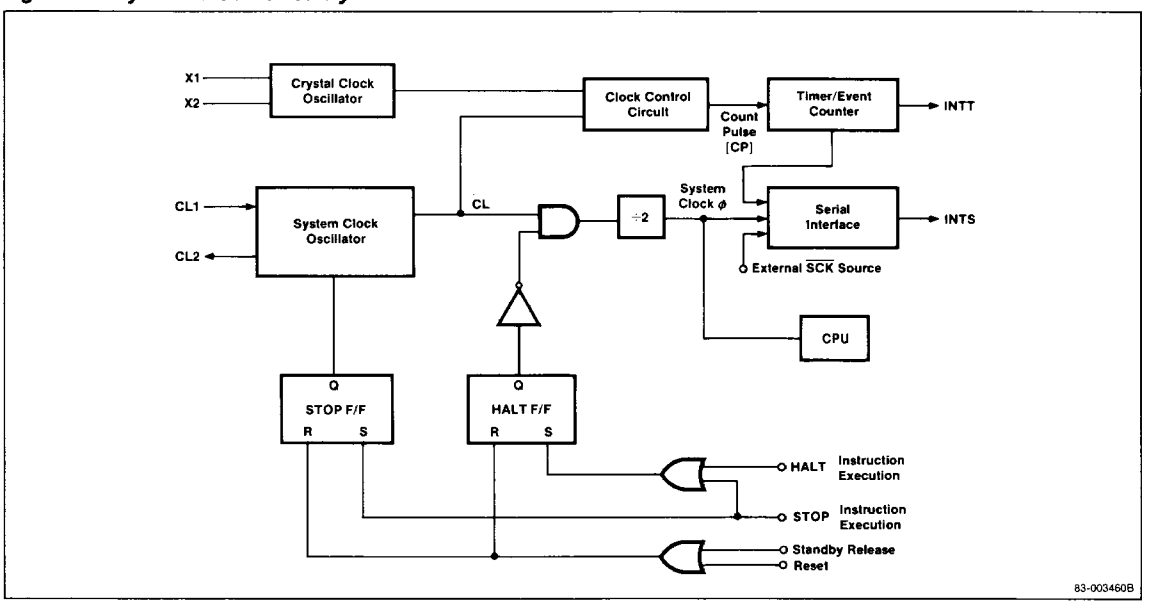


Table 4. Power-Down Operating Status

Logic Block	Power-Down Mode		Data Retention Mode
	HALT	STOP	
System clock	(Note 1)	Disabled	Disabled
X2	Normal	Normal	Disabled
CPU	Disabled	Disabled	Disabled
RAM	Data retained	Data retained	Data retained
Internal registers	Data retained	Data retained	Data retained
Timer/event counter	Normal	(Note 3)	Disabled
Serial interface	(Note 2)	(Note 2)	Disabled
INT0	Normal	Normal	Disabled
INT1	Normal	Disabled	Disabled
RESET	Normal	Normal	(Note 4)

Note:

(1) Supplied to timer/event counter but not to CPU or serial interface.

(2) Can function normally if the serial MSR is set to get the $\overline{SCK}$ signal externally or from the TOUT signal.

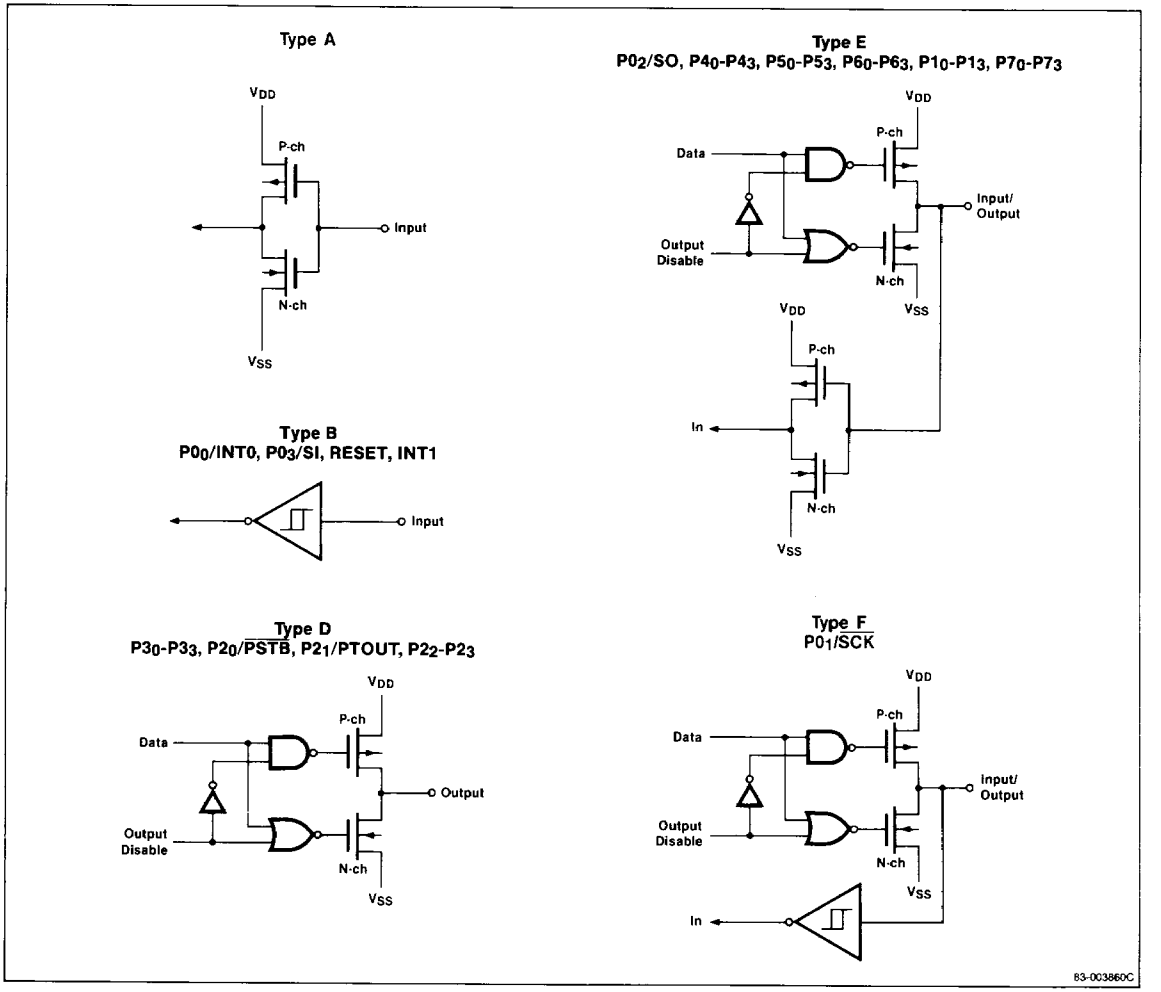
(3) Can function normally if the clock MSR is set to use X1 as the source for the count pulse.

(4) To enter the data retention mode, raise RESET while V_{DD} is lowered. To end the data retention mode, raise RESET when V_{DD} is raised, then lower it. INTT, INT0, INTS or RESET releases the STOP mode. RESET or any interrupt releases the HALT mode.

I/O Port Interfaces

Figure 9 shows the internal circuit configurations at the I/O ports.

Figure 9. Interface at Input/Output Ports



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 to V_{DD} + 0.3 V
Output current high, I_{OH}	
One pin	−17 mA
All pins, total	−30 mA
Output current low, I_{OL}	
One pin	17 mA
Ports 1, 2, 3, 7	25 mA
Ports 4, 5, 6	25 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics 1

For V_{DD} = 2.5 to 3.3 V (7507, 7508 only)

$T_A = -10$ to +70°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −80 μA
Output voltage, low	V_{OL}			0.5	V	I_{OL} = 350 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	V_{LIH2}			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	V_{LIL2}			−10	μA	CL1, X1
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	250	μA	Normal operation, V_{DD} = 3 V ±10%; R = 240 kΩ ±2%, C = 33 pF ±5%
			35	230	μA	Normal operation, V_{DD} = 2.5 V; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
			0.2	10	μA	Stop mode, X1 = 0 V; V_{DD} = 2.5 V
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

DC Characteristics 2

For V_{DD} = 2.7 to 6.0 V (75CG08E, 5 V ±10%)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode, 7507/08 only
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		V_{DD} − 0.5			V	I_{OH} = −100 μA, 7507/08 only
	V_{OH1}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA, 75CG08E only
	V_{OH2}	V_{DD} − 0.75			V	I_{OH} = −5.0 mA, 75CG08E only
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA; V_{DD} = 4.5 to 6.0 V, 7507/08 only
				0.5	V	I_{OL} = 400 μA, 7507/08 only
				0.4	V	I_{OL} = −1.6 mA, 75CG08E only
Input current, high	I_{IH}			300	μA	75CG08E only, $V_I = V_{DD}$, MSEL
Input current, low	I_{IL}			−200	μA	75CG08E only, V_I = 0 V, I_0-I_7
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode, 7507/08 only
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
			70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%, 7507/08 only
	I_{DD2}		1.0	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%, 7507/08 only
			0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%, 7507/08 only
			2	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%, 75CG08E only
	I_{DDDR}		0.2	10	μA	Data retention mode V_{DDDR} = 2.0 V, 7507/08 only

AC Characteristics 1

For V_{DD} = 2.7 to 6.0 V (75CG08, 5 V ±10%)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5.0 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3.0 ±10%; R = 160 kΩ ±2% (Note 1), 7507/08 only
		75		135	kHz	V_{DD} = 3.0 ±10%; R = 160 kΩ ±2% (Note 1), 7507/08 only
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V, 7507/08 only, V_{DD} = 5 V ±5%, 75CG08E only
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V, 7507/08 only
		10		300	kHz	CL1, external clock, 50% duty; 75CG08E only
System clock rise and fall times	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V, 7507/08 only
		1.5		50	μs	CL1, external clock, 75CG08E only
		1.2		50	μs	CL1, external clock; V_{DD} = 5 V ±5%, 75CG08E only
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input; 50% duty; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V, 7507/08 only
		0		300	kHz	X1, external pulse input; 50% duty, 75CG08 only
		0		410	kHz	X1, external pulse input; 50% duty; V_{DD} = 5 V ±5%, 75CG08E only
Counter clock rise and fall times	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V, 7507/08 only
		1.5			μs	X1, external pulse input, 75CG08E only
		1.2			μs	X1, external pulse input; V_{DD} = 5 V ±5%, 75CG08E only
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±5%, 75CG08E only
		8.0			μs	$\overline{SCK}$ as input, 7507/08 only
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±5%, 75CG08E only
		16.0			μs	$\overline{SCK}$ as output, 7507/08 only
		4.0			μs	$\overline{SCK}$ as input, 75CG08E only
		6.7			μs	$\overline{SCK}$ as output, 75CG08E only
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±5%, 75CG08E only
		4.0			μs	$\overline{SCK}$ as input

AC Characteristics 1 (cont)

For V_{DD} = 2.7 to 6.0 V (75CG08, 5 V ±10%)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	2.2			μs	$\overline{SCK}$ as output, V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±10%, 75CG08 only
		8.0			μs	$\overline{SCK}$ as output, 7507/08 only
		1.8			μs	$\overline{SCK}$ input, 75CG08E only
		3.0			μs	$\overline{SCK}$ as output, 75CG08E only
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±10%, 75CG08E only
				1200	ns	7507/08 only
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	(Note 2)			μs	V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±10%, 75CG08E only
		(Note 3)			μs	7507/08 only
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{STP}	100			ns	V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±10%, 75CG08E only
		100			ns	7507/08 only
$\overline{PSTB}$ pulse width	t_{STL}	(Note 2)			μs	V_{DD} = 4.5 to 6.0 V, 7507/08 only V_{DD} = 5 V ±10%, 75CG08E only
		(Note 3)			μs	7507/08 only
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_{CC}$ or $2/f_C$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	7507/08 only
RESET hold time	t_{HRS}	0			ns	7007/08 only

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

(2) $(10^3) \div 2(f_{CC}$ or f_C in kHz) − 0.8 μs.

(3) $(10^3) \div 2(f_{CC}$ or f_C in kHz) − 2.0 μs.

3

AC Characteristics 2

For V_{DD} = 2.5 to 3.3 V (7507, 7508 only)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	R = 240 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.25			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	(Note 2)			μs	
Port 1 output hold time after $\overline{PSTB}$ ↑	t_{STP}	100			ns	
$\overline{PSTB}$ pulse width	t_{STL}	(Note 2)			μs	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	(Note 3)			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Notes:

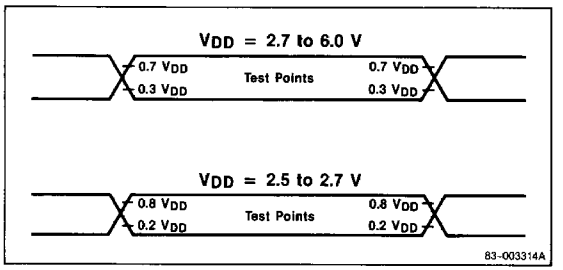
(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

(2) $10^3 \div 2$ (f_{CC} or f_C in kHz) − 2.0.

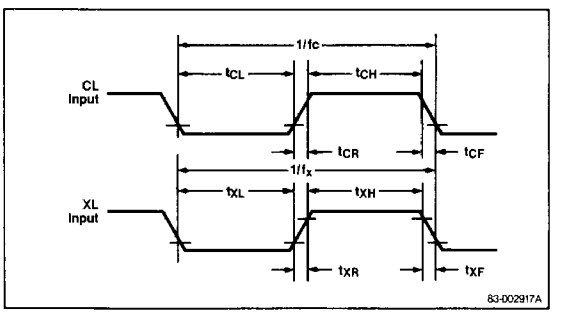
(3) $10^3 \div 2$ (f_{CC} or f_C in kHz).

Timing Waveforms

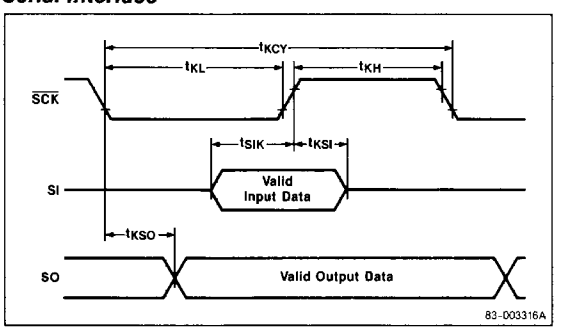
Timing Measurement Points



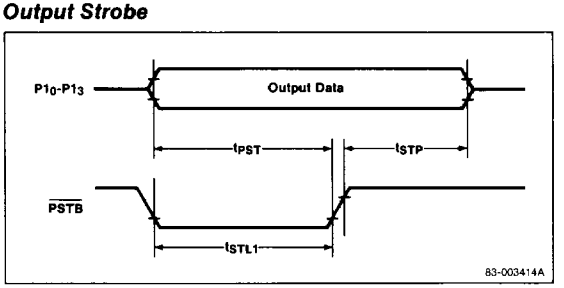
Clocks



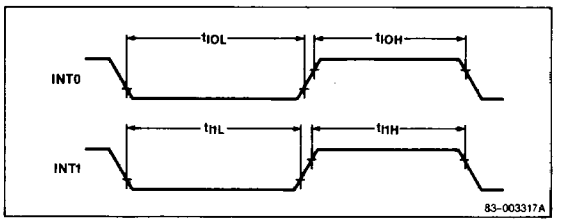
Serial Interface



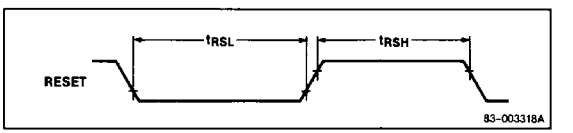
Output Strobe



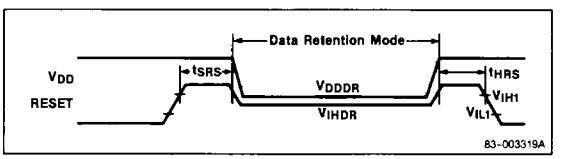
External Interrupts



RESET



Data Retention Mode

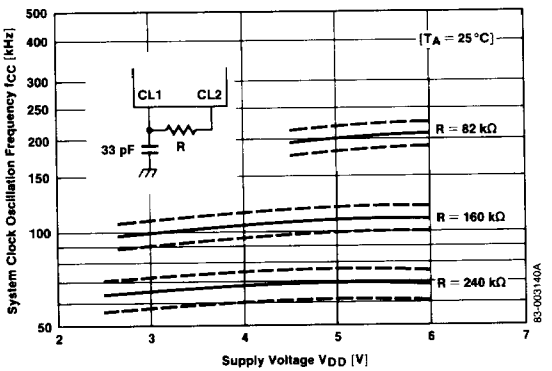


3

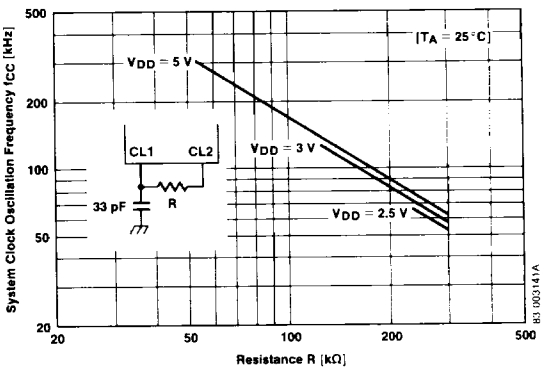
Operating Characteristics

$T_A = 25°C$

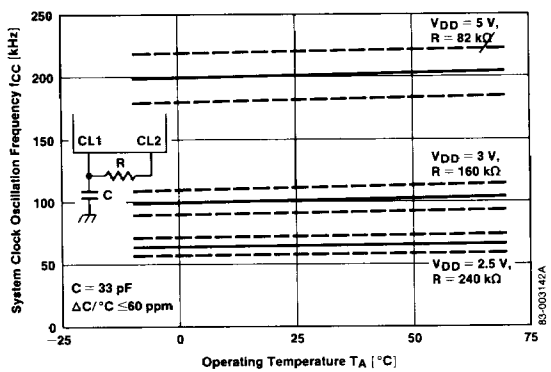
f_{CC} vs V_{DD}



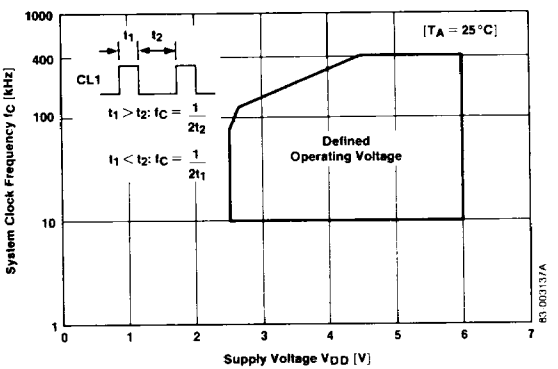
f_{CC} vs R



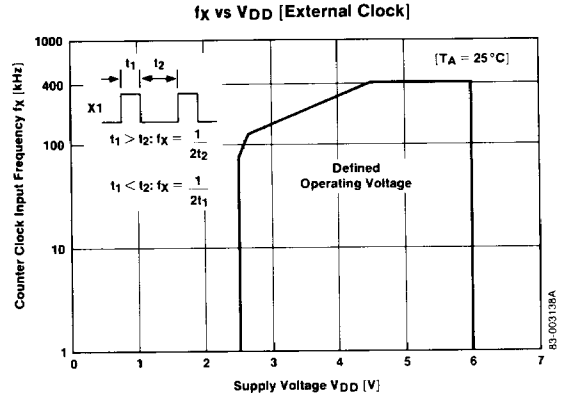
f_{CC} vs T_A



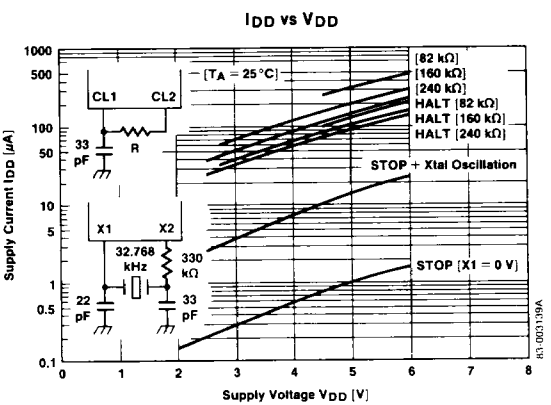
f_C vs V_{DD} [External Clock]



f_X vs V_{DD} [External Clock]



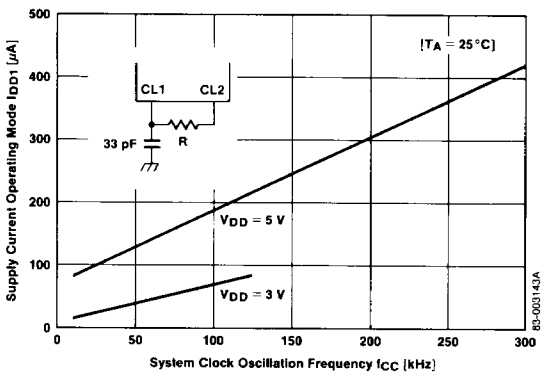
I_{DD} vs V_{DD}



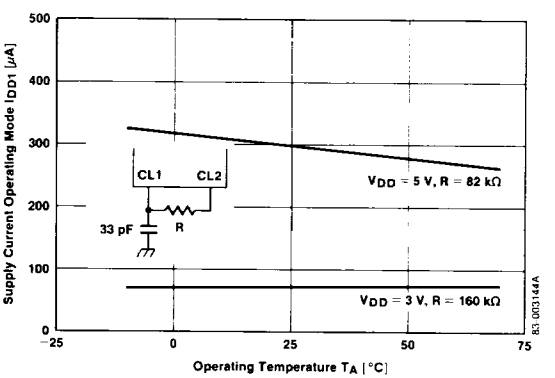
Operating Characteristics (cont)

T_A = 25°C

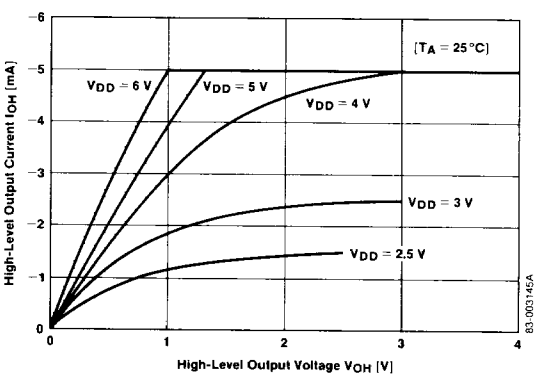
I_{DD1} vs f_{CC}



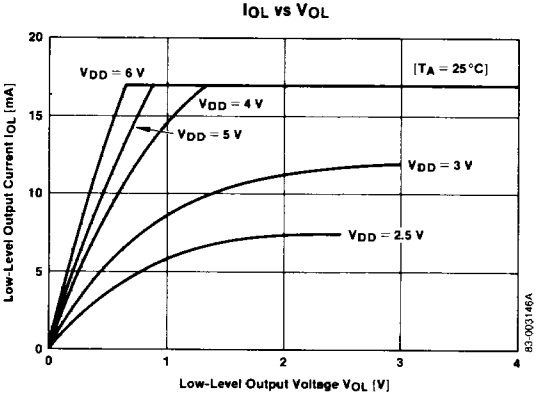
I_{DD1} vs T_A



I_{OH} vs V_{OH}



I_{OL} vs V_{OL}



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