NEC
NEC Electronics Inc.

μPD7506
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER

Description

The μPD7506 CMOS 4-bit single chip microcomputer has the μPD7500 series architecture. Twenty-two I/O lines are organized into the 2-bit input port 0, the 4-bit output port 2, and the 4-bit I/O ports 1, 4, 5, and 6. The device executes 58 of the μPD7500 Set B instructions, and has a 5-μs instruction cycle time. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Due to the CMOS process, the device has a maximum power consumption of 600 μA at 5 V, and this is further reduced in halt and stop modes.

Features

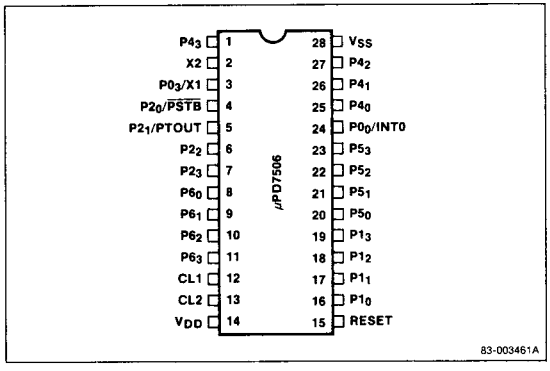
- ☐ 1024 x 8-bit program ROM
- ☐ 64 x 4-bit data RAM
- ☐ 8-bit timer/event counter
- ☐ Two 4-bit general-purpose registers
- ☐ Two testable interrupts
- ☐ 5-μs instruction cycle/400 kHz external clock
- ☐ 600 μA max current consumption
- ☐ 2 standby modes
- ☐ 22 I/O lines

Ordering Information

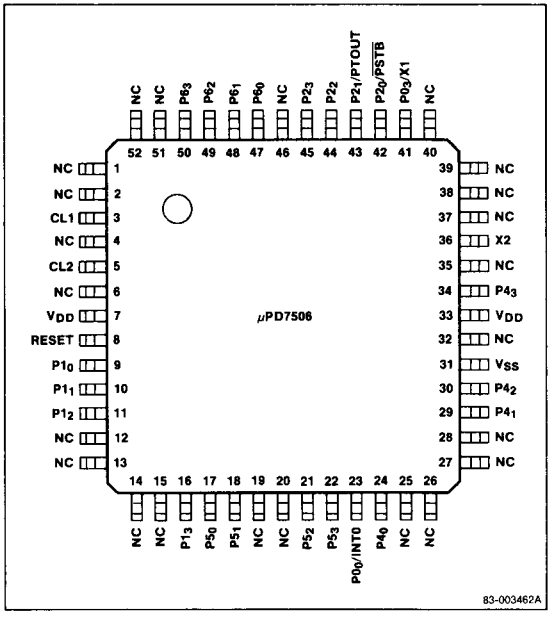
Part No.	Package Type	Max Frequency of Operation
μPD7506C	28-pin plastic DIP	410 kHz
μPD7506CT	28-pin plastic shrink DIP	410 kHz
μPD7506G-00	52-pin plastic miniflat	410 kHz

Pin Configurations

28-Pin Plastic DIPs



52-Pin Plastic Miniflat



Pin Identification

28-Pin Plastic DIPs

No.	Symbol	Function
1, 25-27	$P4_3$-$P4_0$	4-bit I/O port 4
2	X2	External event input
3	$P0_3$/X1	Input port 0/Clock input
4	$P2_0$/$\overline{PSTB}$	Output port 2/Output strobe
5	$P2_1$/PTOUT	Output port 2/Timer out F/F signal
6-7	$P2_2$-$P2_3$	Output port 2
8-11	$P6_0$-$P6_3$	4-bit I/O port 6
12, 13	CL1, CL2	System clock input
14	V_{DD}	Positive power supply
15	RESET	RESET input
16-19	$P1_0$-$P1_4$	4-bit I/O port 1
20-23	$P5_0$-$P5_3$	4-bit I/O port 5
24	$P0_0$/INT0	Input port 0/External Interrupt
28	V_{SS}	Ground

52-Pin Plastic Miniflat

No.	Symbol	Function
3, 5	CL1, CL2	System clock input
7, 33	V_{DD}	Positive power supply
8	RESET	RESET input
9-11, 16	$P1_0$-$P1_4$	4-bit I/O port 1
16-18, 21	$P5_0$-$P5_3$	4-bit I/O port 5
23	$P0_0$/INT0	Input port 0/External interrupt
24, 29, 30, 34	$P4_0$-$P4_3$	4-bit I/O port 4
31	V_{SS}	Ground
36	X2	External event input
41	$P0_3$/X1	Input port 0/Clock input
42	$P2_0$/$\overline{PSTB}$	Output port 2/Output strobe
43	$P2_1$/PTOUT	Output port 2/Timer out F/F signal
44, 45	$P2_2$-$P2_3$	Output port 2
47-50	$P6_0$-$P6_3$	4-bit I/O port 6
1, 2, 4, 6, 12-15, 19, 20, 25-28, 32, 35, 37-40, 46, 51, 52	NC	No connection

Pin Functions

$P0_0$/INT0, $P0_3$/X1 [Port 0]

2-bit input port 0. Line $P0_0$ is shared with external interrupt INT0. Line $P0_3$ is shared with crystal clock/external event input X1. Ground any unused pins.

$P1_0$-$P1_3$ [Port 1]

4-bit input port or three-state output port. Output is strobed in synchronization with the $\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2, Strobe, Timer F/F Output]

4-bit latched, three-state output port. Line $P2_0$ is shared with the port 1 output strobe pulse $\overline{PSTB}$. Line $P2_1$ is shared with the timer out flip flop signal PTOUT. Leave unused pins open.

$P4_3$-$P4_0$ [Port 4]

4-bit input or latched three-state output port. Can perform 8-bit parallel I/O in conjunction with port 5. In input mode, connect unused pins to V_{DD} or V_{SS}. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input or latched three-state output port. Can perform 8-bit parallel I/O in conjunction with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input or latched three-state output port. The port 6 mode select register (MSR) configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

CL1, CL2 [System Clock Input]

Connect a 120-kΩ resistor across CL1 and CL2, and a 33-pF capacitor from CL1 to V_{SS}. Or, connect an external clock source to CL1 and leave CL2 open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, connect external event pulses to input X1 and leave X2 open. If X1 is not used, connect it to V_{SS}. If X2 is not used, leave it open.

RESET

A high level input to this pin initializes the μPD7506.

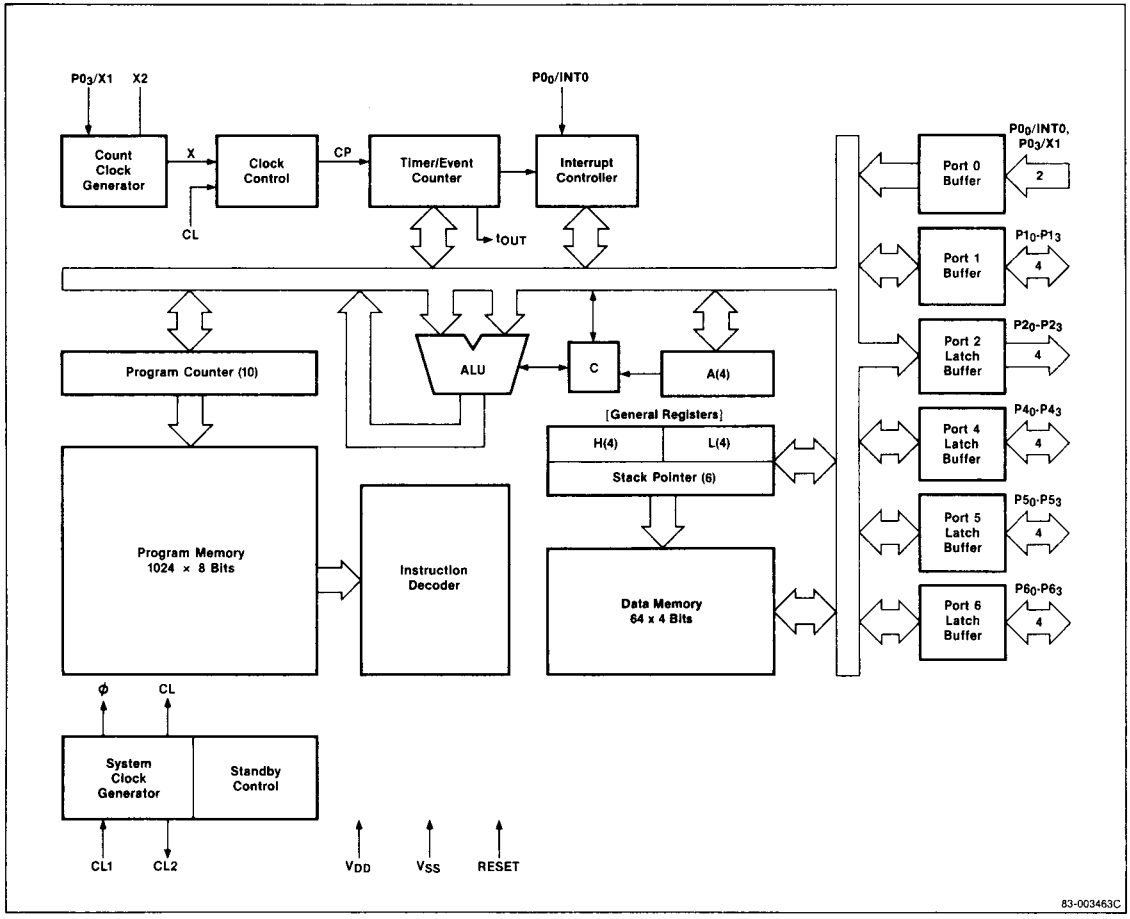
V_{DD}

Positive power supply. For proper operation, apply a single voltage from 2.7 to 6.0 V.

V_{SS}

Ground.

Block Diagram



Clock Control Circuit

This circuit consists of a 4-bit clock mode register (CMR), prescalers 1 and 2, and a multiplexer, as shown in figure 1. The circuit selects the clock source, accepts output from the system clock oscillator (CL) and count clock generator circuit (X), divides the signal according to the setting in the CMR, and outputs the count pulse (CP) to the timer/event counter.

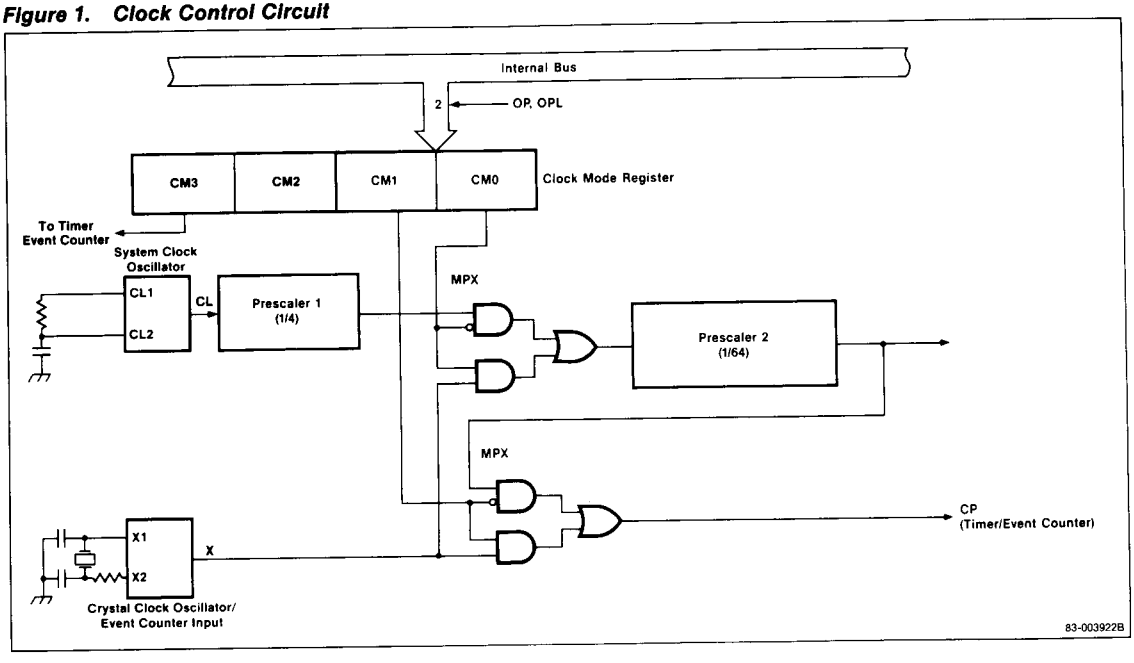
The OP or OPL instruction sets the CMR as defined by table 1. Before loading the CMR, it is necessary to clear bit 2 of the accumulator (A2) to zero.

Table 1. Selecting the Count Pulse Frequency

CM_1	CM_0	Frequency Selected
0	0	CL/256
0	1	X/64
1	0	X
1	1	X

CM_3	TOUT Signal
0	Disabled
1	Enabled

Figure 1. Clock Control Circuit



Timer/Event Counter

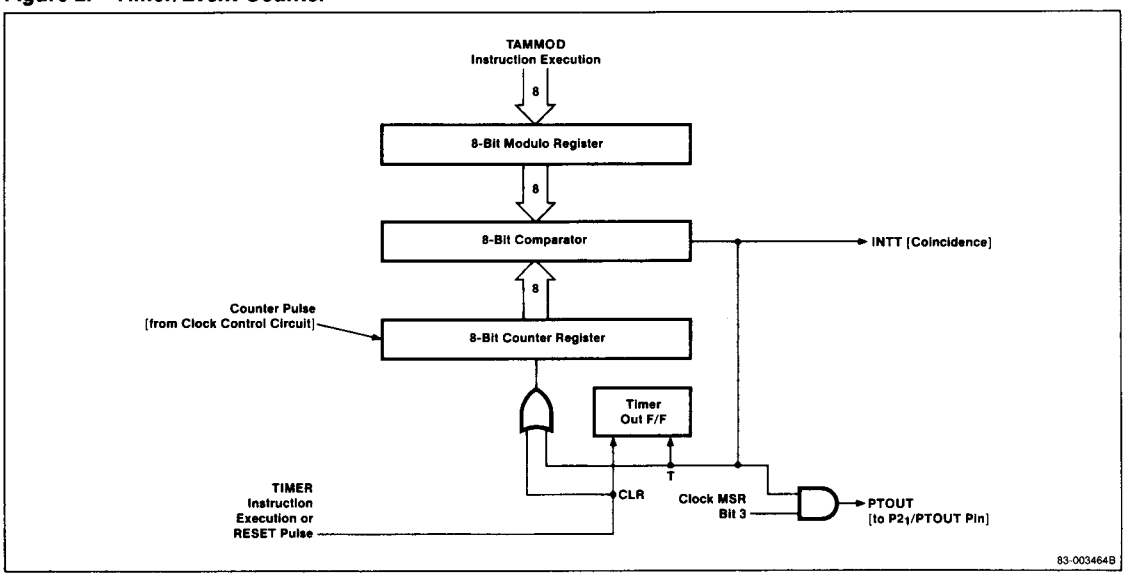
The timer/event counter consists of an 8-bit count register, an 8-bit modulo register, an 8-bit comparator, and a timer out flip flop, as shown in figure 2.

The count register is a binary up-counter that increments each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H. When an overflow occurs, the counter is reset from FFH to 00H.

The modulo register determines the number in the count register. The TAMMOD instruction sets the contents of the modulo register. On reset, its contents are FFH.

The comparator compares the contents of the count register and the modulo register; when equal, the comparator outputs INTT.

Figure 2. Timer/Event Counter



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Interrupts

The μPD7506 has two interrupts, INTT and INT0. INTT is internally generated by the timer/event counter. INT0 is externally generated. See figure 3.

System Clock and Timing Circuitry

Timing for the μPD7506 is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase-shift required for oscillation. Figure 4 shows the connection for an RC circuit. Figure 5 shows the connection for an external clock source.

Table 2 compares stop and halt modes. The main difference is that stop mode stops the system clock; halt does not.

Table 2. Stop and Halt Modes

Mode	CL	φ	X	CPU	Timer
Stop	x	x	0	x	Δ
Halt	0	x	0	x	0

o: operates
x: stops
Δ: external clock source: operates
internal clock source: stops

Figure 3. μPD7506 Interrupts

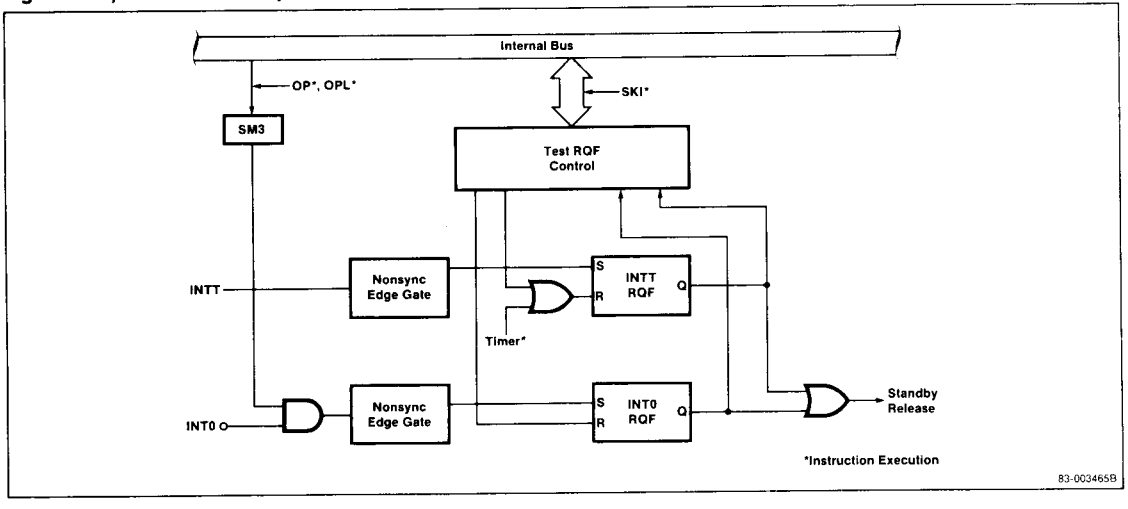


Figure 4. RC Circuit Connection

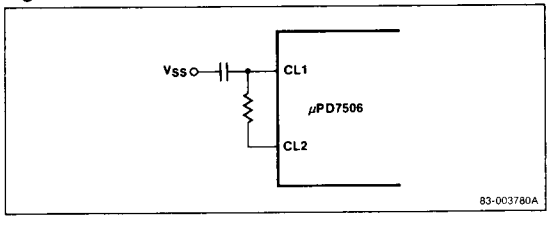
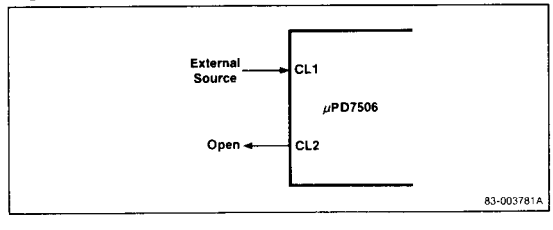


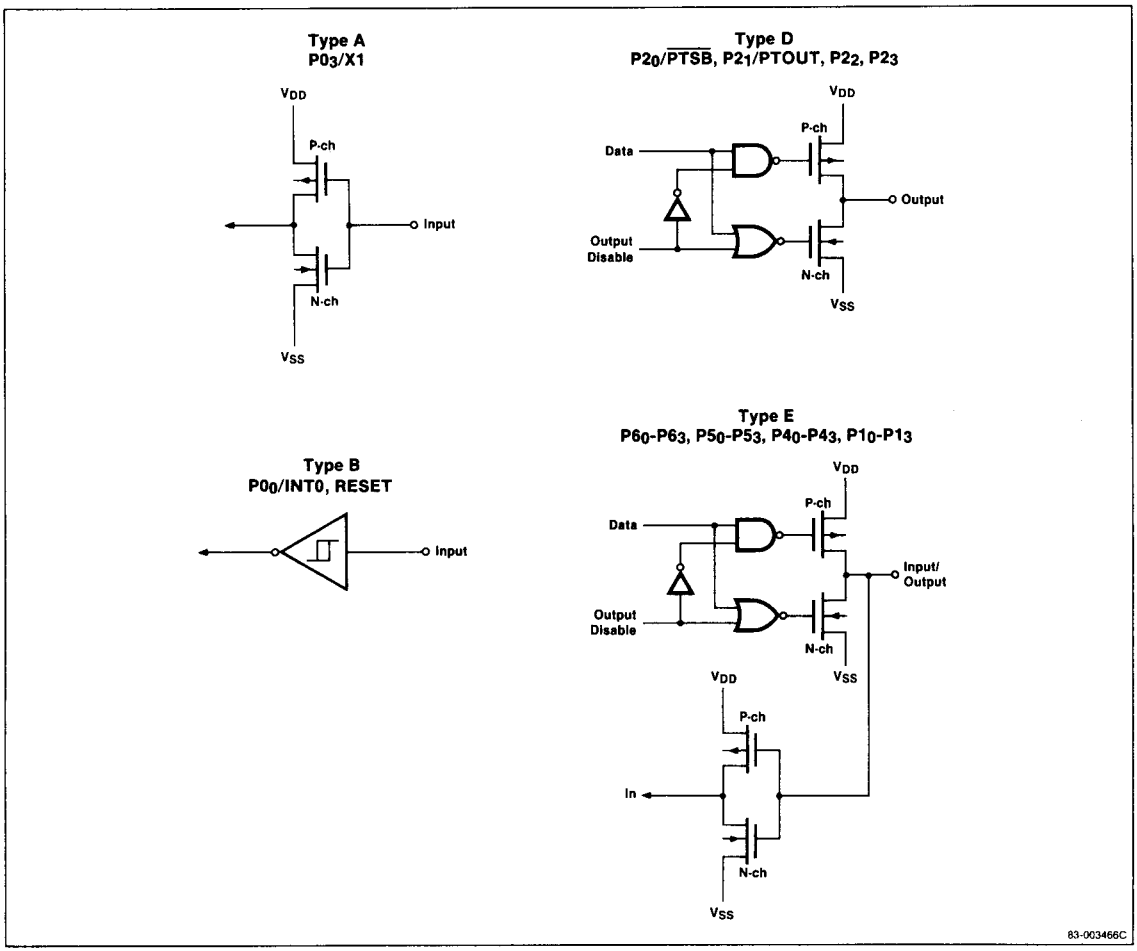
Figure 5. External Clock Source Connection



I/O Pin Configurations

Figure 6 shows the different input and output configurations.

Figure 6. Interface at Input/Output Ports



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Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to 70°C
Storage temperature, T_{STG}	−65 to 150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Total, input and output voltages	0.3 to V_{DD} + 0.3 V
Output current high, I_{OH}	
Per pin	−17 mA
Ports 2, 6	−17 mA
Ports 1, 4, 5	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Ports 2, 6; $P4_3$	25 mA
Ports 1, 5; $P4_0$-$P4_2$	25 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	$f_c = 1$ MHz Unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

For V_{DD} = 2.7 to 6.0 V

$T_A = -10$ to +70°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA; V_{DD} = 4.5 to 6.0 V
		V_{DD} − 0.5			V	I_{OL} = −100 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA; V_{DD} = 4.5 to 6.0 V
				0.5	V	I_{OL} = 400 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 10 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 10 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		200	600	μA	Normal operation, V_{DD} = 5 V ±10%; R = 120 kΩ ±2%, C = 33 pF ±5%
			50	180	μA	Normal operation, V_{DD} = 3 V ±10%; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1.0	10	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	5	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
	I_{DDDR}		0.2	5	μA	Data retention mode, V_{DDDR} = 2.0 V

DC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 V

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −80 μA
Output voltage, low	V_{OL}			0.5	V	I_{OL} = 350 μA
Input leakage current, high	V_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	V_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	V_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	V_{LIL2}			−10	μA	CL1, X1; V_I = 0 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		35	150	μA	Normal operation, V_{DD} = 3 V ±10%; R = 390 kΩ ±2%, C = 33 pF ±5%
			25	130	μA	Normal operation, V_{DD} = 2.5 V; R = 390 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	5	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
			0.2	5	μA	Stop mode, X1 = 0 V; V_{DD} = 2.5 V
	I_{DDDR}		0.2	5	μA	Data retention mode, V_{DDDR} = 2.0 V

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AC Characteristics

For V_{DD} = 2.7 to 6.0 V

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 120 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 240 kΩ ±2% (Note 1)
		75		135	kHz	R = 240 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
Port 1 output set-up time to $\overline{PSTB}$ ↑	t_{PST}	$1/(2f_\phi - 800)$			ns	V_{DD} = 4.5 to 6.0 V
		$1/(2f_{CC} - 2.0)$			ns	
Port 1 output hold time after $\overline{PSTB}$ ↑	t_{STP}	100			ns	V_{DD} = 4.5 to 6.0 V
		100			ns	
$\overline{PSTB}$ pulse width	t_{SWL}	$1/(2f_\phi - 800)$			ns	V_{DD} = 4.5 to 6.0 V
		$1/(2f_{CC} - 2.0)$			ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

AC Characteristics (cont)

For V_{DD} = 2.7 to 3.3 V

T_A = −10 to +70 °C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	R = 310 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 310 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
Port 1 output set-up time to PSTB ↑	t_{PST}	$1/(2f_{CC} - 2)$			ns	
Port 1 output hold time after PSTB ↑	t_{STP}	100			ns	
PSTB pulse width	t_{SWL}	$1/(2f_{CC} - 2)$			ns	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

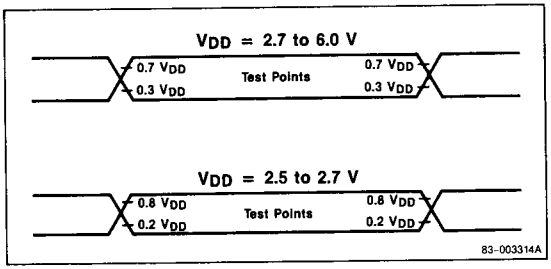
Recommended R and C Values for System Clock Oscillation Circuit

T_A = −10 to +70 °C

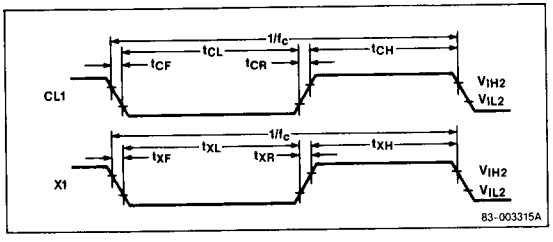
Supply Voltage Range	Recommended Values	Frequency Range
4.5 to 6.0 V	R = 120 kΩ ±2%	150 to 250 kHz, 200 kHz typical
2.7 to 3.3 V	R = 240 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R = 240 kΩ± 2%	75 to 135 kHz
2.5 to 3.3 V	R = 390 kΩ ±2%	50 to 80 kHz
2.5 to 6.0 V	R = 390 kΩ ±2 %	50 to 85 kHz

Timing Waveforms

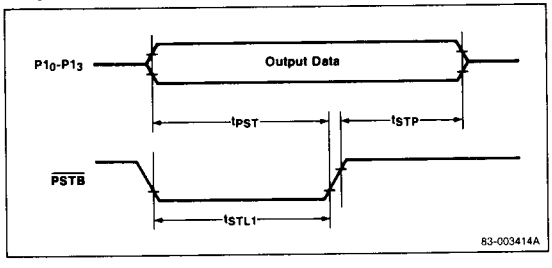
Timing Test Points



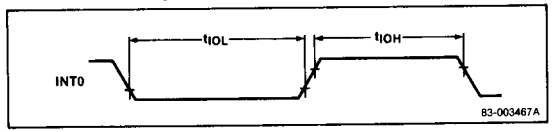
Clocks



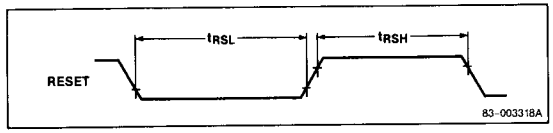
Output Strobe



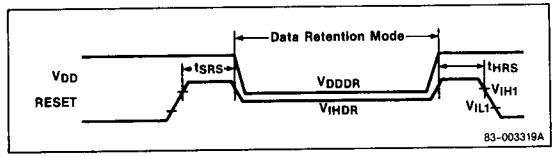
External Interrupt



Reset



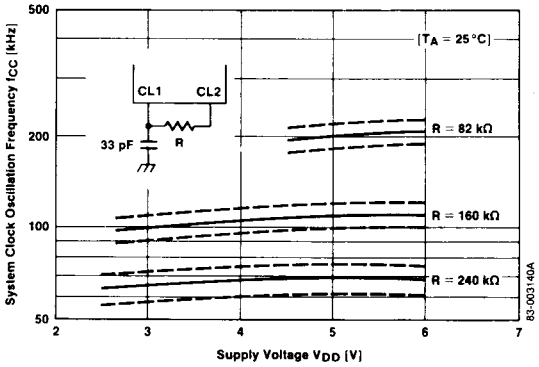
Data Retention Mode



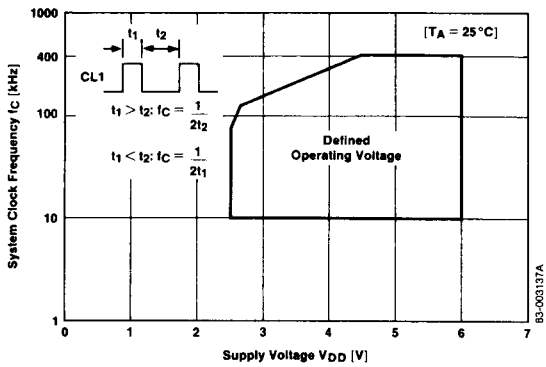
Operating Characteristics

$T_A = 25°C$

f_{CC} vs V_{DD}

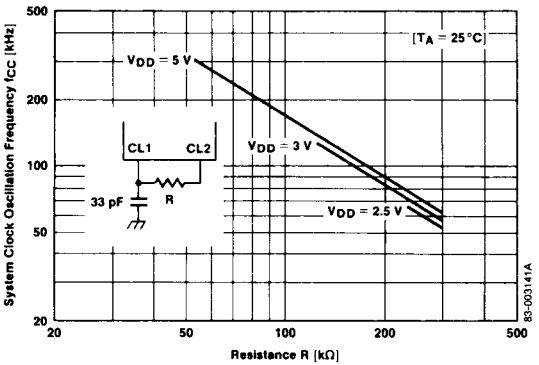


f_C vs V_{DD}

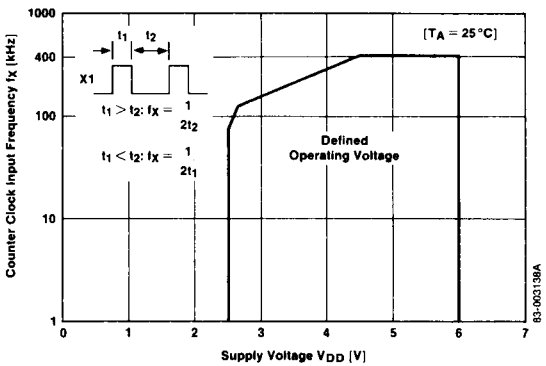


3

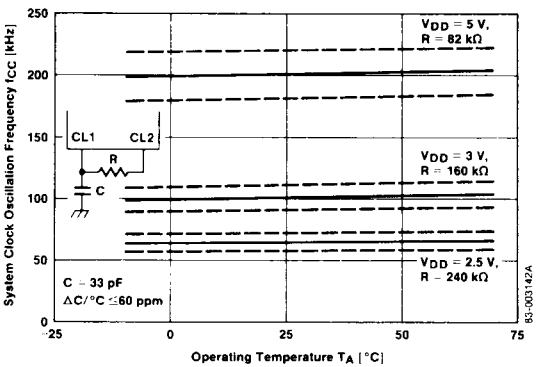
f_{CC} vs R



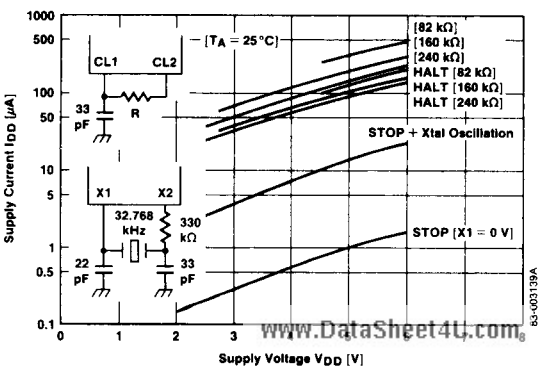
f_X vs V_{DD}



f_{CC} vs T_A

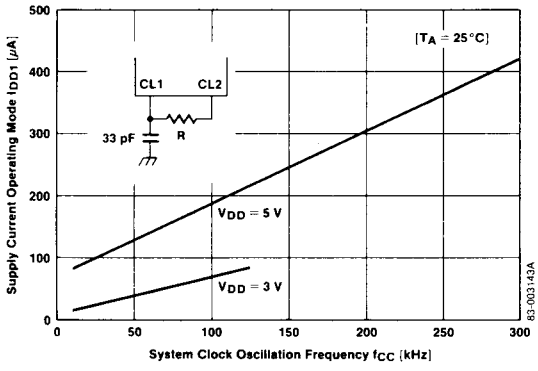


I_{DD} vs V_{DD}

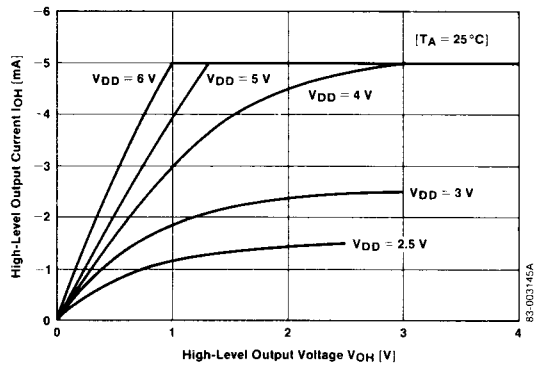


Operating Characteristics (cont)

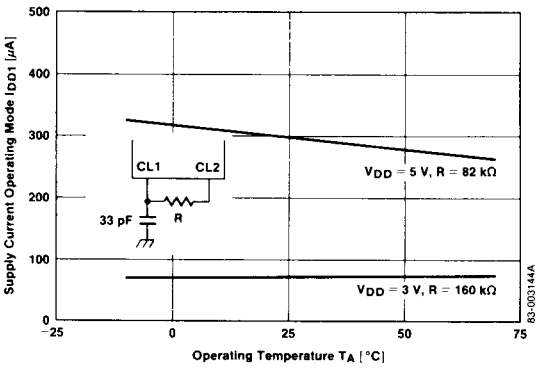
I_{DD1} vs f_{CC}



I_{OH} vs V_{OH}



I_{DD1} vs T_A



I_{OL} vs V_{OL}