4-BIT MICROPROCESSOR μPD750X EVALUATION CHIP

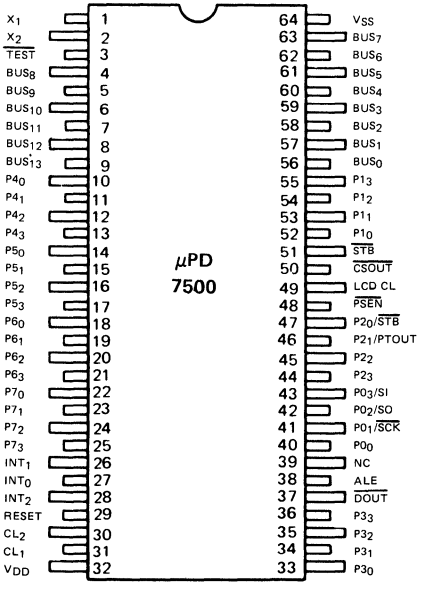
DESCRIPTION

The μPD7500 is a μCOM-75 4-bit microprocessor with a 256 x 4 RAM, a programmable 8-bit timer/event counter, and 5 vectored, prioritized interrupts. It is capable of addressing 8,192 bytes of external memory, and also functions as the prototype Evaluation Chip for the μPD750X family of 4-bit single chip microcomputers. The μPD7500 is manufactured with a low-power-consumption CMOS process, allowing use of a single power supply between 2.7 and 5.5V, and providing programmable power-down capability. It has 46 I/O lines, organized into eight 4-bit parallel ports, one 14-bit parallel address/instruction port, and one 8-bit serial port. The μPD7500 executes 102 instructions of the μCOM-75 instruction set, and it is available in a 64 pin quad-in-line package.

FEATURES

- 4-Bit Microprocessor
- Evaluation Chip for μPD750X Family of 4-Bit Single Chip Microcomputers
- Addresses up to 8,192 Bytes of External Memory
- 256 x 4 Bit RAM
- 10 μs Instruction Cycle Time
- 102 Powerful Instructions
  - Table Look-up Capability with LHLT and LAMTL instructions
  - Indirect indexed addressing with CALT instruction
- RAM Stack
- Extensive I/O Capability
  - One 4-Bit Input Port
  - Two 4-Bit Output Ports
  - Four 4-Bit I/O Ports, of which two are 8-Bit Byte Accessible
  - One 4-Bit I/O Port with Output Strobe
  - One 14-Bit Address/Instruction Port
  - One 8-Bit Serial I/O Port
- Programmable 8-Bit Timer/Event Counter with Crystal Clock Generator
- Vectored, Prioritized Interrupts
  - 3 External
  - 2 Internal (Timer and Serial I/O)
- Programmable Power-Down Operation with HALT and STOP Instructions
- Built-In System Clock Generator
- Built-In Reset Circuitry
- Single Power Supply, Variable from 2.7V to 5.5V
- CMOS LSI
- 64-Pin Quad-In-Line Package

PIN CONFIGURATION



PIN NAMES	
BUS_0-BUS_{13}	Address/Instruction Bus
$P0_0$	Input Port 0_0
$P0_1$/$\overline{SCK}$	Input Port 0_1/Serial Clock
$P0_2$/SO	Input Port 0_2/Serial Output
$P0_3$/SI	Input Port 0_3/Serial Input
$P1_0$-$P1_3$	Input/Output Port 1
$P2_0$/$\overline{STB}$	Output Port 2_0/Port 1 Strobe Output
$P2_1$/PT_{OUT}	Output Port 2_1/Timer Output
$P2_0$-$P2_3$	Output Port 2
$P3_0$-$P3_3$	Output Port 3
$P4_0$-$P4_3$	Input/Output Port 4
$P5_0$-$P5_3$	Input/Output Port 5
$P6_0$-$P6_3$	Input/Output Port 6
$P7_0$-$P7_3$	Input/Output Port 7
INT_0	Interrupt Input 0
INT_1	Interrupt Input 1
INT_2	Interrupt Input 2
CL_1, CL_2	System Clock Input, Output
X_1, X_2	Crystal Clock Input, Output
ALE	Address LATCH ENABLE
$\overline{CSOUT}$	Chip Select Output
$\overline{DOUT}$	
LCD CL	LCD Clock Output
$\overline{PSEN}$	Program Store ENABLE
$\overline{STB}$	Strobe 1
RESET	Reset
V_{DD}	Power Supply Positive
V_{SS}	Ground
$\overline{TEST}$	Factory Test Pin
NC	No Connection

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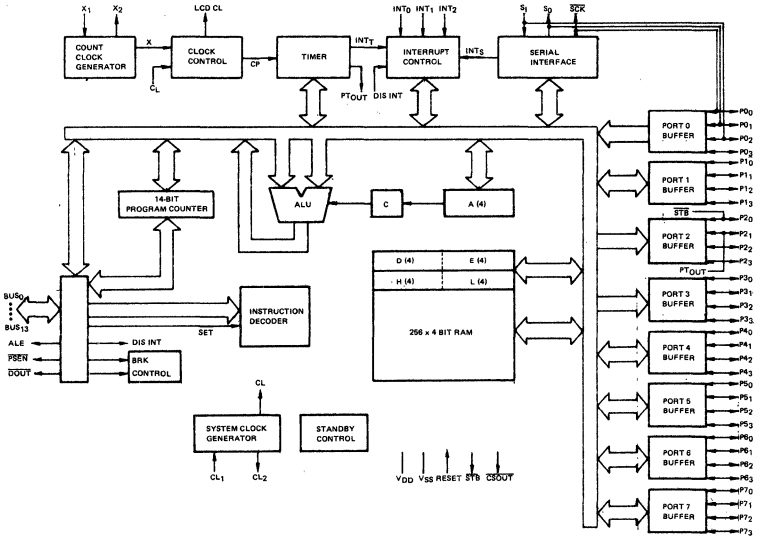
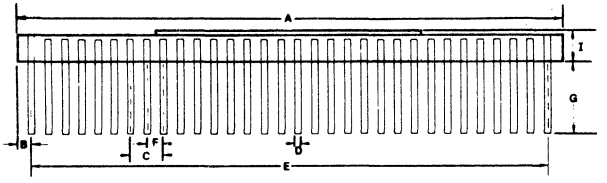
BLOCK DIAGRAM



PACKAGE OUTLINE μPD7500B



Ceramic

ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002