# 3. ELECTRICAL CHARACTERISTICS

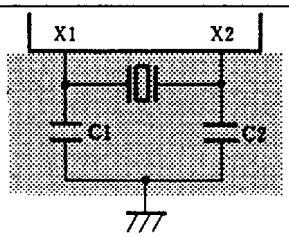
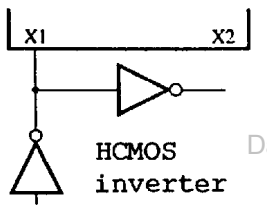
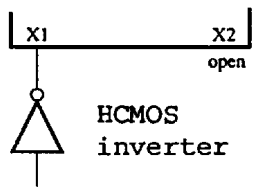
## 3.1 uPD70335-8, 70335-10

### Absolute maximum ratings (Ta=25°C)

| Parameter | Symbol | Test condition | Ratings | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | -0.5 to +7.0 | V |
| | $V_{TH}$ | | -0.5 to $V_{DD}$+0.5 | V |
| Input voltage | $V_I$ | | -0.5 to $V_{DD}$+0.5 | V |
| Output voltage | $V_O$ | | -0.5 to $V_{DD}$+0.5 | V |
| Output low current | $I_{OL}$ | Per pin | 4.0 | mA |
| | | Total, all output | 50 | mA |
| Output high current | $I_{OH}$ | Per pin | -2.0 | mA |
| | | Total, all output | -20 | mA |
| Operation temperature | $T_{opt}$ | | -10 to +70 | °C |
| Storage temperature | $T_{stg}$ | | -65 to +150 | °C |

## Oscillator characteristics

uPD70335-8 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±10%, $V_{SS}$=0V, 0V≦$V_{TH}$≦$V_{DD}$+0.1V)
uPD70335-10 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±5%, $V_{SS}$=0V, 0V≦$V_{TH}$≦$V_{DD}$+0.1V)

| Resonator | Recommended circuit | Parameter | uPD70335-8 | | uPD70335-10 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| Ceramic resonator or crystal resonator |  | Oscillation frequency ($f_{XX}$) | 4 | 16 | 4 | 20 | MHz |
| External clock | ①  or ②  | X1 input frequency ($f_X$) | 4 | 16 | 4 | 20 | MHz |
| | | X1 input rising, falling time ($t_{XR}$, $t_{XF}$) | 0 | 20 | 0 | 15 | ns |
| | | X1 input high, low level width ($t_{WXH}$, $t_{WXL}$) | 20 | | 16 | | ns |

Remarks 1: Put the oscillator near to the X1 and X2 pins as much as possible.
2: Do not pass any other signal line through the shaded area.

Recommended oscillator constant

(1) The following ceramic resonators and external capacitors are recommended:

| Manufacturer | Part number | Recommended constant | |
|---|---|---|---|
| | | C1[pF] | C2[pF] |
| MURATA | CSA16.00MX040 | 30 | 30 |
| | CSA20.00MX040 | 10 | 10 |
| TDK | FCR16.0M2G | 30 | 30 |

(2) The following crystal resonators and external capacitors are recommended:

| Manufacturer | Part number | Recommended constant | |
|---|---|---|---|
| | | C1[pF] | C2[pF] |
| KINSEKI | HC-49/U (KR-100) | 22 | 22 |
| | HC-49/U (KR-160) | 22 | 22 |
| | HC-49/U (KR-200) | 22 | 22 |

Remarks: For such as characteristics of each oscillator, confirm to the each maker.

Capacitance (Ta=25°C, $V_{DD}$=0 V)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | $f_C$=1 MHz Unmeasured pins returned to 0 V | | | 10 | pF |
| Output capacitance | $C_O$ | | | | 20 | pF |
| Input/output capacitance | $C_{IO}$ | | | | 20 | pF |

## DC characteristics

uPD70335-8 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±10%)
uPD70335-10 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±5%)

| Parameter | Symbol | Test condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | | | 0 | | 0.8 | V |
| Input high voltage | $V_{IH1}$ | Except for $\overline{RESET}$, P10/NMI, X1, or X2 | | 2.2 | | $V_{DD}$ | V |
| | $V_{IH2}$ | $\overline{RESET}$, P10/NMI, X1, X2 | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$=1.6 mA | | | | 0.45 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-0.4 mA | | $V_{DD}$-1.0 | | | V |
| Input current | $I_I$ | EA, P10/NMI; $0 \leq V_I \leq V_{DD}$ | | | | ±20 | uA |
| Input leakage current | $I_{LI}$ | Except for EA or P10/NMI; $0 \leq V_I \leq V_{DD}$ | | | | ±10 | uA |
| Output leakage current | $I_{LO}$ | $0 \leq V_O \leq V_{DD}$ | | | | ±10 | uA |
| $V_{TH}$ current | $I_{TH}$ | $0 V \leq V_{TH} \leq V_{DD}$ | | | 0.5 | 1.0 | mA |
| $V_{DD}$ power supply current | $I_{DD1}$ | Operation mode | uPD70335-8 | | 65 | 120 | mA |
| | | | uPD70335-10 | | 95 | 130 | |
| | $I_{DD2}$ | HALT mode | uPD70335-8 | | 25 | 50 | mA |
| | | | uPD70335-10 | | 30 | 55 | |
| | $I_{DD3}$ | STOP mode | | | 10 | 30 | uA |



## AC characteristics

(1) uPD70335-8 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±10%)

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| X1 input cycle time | $t_{CYX}$ | | 62 | 250 | ns |
| X1 input high, low level width | $t_{WXH}$, $t_{WXL}$ | | 20 | | ns |
| X1 input rising, falling time | $t_{XR}$, $t_{XF}$ | | | 20 | ns |
| CLKOUT output cycle time | $t_{CYK}$ | $f_X/2$, $T=t_{CYK}$ | 125 | 200 | ns |
| CLKOUT output high, low level width | $t_{WKH}$, $t_{WKL}$ | | 0.5T-15 | | ns |
| CLKOUT output rising, falling time | $t_{KR}$, $t_{KF}$ | | | 15 | ns |
| Input rising, falling time | $t_{IR}$, $t_{IF}$ | Except for $\overline{RESET}$, NMI, X1 or X2 | | 20 | ns |
| | $t_{IRS}$, $t_{IFS}$ | $\overline{RESET}$, NMI | | 30 | ns |
| Output rising, falling time | $t_{OR}$, $t_{OF}$ | Except for CLKOUT | | 20 | ns |

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| CLKOUT → address delay time | $t_{DKA}$ | | 15 | 90 | ns |
| Address → data input delay time | $t_{DADR}$ | | | (n+1.5)T-70 | ns |
| $\overline{MREQ}$ ↓ → data delay time | $t_{DMRD}$ | | | (n+2)T-60 | ns |
| $\overline{MSTB}$ ↓ → data delay time | $t_{DMSD}$ | | | (n+1)T-60 | ns |
| $\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ delay time | $t_{DMRMS1}$ | Read operation | T-35 | T+35 | ns |
| | $t_{DMRMS2}$ | Write operation | (n+1)T-35 | (n+1)T+35 | ns |
| $\overline{MREQ}$ low level width | $t_{WMRL}$ | | (n+2)T-30 | (n+2)T+30 | ns |
| $\overline{MREQ}$ ↓ → Address hold time | $t_{HMRA}$ | | 0.5T-30 | | ns |
| Address hold time from $\overline{MREQ}$ ↑ | $t_{HMA}$ | | 0.5T-30 | | ns |
| Data input hold time from $\overline{MREQ}$ ↑ | $t_{HMDR}$ | | 0 | | ns |
| Control signal recovery time | $t_{RVC}$ | | T-25 | | ns |
| Address → data output delay time | $t_{DADW}$ | | 0.5T-35 | 0.5T+50 | ns |
| Address setup time to $\overline{MREQ}$ ↓ | $t_{DAMR}$ | | 0.5T-30 | | ns |
| Second address setup time to $\overline{MSTB}$ ↓ | $t_{DRMS}$ | Read operation | 0.5T-30 | | ns |
| | $t_{DWMS}$ | Write operation | (n+0.5)T-30 | | ns |
| $\overline{MSTB}$ low level width | $t_{WMSL1}$ | Read operation | (n+1)T-30 | | ns |
| | $t_{WMSL2}$ | Write operation | T-30 | T+30 | ns |
| Data output setup time to $\overline{MSTB}$ ↑ | $t_{SDM}$ | | (n+2)T-50 | | ns |
| Address setup time to $\overline{IOSTB}$ ↓ | $t_{DAIS}$ | | 0.5T-30 | | ns |
| $\overline{IOSTB}$ ↓ → data delay time | $t_{DISD}$ | | | (n+1)T-60 | ns |
| $\overline{MREQ}$ ↓ → $\overline{IOSTB}$ ↓ delay time | $t_{DMRIS}$ | | T-35 | | ns |
| $\overline{IOSTB}$ low level width | $t_{WISL}$ | | (n+1)T-30 | | ns |
| Address hold time from $\overline{IOSTB}$ ↑ | $t_{HISA}$ | | 0.5T-30 | | ns |
| Data input hold time from $\overline{IOSTB}$ ↑ | $t_{HISDR}$ | | 0 | | ns |
| Data output setup time to $\overline{IOSTB}$ ↑ | $t_{SDIS}$ | | (n+2)T-50 | | ns |
| $\overline{DMARQ}$ setup time to $\overline{MREQ}$ ↓ | $t_{SDADQ}$ | Demand release mode, n≥2 | | (n-1)T-50 | ns |
| $\overline{DMARQ}$ hold time from $\overline{DMAAK}$ ↓ | $t_{HDADQ}$ | Demand release mode | 0 | | ns |
| $\overline{DMAAK}$ output low level width | $t_{WDMRL}$ | | (n+2.5)T-30 | | ns |
| $\overline{DMAAK}$ ↓ → $\overline{TC}$ ↓ delay time | $t_{DDATC}$ | | | 0.5T+50 | ns |
| $\overline{TC}$ low level width | $t_{WTCL}$ | | (n+3)T-30 | | ns |
| $\overline{DMAAK}$ output low level width | $t_{WDMWL}$ | | (n+2)T-30 | | ns |
| Address setup time to $\overline{REFRQ}$ ↓ | $t_{DARF}$ | | 0.5T-30 | | ns |
| $\overline{REFRQ}$ low level width | $t_{WRFL}$ | | (n+2)T-30 | | ns |
| Address hold time from $\overline{REFRQ}$ ↑ | $t_{HRFA}$ | | 0.5T-30 | | ns |

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{RESET}$ low level width | $t_{WRSL1}$ | STOP mode release or power on reset | 30 | | ms |
| | $t_{WRSL2}$ | System reset | 5 | | us |
| READY setup time to $\overline{MREQ}\downarrow$ | $t_{SCRY0}$ | n≧2 | | 2T-100 | ns |
| | $t_{SCRY}$ | n≧3 | | nT-100 | ns |
| READY hold time from $\overline{MREQ}\downarrow$ | $t_{HCRY0}$ | n=2 | 2T | | ns |
| | $t_{HCRY}$ | n≧3 | nT | | ns |
| | $t_{HCRY1}$ | n≧3 | (n-1)T | | ns |
| READY setup time to $\overline{IOSTB}\downarrow$ | $t_{SSRY0}$ | n≧2 | | T-100 | ns |
| | $t_{SSRY}$ | n≧3 | | (n-1)T-100 | ns |
| READY hold time from $\overline{IOSTB}\downarrow$ | $t_{HSRY0}$ | n=2 | T | | ns |
| | $t_{HSRY}$ | n≧3 | (n-1)T | | ns |
| | $t_{HSRY1}$ | n≧3 | (n-2)T | | ns |
| HLDRQ setup time from CLKOUT$\downarrow$ | $t_{SHQK}$ | | 30 | | ns |
| CLKOUT$\uparrow$ → $\overline{HLDAK}\downarrow$ delay time | $t_{DKHA}$ | | 15 | 80 | ns |
| Bus float → $\overline{HLDAK}\downarrow$ delay time | $t_{CFHA}$ | | T-50 | | ns |
| $\overline{HLDAK}\uparrow$ → bus output delay time | $t_{DHAC}$ | | T-50 | | ns |
| HLDRQ$\downarrow$ → $\overline{HLDAK}\uparrow$ delay time | $t_{DHQHA}$ | | | 3T+160 | ns |
| HLDRQ$\downarrow$ → bus output delay time | $t_{DHQC}$ | | 3T+30 | | ns |
| HLDRQ low level width | $t_{WHQL}$ | | 1.5T | | ns |
| $\overline{HLDAK}$ low level width | $t_{WHAL}$ | | T | | ns |
| INT, DMARQ setup time to CLKOUT$\downarrow$ | $t_{SIQK}$ | | 30 | | ns |
| INT, DMARQ high, low level width | $t_{WIQH}$, $t_{WIQL}$ | | 8T | | ns |
| $\overline{POLL}$ setup time to CLKOUT$\downarrow$ | $t_{SPLK}$ | | 30 | | ns |
| NMI high, low level width | $t_{WNIH}$, $t_{WNIL}$ | | 5 | | us |
| $\overline{CTS}$ low level width | $t_{WCTL}$ | | 2T | | ns |
| INT setup time to CLKOUT$\downarrow$ | $t_{SIRK}$ | | 30 | | ns |
| CLKOUT$\downarrow$ → $\overline{INTAK}\downarrow$ delay time | $t_{DKIA}$ | | 15 | 80 | ns |
| INT hold time from $\overline{INTAK}\downarrow$ | $t_{HIAIQ}$ | | 0 | | ns |
| $\overline{INTAK}$ low level width | $t_{WIAL}$ | | 2T-30 | | ns |
| $\overline{INTAK}$ high level width | $t_{WIAH}$ | | T-30 | | ns |
| $\overline{INTAK}\downarrow$ → data delay time | $t_{DIAD}$ | | | 2T-130 | ns |
| Data hold time from $\overline{INTAK}\uparrow$ | $t_{HIAD}$ | | 0 | 0.5T | ns |

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{CYTK}$ | | 1000 | | ns |
| $\overline{SCK0}$ high, low level width | $t_{WSTH}$, $t_{WSTL}$ | | 450 | | ns |
| $\overline{SCK0}\downarrow \longrightarrow$ TxD delay time | $t_{DTKD}$ | | | 210 | ns |
| $\overline{SCK0}\downarrow \longrightarrow$ TxD hold time | $t_{HTKD}$ | | 20 | | ns |
| $\overline{CTS0}$ cycle time | $t_{CYRK}$ | | 1000 | | ns |
| $\overline{CTS0}$ high, low level width | $t_{WSRH}$, $t_{WSRL}$ | | 420 | | ns |
| RxD setup time to, hold time from $\overline{CTS0}\uparrow$ | $t_{SRDK}$, $t_{HKRD}$ | | 80 | | ns |

## (2) uPD70335-10 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±5%)

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| X1 input cycle time | $t_{CYX}$ | | 49 | 250 | ns |
| X1 input high, low level width | $t_{WXH}$, $t_{WXL}$ | | 16 | | ns |
| X1 input rising, falling time | $t_{XR}$, $t_{XF}$ | | | 15 | ns |
| CLKOUT output cycle time | $t_{CYK}$ | $f_X/2$, T=$t_{CYK}$ | 100 | 2000 | ns |
| CLKOUT output high, low level width | $t_{WKH}$, $t_{WKL}$ | | 0.5T-12 | | ns |
| CLKOUT output rising, falling time | $t_{KR}$, $t_{KF}$ | | | 12 | ns |
| Input rising, falling time | $t_{IR}$, $t_{IF}$ | Except for $\overline{RESET}$, NMI, X1, or X2 | | 20 | ns |
| | $t_{IRS}$, $t_{IFS}$ | $\overline{RESET}$, NMI | | 30 | ns |
| Output rising, falling time | $t_{OR}$, $t_{OF}$ | Except for CLKOUT | | 15 | ns |
| CLKOUT → address delay time | $t_{DKA}$ | | 15 | 75 | ns |
| Address → data input delay time | $t_{DADR}$ | | | (n+1.5)T-60 | ns |
| $\overline{MREQ}$ ↓ → data delay time | $t_{DMRD}$ | | | (n+2)T-50 | ns |
| $\overline{MSTB}$ ↓ → data delay time | $t_{DMSD}$ | | | (n+1)T-50 | ns |
| $\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ delay time | $t_{DMRMS1}$ | Read operation | T-30 | T+30 | ns |
| | $t_{DMRMS2}$ | Write operation | (n+1)T-30 | (n+1)T+30 | ns |
| $\overline{MREQ}$ low level width | $t_{WMRL}$ | | (n+2)T-25 | (n+2)T+25 | ns |
| Address hold time from $\overline{MREQ}$ ↑ | $t_{HMRA}$ | | 0.5T-25 | | ns |
| Data input hold time from $\overline{MREQ}$ ↑ | $t_{HMA}$ | | 0.5T-30 | | ns |
| Data input hold time from $\overline{MREQ}$ ↑ | $t_{HMDR}$ | | 0 | | ns |
| Control signal recovery time | $t_{RVC}$ | | T-25 | | ns |
| Address → data output delay time | $t_{DADW}$ | | 0.5T-30 | 0.5T+50 | ns |
| Address setup time to $\overline{MREQ}$ ↓ | $t_{DAMR}$ | | 0.5T-30 | | ns |
| Second address setup time to $\overline{MSTB}$ ↓ | $t_{DRMS}$ | Read operation | 0.5T-30 | | ns |
| | $t_{DWMS}$ | Write operation | (n+0.5)T-30 | | ns |
| $\overline{MSTB}$ low level width | $t_{WMSL1}$ | Read operation | (n+1)T-25 | | ns |
| | $t_{WMSL2}$ | Write operation | T-20 | T+20 | ns |
| Data output setup time to $\overline{MSTB}$ ↑ | $t_{SDM}$ | | (n+2)T-50 | | ns |
| Address setup time to IOSTB ↓ | $t_{DAIS}$ | | 0.5T-30 | | ns |
| $\overline{IOSTB}$ ↓ → data delay time | $t_{DISD}$ | | | (n+1)T-50 | ns |
| $\overline{MREQ}$ ↓ → IOSTB ↓ delay time | $t_{DMRIS}$ | | T-30 | | ns |
| $\overline{IOSTB}$ low level width | $t_{WISL}$ | | (n+1)T-25 | | ns |
| Address hold time from $\overline{IOSTB}$ ↑ | $t_{HISA}$ | | 0.5T-30 | | ns |
| Data input hold time from $\overline{IOSTB}$ ↑ | $t_{HISDR}$ | | 0 | | ns |
| Data output setup time to $\overline{IOSTB}$ ↑ | $t_{SDIS}$ | | (n+2)T-50 | | ns |

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{DMARQ}$ setup time to $\overline{MREQ}\downarrow$ | $t_{SDADQ}$ | Demand release mode, n≧2 | | (n-1)T-50 | ns |
| $\overline{DMARQ}$ hold time from $\overline{DMAAK}\downarrow$ | $t_{HDADQ}$ | Demand release mode | 0 | | ns |
| $\overline{DMAAK}$ output low level width | $t_{WDMRL}$ | | (n+2.5)T-25 | | ns |
| $\overline{DMAAK}\downarrow \rightarrow \overline{TC}\downarrow$ delay time | $t_{DDATC}$ | | | 0.5t+35 | ns |
| $\overline{TC}$ low level width | $t_{WTCL}$ | | (n+3)T-25 | | ns |
| $\overline{DMAAK}$ output low level width | $t_{WDMWL}$ | | (n+2)T-25 | | ns |
| Address setup time to $\overline{REFRQ}\downarrow$ | $t_{DARF}$ | | 0.5T-30 | | ns |
| $\overline{REFRQ}$ low level width | $t_{WRFL}$ | | (n+2)T-25 | | ns |
| Address hold time from $\overline{REFRQ}\downarrow$ | $t_{HRFA}$ | | 0.5T-30 | | ns |
| $\overline{RESET}$ low level width | $t_{WRSL1}$ | STOP mode release or power on reset | 30 | | ms |
| | $t_{WRSL2}$ | System reset | 5 | | us |
| READY setup time to $\overline{MREQ}\downarrow$ | $t_{SCRY0}$ | n≧2 | | 2T-80 | ns |
| | $t_{SCRY}$ | n≧3 | | nT-80 | ns |
| READY hold time from $\overline{MREQ}\downarrow$ | $t_{HCRY0}$ | n=2 | 2T | | ns |
| | $t_{HCRY}$ | n≧3 | nT | | ns |
| | $t_{HCRY1}$ | n≧3 | (n-1)T | | ns |
| READY setup time to $\overline{IOSTB}\downarrow$ | $t_{SSRY0}$ | n≧2 | | T-80 | ns |
| | $t_{SSRY}$ | n≧3 | | (n-1)T-80 | ns |
| READY hold time from $\overline{IOSTB}\downarrow$ | $t_{HSRY0}$ | n=2 | T | | ns |
| | $t_{HSRY}$ | n≧3 | (n-1)T | | ns |
| | $t_{HSRY1}$ | n≧3 | (n-2)T | | ns |
| HLDRQ setup time to CLKOUT$\downarrow$ | $t_{SHQK}$ | | 25 | | ns |
| CLKOUT$\downarrow \rightarrow \overline{HLDAK}\downarrow$ delay time | $t_{DKHA}$ | | 15 | 70 | ns |
| Bus float $\rightarrow \overline{HLDAK}\downarrow$ delay time | $t_{CFHA}$ | | T-35 | | ns |
| $\overline{HLDAK}\uparrow \rightarrow$ bus output delay time | $t_{DHAC}$ | | T-35 | | ns |
| HLDRQ$\downarrow \rightarrow \overline{HLDAK}\downarrow$ delay time | $t_{DHQHA}$ | | | 3T+160 | ns |
| HLDRQ$\downarrow \rightarrow$ bus output delay time | $t_{DHQC}$ | | 3T+30 | | ns |
| HLDRQ low level width | $t_{WHQL}$ | | 1.5T | | ns |
| $\overline{HLDAK}$ low level width | $t_{WHAL}$ | | T | | ns |
| INTP, DMARQ setup time to CLKOUT$\downarrow$ | $t_{SIQK}$ | | 25 | | ns |
| INTP, DMARQ high, low level width | $t_{WIQH}$, $t_{WIQL}$ | | 8T | | ns |
| POLL setup time to CLKOUT$\downarrow$ | $t_{SPLK}$ | | 25 | | ns |
| NMI high, low level width | $t_{WNIH}$, $t_{WNIL}$ | | 5 | | us |
| $\overline{CTS}$ low level width | $t_{WCTL}$ | | 2T | | ns |

Remarks: n denotes the number of wait states. When no wait states are inserted, n is 0.

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| INT setup time to CLKOUT↓ | $t_{SIRK}$ | | 25 | | ns |
| CLKOUT ↓ → $\overline{INTAK}$↓ delay time | $t_{DKIA}$ | | 15 | 70 | ns |
| INT hold time from $\overline{INTAK}$↓ | $t_{HIAIQ}$ | | 0 | | ns |
| $\overline{INTAK}$ low level width | $t_{WIAL}$ | | 2T-25 | | ns |
| $\overline{INTAK}$ high level width | $t_{WIAH}$ | | T-25 | | ns |
| $\overline{INTAK}$ ↓ → data delay time | $t_{DIAD}$ | | | 2T-100 | ns |
| Data hold time from $\overline{INTAK}$↑ | $t_{HIAD}$ | | 0 | 0.5T | ns |
| $\overline{SCKO}$ cycle time | $t_{CYTK}$ | | 1000 | | ns |
| $\overline{SCKO}$ high, low level width | $t_{WSTH}$, $t_{WSTL}$ | | 450 | | ns |
| $\overline{SCKO}$ ↓ → TxD delay time | $t_{DTKD}$ | | | 210 | ns |
| $\overline{SCKO}$ ↓ → TxD hold time | $t_{HTKD}$ | | 20 | | ns |
| $\overline{CTSO}$ cycle time | $t_{CYRK}$ | | 1000 | | ns |
| $\overline{CTSO}$ high, low level width | $t_{WSRH}$, $t_{WSRL}$ | | 420 | | ns |
| RxD setup time to, hold time from $\overline{CTSO}$↑ | $t_{SRDK}$, $t_{HKRD}$ | | 80 | | ns |

## Comparator characteristics

uPD70335-8 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±10%)
uPD70335-10 (Ta=-10 to +70°C, $V_{DD}$=+5.0V±5%)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Comparison accuracy | $V_{ACOMP}$ | | | | ±100 | mV |
| Threshold voltage | $V_{TH}$ | | 0 | | $V_{DD}$+0.1 | V |
| Comparison time | $t_{COMP}$ | | 64 | | 65 | $t_{CYK}$ |
| PT input voltage | $V_{IPT}$ | | 0 | | $V_{DD}$ | V |

## Data memory STOP mode low supply voltage data retention characteristics (Ta=-10 to +70°C)

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 2.5 | 5.5 | V |
| $V_{DD}$ rising, falling time | $t_{RVD}$, $t_{FVD}$ | | 200 | | us |

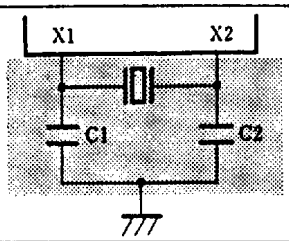
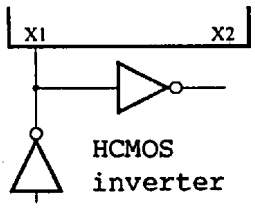
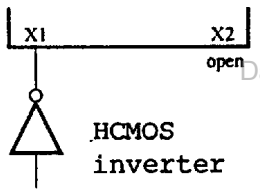
## 3.2 uPD70335(A)-9

### Absolute maximum ratings (Ta=25°C)

| Parameter | Symbol | Test condition | Ratings | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | -0.5 to +7.0 | V |
| | $V_{TH}$ | | -0.5 to $V_{DD}$+0.5 | V |
| Input voltage | $V_I$ | | -0.5 to $V_{DD}$+0.5 | V |
| Output voltage | $V_O$ | | -0.5 to $V_{DD}$+0.5 | V |
| Output low current | $I_{OL}$ | Per pin | 4.0 | mA |
| | | Total, all output | 50 | mA |
| Output high current | $I_{OH}$ | Per pin | -2.0 | mA |
| | | Total, all output | -20 | mA |
| Operation temperature | $T_{opt}$ | | -40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | -65 to +150 | °C |

## Oscillator characteristics

uPD70335(A)-9 (Ta=-40 to +85°C, $V_{DD}$=+5.0V±5%, $V_{SS}$=0V, 0V≦$V_{TH}$≦$V_{DD}$+0.1V)

| Resonator | Recommended circuit | Parameter | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Ceramic resonator or crystal resonator |  | Oscillation frequency ($f_{XX}$) | 4 | 18 | MHz |
| External clock | ①  or ②  | X1 input frequency ($f_X$) | 4 | 18 | MHz |
| | | X1 input rising, falling time ($t_{XR}$, $t_{XF}$) | 0 | 15 | ns |
| | | X1 input high, low level width ($t_{WXH}$, $t_{WXL}$) | 17 | | ns |

Remarks 1: Place the oscillator as close as possible to the X1 and X2 pins.

2: Do not pass any other signal line through the shaded portion.

## Capacitance (Ta=25°C, $V_{DD}$=0 V)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | $f_C$=1 MHz<br>Unmeasured pins returned to 0 V | | | 10 | pF |
| Output capacitance | $C_O$ | | | | 20 | pF |
| Input/output capacitance | $C_{IO}$ | | | | 20 | pF |

## DC characteristics

### uPD70335(A)-9 (Ta=-40 to +85°C, $V_{DD}$=+5.0V±5%)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | | 0 | | 0.8 | V |
| Input high voltage | $V_{IH1}$ | Except for $\overline{RESET}$, P10/NMI, X1, or X2 | 2.2 | | $V_{DD}$ | V |
| | $V_{IH2}$ | $\overline{RESET}$, P10/NMI, X1, X2 | $0.8V_{DD}$ | | $V_{DD}$ | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$=1.6 mA | | | 0.45 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$=-0.4 mA | $V_{DD}$-1.0 | | | V |
| Input current | $I_I$ | $\overline{EA}$, P10/NMI; $0 \leq V_I \leq V_{DD}$ | | | ±20 | uA |
| Input leakage current | $I_{LI}$ | Except for $\overline{EA}$ or P10/NMI; $0 \leq V_I \leq V_{DD}$ | | | ±10 | uA |
| Output leakage current | $I_{LO}$ | $0 \leq V_O \leq V_{DD}$ | | | ±10 | uA |
| $V_{TH}$ current | $I_{TH}$ | $0\ V \leq V_{TH} \leq V_{DD}$ | | 0.5 | 1.0 | mA |
| $V_{DD}$ power supply current | $I_{DD1}$ | Operation mode | | 95 | 130 | mA |
| | $I_{DD2}$ | HALT mode | | 30 | 55 | mA |
| | $I_{DD3}$ | STOP mode | | 15 | 35 | uA |

## AC characteristics

### uPD70335(A)-9 (Ta=-40 to +85°C, $V_{DD}$=+5.0V±5%)

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| X1 input cycle time | $t_{CYX}$ | | 55 | 250 | ns |
| X1 input high, low level width | $t_{WXH}$, $t_{WXL}$ | | 17 | | ns |
| X1 input rising, falling time | $t_{XR}$, $t_{XF}$ | | | 15 | ns |
| CLKOUT output cycle time | $t_{CYK}$ | $f_X/2$, T=$t_{CYK}$ | 111 | 2000 | ns |
| CLKOUT output high, low level width | $t_{WKH}$, $t_{WKL}$ | | 0.5T-12 | | ns |
| CLKOUT output rising, falling time | $t_{KR}$, $t_{KF}$ | | | 12 | ns |
| Input rising, falling time | $t_{IR}$, $t_{IF}$ | Except for $\overline{RESET}$, NMI, X1 or X2 | | 20 | ns |
| | $t_{IRS}$, $t_{IFS}$ | $\overline{RESET}$, NMI | | 30 | ns |
| Output rising, falling time | $t_{OR}$, $t_{OF}$ | Except for CLKOUT | | 15 | ns |
| CLKOUT → address delay time | $t_{DKA}$ | | 15 | 80 | ns |
| Address → data input delay time | $t_{DADR}$ | | | (n+1.5)T-60 | ns |
| $\overline{MREQ}$ ↓ → data delay time | $t_{DMRD}$ | | | (n+2)T-50 | ns |
| $\overline{MSTB}$ ↓ → data delay time | $t_{DMSD}$ | | | (n+1)T-50 | ns |
| $\overline{MREQ}$ ↓ → $\overline{MSTB}$ ↓ delay time | $t_{DMRMS1}$ | Read operation | T-30 | T+30 | ns |
| | $t_{DMRMS2}$ | Write operation | (n+1)T-30 | (n+1)T+30 | ns |
| $\overline{MREQ}$ low level width | $t_{WMRL}$ | | (n+2)T-25 | (n+2)T+25 | ns |
| $\overline{MREQ}$ ↓ → address hold time | $t_{HMRA}$ | | 0.5T-30 | | ns |
| Address hold time from $\overline{MREQ}$ ↑ | $t_{HMA}$ | | 0.5T-35 | | ns |
| Data input hold time from $\overline{MREQ}$ ↑ | $t_{HMDR}$ | | 0 | | ns |
| Control signal recovery time | $t_{RVC}$ | | T-25 | | ns |
| Address → data output delay time | $t_{DADW}$ | | | 0.5T+50 | ns |
| Address setup time to $\overline{MREQ}$ ↓ | $t_{DAMR}$ | | 0.5T-35 | | ns |
| Second address setup time to $\overline{MSTB}$ ↓ | $t_{DRMS}$ | Read operation | 0.5T-30 | | ns |
| | $t_{DWMS}$ | Write operation | (n+0.5)T-30 | | ns |
| $\overline{MSTB}$ low level width | $t_{WMSL1}$ | Read operation | (n+1)T-25 | | ns |
| | $t_{WMSL2}$ | Write operation | T-25 | T+25 | ns |
| Data output setup time to $\overline{MSTB}$ ↑ | $t_{SDM}$ | | (n+2)T-50 | | ns |
| Address setup time to $\overline{IOSTB}$ ↓ | $t_{DAIS}$ | | 0.5T-30 | | ns |
| $\overline{IOSTB}$ ↓ → data delay time | $t_{DISD}$ | | | (n+1)T-50 | ns |
| $\overline{MREQ}$ ↓ → IOSTB ↓ delay time | $t_{DMRIS}$ | | T-35 | | ns |
| IOSTB low level width | $t_{WISL}$ | | (n+1)T-30 | | ns |
| Address hold time from $\overline{IOSTB}$ ↑ | $t_{HISA}$ | | 0.5T-30 | | ns |
| Data input hold time from $\overline{IOSTB}$ ↑ | $t_{HISDR}$ | | 0 | | ns |
| Data output setup time to $\overline{IOSTB}$ ↑ | $t_{SDIS}$ | | (n+2)T-50 | | ns |

Remarks: n represents the number of wait states. n=0 means no wait.

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| $\overline{DMARQ}$ setup time to $\overline{MREQ}\downarrow$ | $t_{SDADQ}$ | Demand release mode, n≥2 | | (n-1)T-50 | ns |
| $\overline{DMARQ}$ hold time from $\overline{DMAAK}\downarrow$ | $t_{HDADQ}$ | Demand release mode | 0 | | ns |
| $\overline{DMAAK}$ output low level width | $t_{WDMRL}$ | | (n+2.5)T-25 | | ns |
| $\overline{DMAAK}\downarrow \rightarrow TC\downarrow$ delay time | $t_{DDATC}$ | | | 0.5T+35 | ns |
| $\overline{TC}$ low level width | $t_{WTCL}$ | | (n+3)T-25 | | ns |
| $\overline{DMAAK}$ output low level width | $t_{WDMWL}$ | | (n+2)T-25 | | ns |
| Address setup time to $\overline{REFRQ}\downarrow$ | $t_{DARF}$ | | 0.5T-35 | | ns |
| $\overline{REFRQ}$ low level width | $t_{WRFL}$ | | (n+2)T-25 | | ns |
| Address hold time from $\overline{REFRQ}\downarrow$ | $t_{HRFA}$ | | 0.5T-35 | | ns |
| $\overline{RESET}$ low level width | $t_{WRSL1}$ | STOP mode release/ power on reset | 30 | | ms |
| | $t_{WRSL2}$ | System reset | 5 | | us |
| READY setup time to $\overline{MREQ}\downarrow$ | $t_{SCRY0}$ | n≥2 | | 2T-80 | ns |
| | $t_{SCRY}$ | n≥3 | | nT-80 | ns |
| READY hold time from $\overline{MREQ}\downarrow$ | $t_{HCRY0}$ | n=2 | 2T | | ns |
| | $t_{HCRY}$ | n≥3 | nT | | ns |
| | $t_{HCRY1}$ | n≥3 | (n-1)T | | ns |
| READY setup time to $\overline{IOSTB}\downarrow$ | $t_{SSRY0}$ | n≥2 | | T-80 | ns |
| | $t_{SSRY}$ | n≥3 | | (n-1)T-80 | ns |
| READY hold time from $\overline{IOSTB}\downarrow$ | $t_{HSRY0}$ | n=2 | T | | ns |
| | $t_{HSRY}$ | n≥3 | (n-1)T | | ns |
| | $t_{HSRY1}$ | n≥3 | (n-2)T | | ns |
| HLDRQ setup time to CLKOUT$\downarrow$ | $t_{SHQK}$ | | 25 | | ns |
| CLKOUT$\downarrow \rightarrow \overline{HLDAK}\downarrow$ delay time | $t_{DKHA}$ | | 15 | 75 | ns |
| Bus float $\rightarrow \overline{HLDAK}\downarrow$ delay time | $t_{CFHA}$ | | T-35 | | ns |
| $\overline{HLDAK}\downarrow \rightarrow$ bus output delay time | $t_{DHAC}$ | | T-35 | | ns |
| HLDRQ$\downarrow \rightarrow \overline{HLDAK}\downarrow$ delay time | $t_{DHQHA}$ | | | 3T+160 | ns |
| HLDRQ$\downarrow \rightarrow$ bus output delay time | $t_{DHQC}$ | | 3T+30 | | ns |
| HLDRQ low level width | $t_{WHQL}$ | | 1.5T | | ns |
| $\overline{HLDAK}$ low level width | $t_{WHAL}$ | | T | | ns |
| INT, DMARQ setup time to CLKOUT$\downarrow$ | $t_{SIQK}$ | | 25 | | ns |
| INT, DMARQ high, low level width | $t_{WIQH}$, $t_{WIQL}$ | | 8T | | ns |
| $\overline{POLL}$ setup time to CLKOUT$\downarrow$ | $t_{SPLK}$ | | 30 | | ns |
| NMI high, low level width | $t_{WNIH}$, $t_{WNIL}$ | | 5 | | us |
| $\overline{CTS}$ low level width | $t_{WCTL}$ | | 2T | | ns |

Remarks: n represents the number of wait states. n=0 means no wait.

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| INT setup time to CLKOUT ↓ | $t_{SIRK}$ | | 25 | | ns |
| CLKOUT ↓ → $\overline{INTAK}$ ↓ delay time | $t_{DKIA}$ | | 15 | 75 | ns |
| INT hold time from $\overline{INTAK}$ ↓ | $t_{HIAIQ}$ | | 0 | | ns |
| $\overline{INTAK}$ low level width | $t_{WIAL}$ | | 2T-25 | | ns |
| $\overline{INTAK}$ high level width | $t_{WIAH}$ | | T-25 | | ns |
| $\overline{INTAK}$ ↓ → data delay time | $t_{DIAD}$ | | | 2T-100 | ns |
| Data hold time from $\overline{INTAK}$ ↑ | $t_{HIAD}$ | | 0 | 0.5T | ns |
| $\overline{SCK0}$ cycle time | $t_{CYTK}$ | | 1000 | | ns |
| $\overline{SCK0}$ high, low level width | $t_{WSTH}$, $t_{WSTL}$ | | 450 | | ns |
| $\overline{SCK0}$ ↓ → TxD delay time | $t_{DTKD}$ | | | 210 | ns |
| $\overline{SCK0}$ ↓ → TxD hold time | $t_{HTKD}$ | | 20 | | ns |
| $\overline{CTS0}$ cycle time | $t_{CYRK}$ | | 1000 | | ns |
| $\overline{CTS0}$ high, low level width | $t_{WSRH}$, $t_{WSRL}$ | | 420 | | ns |
| RxD setup time to CTS0, hold time from $\overline{CTS0}$ ↑ | $t_{SRDK}$, $t_{HKRD}$ | | 80 | | ns |

## Comparator characteristics

uPD70335(A)-9 (Ta=-40 to +85°C, $V_{DD}$=+5.0V±5%)

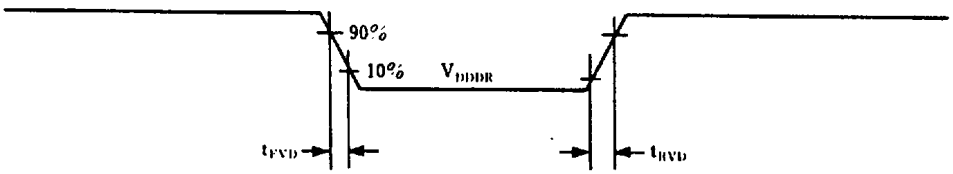


| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Comparison accuracy | $V_{ACOMP}$ | | | | ±100 | mV |
| Threshold voltage | $V_{TH}$ | | 0 | | $V_{DD}$+0.1 | V |
| Comparison time | $t_{COMP}$ | | 64 | | 6.5 | $t_{CYK}$ |
| PT input voltage | $V_{IPT}$ | | 0 | | $V_{DD}$ | V |

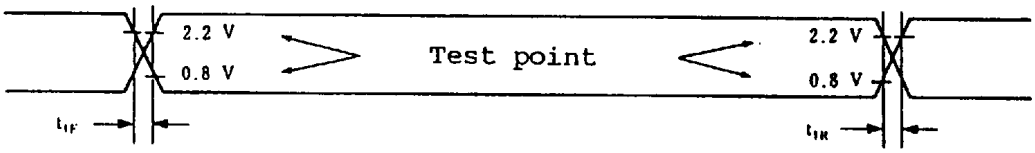
## Data memory STOP mode low supply voltage data retention characteristics (Ta=-40 to +85°C)

| Parameter | Symbol | Test condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 2.5 | 5.5 | V |
| $V_{DD}$ rising, falling time | $t_{RVD}$, $t_{FVD}$ | | 200 | | us |

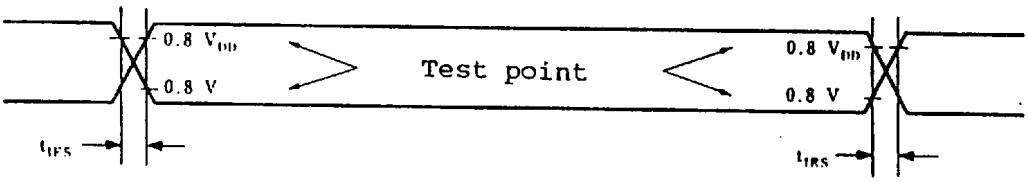
Data retention timing




AC test input waveform (except for RESET, NMI, X1, or X2)



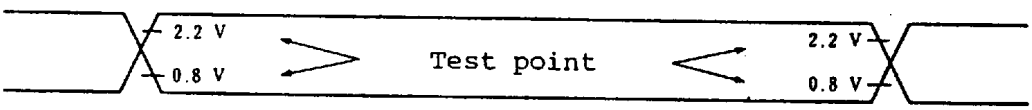

AC test input waveform (RESET, NMI, X1, X2)



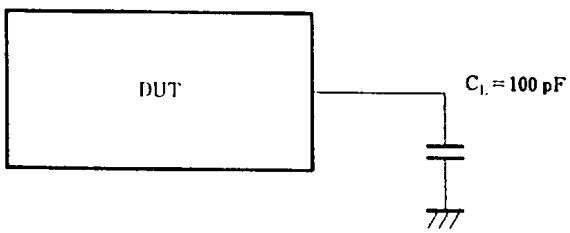

AC test output test points



Output load condition: 100 pF

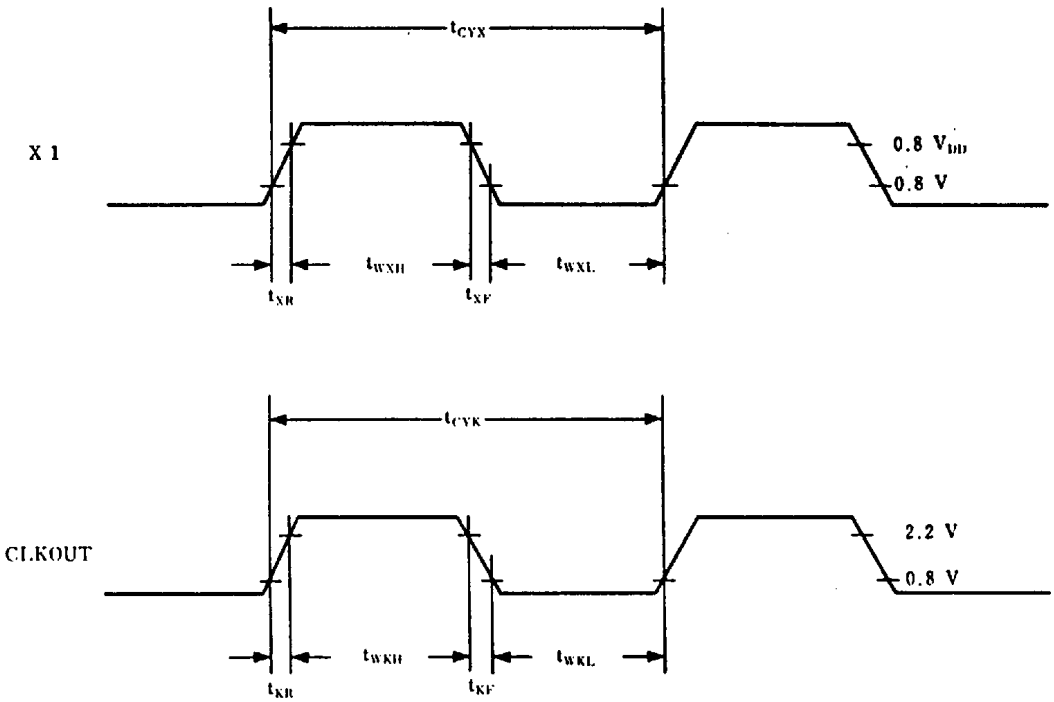



Load condition



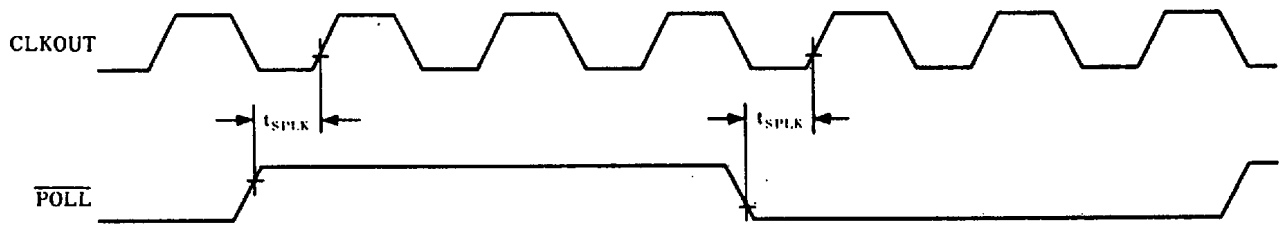

Caution: If the load capacitance exceeds 100 pF because of the circuit configuration, set the load capacitance of the device to 100 pF or less by inserting a buffer, etc.

## Clock timing



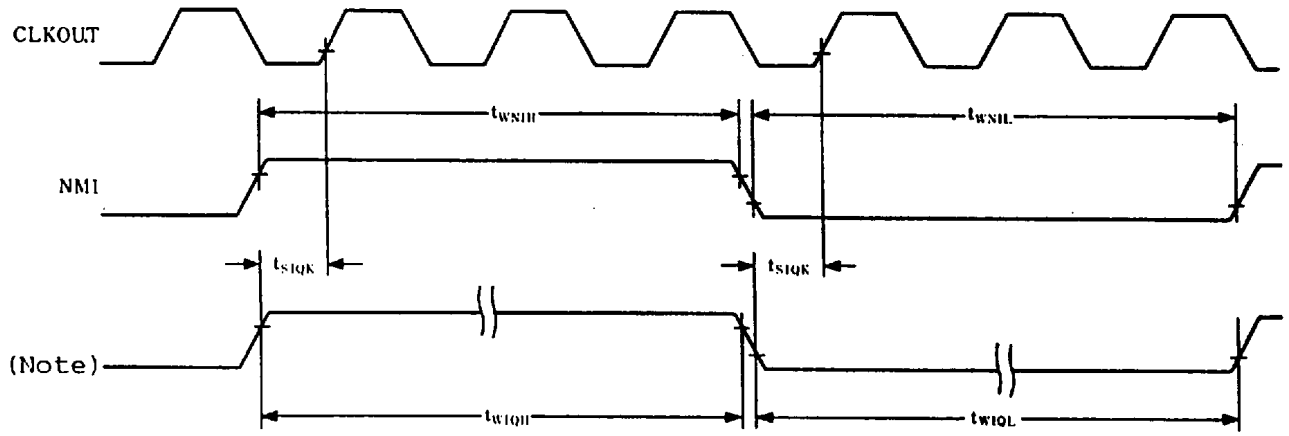

## $\overline{\text{POLL}}$ input timing





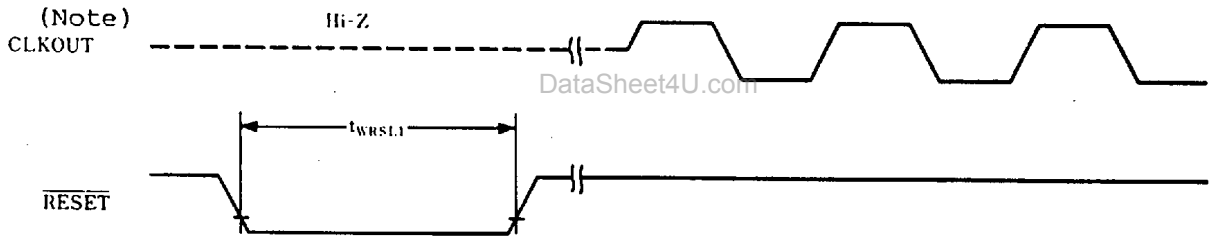

## $\overline{\text{CTS0}}$-$\overline{\text{CTS1}}$ input timing

Interrupt input/DMA input timing



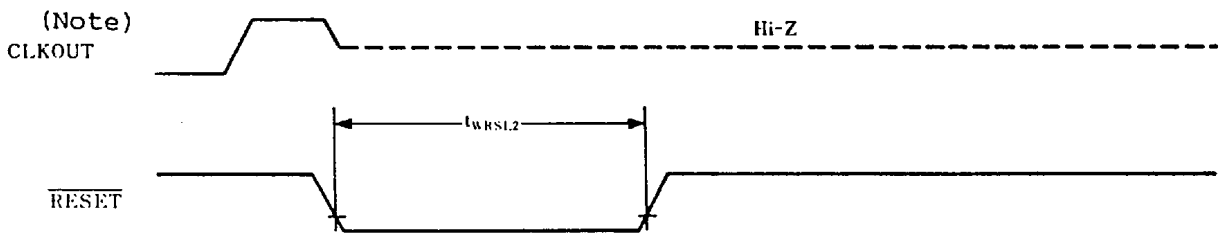

$\overline{\text{RESET}}$ input timing

At STOP mode release or power on reset:




Note: The CLKOUT signal is set in CLKOUT output, then output.

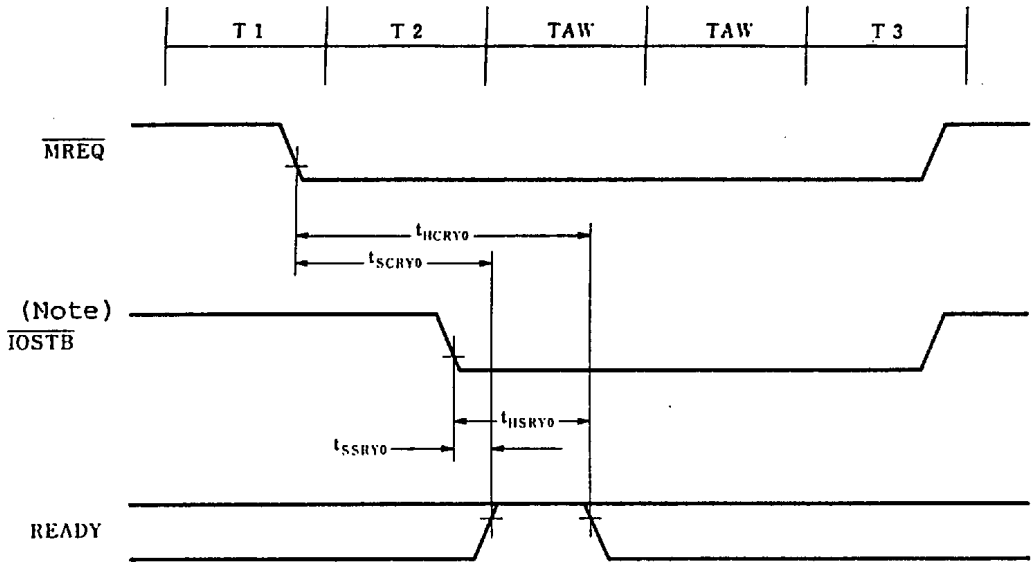
At system reset:



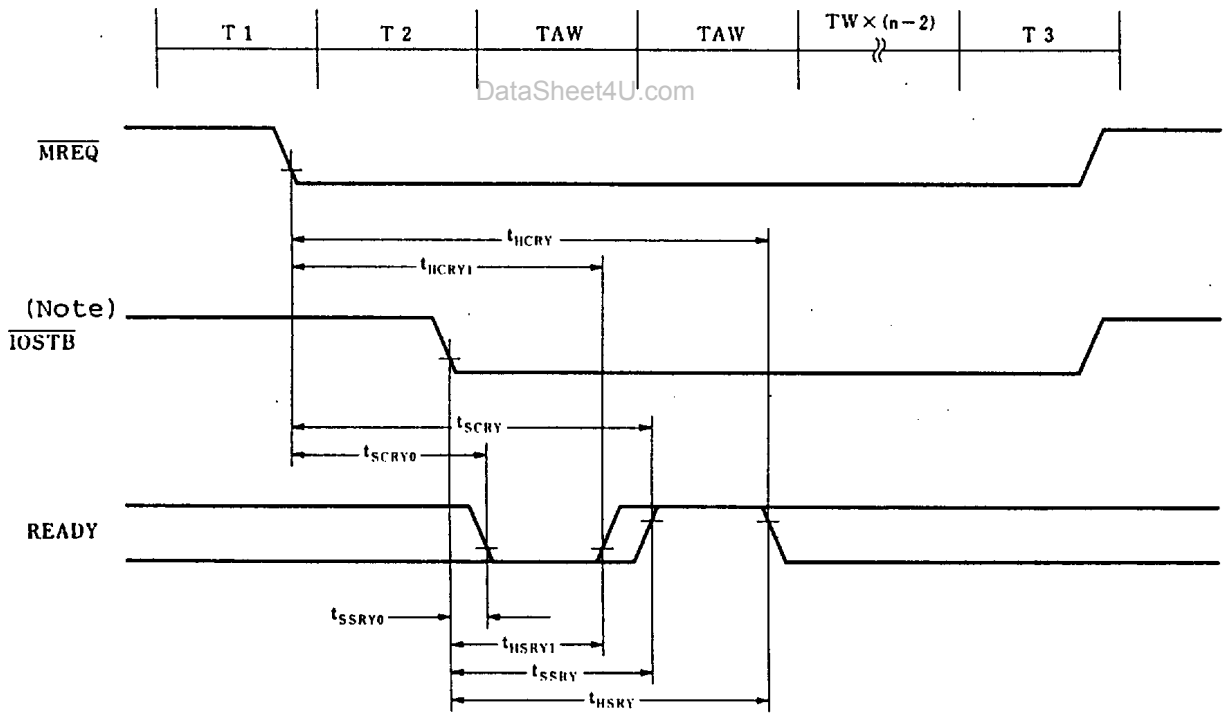

Note: CLKOUT output is set in the input port when RESET is input.

## Ready timing

When two wait states are inserted:




When extra (n-2) wait states are inserted:

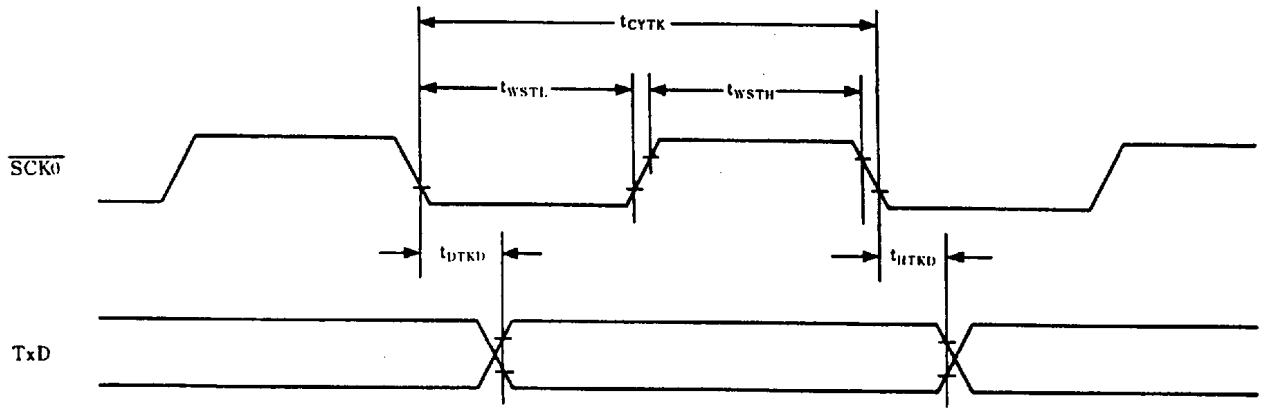



Note: Only I/O cycle

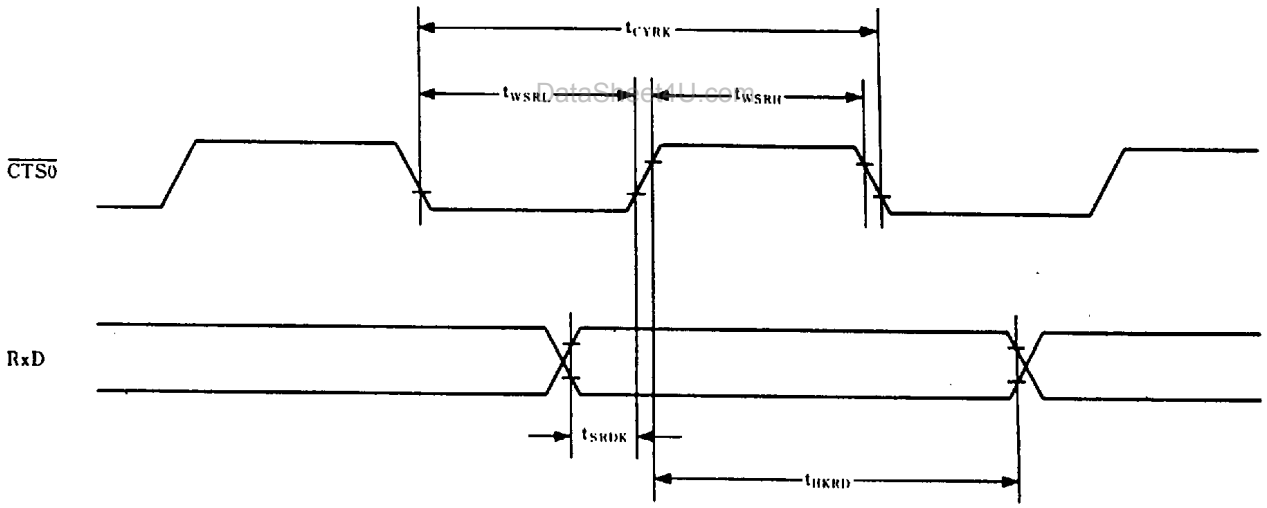
Caution: For wait state insertion by external READY signal, the wait control register (WTC) must be set to 11 (two waits + inserted states by READY pin)

## Serial operation

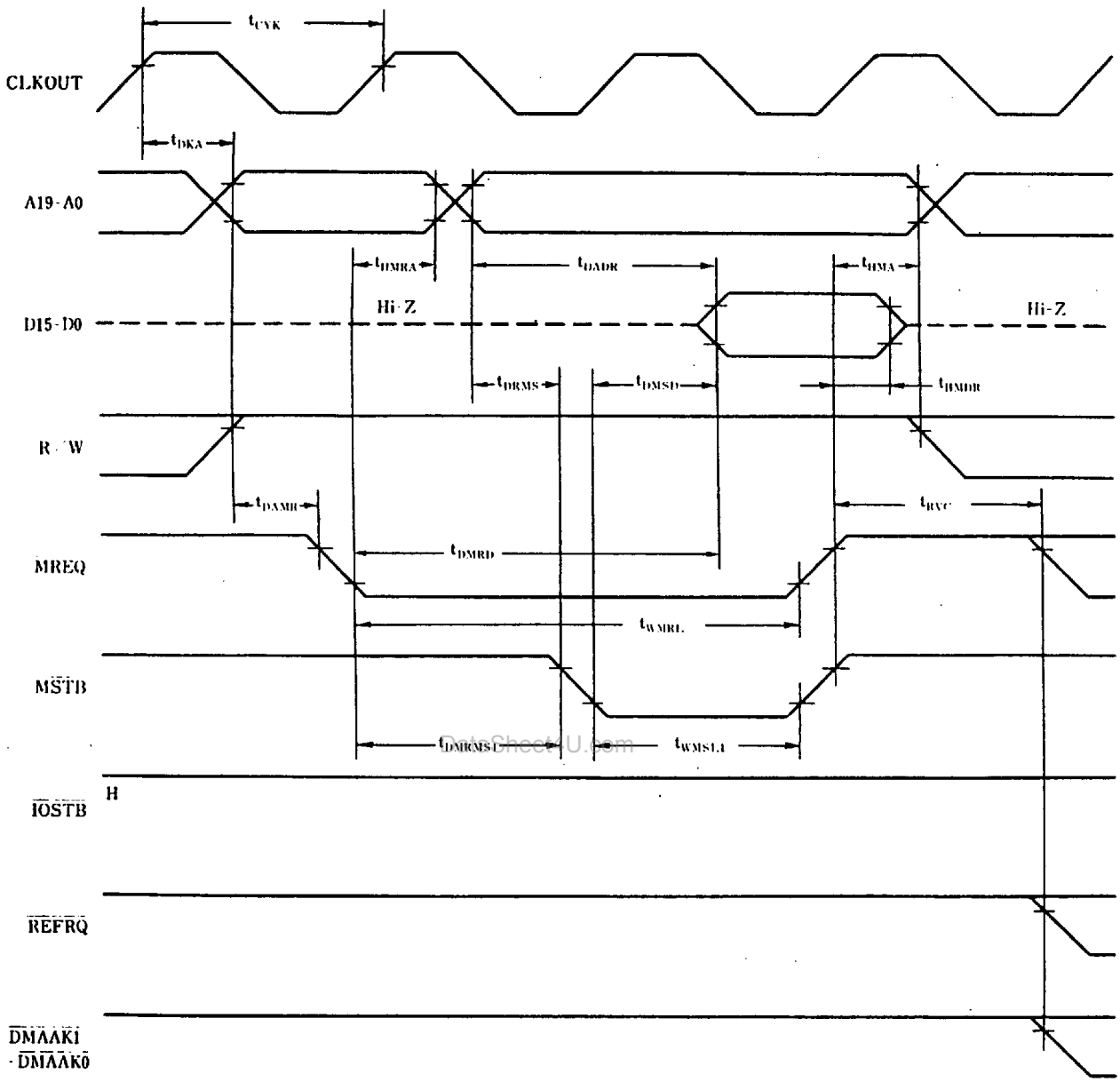
### In I/O interface mode transmission



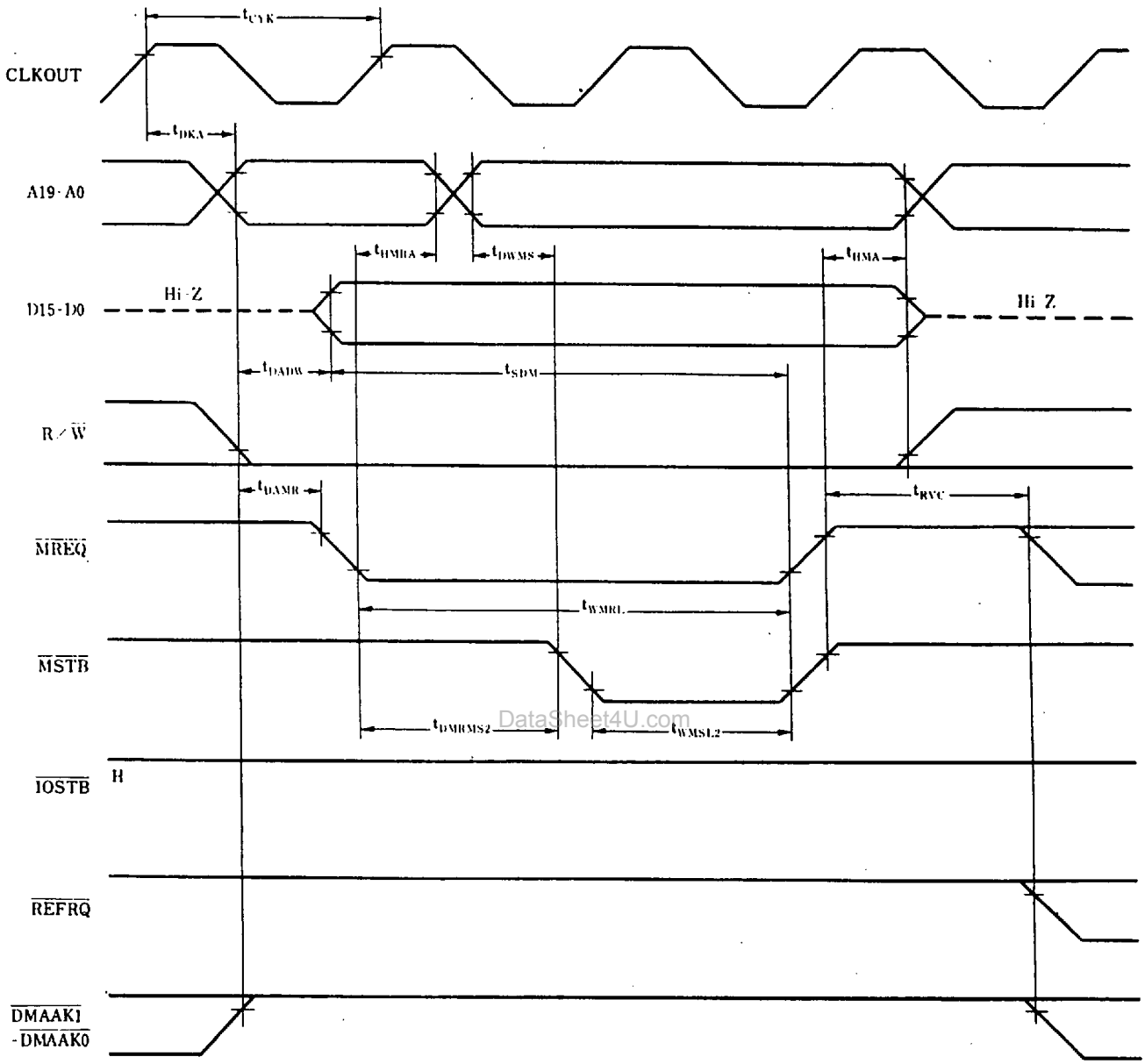

### In I/O interface mode reception



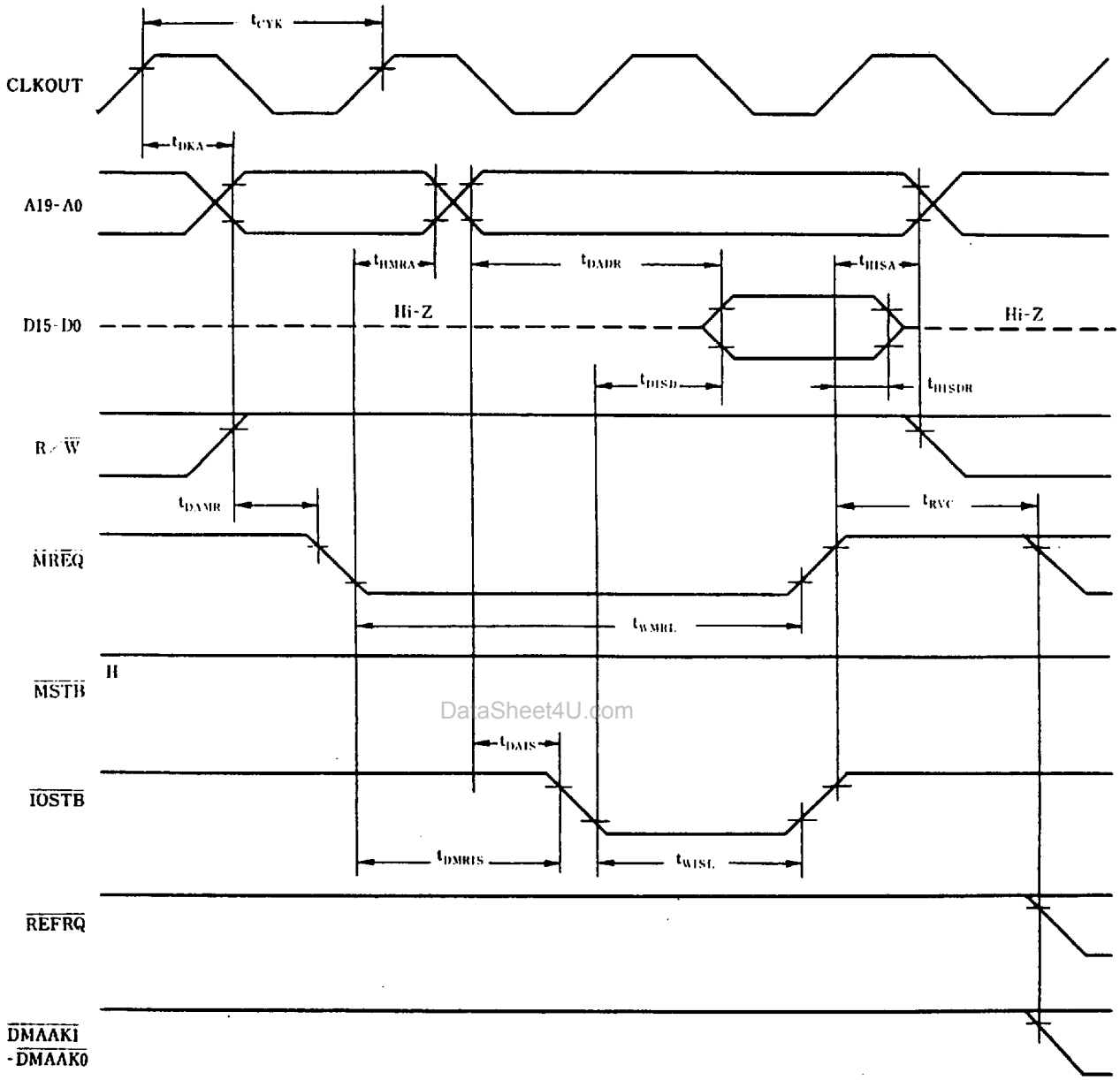
## Read operation



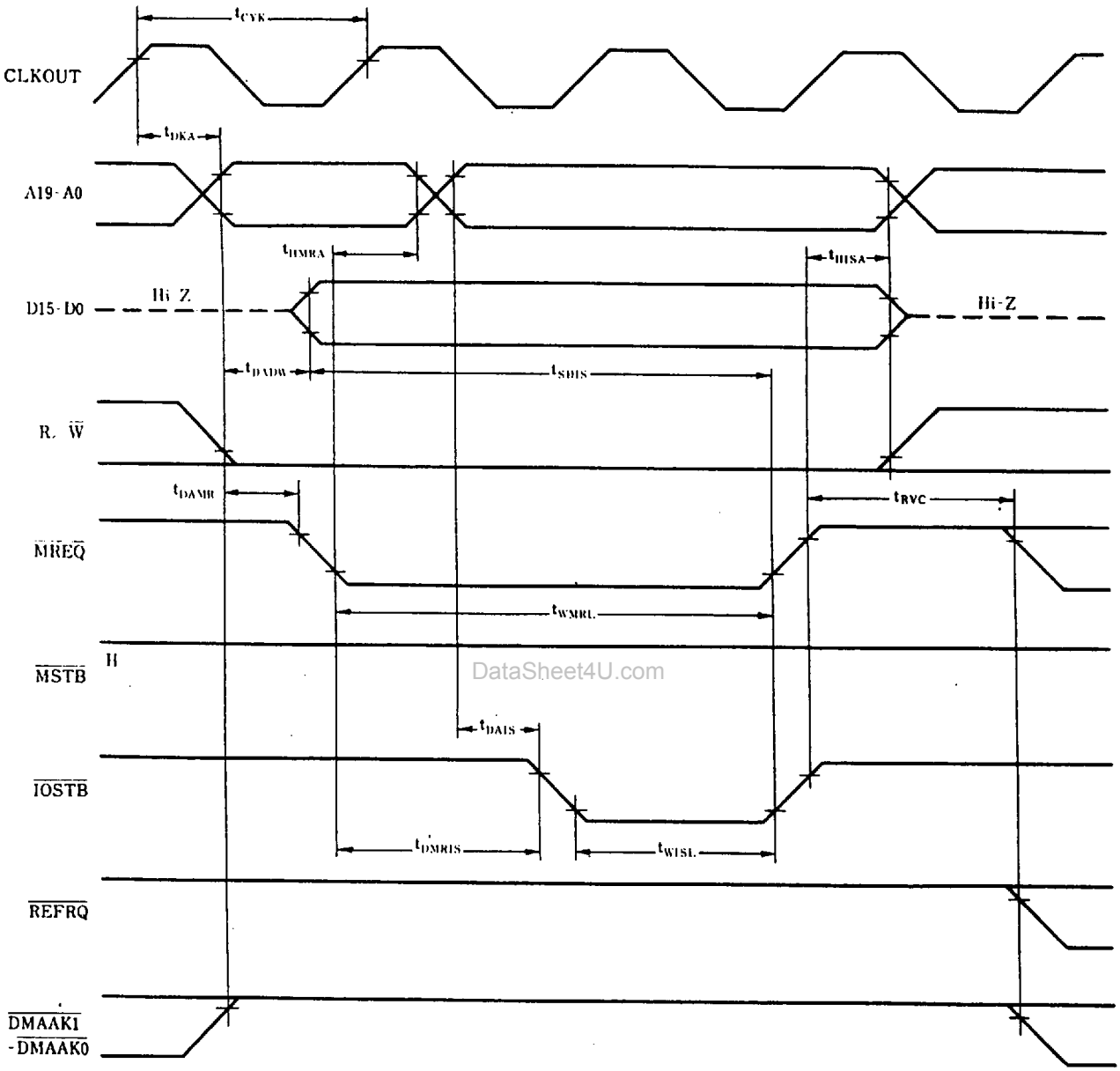
## Write operation



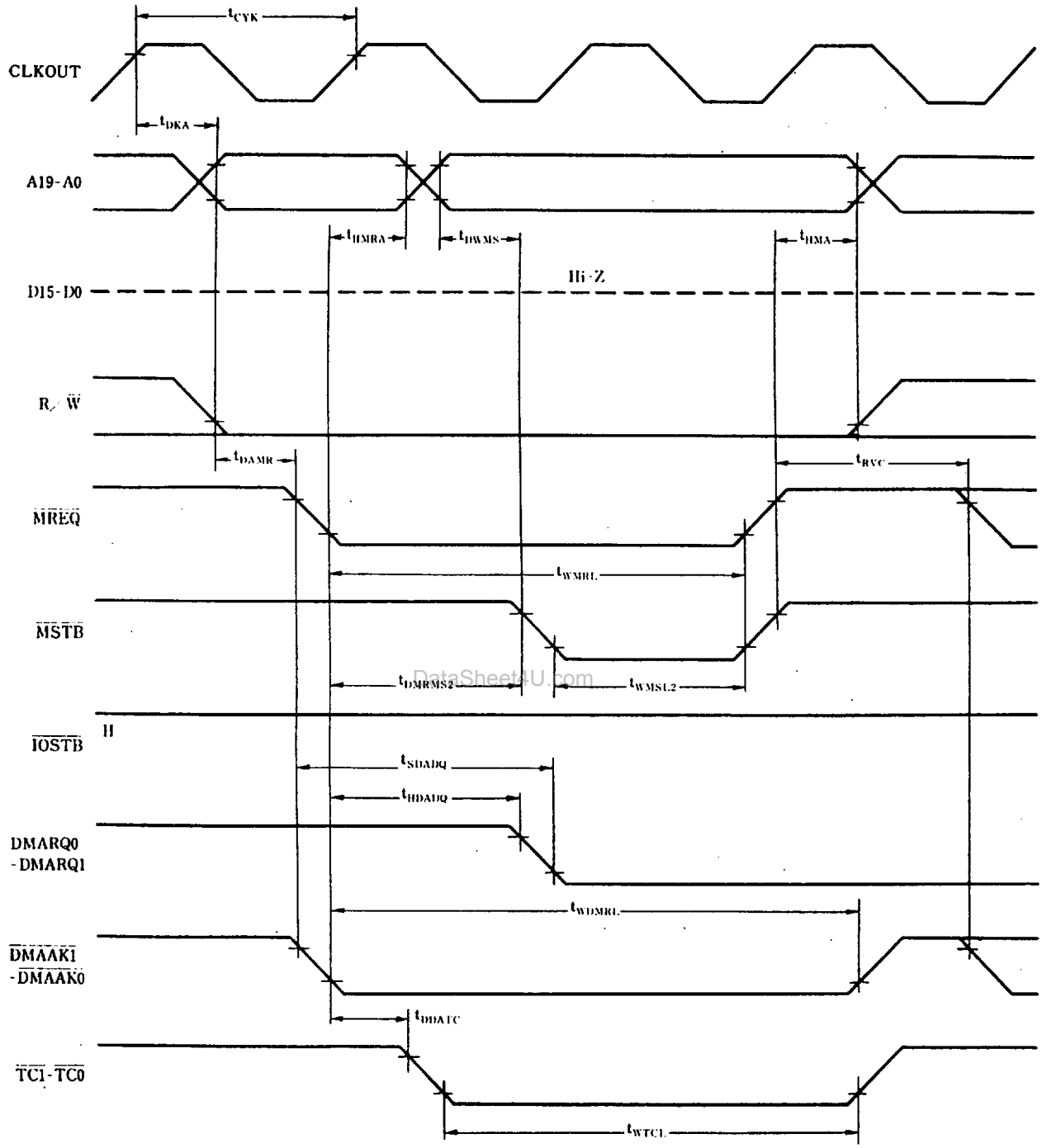
## I/O read timing



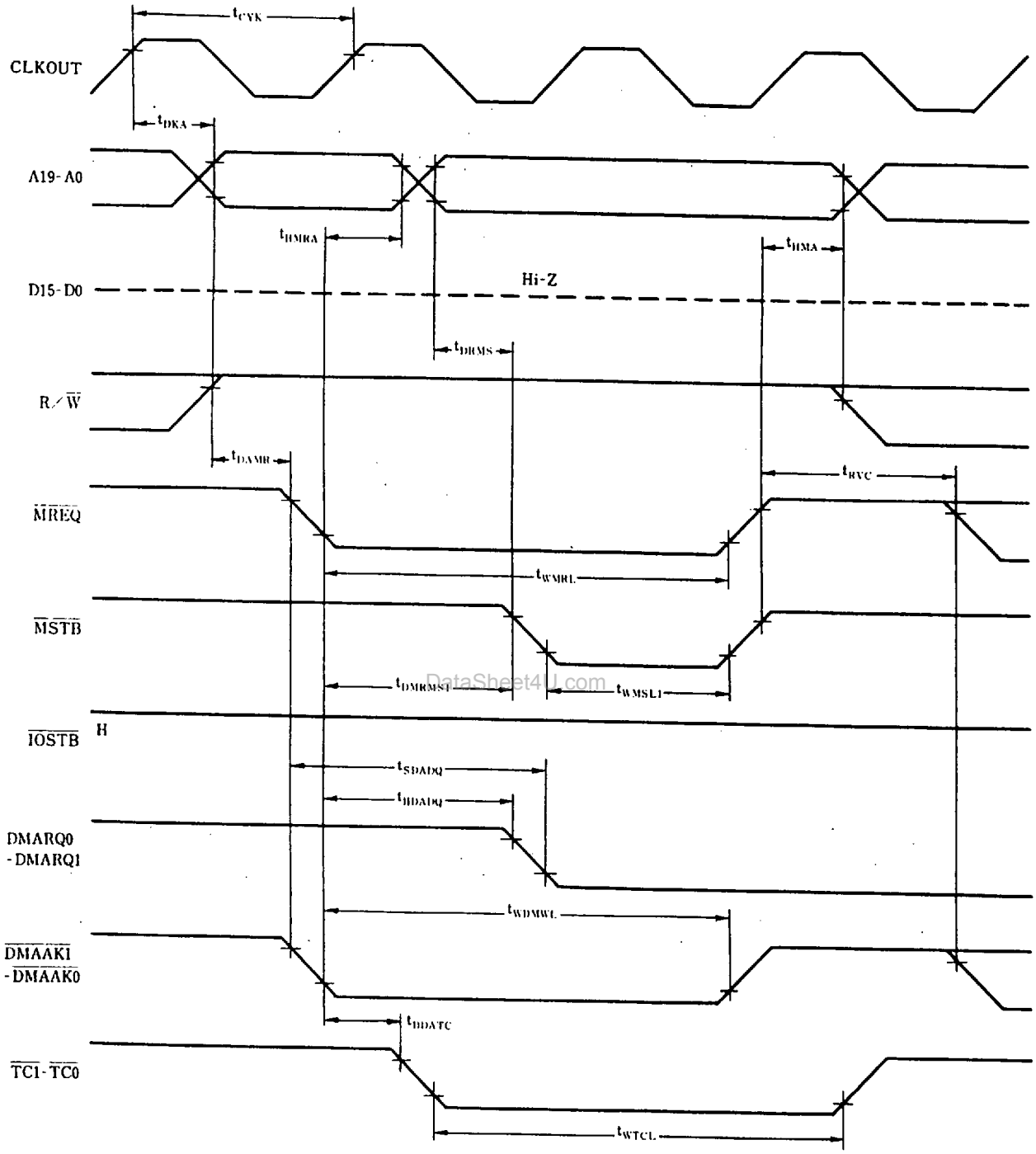
# I/O write timing



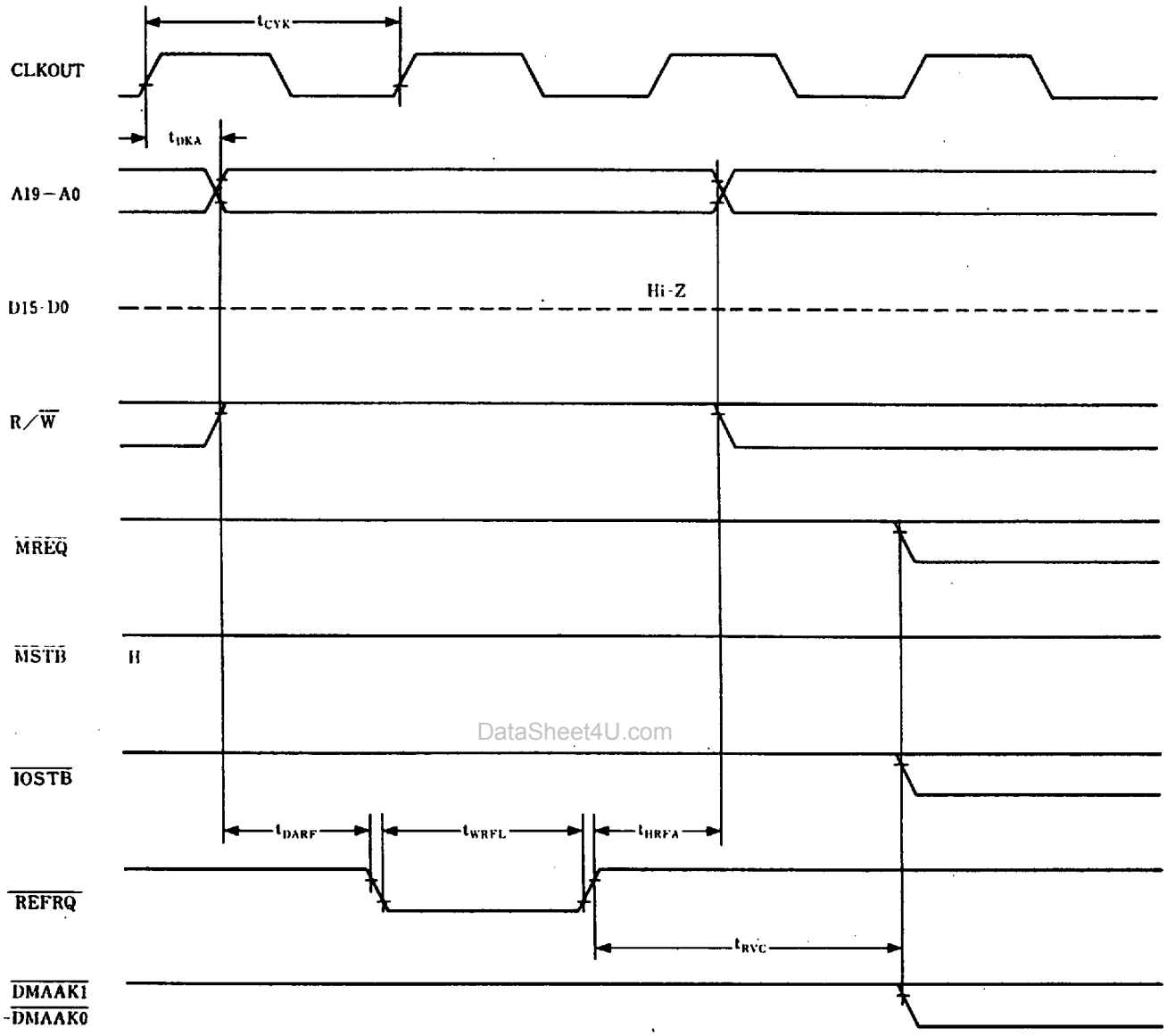
# DMA (I/O to memory) timing



## DMA (memory to I/O) timing

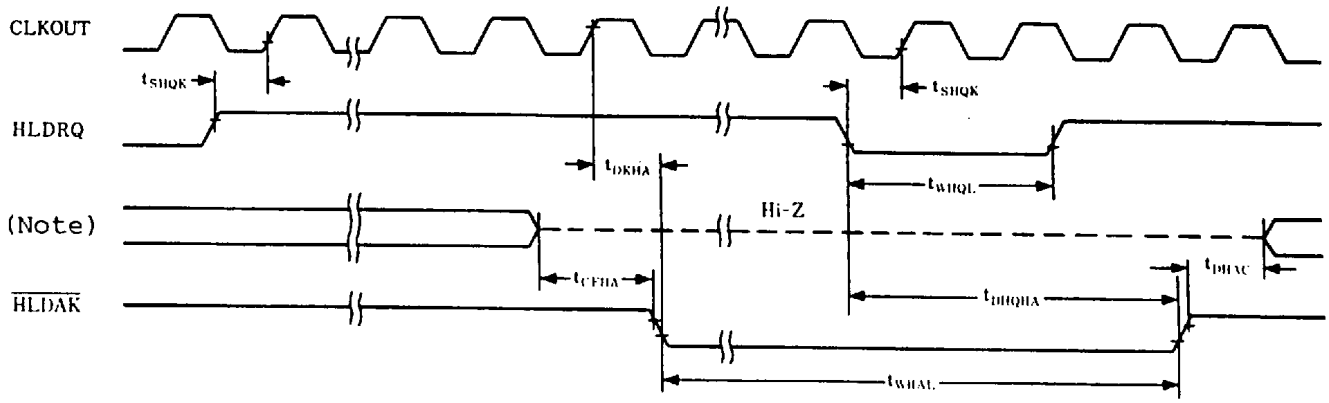


## Refresh timing

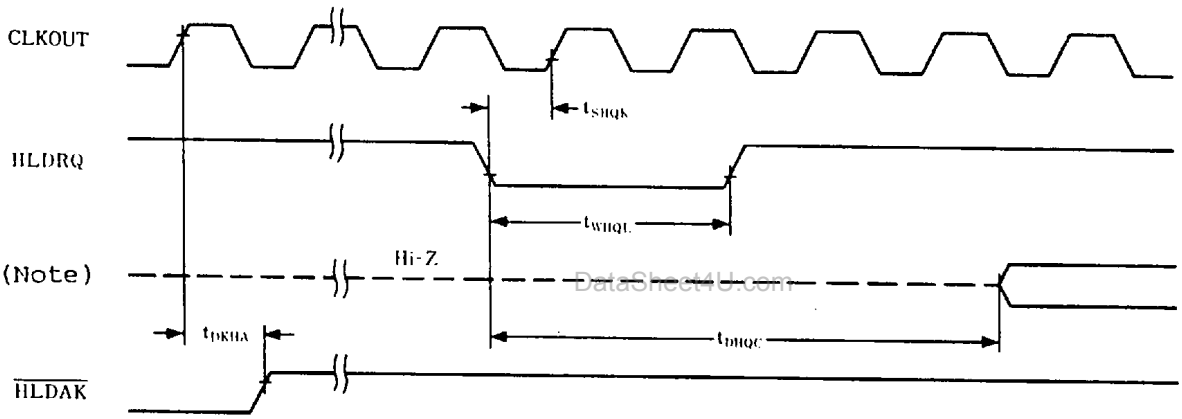


## Hold request/acknowledge timing

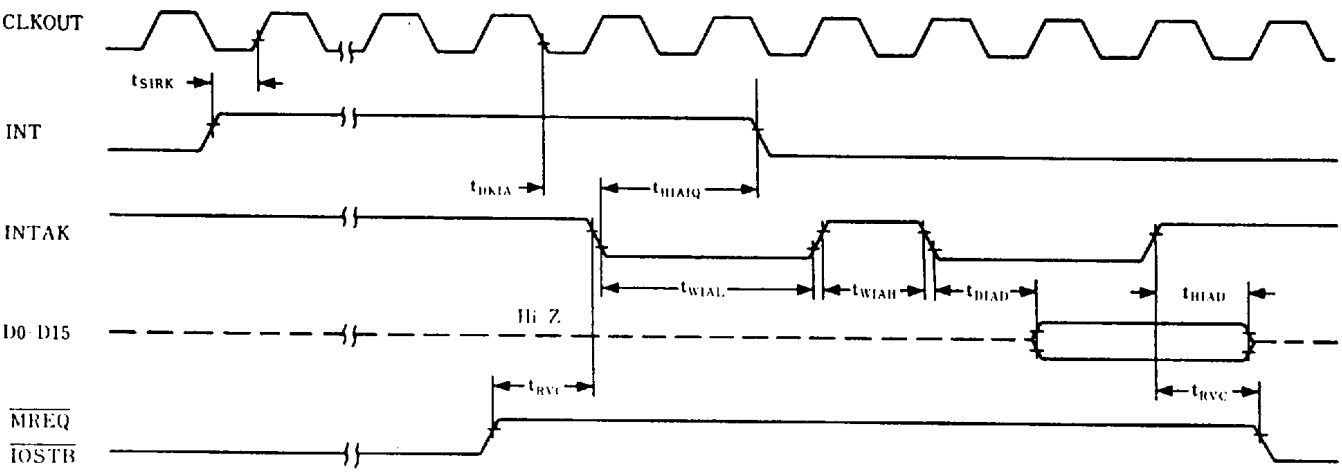
### Normal mode




### HOLD mode release when memory is refreshed

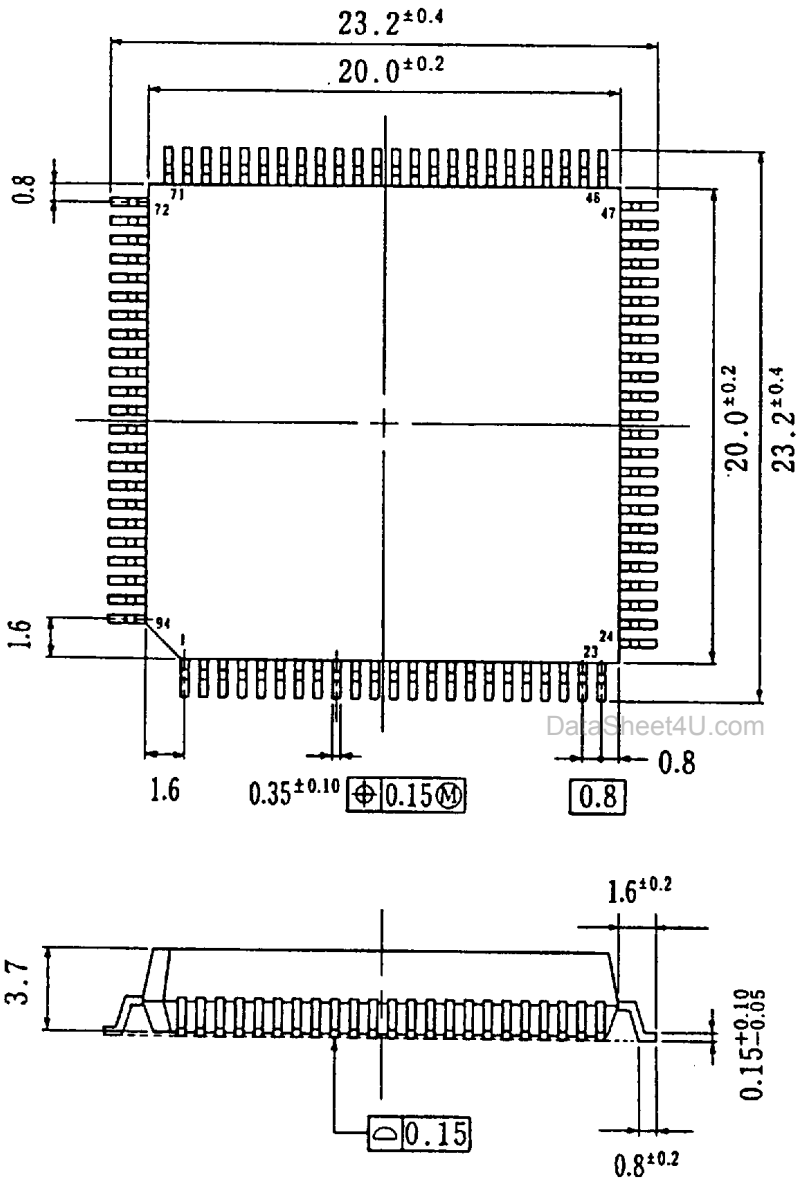



## External interrupt request/acknowledge timing

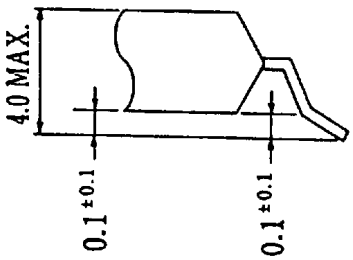


# 4. PACKAGE INFORMATION

Package Information of 94-pin Plastic QFP (□20)
(Dimension unit: mm)

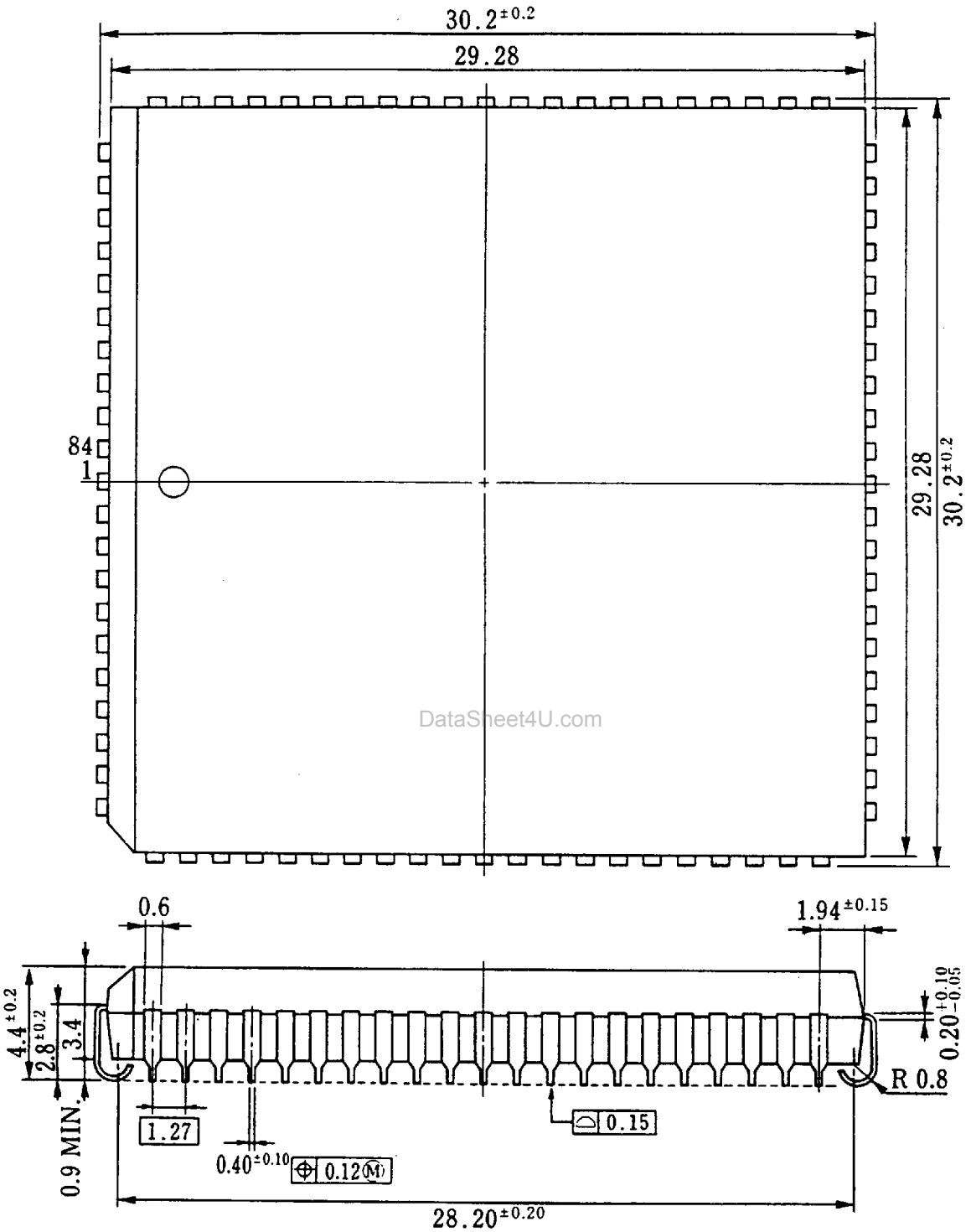



Detailed drawing of pin tip form




S94GJ-80-5BG-1

## 84-pin Plastic Leaded Chip Carrier (□1150) (Dimension unit: mm)




P84L-50A3-1