μCOM-4 4-BIT SINGLE CHIP ROM-LESS EVALUATION CHIP

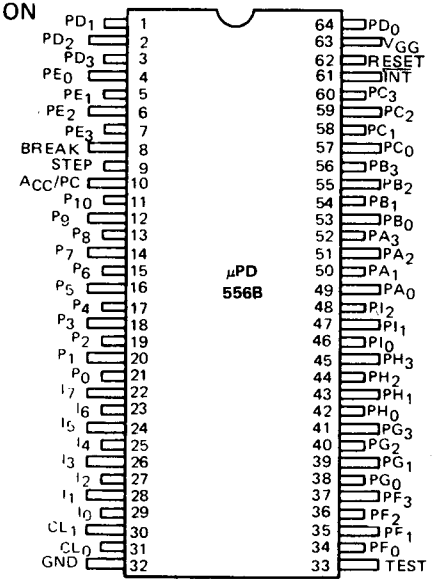
DESCRIPTION

The μPD556B is the ROM-less evaluation chip for the μCOM-4 4-bit single chip microcomputer family. The μPD556B is used in conjunction with an external 2048 x 8-bit program memory, such as the μPD2716 UV EPROM, to emulate each of the 14 different μCOM-4 single chip microcomputers.

The μPD556B contains a 96 x 4-bit RAM, which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The μPD556B executes all 80 instructions of the extended μCOM-4 family instruction set.

The μPD556B provides 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. It typically executes its instructions with a 10μs instruction cycle time. The μPD556B is manufactured with a standard PMOS process, allowing use of a single -10V power supply, and is available in a 64-pin quad-in-line ceramic package.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
I_{0-7}	Instruction Input
PC_{0-10}	Program Counter Output
A_{CC}/PC	Accumulator/Program Counter Select
BREAK	Break Input
STEP	Single Step Input
CL_0-CL_1	External Clock Source
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

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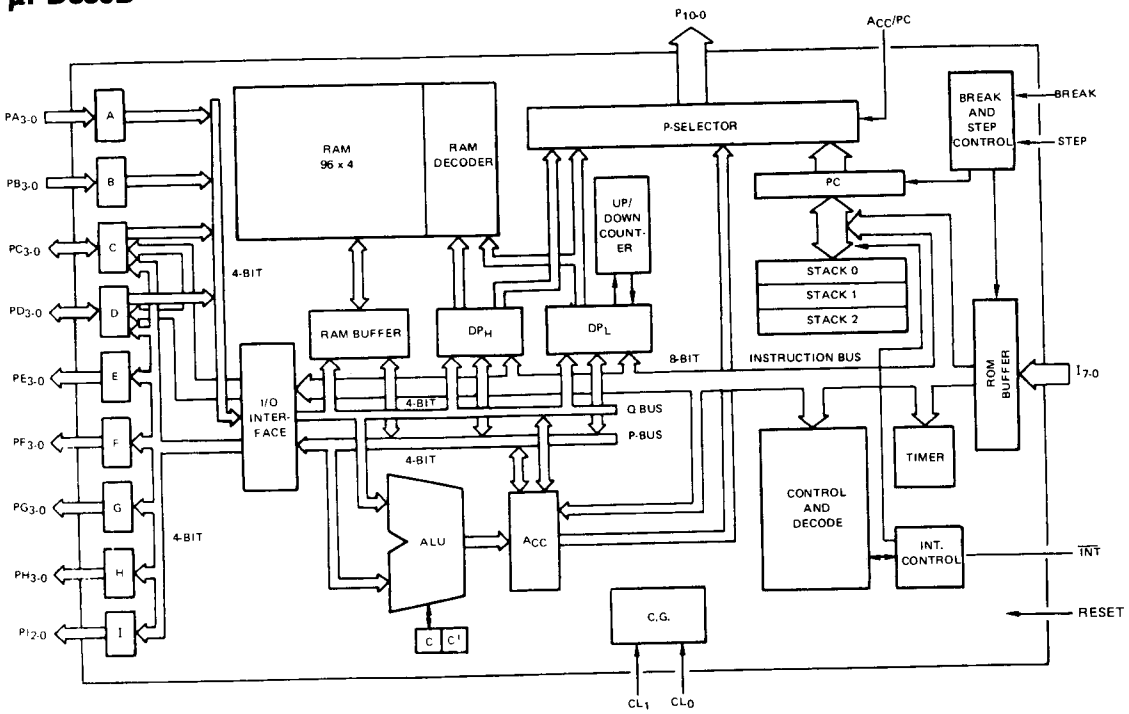
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage, V_{GG}	-15V to +0.3V
All Input Voltages	-15V to +0.3V
All Output Voltages	-15V to +0.3V
Output Current (total, all ports)	-4 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−2.0	V	Ports A to D, I_{7-0} BREAK, STEP, $\overline{INT}$, RESET, and A_{CC}/PC
Input Low Voltage	V_{IL}	−4.3		V_{GG}	V	Ports A to D, I_{7-0} BREAK, STEP, $\overline{INT}$, RESET, and A_{CC}/PC
Clock High Voltage	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Low Voltage	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, I_{7-0} $\overline{INT}$, RESET, BREAK, STEP, A_{CC}/PC, V_I = −1V
				+10	μA	Ports C and D, V_I = −1V
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A and B, I_{7-0} $\overline{INT}$, RESET, BREAK, STEP, A_{CC}/PC, V_I = −11V
				−10	μA	Ports C and D, V_I = −11V
Clock Input Leakage High	$I_{L\phi H}$			+200	μA	CL_0 Input, External Clock, $V_{\phi H}$ = 0V
Clock Input Leakage Low	$I_{L\phi L}$			−200	μA	CL_0 Input, External Clock, $V_{\phi L}$ = −11V
Output High Voltage	V_{OH1}			−1.0	V	Ports C to I, P_{10-0} I_{OH} = −1.0 mA
	V_{OH2}			−2.3	V	Ports C to I, P_{10-0} I_{OH} = −3.3 mA
Output Leakage Current Low	I_{LOL}			−30	μA	Ports C to I, P_{10-0} V_O = −11V
Supply Current	I_{GG}		−30	−50	mA	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%

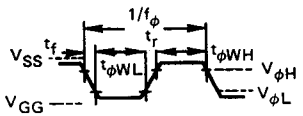
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Frequency	f_ϕ	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t_{\phi WH}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi WL}$	0.5		5.6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	200			μs	f = 400 KHz, "1" Written
STEP to RUN Interval	t_{SB}	200			μs	f = 400 KHz, "1" Written
STEP Pulse Width	t_{WS}	30			μs	f = 400 KHz, "1" Written
BREAK to A_{CC} Interval	t_{BA}	200			μs	f = 400 KHz, "1" Written
A_{CC}/PC Pulse Width	t_{WA}	30			μs	f = 400 KHz, "1" Written
STEP to A_{CC} Interval	t_{SA1}	200			μs	f = 400 KHz, "1" Written
PC to STEP Overlap	t_{SA2}			5	μs	f = 400 KHz, "1" Written
PC to RUN Interval	t_{AB}	0			μs	f = 400 KHz, "1" Written
A_{CC}/PC - P_{10-0} Delay	t_{DAP1}			15	μs	f = 400 KHz, "1" Written
	t_{DAP2}			15	μs	f = 400 KHz, "1" Written

CAPACITANCE

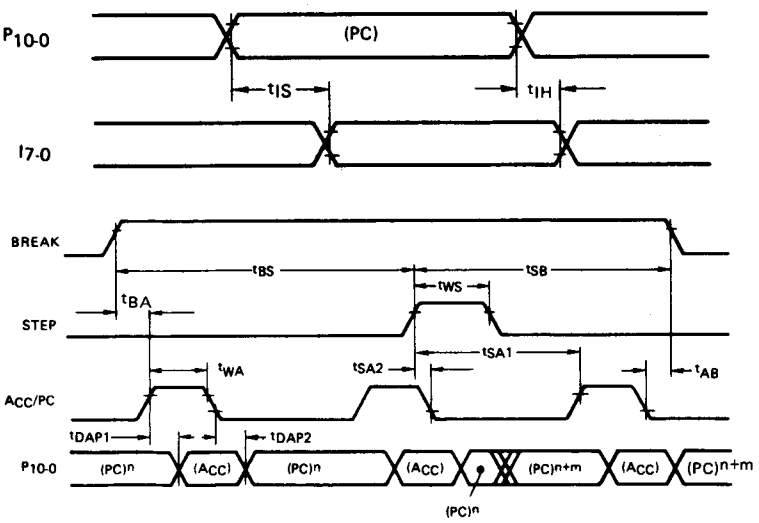
T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

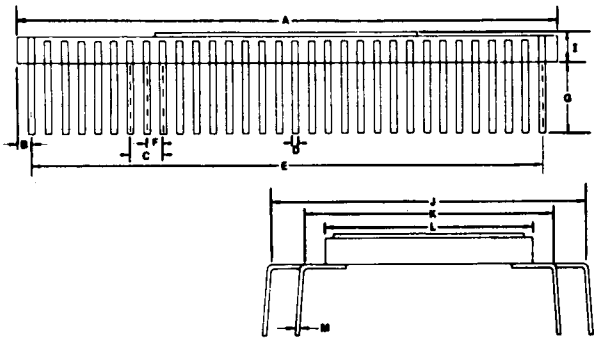
CLOCK WAVEFORM



TIMING WAVEFORMS



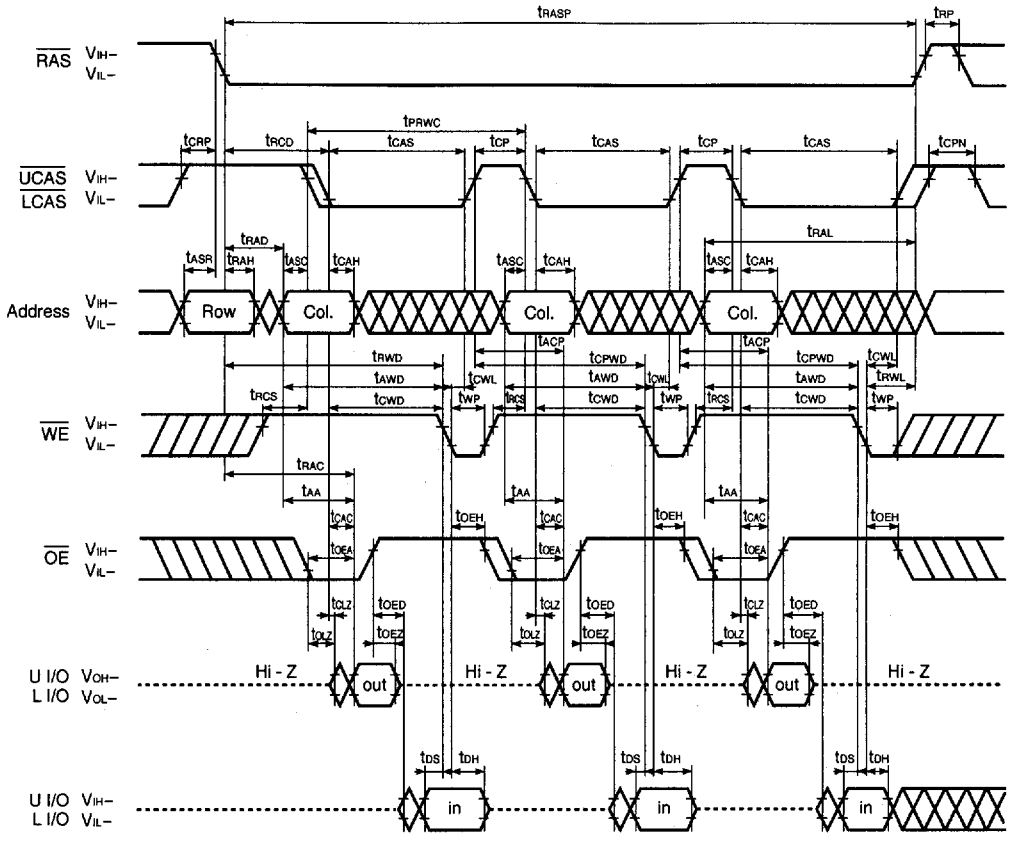
PACKAGE OUTLINE μPD556B



CERAMIC

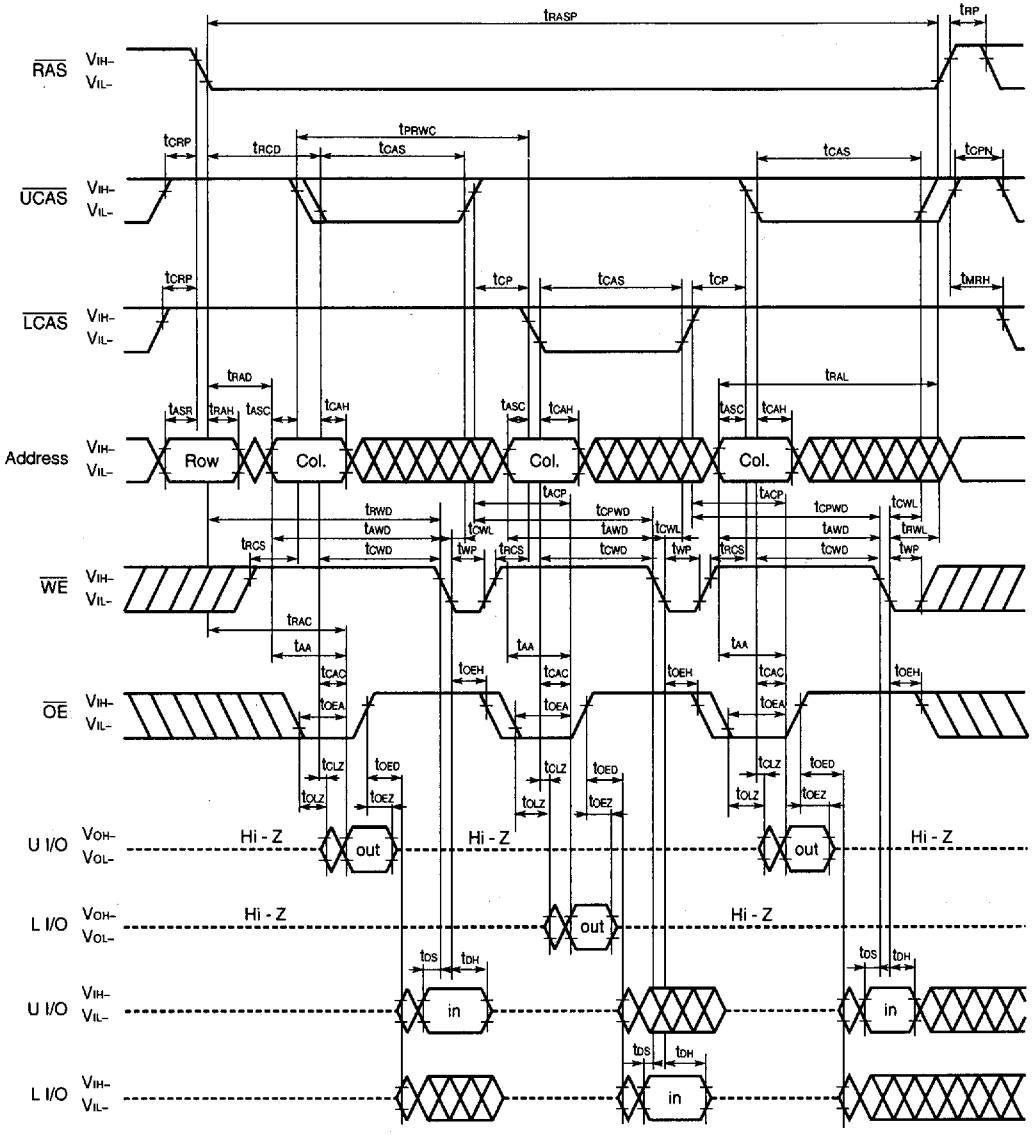
ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

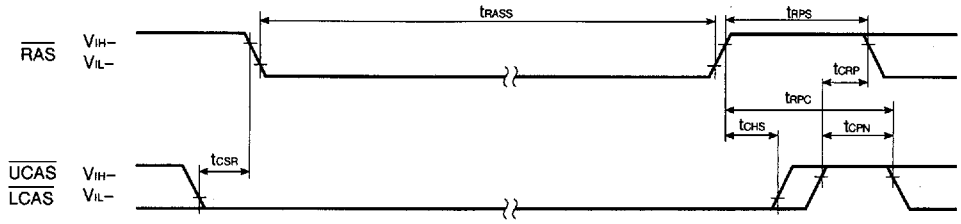
Fast Page Mode Byte Read Modify Write Cycle



Remarks 1. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18160)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

μPD42S18160: 1,024 times within a 16 ms interval

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh as follows just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

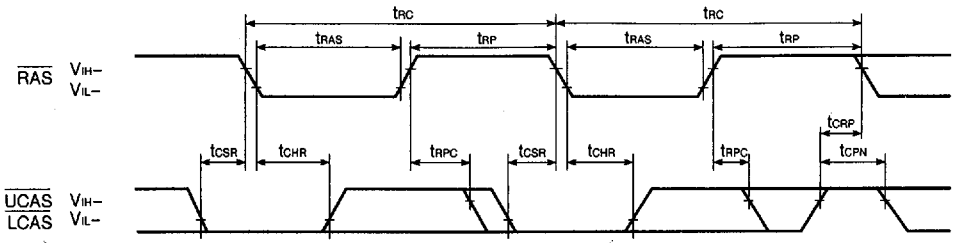
μPD42S18160: 1,024 times within a 16 ms interval

(3) If $t_{RASS\ (MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100\ \mu s$), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If $10\ \mu s < t_{RAS} < 100\ \mu s$, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh (t_{RPS}) is applied.
And refresh cycles as follows should be met.

μPD42S18160: 1,024 times within a 128 ms interval

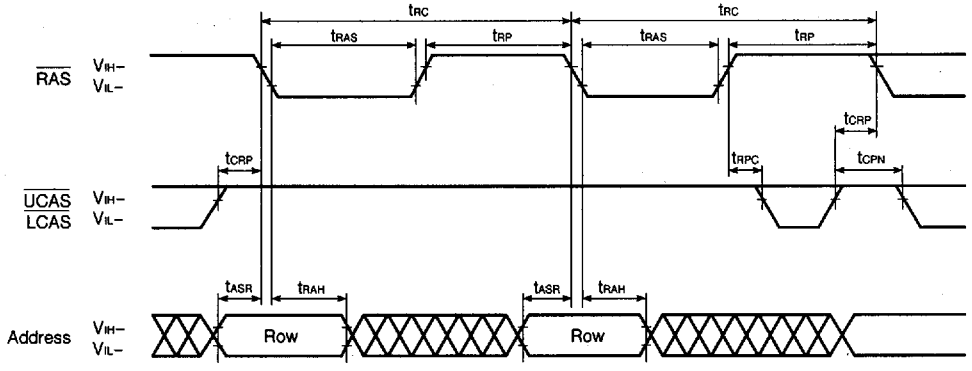
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle



Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

Hidden Refresh Cycle (Read)