NEC
μPD447
μPD447-1
μPD447-2
PRELIMINARY

2048 x 8 BIT STATIC CMOS RAM

DESCRIPTION

The μPD447 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD447 a very low operating power device which requires no clock or refreshing to operate.

Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE2}$ equals V_{CC} independently of the other input levels.

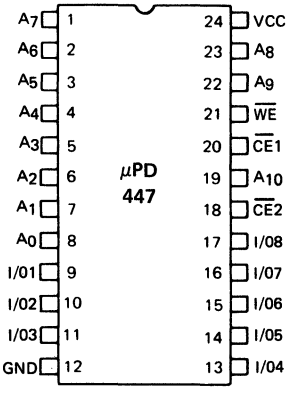
Data Retention is guaranteed at a power supply voltage as low as 2V.

The μPD447 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

FEATURES

- Single +5V Supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Inputs and Outputs
- Common Data Input and Output Using Three-State Output
- Two Chip Enable Inputs for Battery Operation
- Max Access/Min Cycle Times Down to 120 ns
- Low Power Dissipation; 45 mA Max Active/100 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage – 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs

PIN CONFIGURATION



PIN NAMES

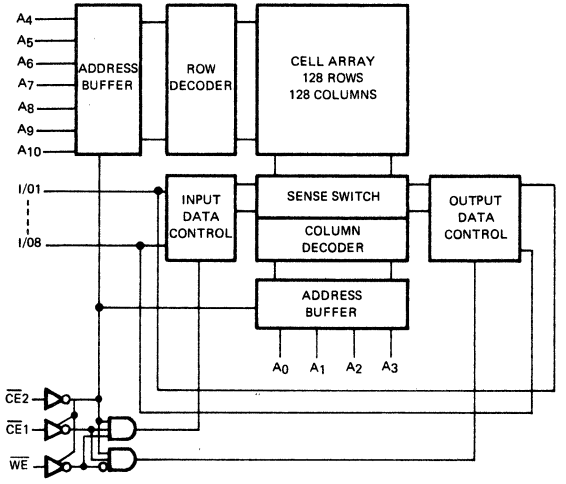
A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE1}$-$\overline{CE2}$	Chip Enable Inputs
I/01-I/08	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	MODE	I/O	ICC
X	H	X	NOT SELECTED	HZ	STANDBY
H	X	X	NOT SELECTED	HZ	ACTIVE
L	L	L	WRITE	D_{IN}	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE

μPD447

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . . -0.3 to VCC + 0.3V
Storage Temperature Range . . . . . -55°C to 125°C
Operating Temperature Range . . . . . 0°C to 70°C

COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS μPD447-2 MIN	μPD447-2 TYP	μPD447-2 MAX	μPD447-1 MIN	μPD447-1 TYP	μPD447-1 MAX	μPD447 MIN	μPD447 TYP	μPD447 MAX	UNIT
Input High Voltage	V_{IH}		2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	-0.3		0.8	-0.3		0.8	V
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA
I/O Leakage Current	I_{LO}	$V_{\overline{CE}2}$ = V_{IH} $V_{I/O}$ = 0 ~ V_{CC}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA
Operating Supply Current	I_{CCA1}	$V_{\overline{CE}2}$ = V_{IL} $I_{I/O}$ = 0 MIN TCYCLE		30	45		25	39		20	30	mA
	I_{CCA2}	$V_{\overline{CE}2}$ = V_{IL} $I_{I/O}$ = 0 DC CURRENT		5	10		5	10		5	10	mA
Standby Current	I_{CCS}	$V_{\overline{CE}2}$ = V_{CC} V_{IN} = 0 ~ V_{CC}			100			100			100	μA
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			2.4			2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.4			0.4			0.4	V

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS μPD447-2 MIN	LIMITS μPD447-2 MAX	LIMITS μPD447-1 MIN	LIMITS μPD447-1 MAX	LIMITS μPD447 MIN	LIMITS μPD447 MAX	UNIT
Read Cycle Time	t_{RC}	120		150		200		ns
Access Time	t_A		120		150		200	ns
Chip Enable (CE1) to Output Valid	t_{CO1}		60		75		100	ns
Chip Enable (CE2) to Output Valid	t_{CO2}		120		150		200	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Enable (CE1) to Output in LZ	t_{LZ1}	10		10		10		ns
Chip Enable (CE2) to Output in LZ	t_{LZ2}	10		10		10		ns
Chip Enable (CE1) to Output in HZ	t_{HZ1}		60		75		100	ns
Chip Enable (CE2) to Output in HZ	t_{HZ2}		60		75		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS μPD447-2 MIN	LIMITS μPD447-2 MAX	LIMITS μPD447-1 MIN	LIMITS μPD447-1 MAX	LIMITS μPD447 MIN	LIMITS μPD447 MAX	UNIT
Write Cycle Time	t_{WC}	120		150		200		ns
Chip Enable (CE1) to End of Write	t_{CW1}	100		125		170		ns
Chip Enable (CE2) to End of Write	t_{CW2}	100		125		170		ns
Address Setup Time	t_{AW}	0		0		0		ns
Write Pulsewidth	t_{WP}	100		125		170		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write Enable to Output in HZ	t_{WZ}		60		75		100	ns
Output Active from End of Write	t_{OW}	20		20		20		ns
Data Valid to End of Write	t_{DW}	60		75		100		ns
Data Hold Time	t_{DH}	0		0		0		ns

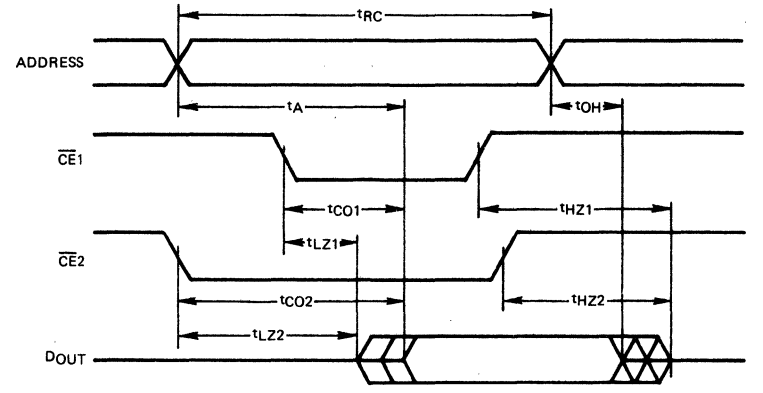
LOW VCC DATA RETENTION

T_a = 0°C to 70°C

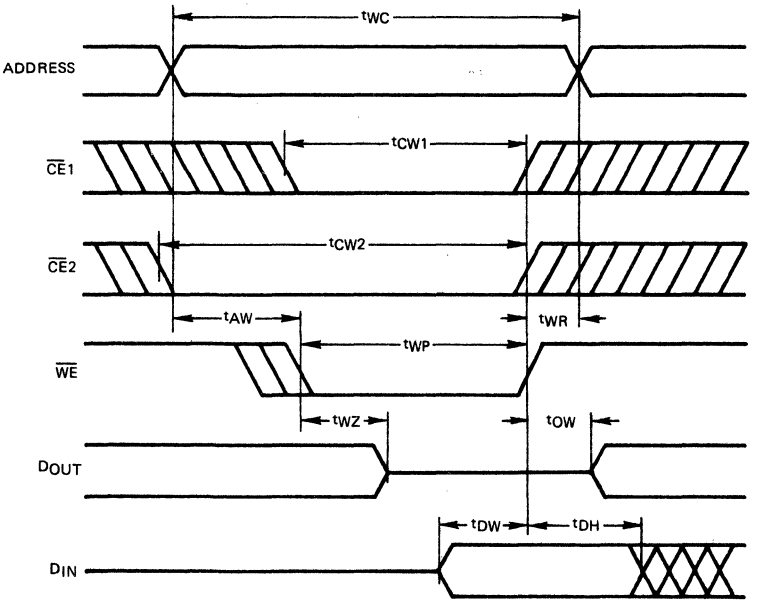
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{CC} for Data Retention	V_{CCDR}	V_{IN} = 0 ~ V_{CC}, $V_{\overline{CE2}}$ = V_{CC}	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, V_{IN} = 0 ~ V_{CC} $V_{\overline{CE2}}$ = V_{CC}		0.1	10	μA
Chip Disable to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

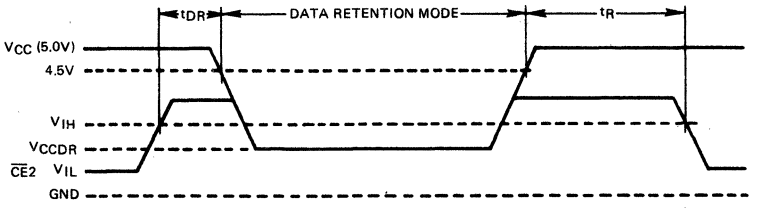
TIMING WAVEFORMS

READ CYCLE TIMING CHART



WRITE CYCLE TIMING CHART



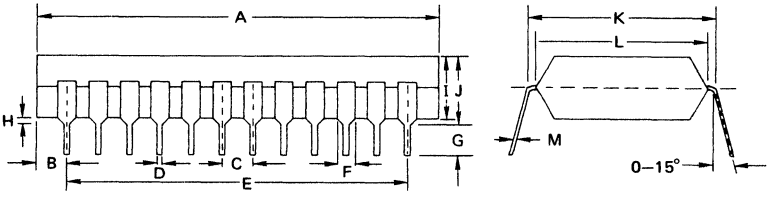


LOW VCC
DATA RETENTION
TIMING CHART

AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF

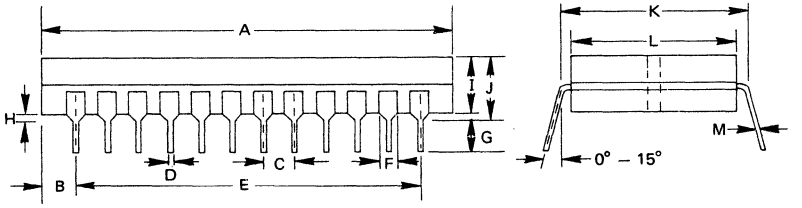
PACKAGE OUTLINE μPD447C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD447D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$