

## Description

The  $\mu$ PD4361B is a 65,536-word by 1-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the  $\mu$ PD4361B a high-speed device that requires very low power and no clock or refreshing.

The device is packaged in a 22-pin plastic DIP and 24-pin plastic SOJ and has two types of access times, address and chip select.

## Features

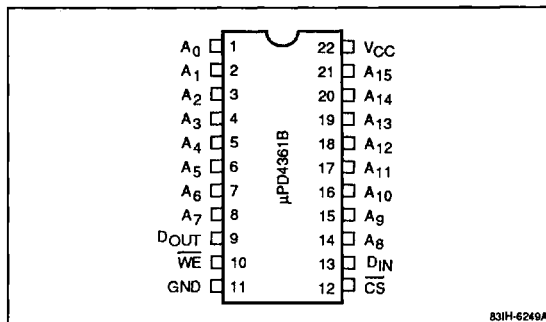
- 65,536 x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Standard 22-pin plastic DIP and 24-pin plastic SOJ

## Ordering Information

| Part Number        | Access Time (max) | Package            |
|--------------------|-------------------|--------------------|
| $\mu$ PD4361BCR-12 | 12 ns             | 22-pin plastic DIP |
| CR-15              | 15 ns             |                    |
| CR-20              | 20 ns             |                    |
| $\mu$ PD4361BLA-12 | 12 ns             | 24-pin plastic SOJ |
| LA-15              | 15 ns             |                    |
| LA-20              | 20 ns             |                    |

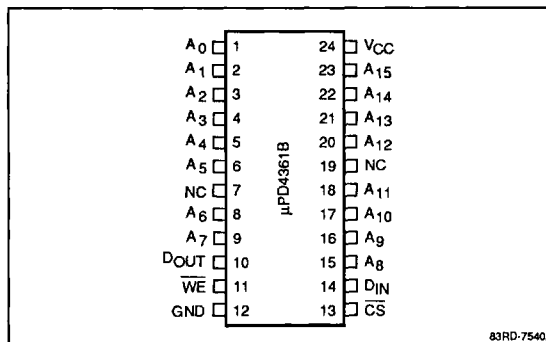
## Pin Configurations

### 22-Pin Plastic DIP



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### 24-Pin Plastic SOJ



## Pin Identification

| Symbol                           | Function             |
|----------------------------------|----------------------|
| A <sub>0</sub> - A <sub>15</sub> | Address inputs       |
| D <sub>IN</sub>                  | Data input           |
| D <sub>OUT</sub>                 | Data output          |
| CS                               | Chip select          |
| WE                               | Write enable         |
| GND                              | Ground               |
| V <sub>CC</sub>                  | +5-volt power supply |

### Absolute Maximum Ratings

|                                                 |                          |
|-------------------------------------------------|--------------------------|
| Supply voltage, $V_{CC}$                        | -0.5 to +7.0 V           |
| Input voltage output voltage, $V_{IN}$ (Note 1) | -0.5 to $V_{CC}$ + 0.5 V |
| Operating temperature, $T_{OPR}$                | 0 to +70°C               |
| Storage temperature, $T_{STG}$                  | -55 to +125°C            |
| Power dissipation, $P_D$                        | 1.0 W                    |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

#### Notes:

(1)  $V_{IN}$  = -3.0 V minimum for 10 ns maximum pulse.

### Truth Table

| Function     | $\overline{CS}$ | $\overline{WE}$ | Input/Output | $I_{CC}$ |
|--------------|-----------------|-----------------|--------------|----------|
| Not selected | H               | X               | High-Z       | Standby  |
| Read         | L               | H               | $D_{OUT}$    | Active   |
| Write        | L               | L               | High-Z       | Active   |

### Recommended Operating Conditions

| Parameter             | Symbol   | Min  | Typ | Max            | Unit |
|-----------------------|----------|------|-----|----------------|------|
| Supply voltage        | $V_{CC}$ | 4.5  | 5.0 | 5.5            | V    |
| Input voltage, high   | $V_{IH}$ | 2.2  |     | $V_{CC} + 0.3$ | V    |
| Input voltage, low    | $V_{IL}$ | -0.5 |     | 0.8            | V    |
| Operating temperature | $T_A$    | 0    |     | 70             | °C   |

#### Notes:

(1)  $V_{IL}$  = -3.0 V minimum for 10 ns maximum pulse.

### Capacitance

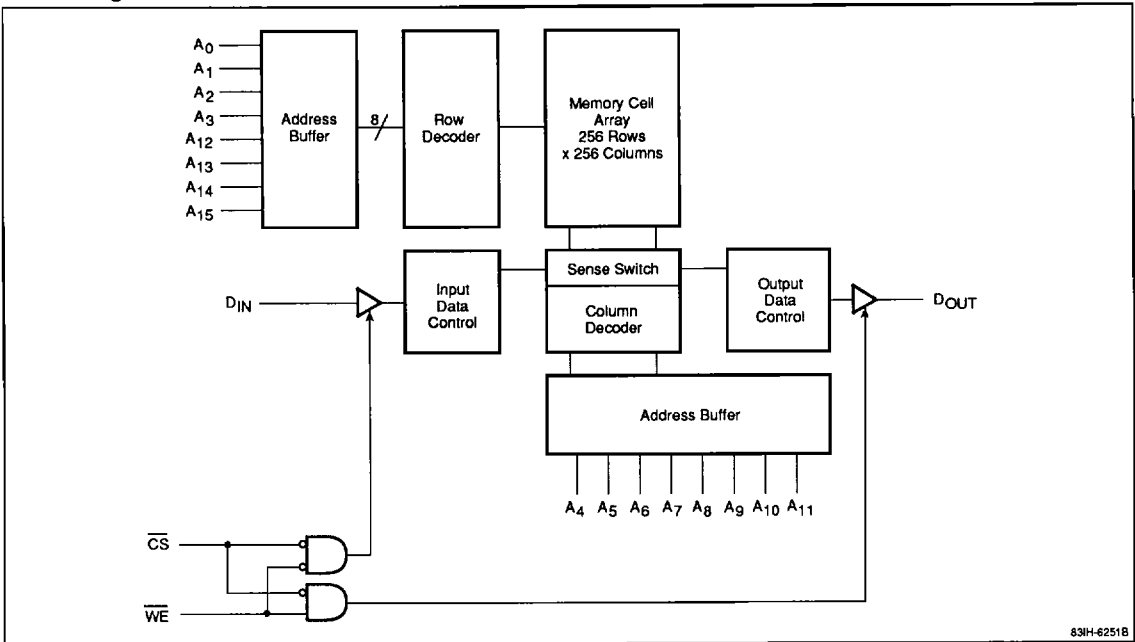
$T_A$  = 25°C;  $f$  = 1 MHz;  $V_{IN}$  and  $V_{OUT}$  = 0 V (Note 1)

| Parameter          | Symbol     | Min | Typ | Max | Unit |
|--------------------|------------|-----|-----|-----|------|
| Input capacitance  | $C_{IN}$   |     |     | 6   | pF   |
| Output capacitance | $C_{DOUT}$ |     |     | 8   | pF   |

#### Notes:

(1) This parameter is sampled and not 100% tested.

### Block Diagram



63H-6251B

### DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$ ;  $V_{CC} = +5.0 \text{ V} \pm 10\%$

| Parameter              | Symbol    | Min | Typ | Max | Unit | Test Conditions                                                                                            |
|------------------------|-----------|-----|-----|-----|------|------------------------------------------------------------------------------------------------------------|
| Input leakage current  | $I_{LI}$  | -2  |     | 2   | μA   | $V_{IN} = 0 \text{ V to } V_{CC}$                                                                          |
| Output leakage current | $I_{LO}$  | -2  |     | 2   | μA   | $V_{OUT} = 0 \text{ V to } V_{CC}$ ; $\overline{CS} = V_{IH}$                                              |
| Standby supply current | $I_{SB}$  |     |     | 20  | mA   | $\overline{CS} = V_{IH}$                                                                                   |
|                        | $I_{SB1}$ |     |     | 2   | mA   | $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ ; $V_{IN} \leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$ |
| Output voltage, low    | $V_{OL}$  |     |     | 0.4 | V    | $I_{OL} = 8.0 \text{ mA}$                                                                                  |
| Output voltage, high   | $V_{OH}$  | 2.4 |     |     | V    | $I_{OH} = -4.0 \text{ mA}$                                                                                 |

### AC Characteristics

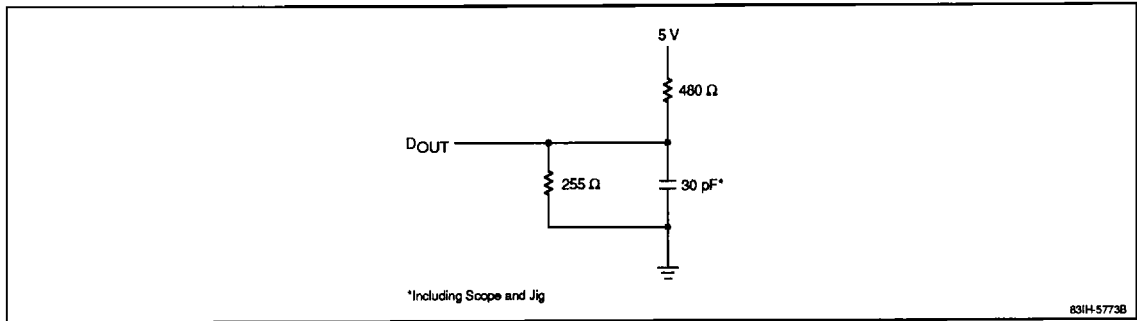
$T_A = 0 \text{ to } +70^\circ\text{C}$ ;  $V_{CC} = +5.0 \text{ V} \pm 10\%$

| Parameter                         | Symbol           | μPD4361B-12 |     | μPD4361B-15 |     | μPD4361B-20 |     | Unit | Test Conditions                                   |
|-----------------------------------|------------------|-------------|-----|-------------|-----|-------------|-----|------|---------------------------------------------------|
|                                   |                  | Min         | Max | Min         | Max | Min         | Max |      |                                                   |
| <b>Read Operation</b>             |                  |             |     |             |     |             |     |      |                                                   |
| Operating supply current          | I <sub>CC</sub>  |             | 130 |             | 120 |             | 110 | mA   | $\overline{CS} = V_{IL}; I_{DOUT} = 0 \text{ mA}$ |
| Read cycle time                   | t <sub>RC</sub>  | 12          |     | 15          |     | 20          |     | ns   | (Note 2)                                          |
| Address access time               | t <sub>AA</sub>  |             | 12  |             | 15  |             | 20  | ns   |                                                   |
| Chip select access time           | t <sub>ACS</sub> |             | 12  |             | 15  |             | 20  | ns   |                                                   |
| Output hold from address change   | t <sub>OH</sub>  | 2           |     | 3           |     | 3           |     | ns   |                                                   |
| Chip select to output in low-Z    | t <sub>LZ</sub>  | 2           |     | 3           |     | 3           |     | ns   | (Note 3)                                          |
| Chip deselect to output in high-Z | t <sub>HZ</sub>  | 0           | 7   | 0           | 7   | 0           | 8   | ns   | (Note 4)                                          |
| Chip select to power-up time      | t <sub>PU</sub>  | 0           |     | 0           |     | 0           |     | ns   |                                                   |
| Chip deselect to power-down time  | t <sub>PD</sub>  | 0           | 7   | 0           | 8   | 0           | 15  | ns   |                                                   |
| <b>Write Operation</b>            |                  |             |     |             |     |             |     |      |                                                   |
| Write cycle time                  | t <sub>WC</sub>  | 12          |     | 15          |     | 20          |     | ns   | (Note 2)                                          |
| Chip select to end of write       | t <sub>CW</sub>  | 11          |     | 13          |     | 15          |     | ns   |                                                   |
| Address valid to end of write     | t <sub>AW</sub>  | 11          |     | 13          |     | 15          |     | ns   |                                                   |
| Address setup time                | t <sub>AS</sub>  | 0           |     | 0           |     | 0           |     | ns   |                                                   |
| Write pulse width                 | t <sub>WP</sub>  | 10          |     | 12          |     | 14          |     | ns   |                                                   |
| Write recovery time               | t <sub>WR</sub>  | 0           |     | 0           |     | 0           |     | ns   |                                                   |
| Data valid to end of write        | t <sub>DW</sub>  | 7           |     | 7           |     | 8           |     | ns   |                                                   |
| Data hold time                    | t <sub>DH</sub>  | 0           |     | 0           |     | 0           |     | ns   |                                                   |
| Write enable to output in high-Z  | t <sub>WZ</sub>  | 0           | 7   | 0           | 7   | 0           | 8   | ns   | (Note 4)                                          |
| Output active from end of write   | t <sub>OW</sub>  | 0           |     | 0           |     | 0           |     | ns   | (Note 3)                                          |

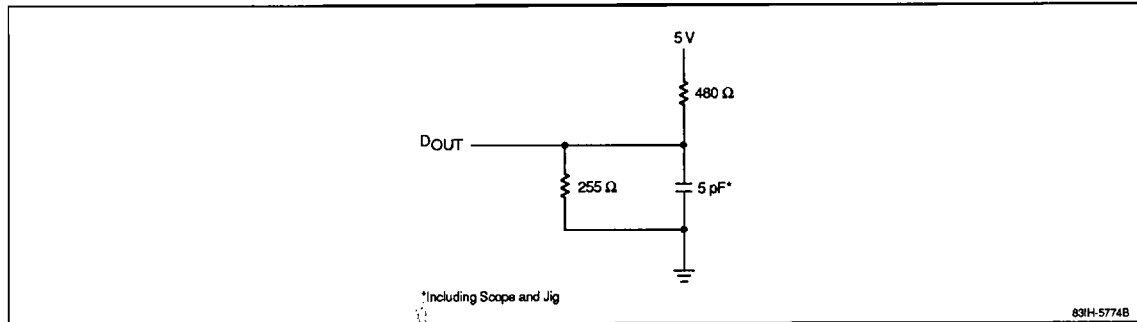
#### Notes:

- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.
- (2) All read cycle timings are referenced from the last valid address to the first transitioning address.
- (3) Transition is measured at  $\pm 200 \text{ mV}$  from steady-state voltage with the loading shown in figure 2.
- (4) Transition is measured at  $V_{OL} + 200 \text{ mV}$  and  $V_{OH} - 200 \text{ mV}$  with the loading shown in figure 2.

**Figure 1. Output Load**

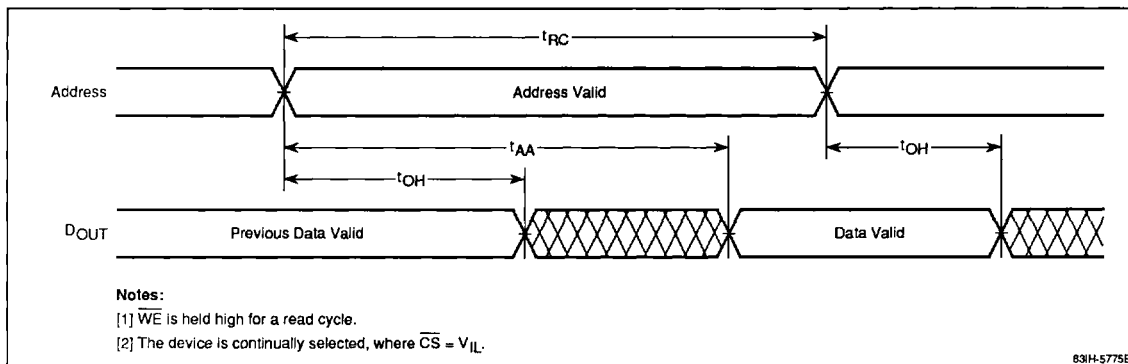


**Figure 2. Output Load for  $t_{HZ}$ ,  $t_{LZ}$ ,  $t_{WZ}$ , and  $t_{OW}$**



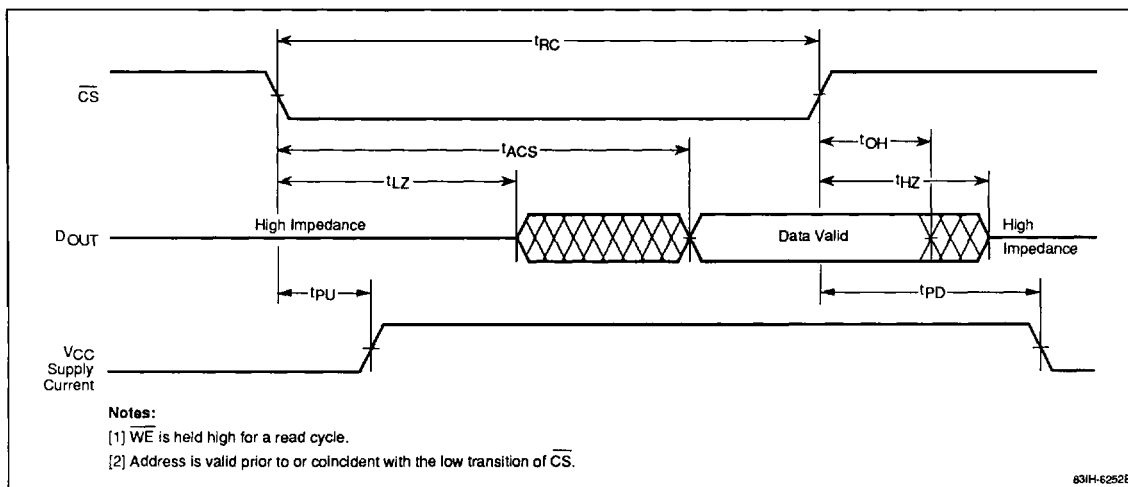
## Timing Waveforms

### Address Access Cycle



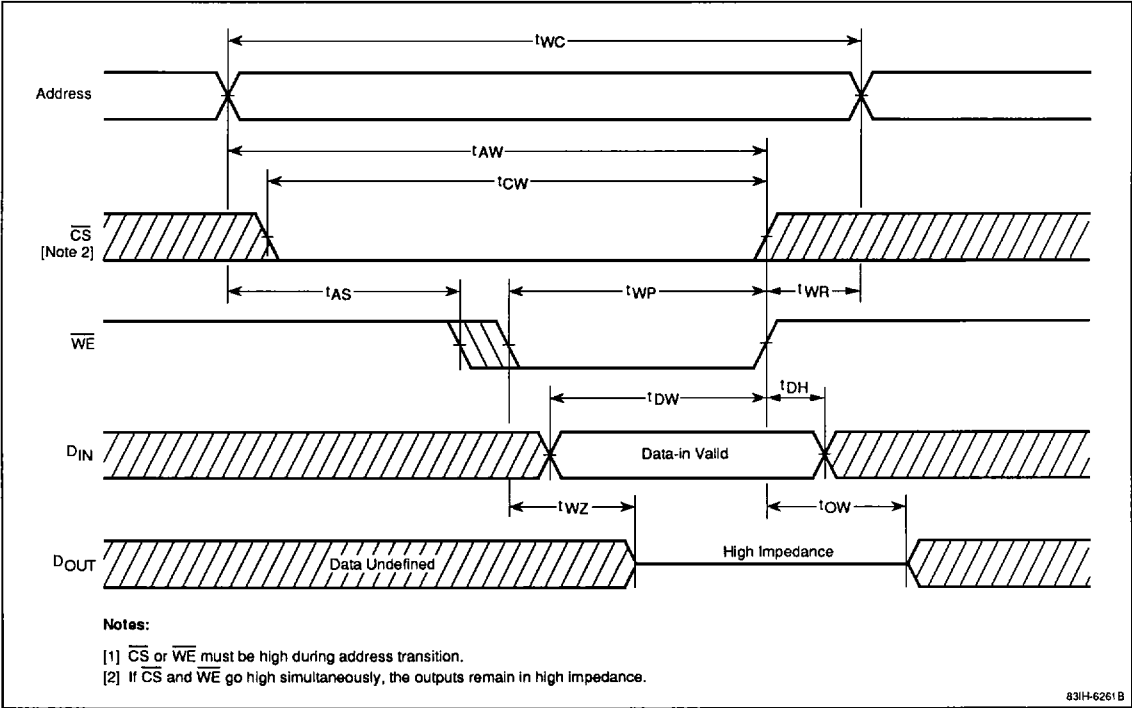
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### Chip Select Access Cycle



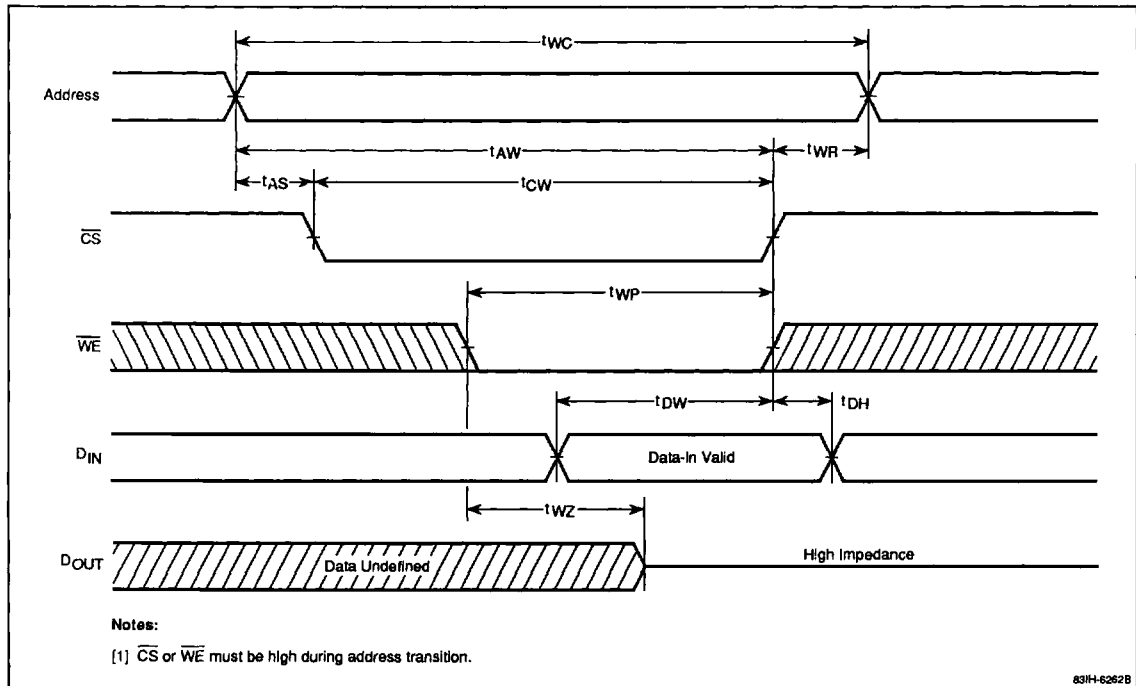
**Timing Waveforms (cont)**

***$\overline{WE}$ -Controlled Write Cycle***



## Timing Waveforms (cont)

### $\overline{CS}$ -Controlled Write Cycle



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