NEC Electronics Inc.

μPD424268
262,144 x 4-Bit Dynamic CMOS RAM

Description

The μPD424268 is a 262,144 by 4-bit dynamic RAM designed with a write-per-bit option to operate from a single + 5-volt power supply. Advanced polycide technology using trench capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CS}$ low. Data outputs return to high impedance when $\overline{CS}$ goes high. Static-column read and write cycles can be executed by switching the column address inputs.

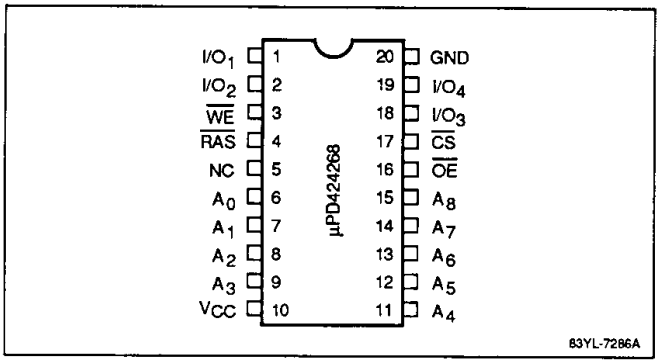
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms refresh period.

Features

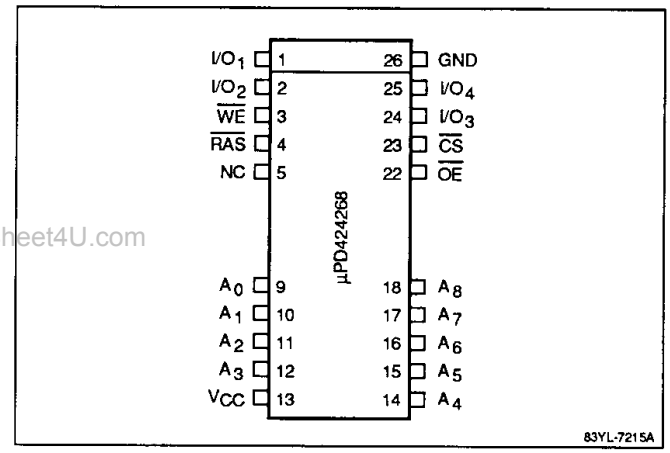
- 262,144 by 4-bit organization
- Single + 5-volt power supply
- Write-per-bit option
- Static-column option
- Low power dissipation
- $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Nonlatched, three-state outputs
- Low input capacitance
- 512 refresh cycles every 8 ms
- High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

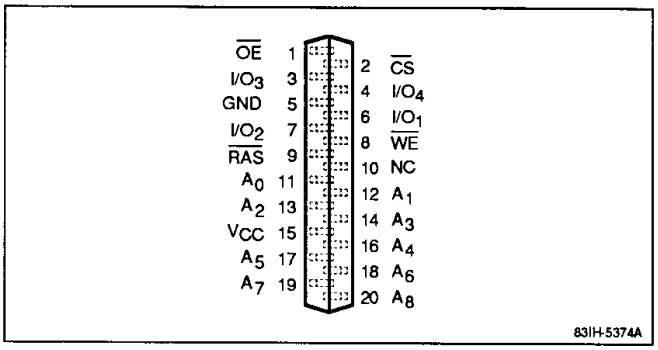
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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TSOP package will be available in 1991.

Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	I/O_1 – I/O_4

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Absolute Maximum Ratings

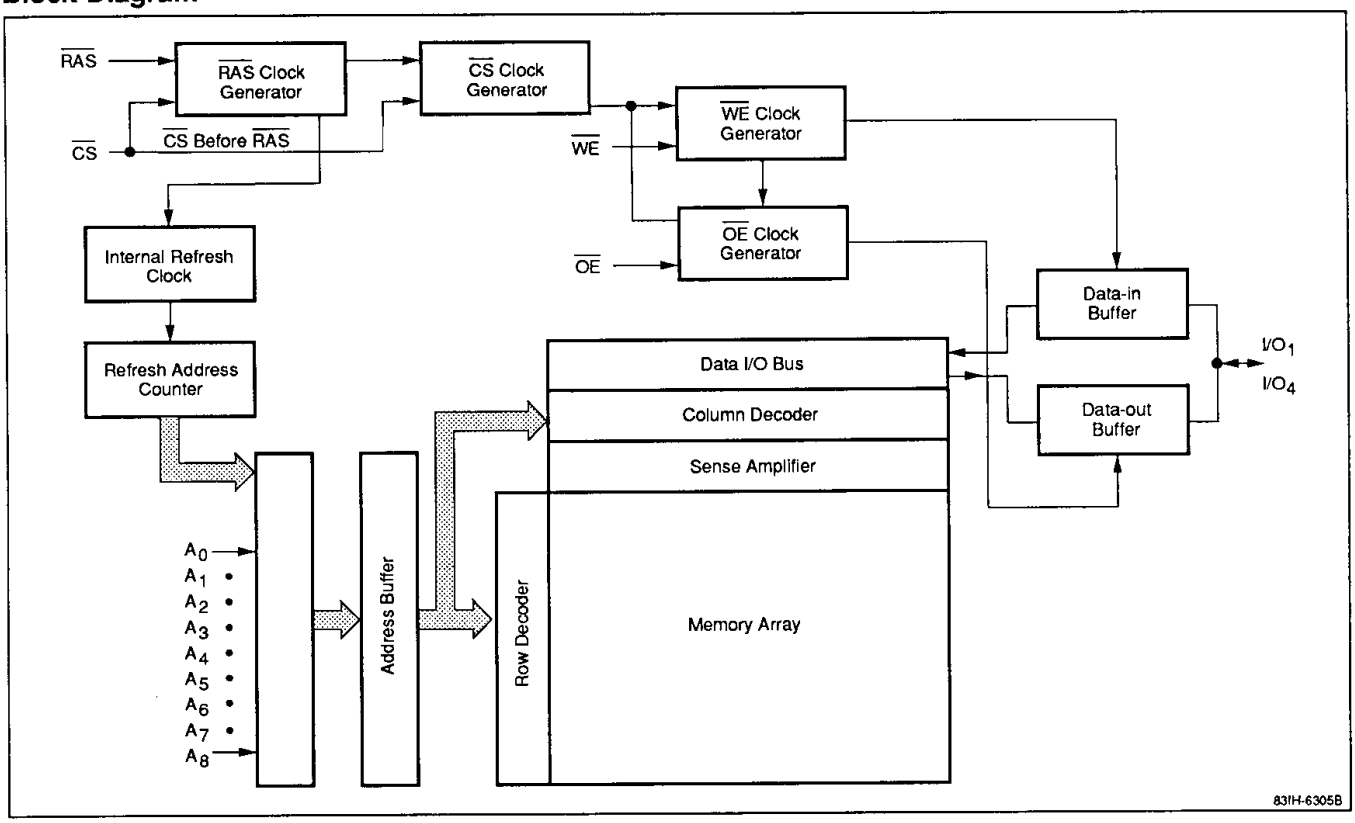
Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Static-Column Cycle (max)	Package
μPD424268C-60	60 ns	120 ns	35 ns	20-pin plastic DIP
C-70	70 ns	130 ns	40 ns	
C-80	80 ns	160 ns	45 ns	
C-10	100 ns	190 ns	55 ns	
μPD424268LA-60	60 ns	120 ns	35 ns	26/20-pin plastic SOJ
LA-70	70 ns	130 ns	40 ns	
LA-80	80 ns	160 ns	45 ns	
LA-10	100 ns	190 ns	55 ns	
μPD424268V-60	60 ns	120 ns	35 ns	20-pin plastic ZIP
V-70	70 ns	130 ns	40 ns	
V-80	80 ns	160 ns	45 ns	
V-10	100 ns	190 ns	55 ns	

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} \geq V_{IH}$ (min); I_O = 0 mA
				1.0	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2$ V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80		70		60	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80		70		60	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, static-column cycle, average	I_{CC4}		80		70		60		50	mA	$\overline{RAS} = \overline{CS} = V_{IL}$; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min (Note 5)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		90		80		70		60	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 10)
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	50		55		65		80		ns	(Note 17)
Access time from $\overline{CS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CS}$ precharge time	t_{CP}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 13)
$\overline{CS}$ pulse width	t_{CS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		45		55		ns	(Note 17)
Write command to $\overline{CS}$ lead time	t_{CWL}	15		15		20		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 16)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 16)
Access time from $\overline{OE}$	t_{OEA}		20		20		20		25	ns	(Note 7)
$\overline{OE}$ data delay time	t_{OED}	15		15		20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Output hold time from address	t_{OH}	5		5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		25		25		25	ns	(Note 7)
Access time from $\overline{WE}$	t_{PWA}		60		70		80		100	ns	(Notes 7, 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Column address hold time referenced to $\overline{WE}$	t_{PWH}	60		70		80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, static-column cycle	t_{RASC}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		0		ns	(Note 14)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		50		70		80		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 14)
Static-column read cycle time	t_{RSC}	35		40		45		55		ns	(Note 6)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	75		85		95		115		ns	
Read-write cycle time	t_{RWC}	165		175		215		255		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		90		105		130		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Static-column read-modify-write cycle time	t_{RWSC}	85		95		110		135		ns	(Note 6)
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
$\overline{WE}$ to column address delay time	t_{WAD}	20	30	22	35	25	40	25	50	ns	(Note 18)
Write-per-bit hold time	t_{WBH}	10		10		10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		0		0		ns	
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 17)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write-per-bit mask data hold time	t_{WH}	10		10		10		10		ns	
Write-per-bit mask data setup time	t_{WS}	0		0		0		0		ns	
Write invalid time	t_{WI}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 15)
Static-column write cycle time	t_{WSC}	35		40		45		55		ns	(Note 6)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each static-column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.4 V, V_{OL} = 0.4 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}, t_{AA}, or t_{OEA}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

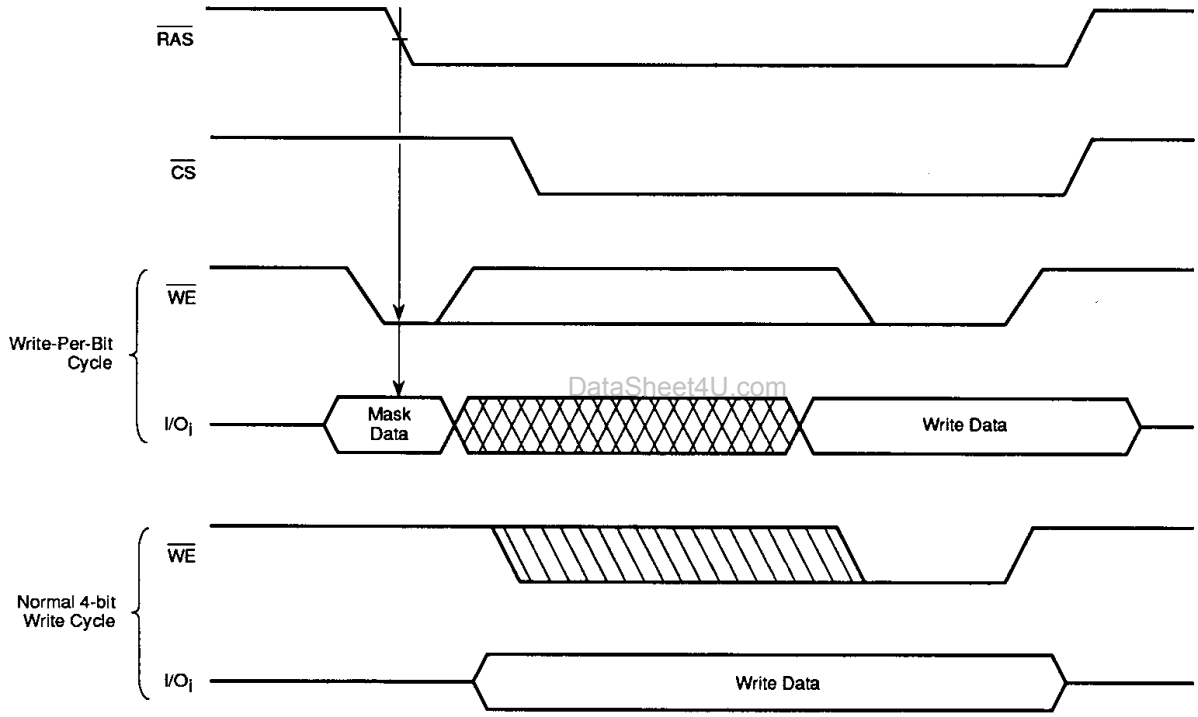
(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(18) If $t_{WAD} \leq t_{WAD}$ (max), then the access time is defined by t_{PWA}.

Write-Per-Bit Option

The write-per-bit option may be used to allow a write cycle to change any number of bits in the 4-bit word. The mask is loaded from the four I/O lines at the falling edge of $\overline{RAS}$ if $\overline{WE} = V_{IL}$. If the I/O line is high, then the corresponding bit will be written when the write cycle executes. If an I/O line is low, the corresponding bit does not change. A mask loaded during static-column operation will remain set and active for each write cycle that executes while $\overline{RAS}$ remains low. The mask may be changed at the falling edge of $\overline{RAS}$ only.

Comparison of Write-Per-Bit Cycle Versus Standard 4-Bit Write Cycle



I/O	Mask Data		Write Operation
I/O_1	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_2	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_3	1	(High)	Write Bit
	0	(Low)	Disable Bit Write
I/O_4	1	(High)	Write Bit
	0	(Low)	Disable Bit Write

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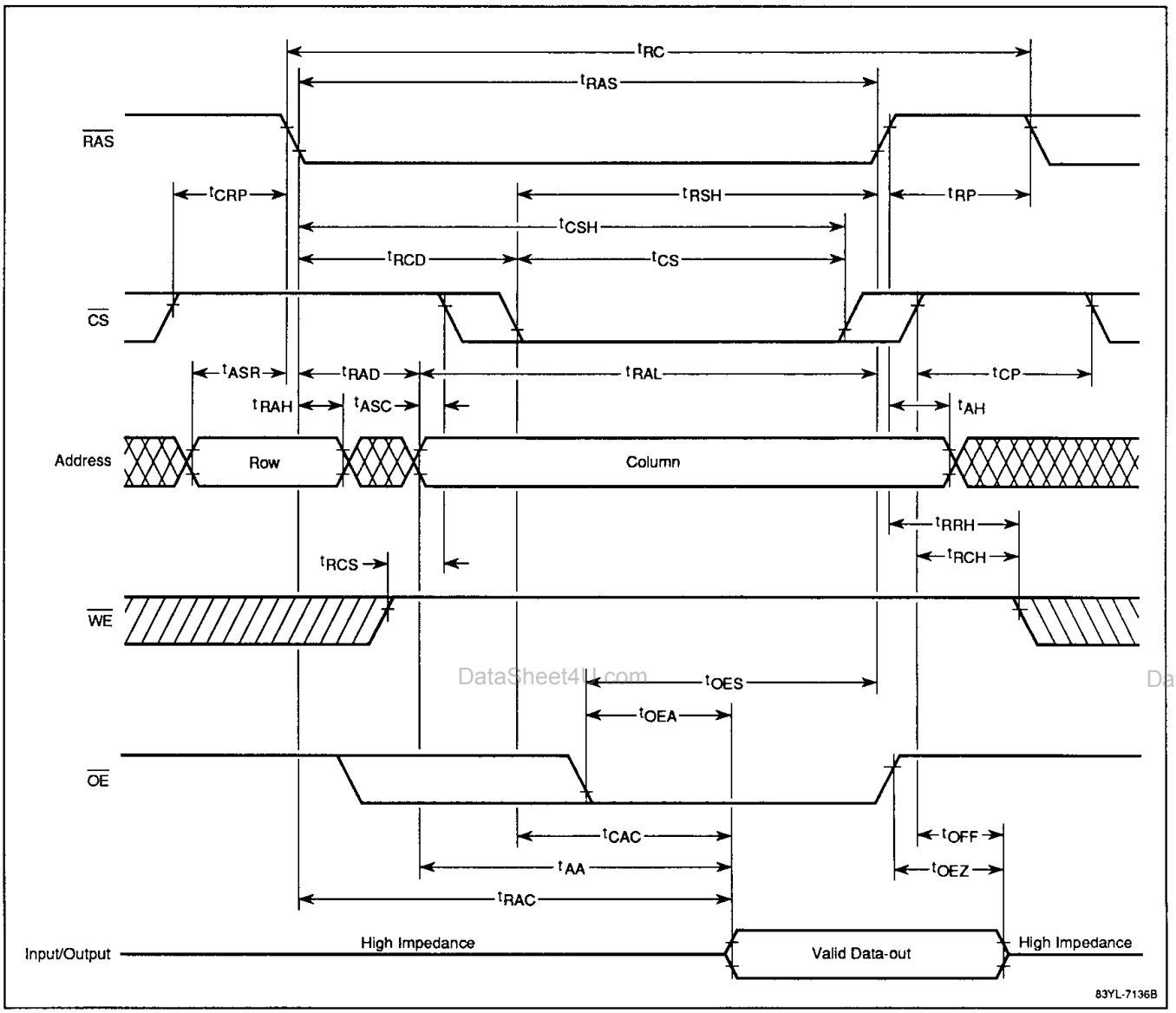
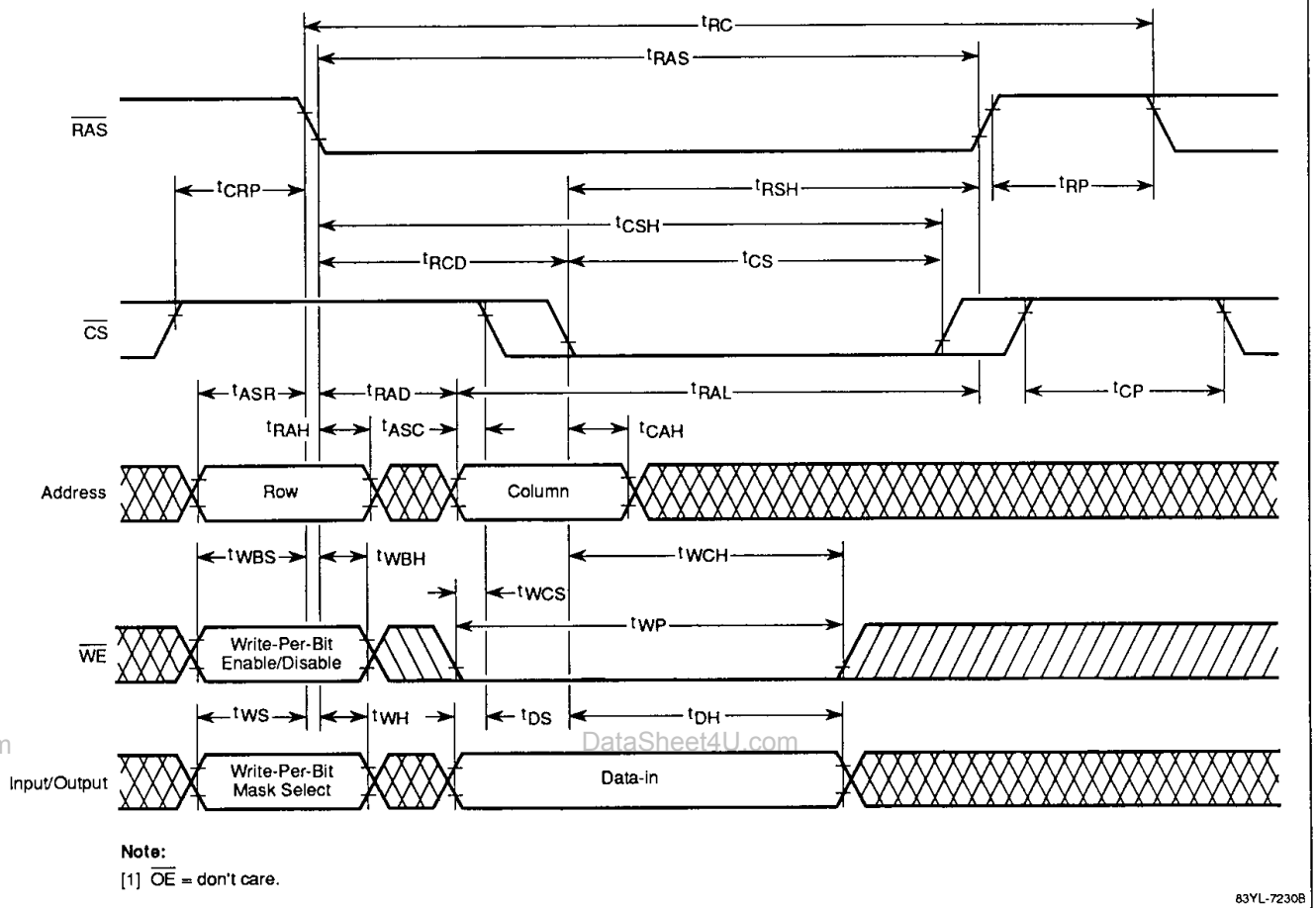
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



Note:

[1] $\overline{OE}$ = don't care.

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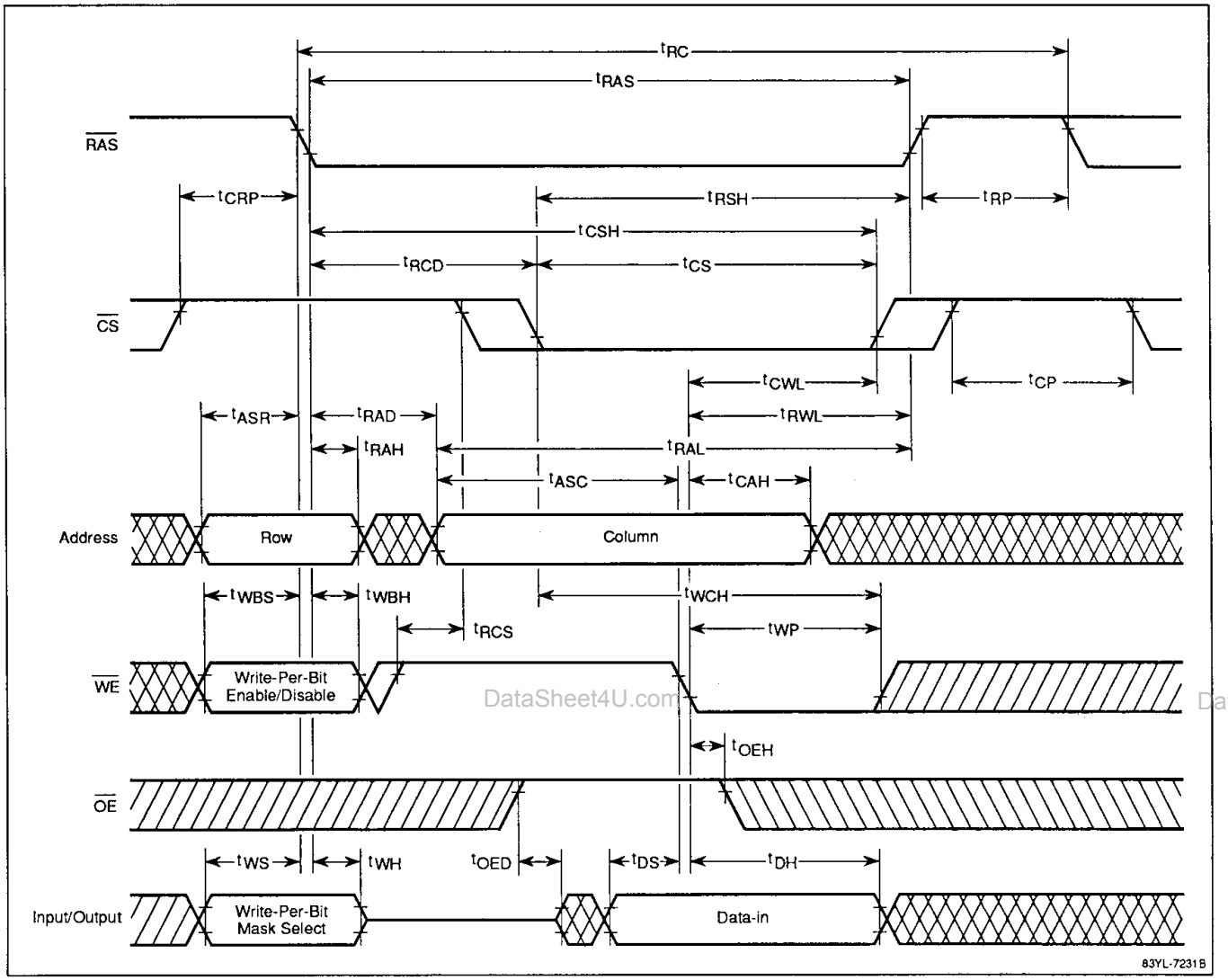
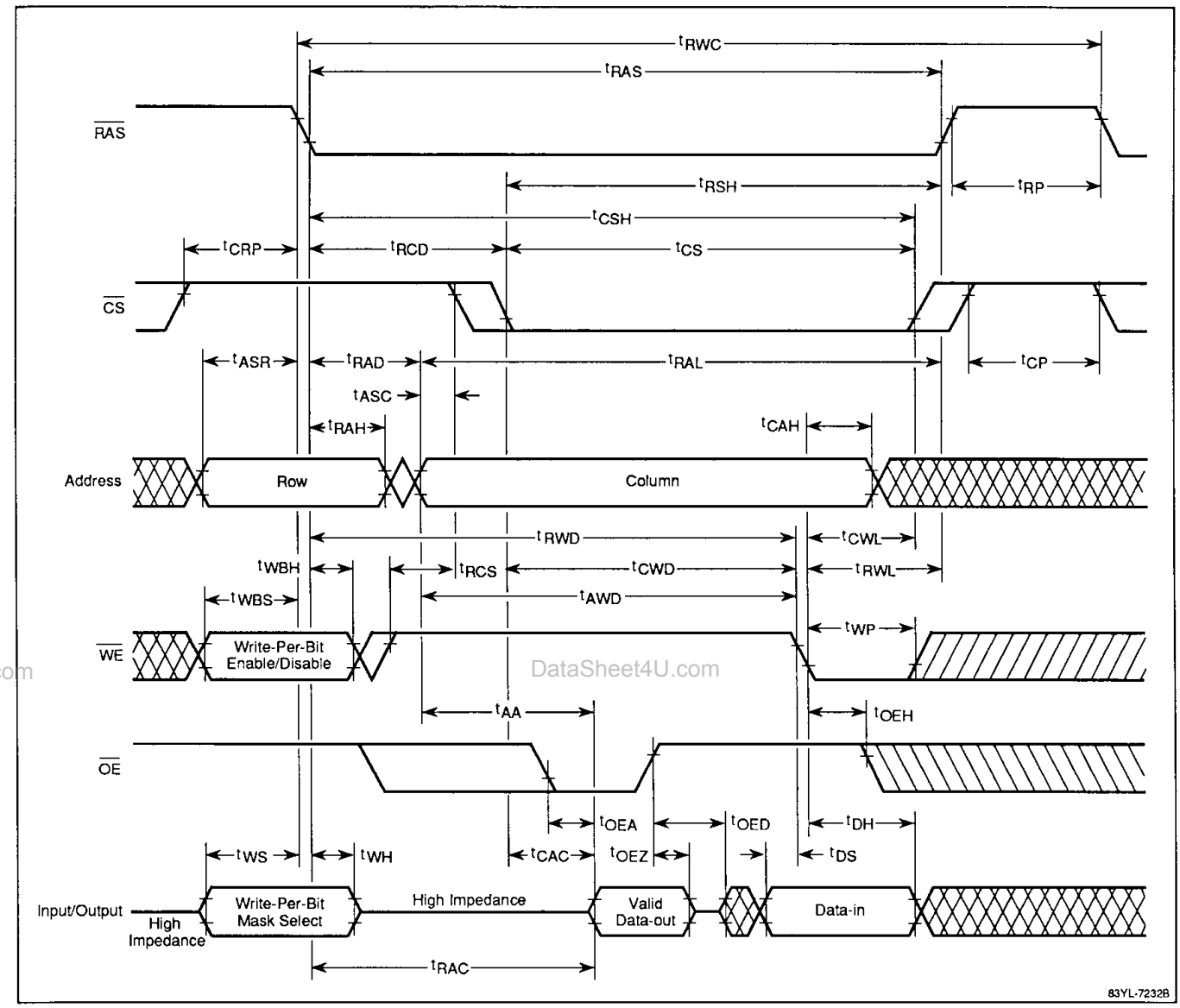
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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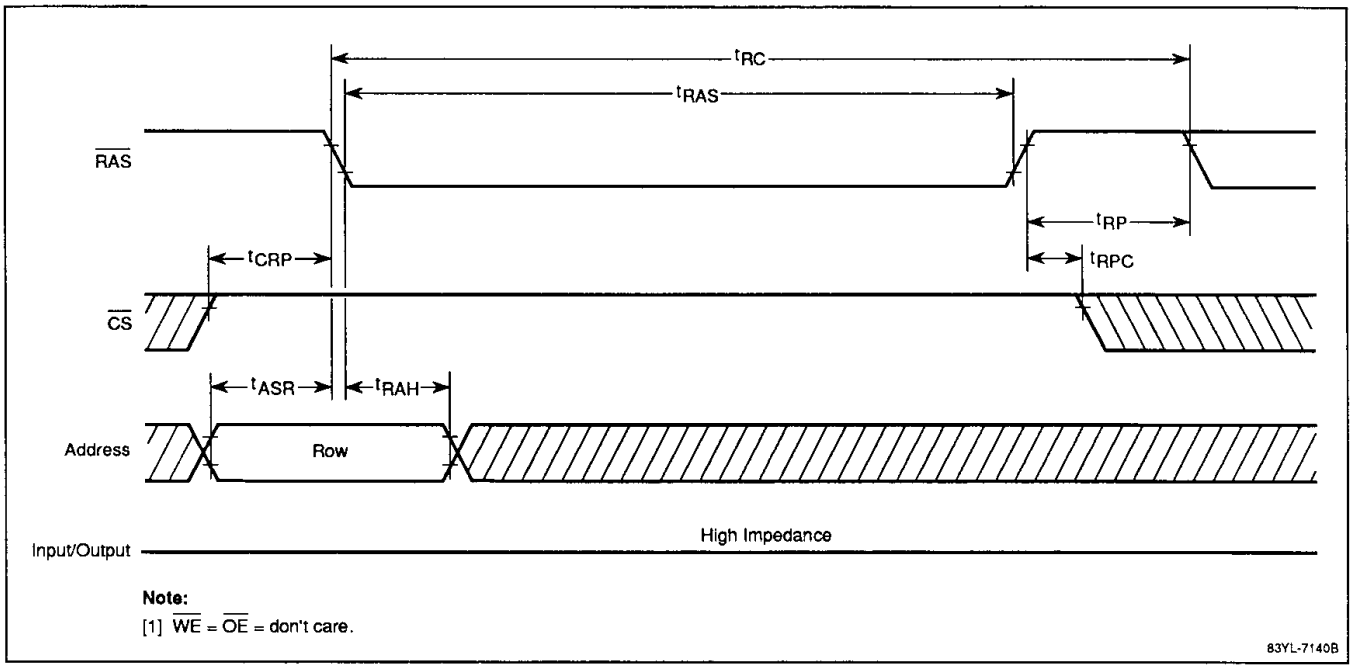
Timing Waveforms (cont)

RAS-Only Refresh Cycle



Note:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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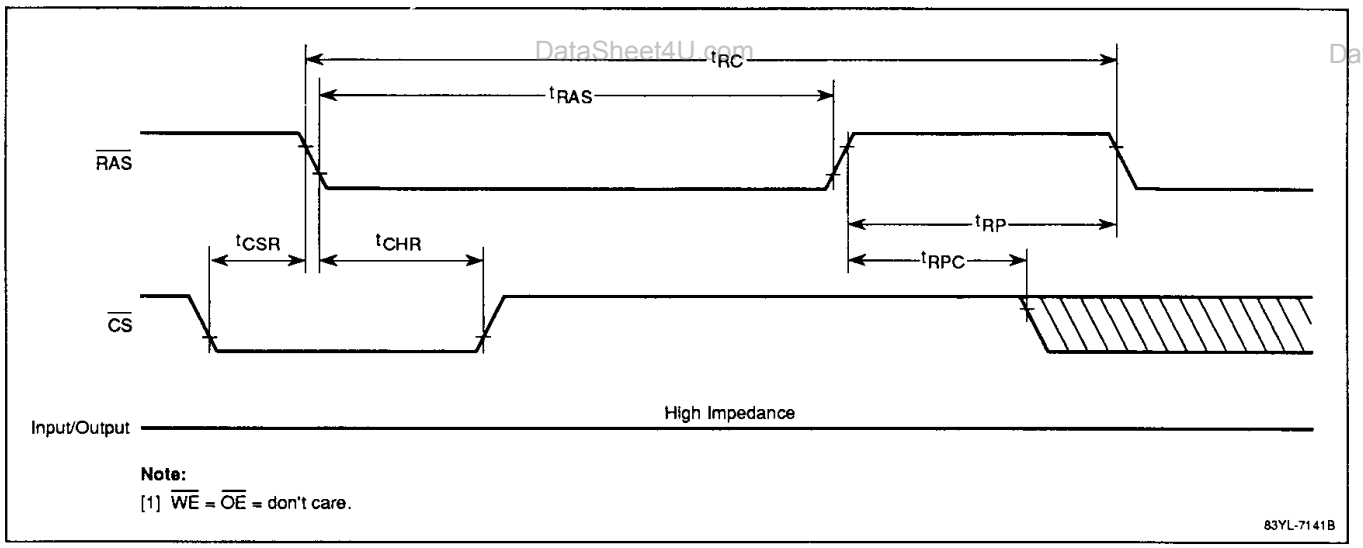
CS Before RAS Refresh Cycle



Note:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

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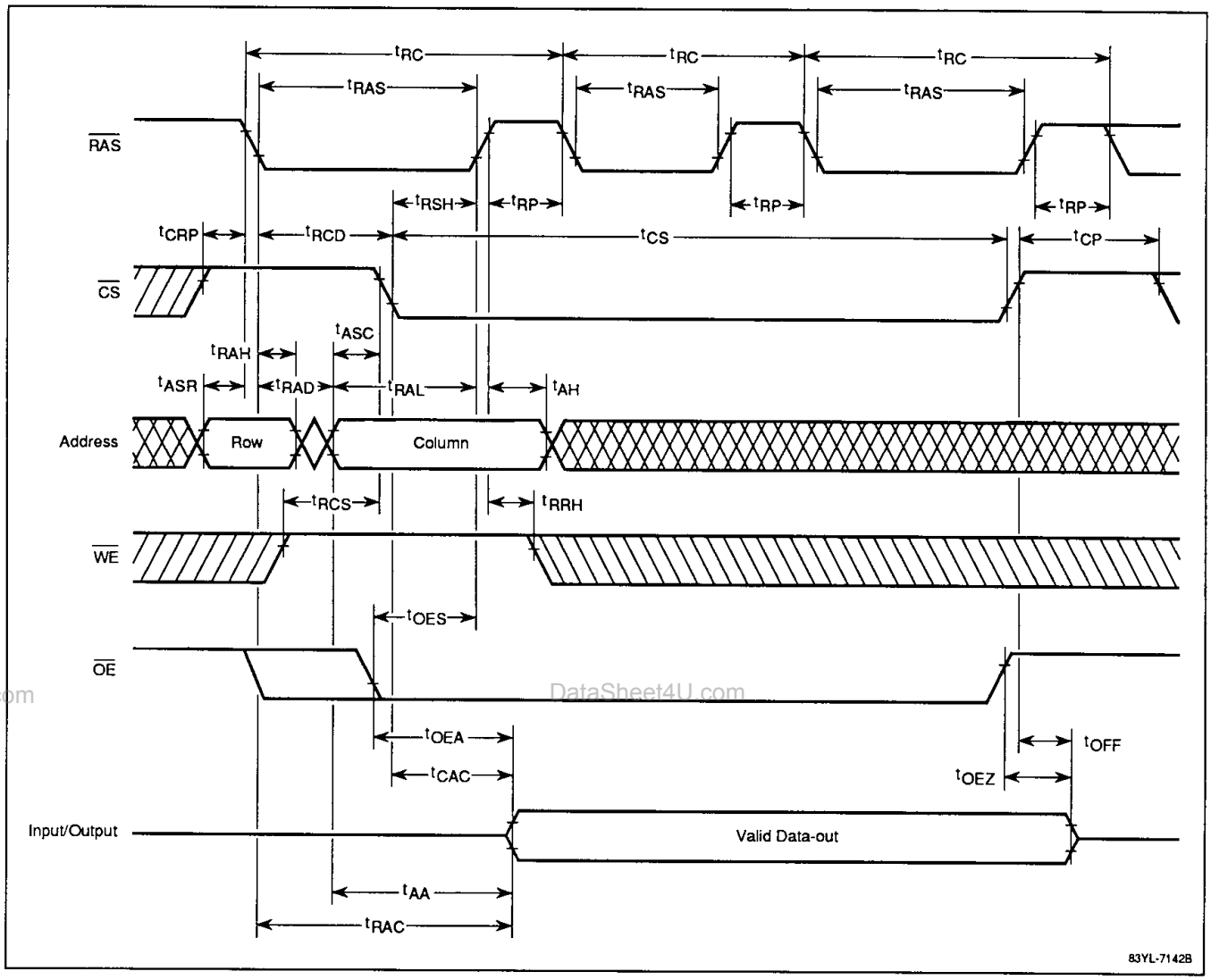
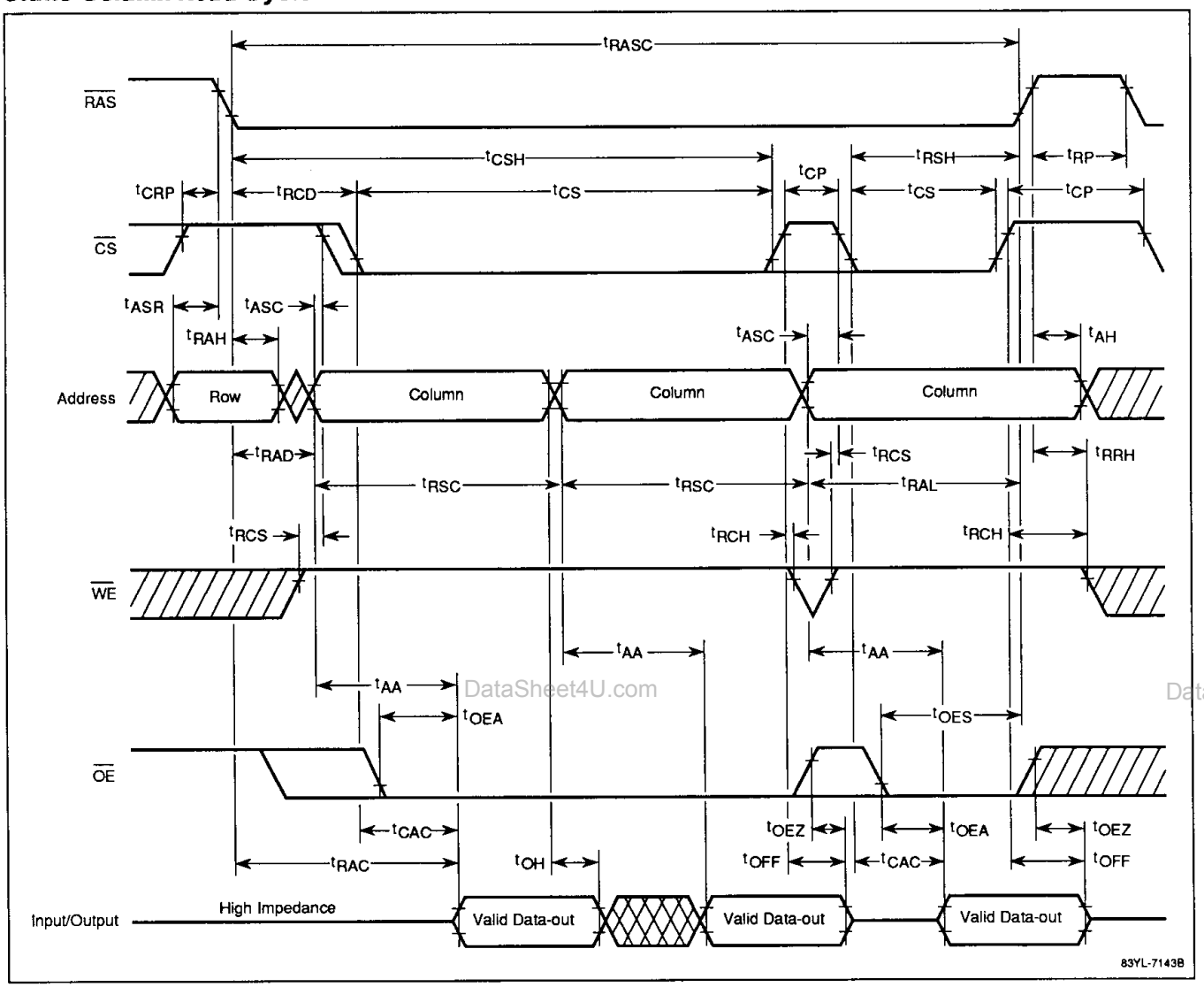
Timing Waveforms (cont)

Hidden Refresh Cycle



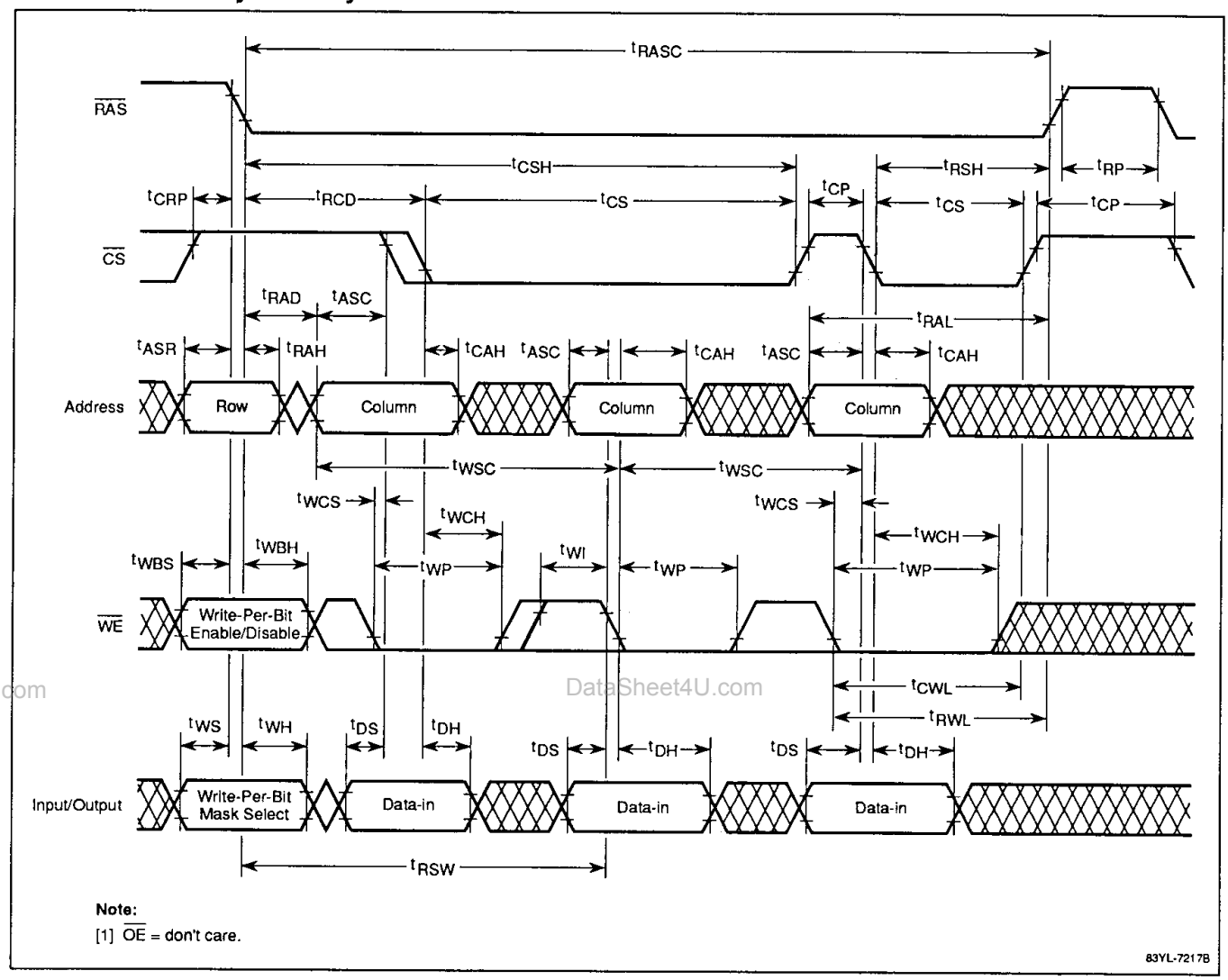
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Early Write Cycle



Note:
[1] $\overline{OE}$ = don't care.

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Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle