DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
μPD35H71A

5000-BIT CCD LINEAR IMAGE SENSOR

The μPD35H71A is a high sensitivity 5000-bit linear image sensor consisting of charge coupled devices (CCD) which changes optical images to electrical signal.

Especially, the μPD35H71A has extra high speed CCD register, so it is suitable for high resolution scanner and facsimile which scan high definition document at high speed.

FEATURES

- Valid photocell: 5000-bit
- Photocell's pitch: 7 μm
- Low Image Lag: Image lag is 1 % or less. One fifth of the existing equivalent NEC product (μPD35H71).
- High response sensitivity: Providing a response three times better than the existing equivalent NEC product (μPD3571) to the light from a day light fluorescent lamp. Equal with μPD35H71.
- High resolution: 16 dot/mm across the shorter side of a A3-size (297 x 420 mm) sheet
- 40 MHz high speed scan: 126 μs/line
- Peak response wavelength: 550 nm (green)
- Power supply: +12 V
- All clock signal input level: CMOS output under +5 V operation

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD35H71AD	CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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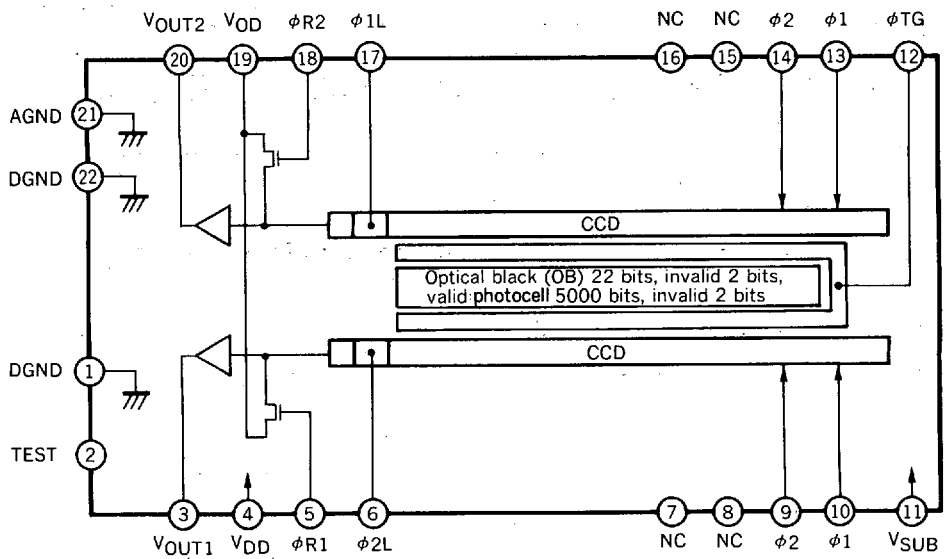
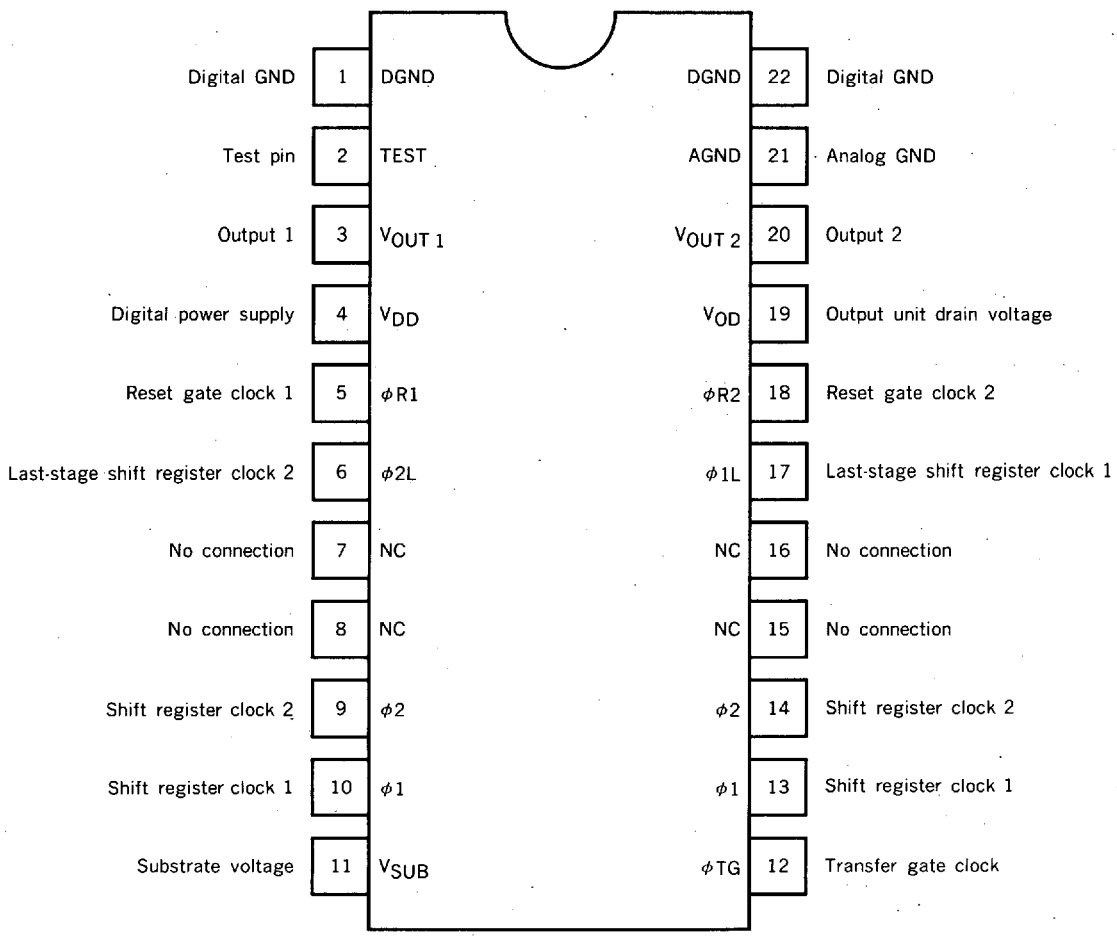
BLOCK DIAGRAM

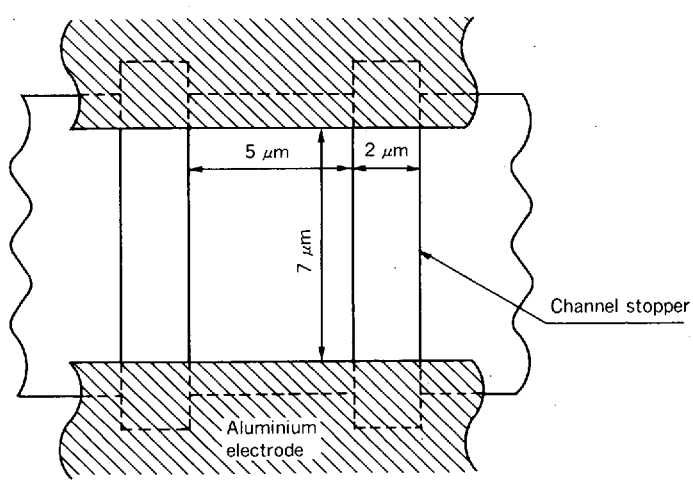


PIN CONFIGURATION (Top View)

CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)



PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C)

Parameter	Symbol	Ratings	Unit
Output unit drain voltage	V_{OD}	−0.3 to +15	V
Digital power supply	V_{DD}	−0.3 to +15	V
Substrate voltage	V_{SUB}	−0.3 to +15	V
Shift register clock voltage	$V_{\phi1,\phi2}$	−0.3 to +15	V
Reset signal voltage	$V_{\phi R}$	−0.3 to +15	V
Transfer gate signal voltage	$V_{\phi TG}$	−0.3 to +15	V
Operating ambient temperature	T_{opt}	−25 to +55	°C
Storage temperature	T_{stg}	−40 to +100	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −25 to +55 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output unit drain voltage	V_{OD}	11.4	12.0	12.6	V
Digital power supply	V_{DD}	11.4	12.0	12.6	V
Substrate voltage	V_{SUB}	11.4	12.0	12.6	V
Shift register clock $\phi1$, $\phi1$L signal high level	$V_{\phi1H}$	4.5	5.0	5.5	V
Shift register clock $\phi1$, $\phi1$L signal low level	$V_{\phi1L}$	−0.3	0	+0.5	V
Shift register clock $\phi2$, $\phi2$L signal high level	$V_{\phi2H}$	4.5	5.0	5.5	V
Shift register clock $\phi2$, $\phi2$L signal low level	$V_{\phi2L}$	−0.3	0	+0.5	V
Reset signal ϕR1 high level	$V_{\phi R1H}$	4.5	5.0	5.5	V
Reset signal ϕR1 low level	$V_{\phi R1L}$	−0.3	0	+0.5	V
Reset signal ϕR2 high level	$V_{\phi R2H}$	4.5	5.0	5.5	V
Reset signal ϕR2 low level	$V_{\phi R2L}$	−0.3	0	+0.5	V
Transfer gate signal high level	$V_{\phi TGH}$	4.5	5.0	5.5	V
Transfer gate signal low level	$V_{\phi TGL}$	−0.3	0	+0.5	V
Date rate	$f_{\phi R}$		2	40	MHz

Caution
1. **Leave Test pin (pin 2) unconnected.**
2. **Input reset signal ϕR1, ϕR2 to pin 5, 18 via resistor and capacitor. Concerning the connection method refer to APPLICATION CIRCUIT.**
3. **Operating conditions of reset signal ϕR1, ϕR2 are not the condition at device pins but the condition of the signal which applied to resistor.**

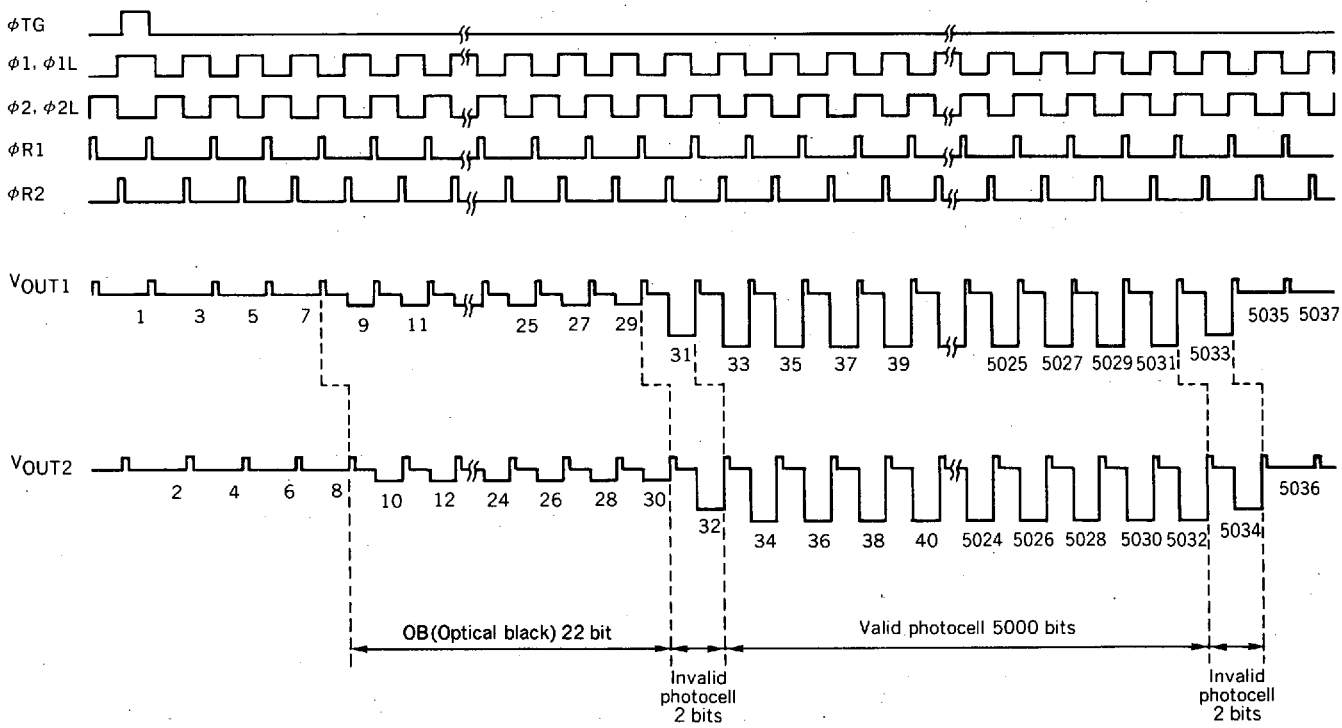
ELECTRICAL CHARACTERISTICS

T_a = +25 °C, V_{DD} = 12 V, $f_{\phi 1}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms,
light source = 3200 K halogen lamp +C500 (infrared cut filter), input signal clock = 5 V_{P-P}

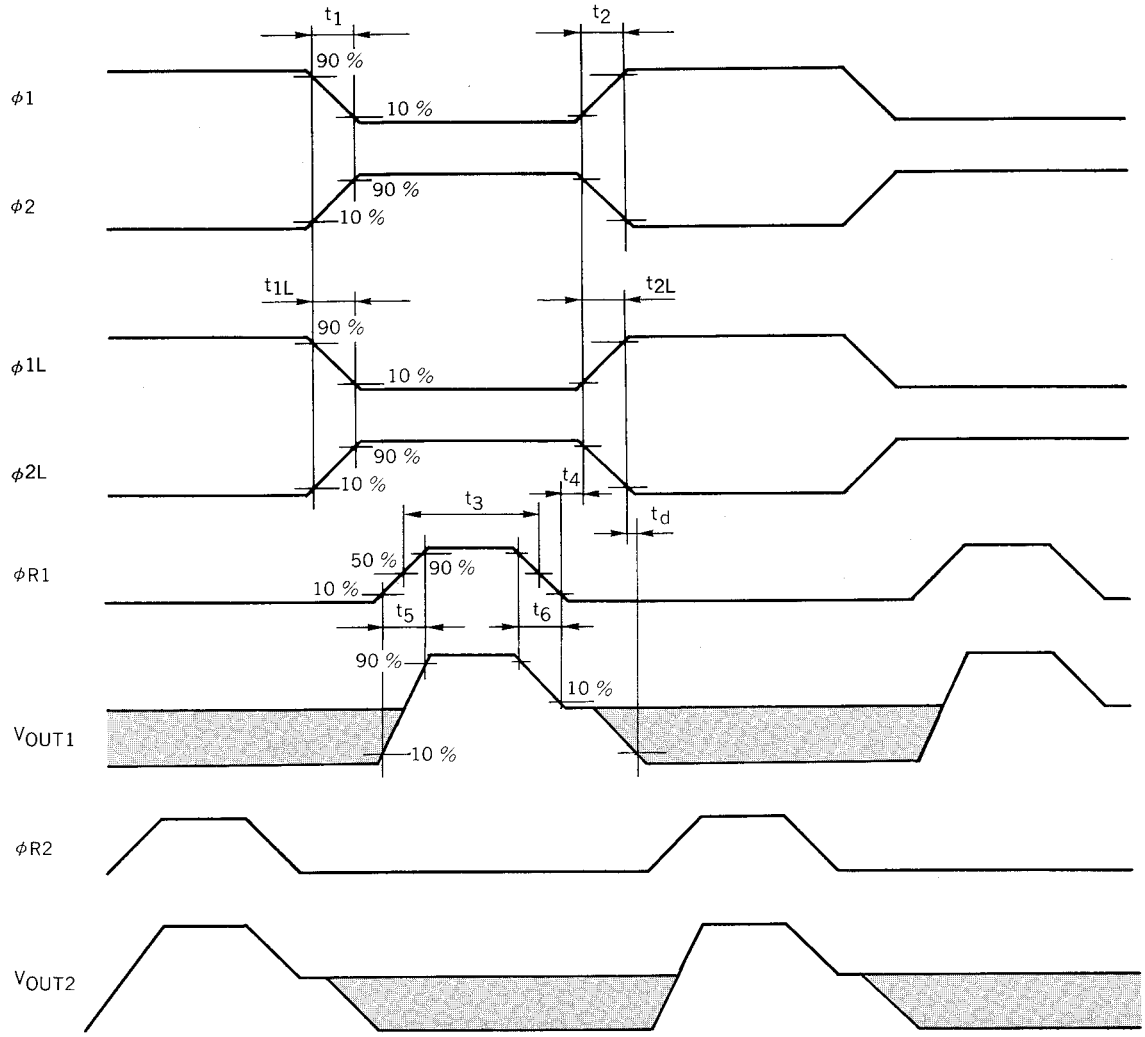
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}		1.0	1.5		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.29		lx·s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		±5	±10	%
Average dark signal	ADS	Light shielding		1.0	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding	−3	$^{+3}_{-1}$	+6	mV
Power consumption	P_W			200		mW
Output impedance	Z_O			0.2	0.5	kΩ
Response	R_F	Daylight color fluorescent lamp	4.15	5.2	6.25	V/lx·s
Response peak wavelength				550		nm
Image lag	IL	V_{OUT}=1V		0.3	1.0	%
Offset level	V_{OS}		2.0	3.0	5.0	V
Shift register clock input capacitance	$C_{\phi 1}$ $C_{\phi 2}$		400	500	800	pF
Last-stage shift register clock input capacitance	$C_{\phi 1L}$ $C_{\phi 2L}$		40	50	100	pF
Reset input capacitance	$C_{\phi R1}$ $C_{\phi R2}$		8	10	15	pF
Transfer gate signal input capacitance	$C_{\phi TG}$		100	150	200	pF
Output rise delay time	t_d **Note**	Time from 90 % to 10 % of φ2L fall is 5 ns.		20		ns
Register imbalance	RI	V_{OUT} = 500 mV		0	4	%
Transfer efficiency	TTE	V_{OUT} = 500 mV, $f_{\phi R1}$ = 20 MHz	92	98		%
Dynamic range	DR	V_{sat}/DSNU		500		times
Reset feed through noise	RFSN	Light shielding		250	500	mV

Note t_d is defined as a time from 10 % of φ2L to 10 % of V_{OUT}, output after passing through two steps of emitter follower in the **APPLICATION CIRCUIT.**

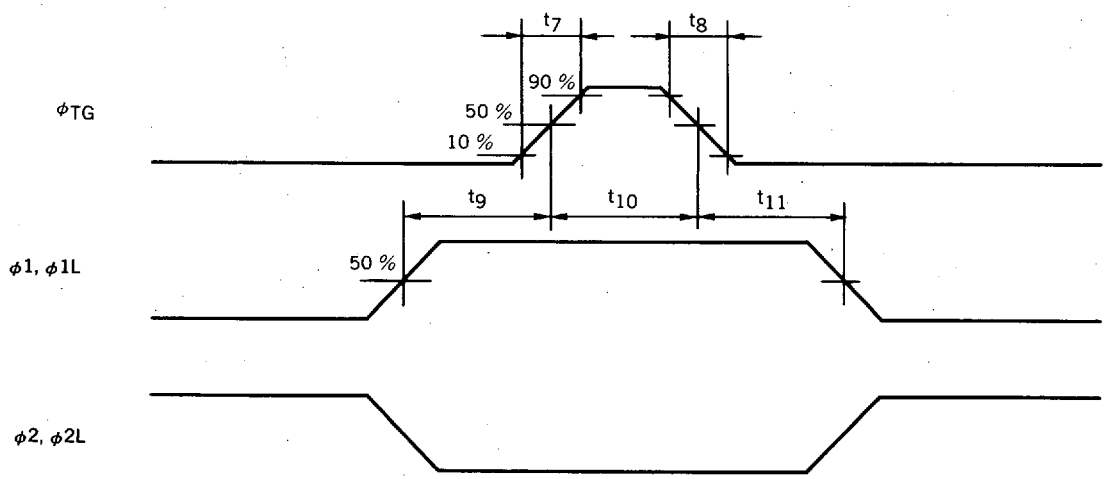
TIMING CHART 1



TIMING CHART 2



TIMING CHART 3

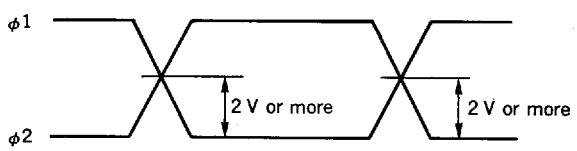


Recommended Timing (Unit: ns)

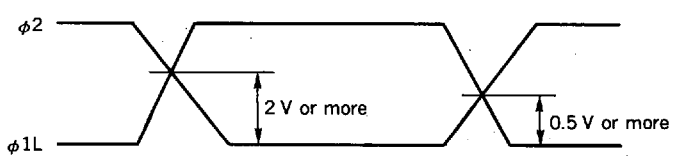
Parameter	MIN.	TYP.	MAX.
t_1, t_2	0	50	200
t_{1L}, t_{2L}	0	5	25
t_3	15	50	(500)
t_4	5	20	(500)
t_5, t_6	0	20	50
t_7, t_8	0	50	100
t_9, t_{11}	10	100	(500)
t_{10}	1000	2000	(5000)

Remark The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for general purpose, does not show the limit above which the μPD35H71A is destroied.

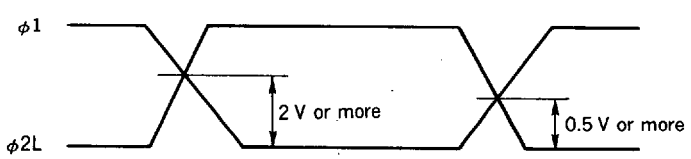
CROSS POINTS for φ1, φ2



CROSS POINTS for φ1L, φ2



CROSS POINTS for φ1, φ2L



Remark Adjust cross point of (φ1, φ2), (φ1L, φ2), (φ1, φ2L) by each pin external input resistor.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage: V_{sat}

   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE

   Product of intensity of illumination (lx) and storage time(s) when saturation of output voltage occurs.

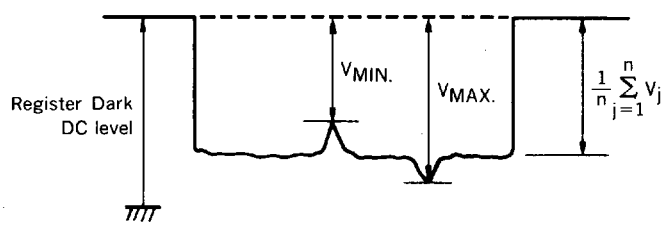
3. Photo response non-uniformity: PRNU

   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU(\%) = \left(\frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

   n : Number of valid bits

   V_j : Output voltage of each bit



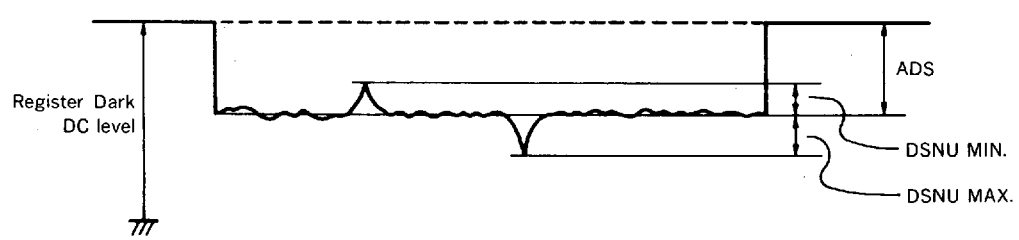
4. Average dark signal: ADS

   Output average voltage in light shielding.

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

5. Dark signal non-uniformity: DSNU

   The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: Z_o

   Output pin impedance viewed from outside.

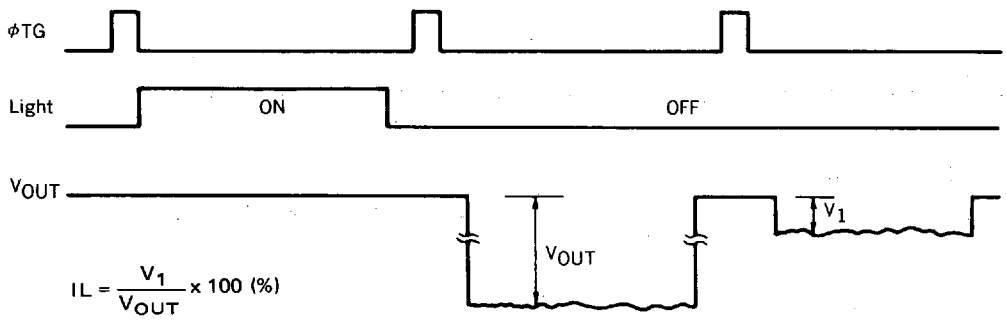
7. Response: R

   Output voltage divided by exposure (lx·s).

   Note that the response varies with the light source.

8. Image Lag: IL

The rate between the last output voltage and the next one after read out the data of a line.



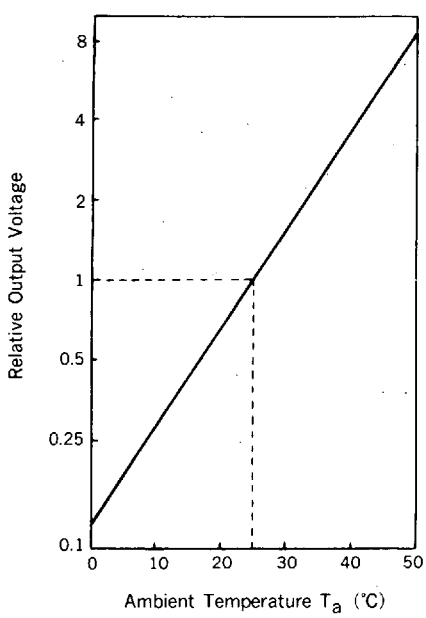
9. Register Imbalance: RI

The rate of the difference between the average of the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

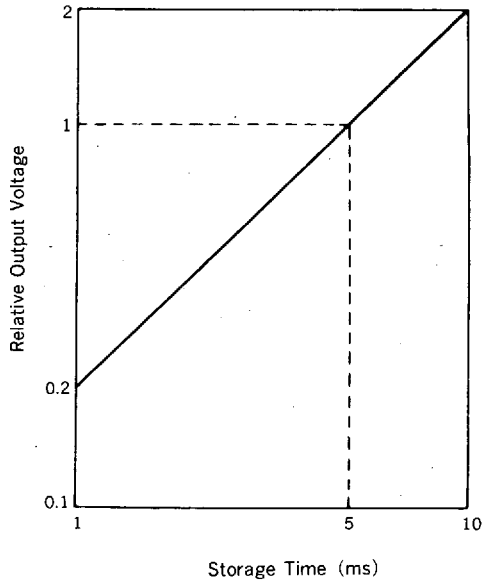
$$RI = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100\ (\%)$$

STANDARD CHARACTERISTIC CURVES (T_a = +25 °C)

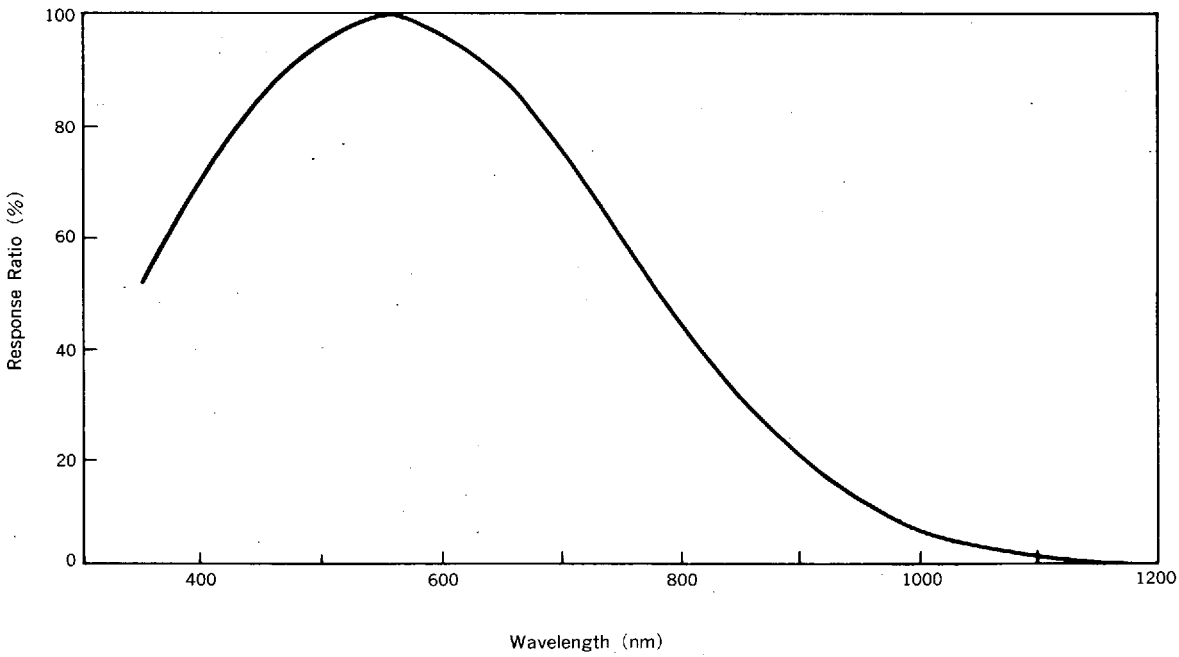
DARK OUTPUT TEMPERATURE CHARACTERISTIC



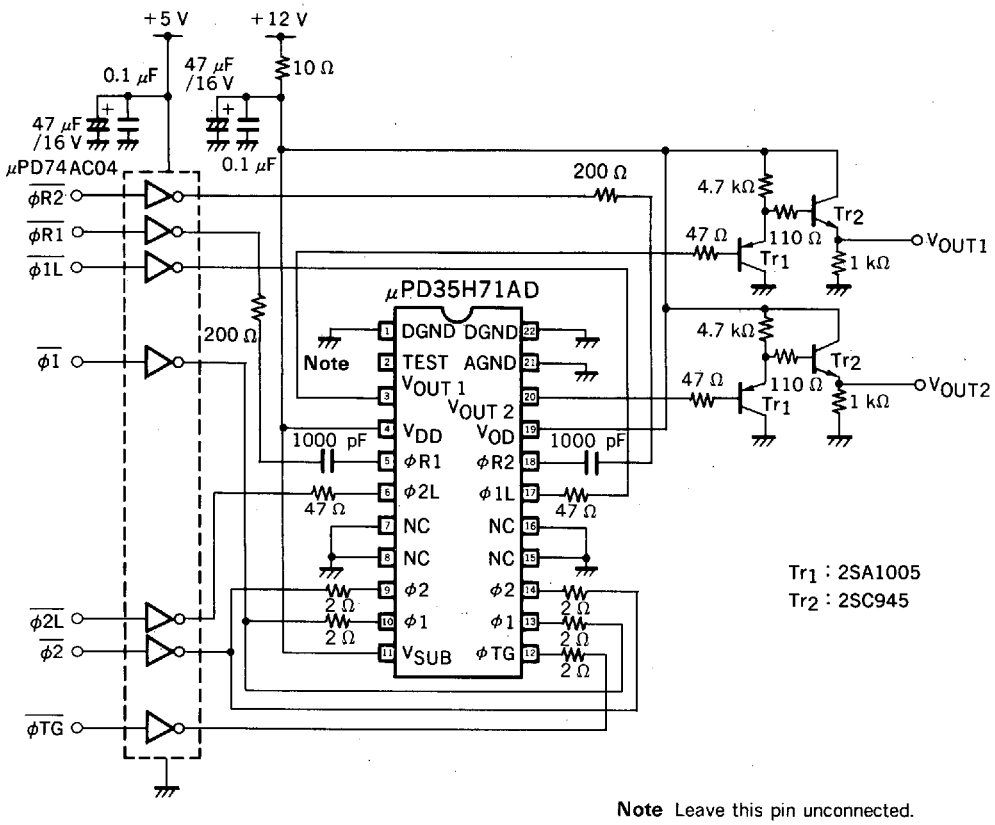
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC



SPECTRAL RESPONSE CHARACTERISTIC



APPLICATION CIRCUIT



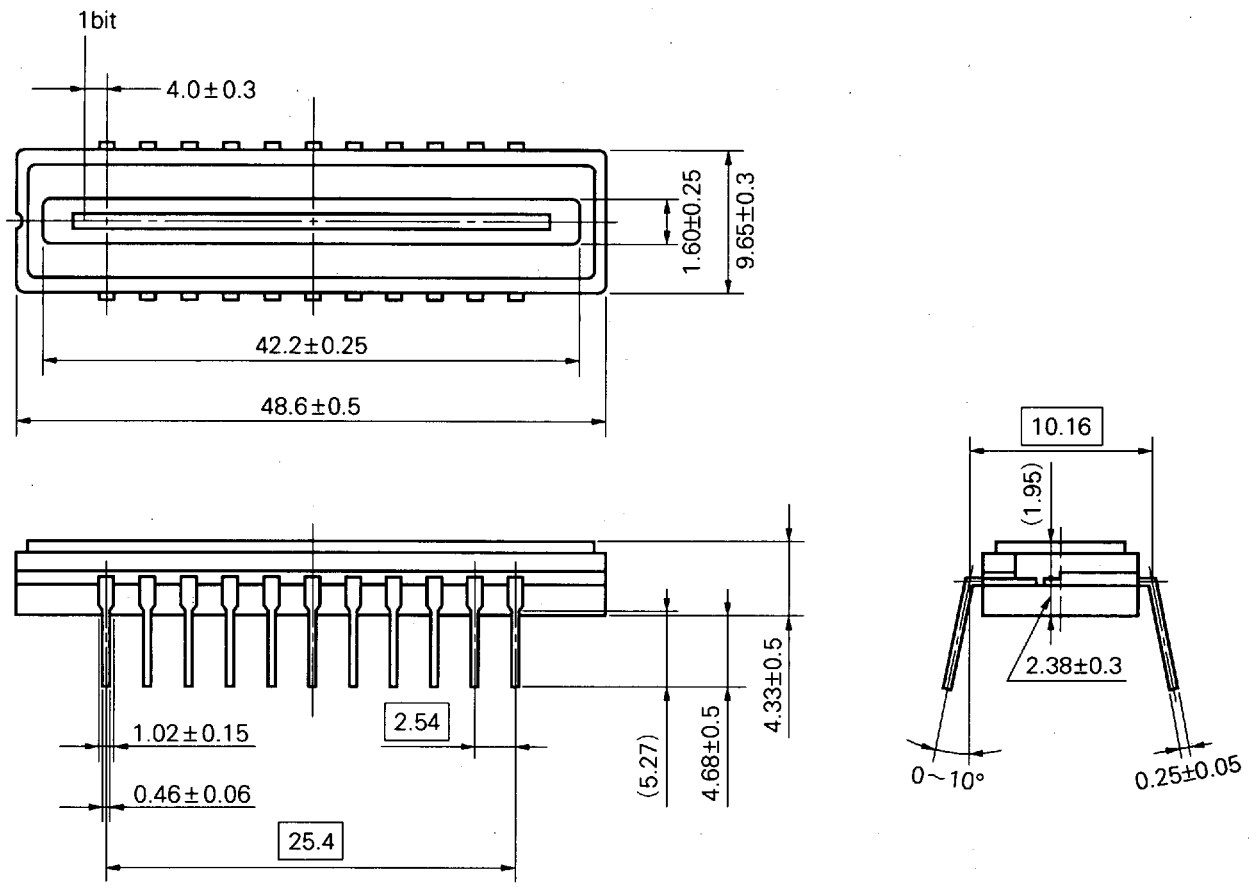
Note Leave this pin unconnected.

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

PACKAGE DIMENSIONS

CCD LINEAR IMAGE SENSOR 22PIN CERAMIC DIP(CERDIP)(400mil)

(Unit : mm)



Name	Dimensions	Refractive index
Glass cap	47.5×9.25×0.7	1.5

22D-1CCD-PKG8

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).**

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 1 Type of Through Hole Device

μPD35H71AD: CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)

Soldering Process	Soldering Conditions
Wave soldering (For leads only)	Solder temperature: 260 °C or below Flow time: 10 seconds or below
Partial heating method	Pin temperature: 260 °C or below Time: 10 seconds or below

Caution Do not jet molten solder on the surface of package.