NEC

MOS INTEGRATED CIRCUIT

μPD16664

144/160/184/208-OUTPUT LCD COLUMN (SEGMENT) DRIVER WITH RAM

DESCRIPTION

The μPD16664 is a column (segment) driver with internal RAM and can drive a full-dot LCD. Equipped with 144/160/184/208-output pins and a display RAM of 208 x 160 x 2 bits, this driver can display any of four gray levels selected from a 25-level palette. By using this IC in combination with the μPD16667, 144 x 128 pixels to 416 x 320 pixels can be displayed.

FEATURES

- Internal display RAM : 208 x 160 x 2 bits
- Logic voltage : 2.4 to 3.6 V
- Duty : 1/128, 1/160 selectable
- Number of outputs : 144,160,184 and 208 pins selectable
- Display : Four gray levels (selectable from 25-level palette)
- Memory management : Packed pixel method
- Supports 8/16-bit data bus

ORDERING INFORMATION

Part number	Package
μPD16664N-xxx	TCP (TAB)
μPD16664N-001	2/4-side Standard TCP

Remark The TCP's external shape is customized. To order the required shape, please contact an NEC salesperson.

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The mark ★ shows major revised points.

1. PIN NAME

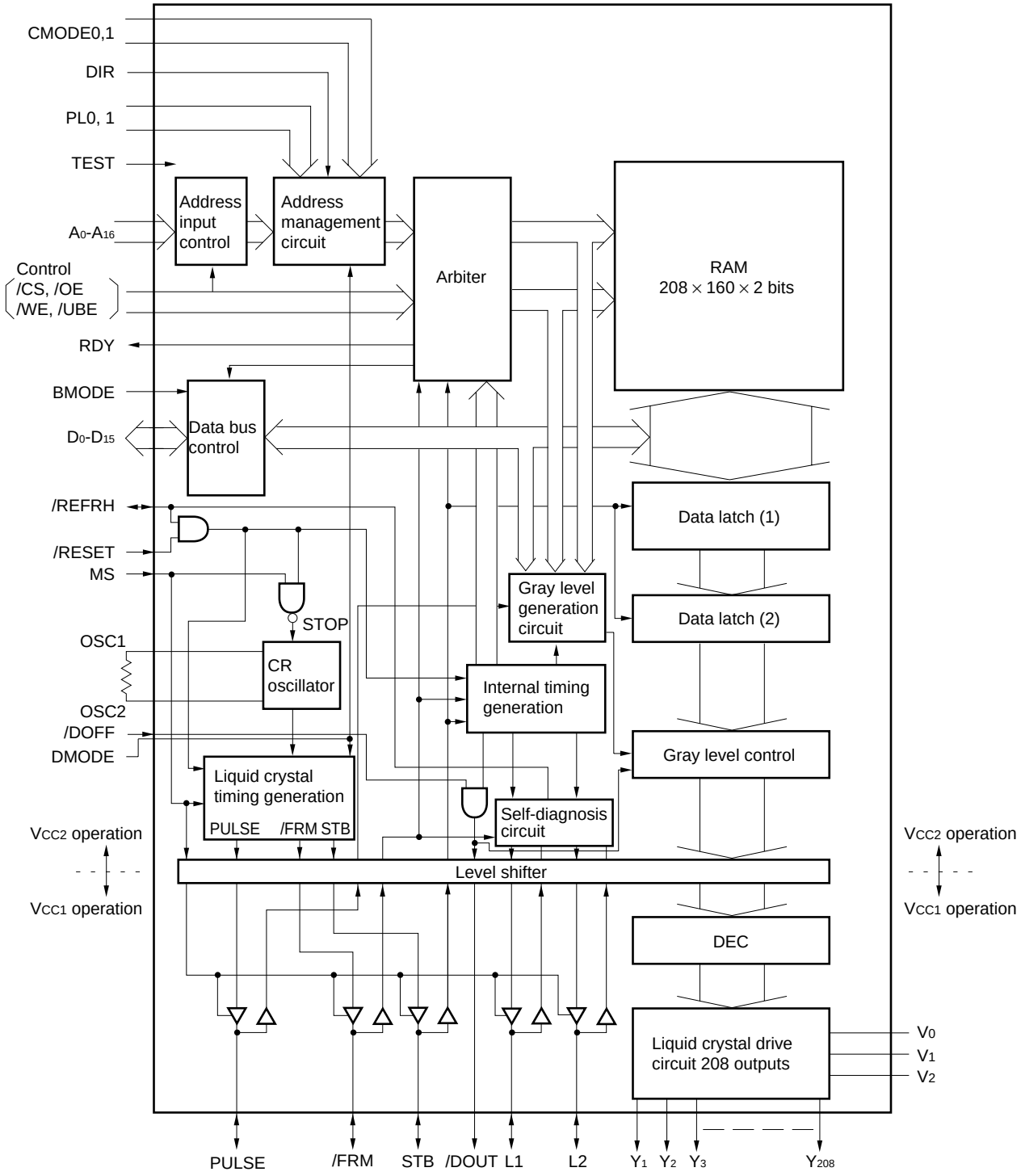
Classification	Pin Name[Note]	I/O	Function
CPU interface (V_{CC2})	D_0-D_{15}	I/O	Data bus: 16 bits
	A_0-A_{16}	I	Address bus: 17 bits
	/CS	I	Chip select
	/OE	I	Read signal
	/WE	I	Write signal
	/UBE	I	Upper byte enable
	RDY	O	Ready signal to CPU (“H”: ready)
Control signals (V_{CC2})	PL0	I	Specifies LSI layout position (No. 0 to 3)
	PL1	I	Specifies LSI layout position (No. 0 to 3)
	DIR	I	Specifies liquid crystal panel layout position
	DMODE	I	Duty selection (“H” = 1/128 duty, “L” =1/160 duty)
	CMODE0,1	I	Number of column outputs selection
	MS	I	Master/slave selection (“H”: master mode)
	BMODE	I	Data bus bit selection (“H” = 8 bits, “L” = 16 bits)
	/REFRH	I/O	Self-diagnosis reset pin (wired-OR connection)
	TEST	I	Test pin (“H” = test mode, with pull-down resistor)
	/RESET	I	Reset signal
	/DOFF	I	Display OFF input signal
	OSC1	–	External resistor pin for oscillator
	OSC2	–	External resistor pin for oscillator
(V_{CC1})	STB	I/O	Column drive signal (MS pin “H” = output, MS pin “L” = input)
	/FRM	I/O	Frame signal (MS pin “H” = output, MS pin “L” = input)
	PULSE	I/O	25-level pulse modulation clock
	L1	I/O	Row driver drive level select signal (first line)
	L2	I/O	Row driver drive level select signal (second line)
	/DOUT	O	Display OFF output signal
Liquid crystal drive	Y_1-Y_{208}	O	Liquid crystal drive output
Power	GND	–	Ground (two pins for V_{CC1} system, three pins for V_{CC2} system)
	V_{CC1}	–	Power supply for liquid crystal drive and row driver interface
	V_{CC2}	–	Power supply for logic
	V_0	–	Liquid crystal drive analog power
	V_1	–	Liquid crystal drive analog power
	V_2	–	Liquid crystal drive analog power

Note V_{CC2} system pins : D_0 to D_{15}, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, BMODE, PL0, PL1, DIR, OSC1, OSC2, /RESET, /DOFF, TEST, MS, CMODE0, CMODE1, DMODE

V_{CC1} system pins : STB, /FRM, L1, L2, /DOUT, PULSE

Remark /xxx indicates active low signals.

2. BLOCK DIAGRAM



3. BLOCK FUNCTION

(1) Address management circuit

This circuit converts addresses from the system via A_0 to A_{16} into addresses corresponding to the memory map of the internal RAM.

By using this function and four μPD16664 modules, addresses for up to 416 × 320 pixels can be managed, making it easy to construct a liquid crystal display system.

Addresses 1FF00H to 1FF1EH are allocated to a gray level palette register, and any four gray levels can be selected from a 25-level palette.

(2) Arbiter

This circuit arbitrates conflicts between access by the system to the RAM and reading the RAM by the LCD driver.

(3) RAM

This is a static RAM of 208 x 160 x 2 bits (single port).

(4) Data bus control

This circuit controls the data transfer direction depending on whether the system reads or writes the RAM of the μPD16664.

The data bus width can be changed between 8 and 16 bits by the BMODE pin.

(5) Gray level generation circuit

This circuit offers 25 levels by means of frame interpolation and pulse width modulation.

(6) Internal timing generation

This circuit generates internal timing signals for each block from the /FRM and STB signals.

(7) CR oscillator

This oscillator generates a clock that serves as the reference of the frame frequency in the master mode. Because this CR oscillator has an on-chip capacitor, the necessary oscillation frequency can be adjusted by using an external resistor.

Oscillation is stopped in the slave mode.

(a) 1/160 duty

The frame frequency is 1/1296 of the oscillation frequency of this oscillator. For example, when the frame frequency is 70 Hz, the oscillation frequency is 90.72 kHz.

(b) 1/128 duty

The frame frequency is 1/1040 of the oscillation frequency of this oscillator. For example, when the frame frequency is 70 Hz, the oscillation frequency is 72.80 kHz.

(8) Liquid crystal timing generation

This circuit generates the /FRM (frame signal), STB(column drive signal strobe), and PULSE (25-level pulse modulation clock) signals in the master mode.

(9) Gray level control

This circuit implements the 4-gray level display.

(10) Data latch (1)

This circuit reads data for 208 pixels from RAM and latches it.

(11) Data latch (2)

This circuit latches data for 208 pixels in synchronization with the STB signal.

(12) Level shifter

The level shifter converts the operating voltage of the internal circuit(V_{CC2}) into the voltage for the liquid crystal driver circuit and row driver interface (V_{CC1}).

(13) DEC

This is a decoder that decodes gray level display data to liquid crystal drive voltages V_0, V_1, or V_2.

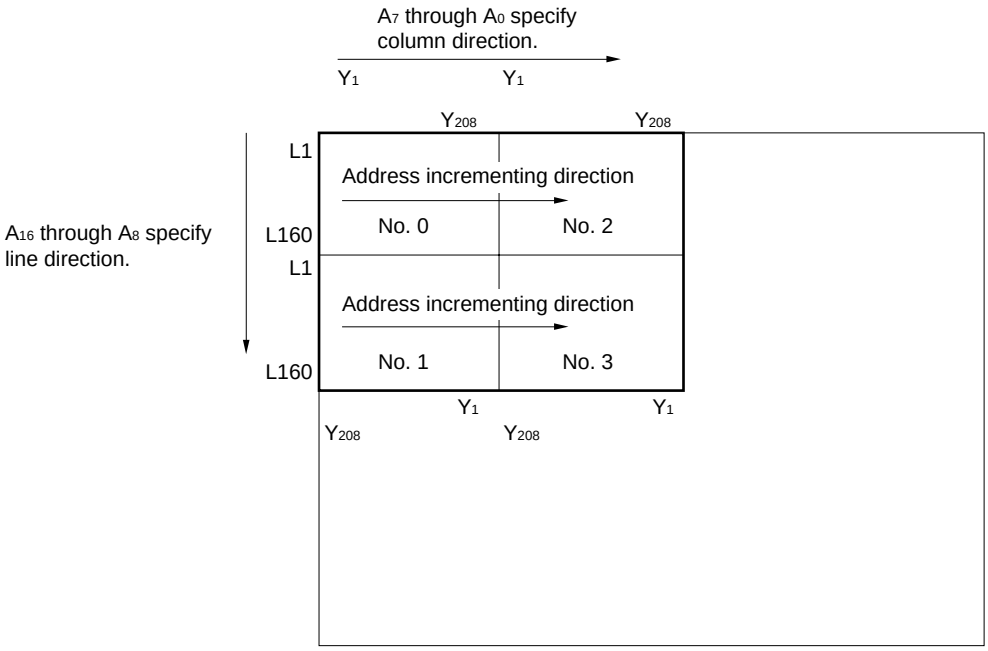
(14) Liquid crystal drive circuit

This circuit selects liquid crystal drive voltage V_0, V_1, or V_2 corresponding to gray level display data and the display OFF signal (/DOFF), to generate a liquid crystal application voltage.

(15) Self-diagnosis circuit

If the operation timing of the master chip and that of the slave chip differ due to external noise, this circuit automatically detects the difference and generates a refresh signal to all column drivers.

Address Map Image (CMODE0 = L, CMODE1 = L, DMODE = L)



4. DATA BUS

The byte data ordering on the data bus is little endian, in common with most NEC and Intel buses.

4.1 16-bit Data Bus (BMODE = L)

Byte access

	D_0 to D_7	D_8 to D_{15}
	00000H	00001H
Address incrementing	00002H	00003H
direction →	00004H	00005H
	:	:
	:	:

Word access

	D_0 to D_7	D_8 to D_{15}
	00000H	
Address incrementing	00002H	
direction →	00004H	
	:	
	:	

If the system accesses the μPD16664 in word(16-bit) or byte(8-bit) units, /UBE (upper byte enable) and A_0 specify whether bytes D_0 to D_7 or bytes D_8 to D_{15} have valid data.

/CS	/OE	/WE	/UBE	A_0	MODE	I/O	
						D_0 to D_7	D_8 to D_{15}
H	X	X	X	X	Not selected	Hi-Z	Hi-Z
L	L	H	L	L	Read	Dout	Dout
			L	H		Hi-Z	Dout
			H	L		Dout	Hi-Z
L	H	L	L	L	Write	Din	Din
			L	H		X	Din
			H	L		Din	X
L	H	H	X	X	Output	Hi-Z	Hi-Z
L	X	X	H	H	Disable	Hi-Z	Hi-Z

Remark X : Don't care
Hi-Z : High impedance

4.2 8-bit Data Bus (BMODE = H)

Address incrementing direction →

D_0 to D_7
00000H
00001H
00002H
:
:

/CS	/OE	/WE	MODE	I/O	
				D_0 to D_7	D_8 to D_{15}
H	X	X	Not selected	Hi-Z	**Note**
L	L	H	Read	Dout	**Note**
L	H	L	Write	Din	**Note**
L	H	H	Output disable	Hi-Z	**Note**

Note Leave D_8 to D_{15} open because they are internally pulled down.

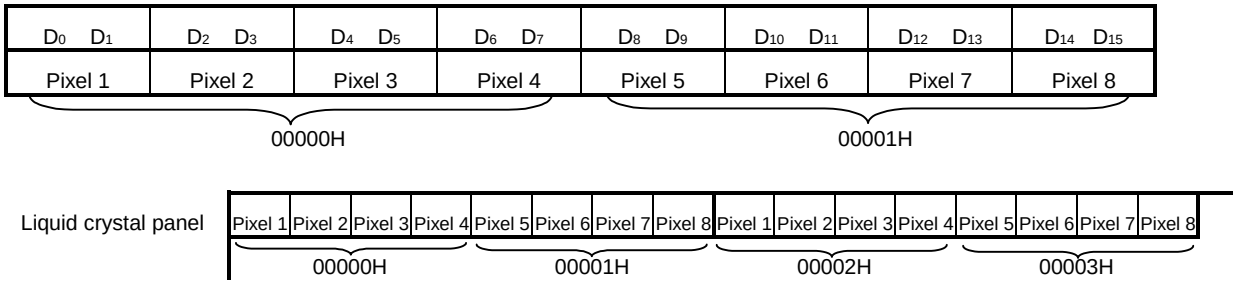
Remark X: Don't care
Hi-Z: High impedance

5. RELATION BETWEEN DATA BITS AND PIXELS

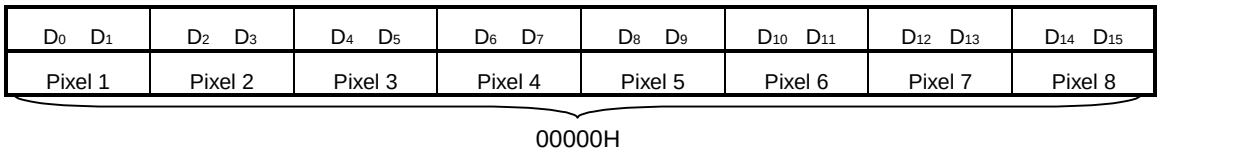
Because the μPD16664 displays four gray levels, 1 pixel consists of 2 bits. The RAM consists of 4 pixels (8 pixels per word) using the packed pixel method.

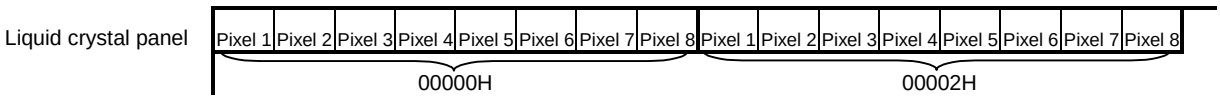
(1) BMODE = L

Byte (8-bit) access

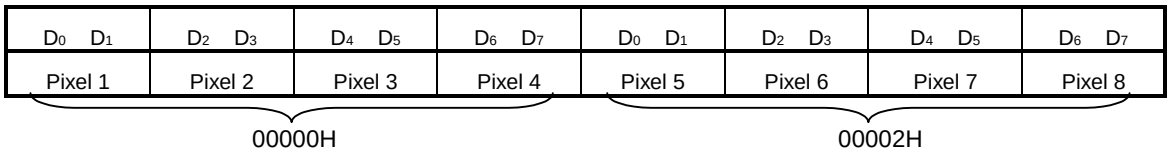


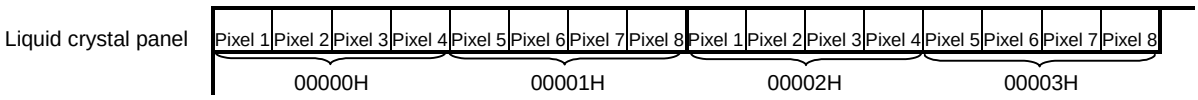
Word (16-bit) access





(2) BMODE = H





6. GRAY LEVEL CONTROL

The gray level control of the μPD16664 offers a 25-level palette by means of frame interpolation and pulse width modulation. From this palette, four gray levels are selected and registered in a gray level palette register.

7. GRAY LEVEL PALETTE REGISTER

The gray level palette register selects four gray levels from 25 levels in advance. This register is allocated to 1FF00H to 1FF1EH, and its relation with gray level data is as shown below.

The gray level palette register can be set for each layout position of the column driver (No. 0 to 3) that is determined by PL0 and PL1.

Address	Layout Position No.	Gray Level Data (Display Data)	
		Dn+1[Note]	Dn[Note]
1FF00H	No.0	0	0
1FF02H		0	1
1FF04H		1	0
1FF06H		1	1
1FF08H	No.1	0	0
1FF0AH		0	1
1FF0CH		1	0
1FF0EH		1	1
1FF10H	No.2	0	0
1FF12H		0	1
1FF14H		1	0
1FF16H		1	1
1FF18H	No.3	0	0
1FF1AH		0	1
1FF1CH		1	0
1FF1EH		1	1

Note n = 0, 2, 4, 6, 8, 10, 12, or 14

8. RELATION BETWEEN GRAY LEVELS AND GRAY LEVEL PALETTE DATA

The relation between the gray levels and the gray level palette data set by the gray level palette register is as follows:

PMODE	Gray Level Palette Data					Remark
	D_4	D_3	D_2	D_1	D_0	
Gray level 0	0	0	0	0	0	OFF
Gray level 1	0	0	0	0	1	
Gray level 2	0	0	0	1	0	
Gray level 3	0	0	0	1	1	
Gray level 4	0	0	1	0	0	
Gray level 5	0	0	1	0	1	
Gray level 6	0	0	1	1	0	
Gray level 7	0	0	1	1	1	
Gray level 8	0	1	0	0	0	1/3
Gray level 9	0	1	0	0	1	
Gray level 10	0	1	0	1	0	
Gray level 11	0	1	0	1	1	
Gray level 12	0	1	1	0	0	
Gray level 13	0	1	1	0	1	
Gray level 14	0	1	1	1	0	
Gray level 15	0	1	1	1	1	
Gray level 16	1	0	0	0	0	2/3
Gray level 17	1	0	0	0	1	
Gray level 18	1	0	0	1	0	
Gray level 19	1	0	0	1	1	
Gray level 20	1	0	1	0	0	
Gray level 21	1	0	1	0	1	
Gray level 22	1	0	1	1	0	
Gray level 23	1	0	1	1	1	
Gray level 24	1	1	0	0	0	ON

9. LSI LAYOUT AND ADDRESS MANAGEMENT

Addresses are managed so that up to four μPD16664s can be used to organize a liquid crystal display of 416 x 320 pixels.

Four modules can be connected on the same bus with the /CS, /WE, and /OE pins shared.

The system can treats one screenful of the liquid crystal display as one memory area, and does not have to decode more than one LSI.

Specify an LSI No. by using the PL0 and PL1 pin to determine the layout of the LSIs, and determine the direction (vertical or horizontal) of the liquid crystal display by using the DIR pin.

PL1	PL0	LSI No.
0	0	No. 0
0	1	No. 1
1	0	No. 2
1	1	No. 3

10. NUMBER OF COLUMN OUTPUTS SELECTION

CMODE1	CMODE0	Number of Column Outputs	Valid Pins
0	0	208	Y_1 to Y_{208}
0	1	184	Y_1 to Y_{184}
1	0	160	Y_1 to Y_{160}
1	1	144	Y_1 to Y_{144}

Remark Invalid column outputs are fastened to V_1 level.

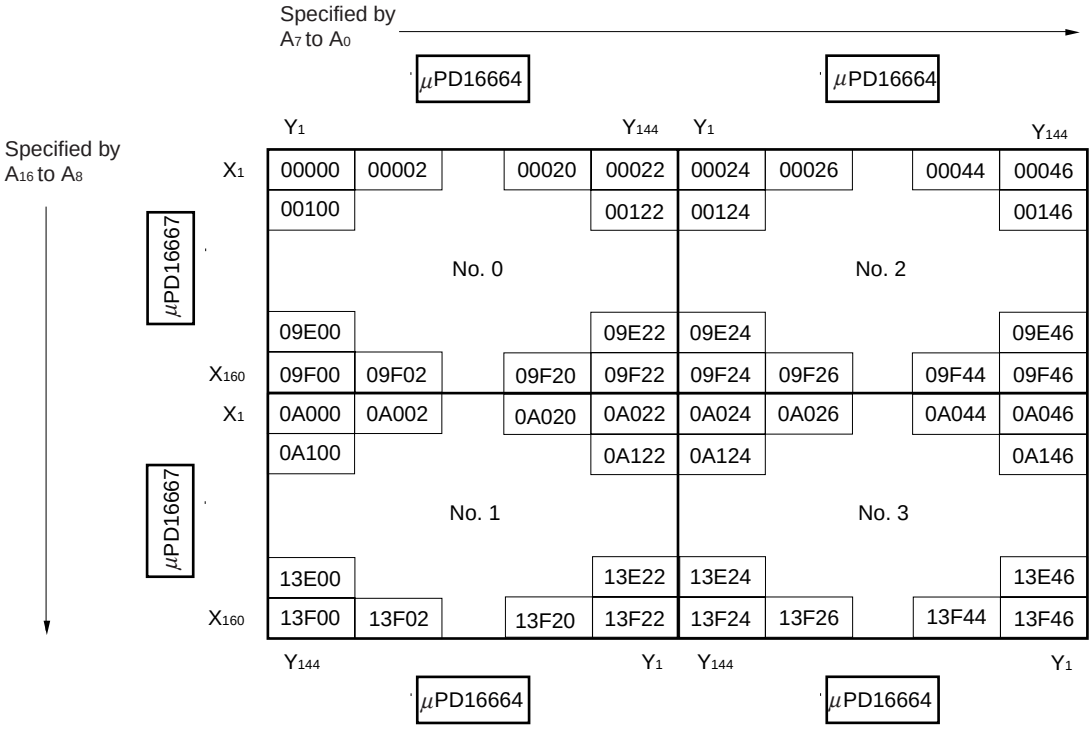
11. DUTY SELECTION

DMODE	Duty
0	1/160
1	1/128 [Note]

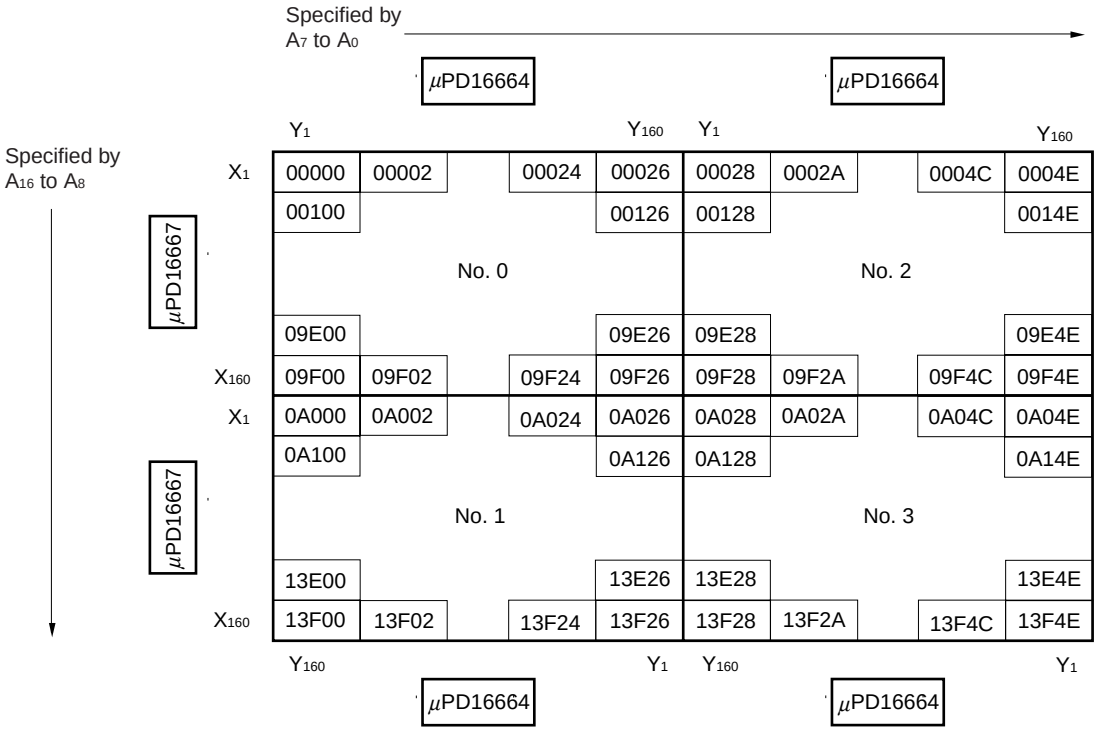
Note Valid row outputs of μPD16667 are X_1 to X_{128}. Invalid row outputs are undefined.

★ **Horizontally Long Address** **DIR = L, DMODE = L**

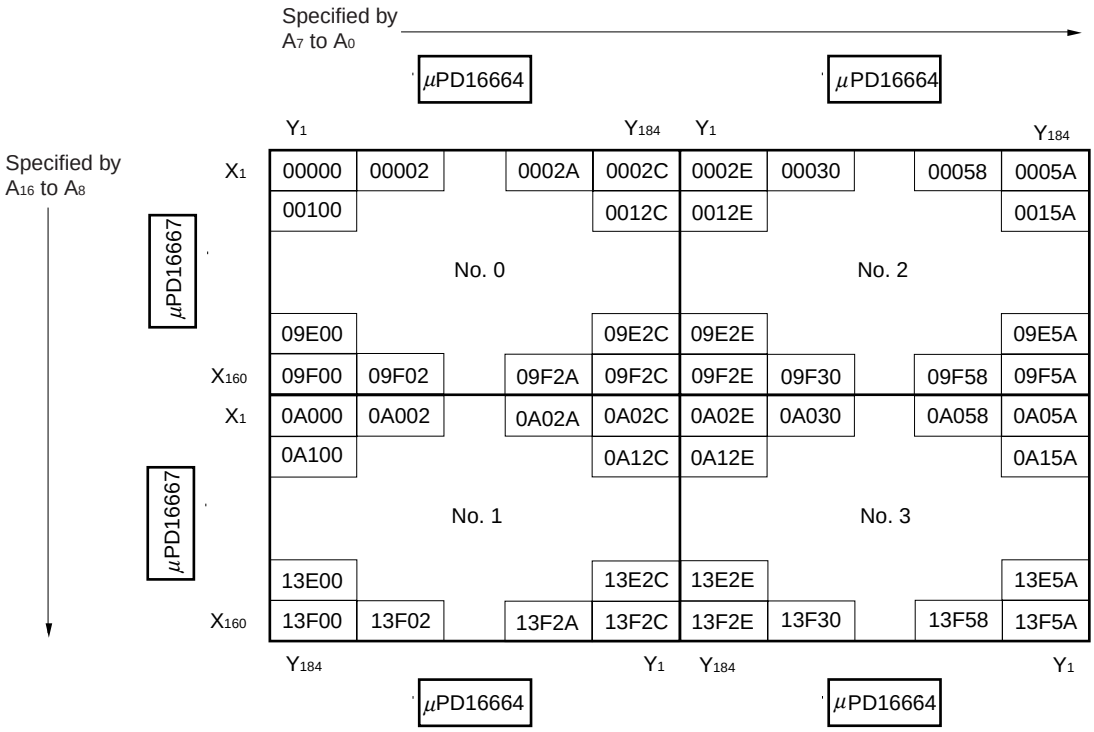
• 144-output Mode



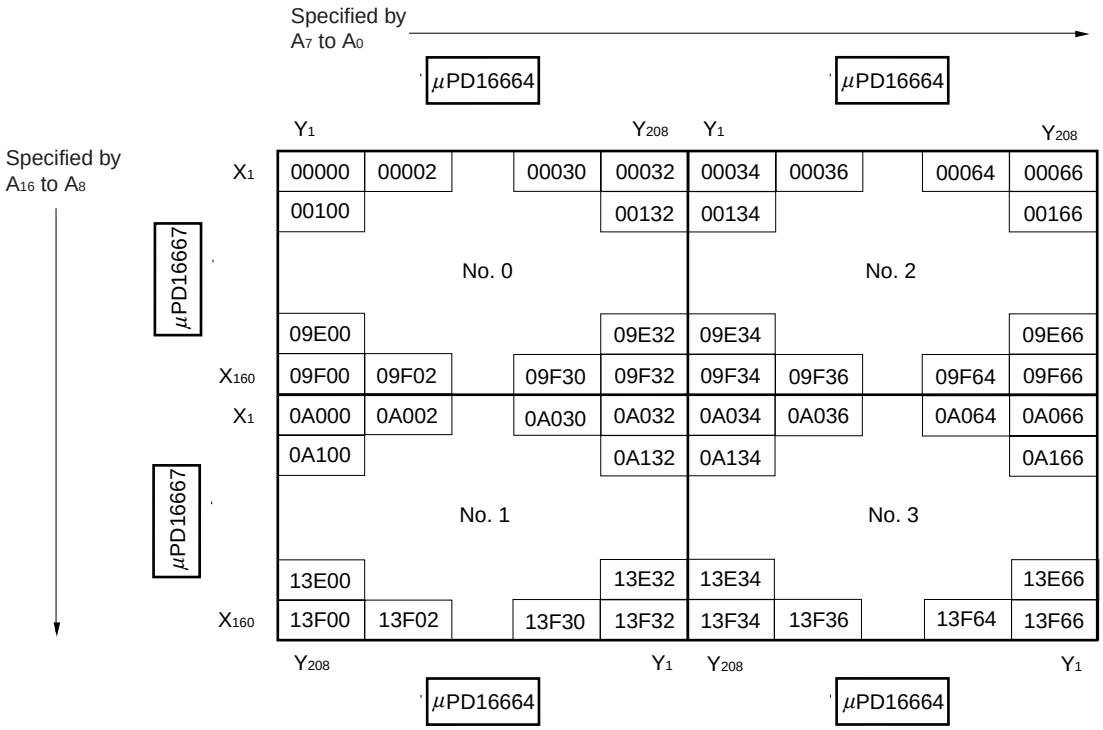
• 160-output Mode



● **184-output Mode**

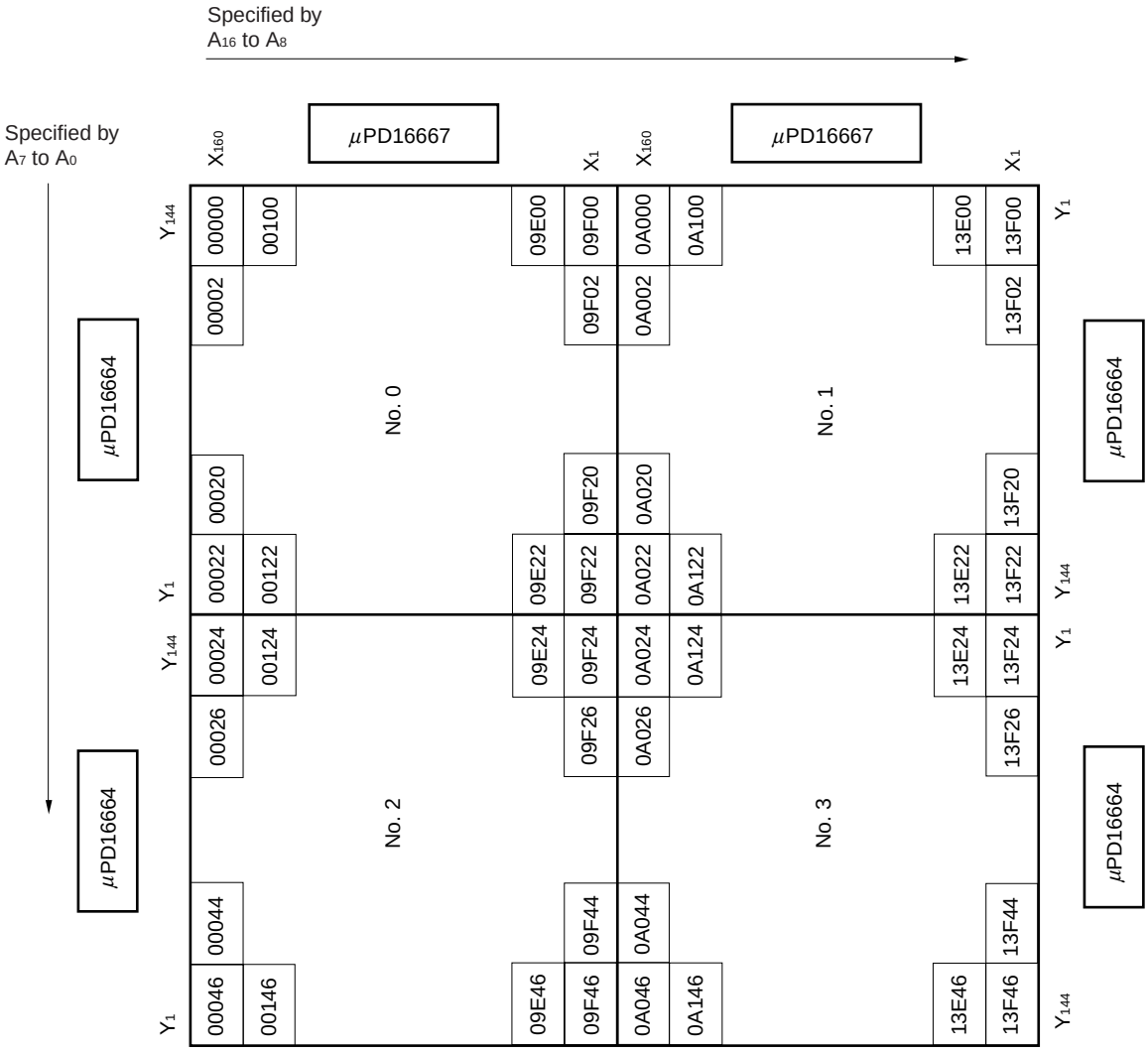


● **208-output Mode**

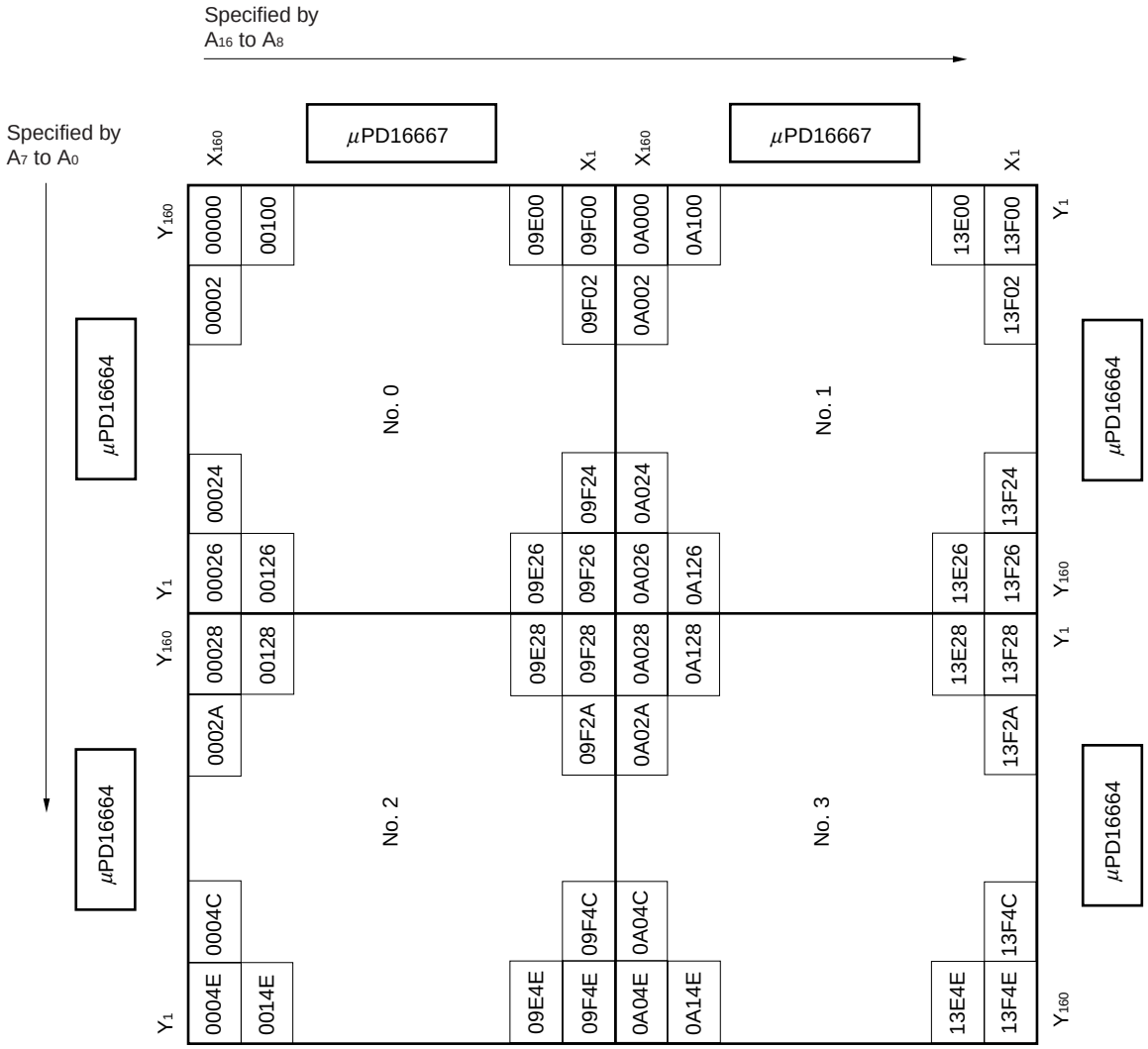


★ **Vertically Long Address** **DIR = H, DMODE = L**

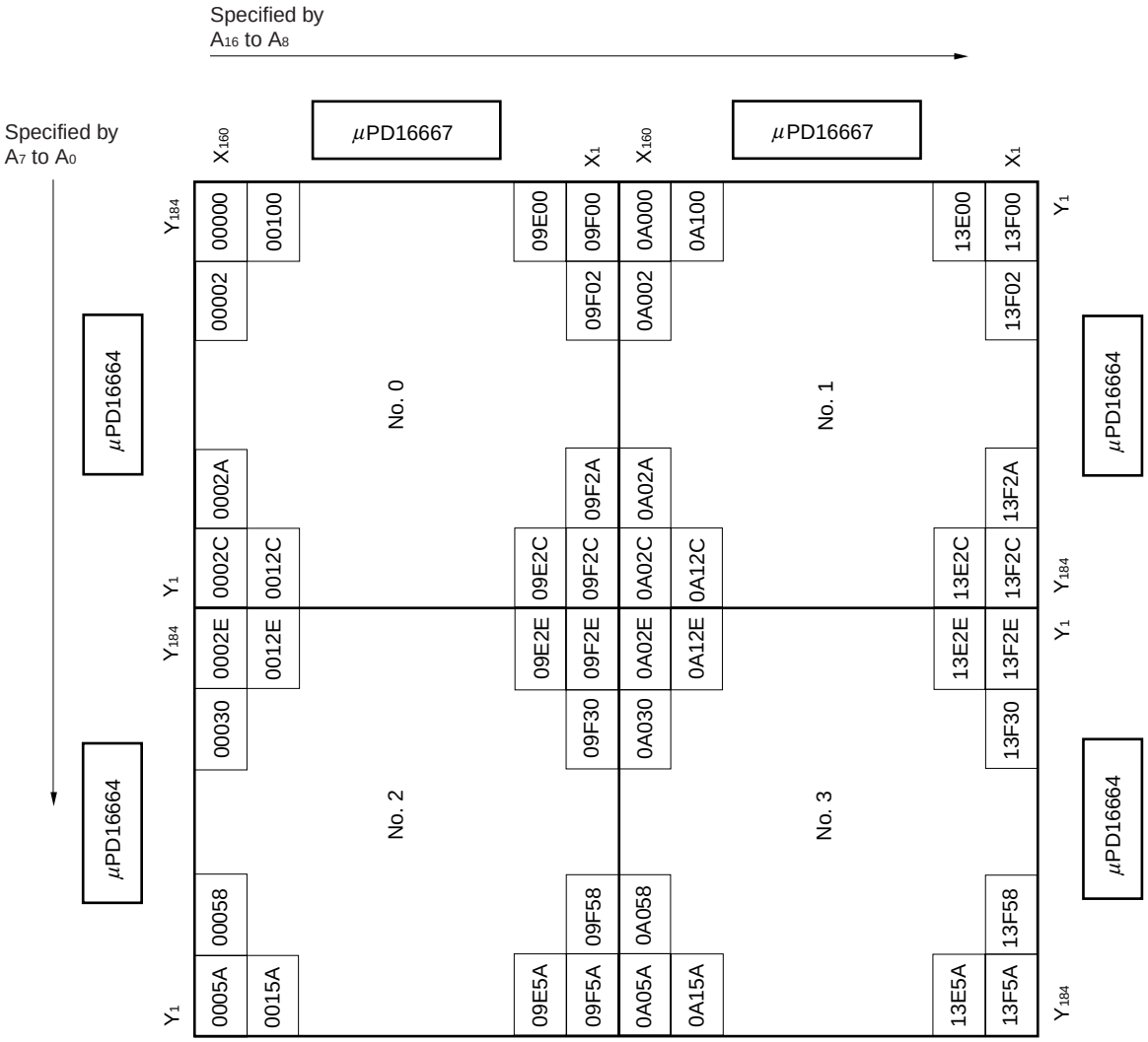
• 144-output Mode



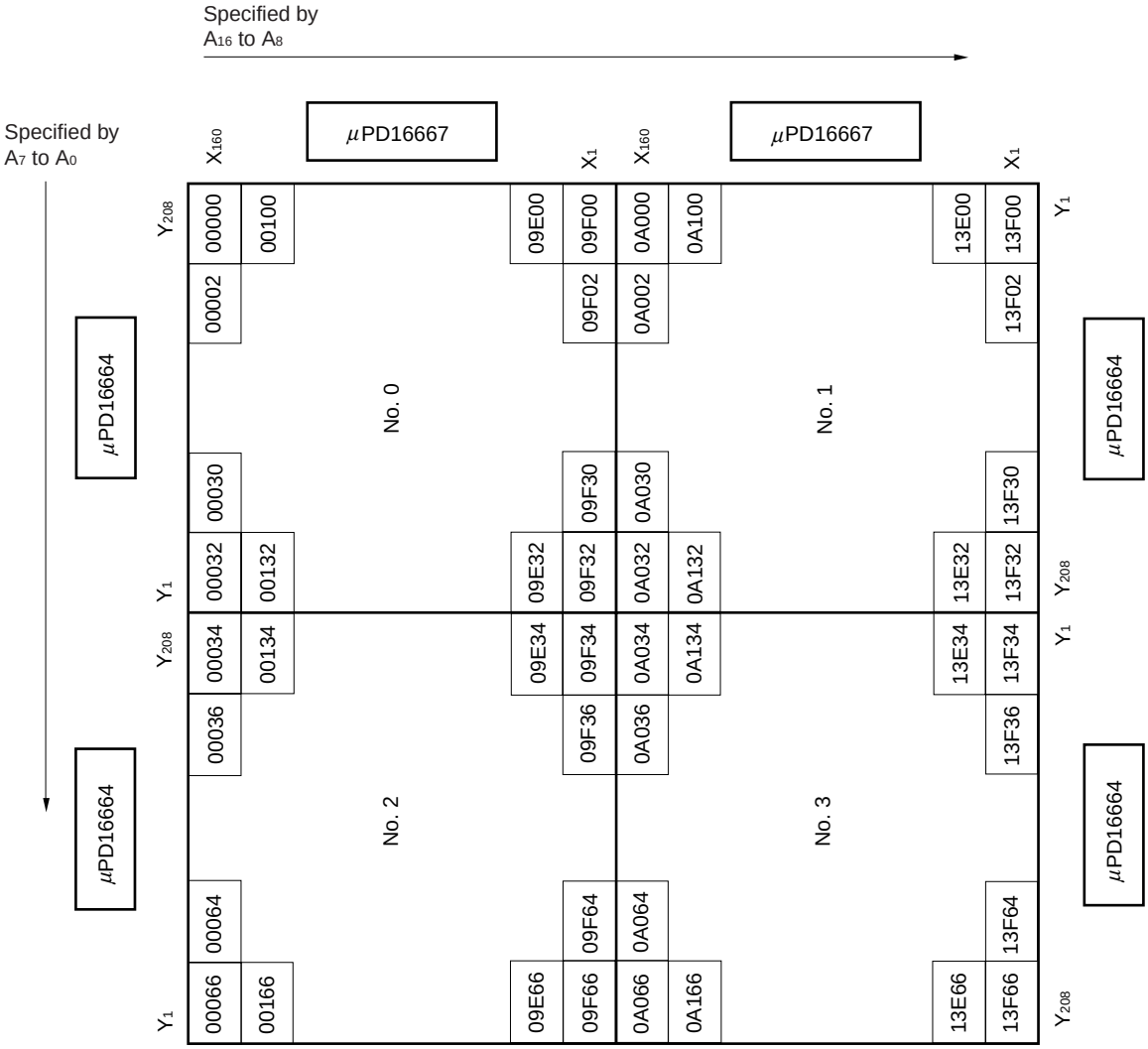
• 160-output Mode



● 184-output Mode

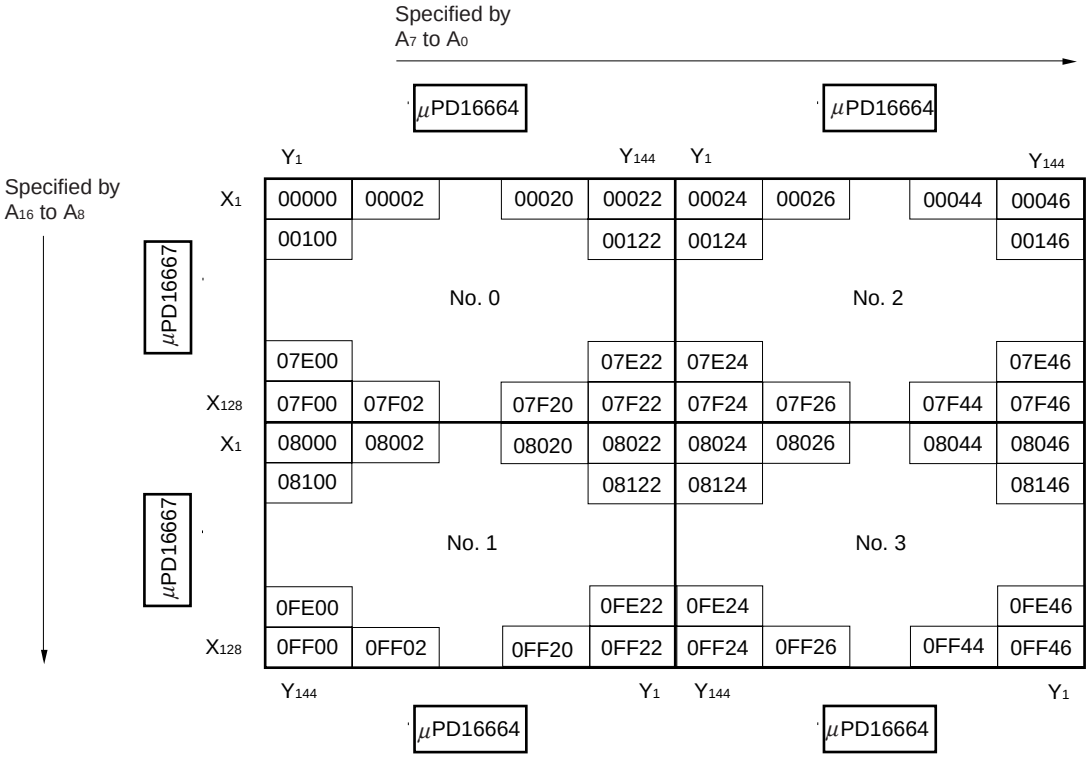


• 208-output Mode

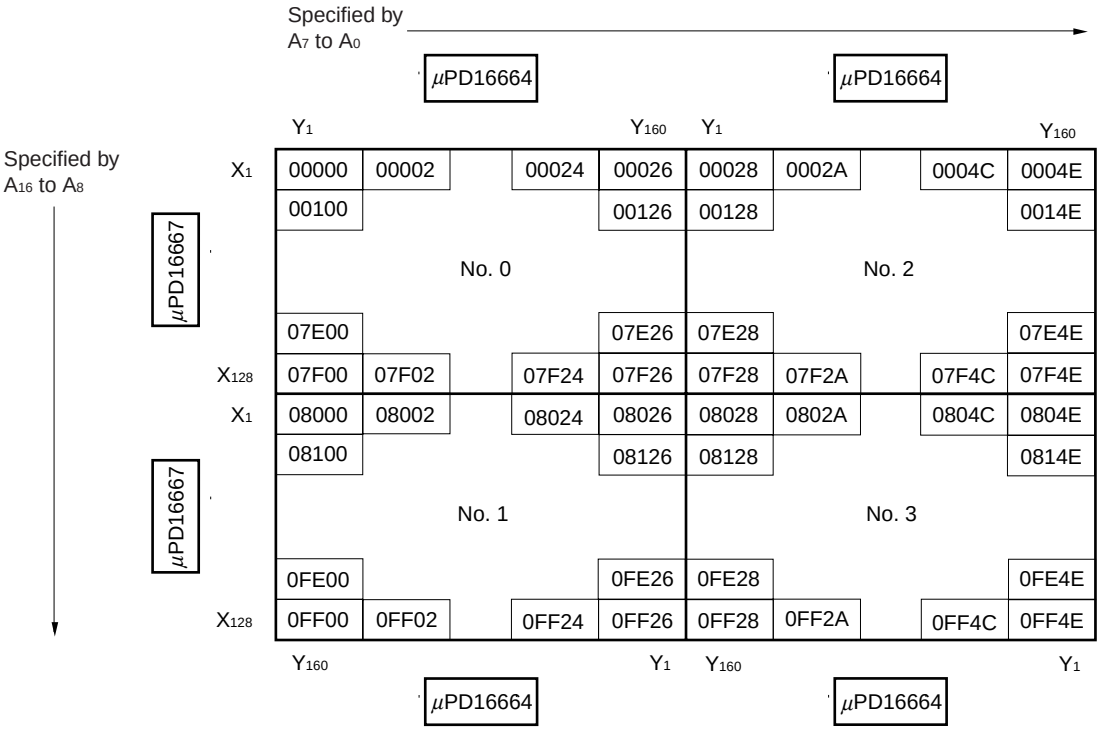


★ **Horizontally Long Address** **DIR = L, DMODE = H**

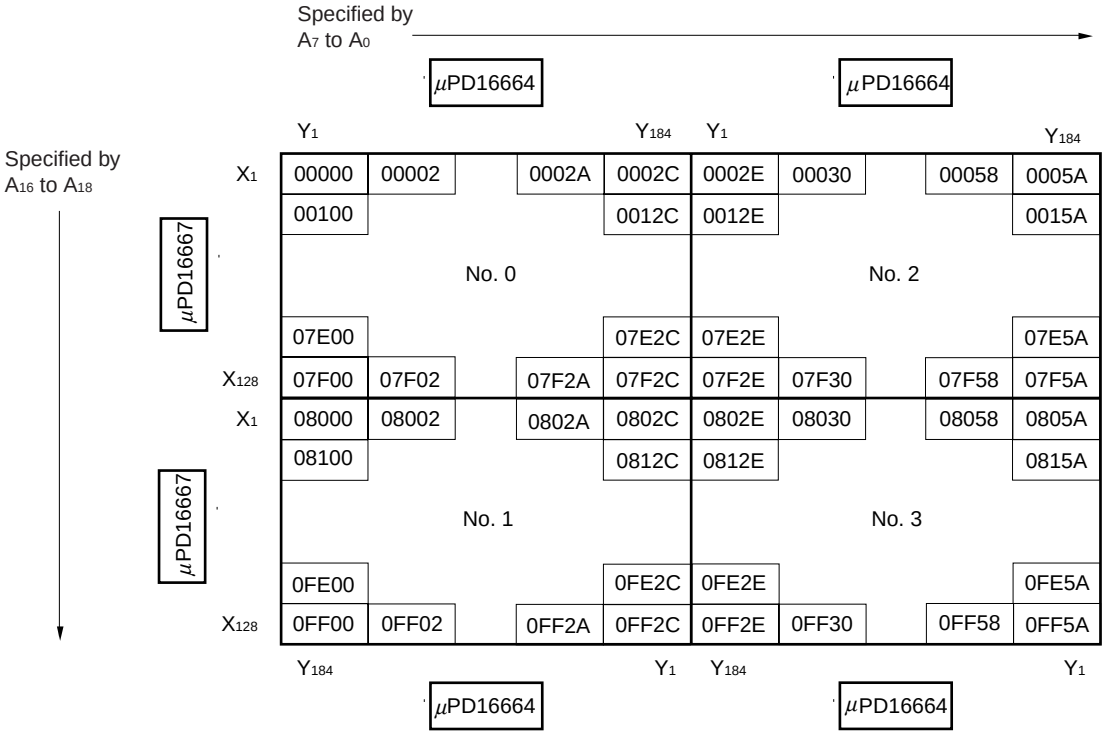
• 144-output Mode



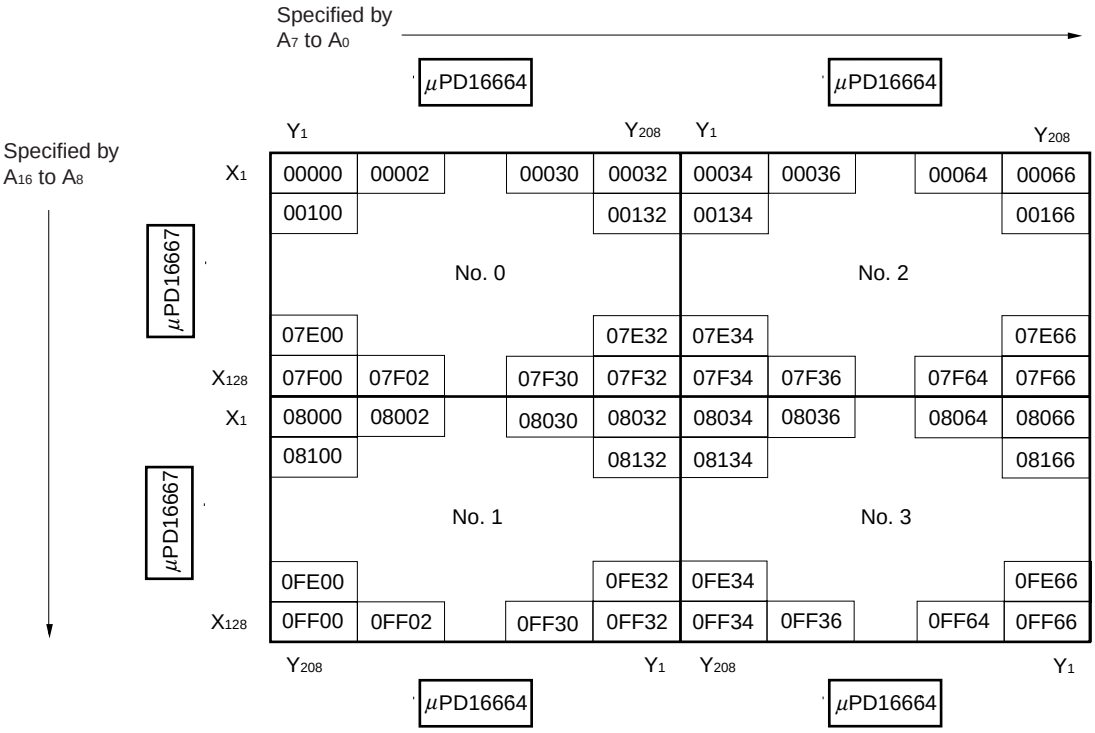
• 160-output Mode



• 184-output Mode

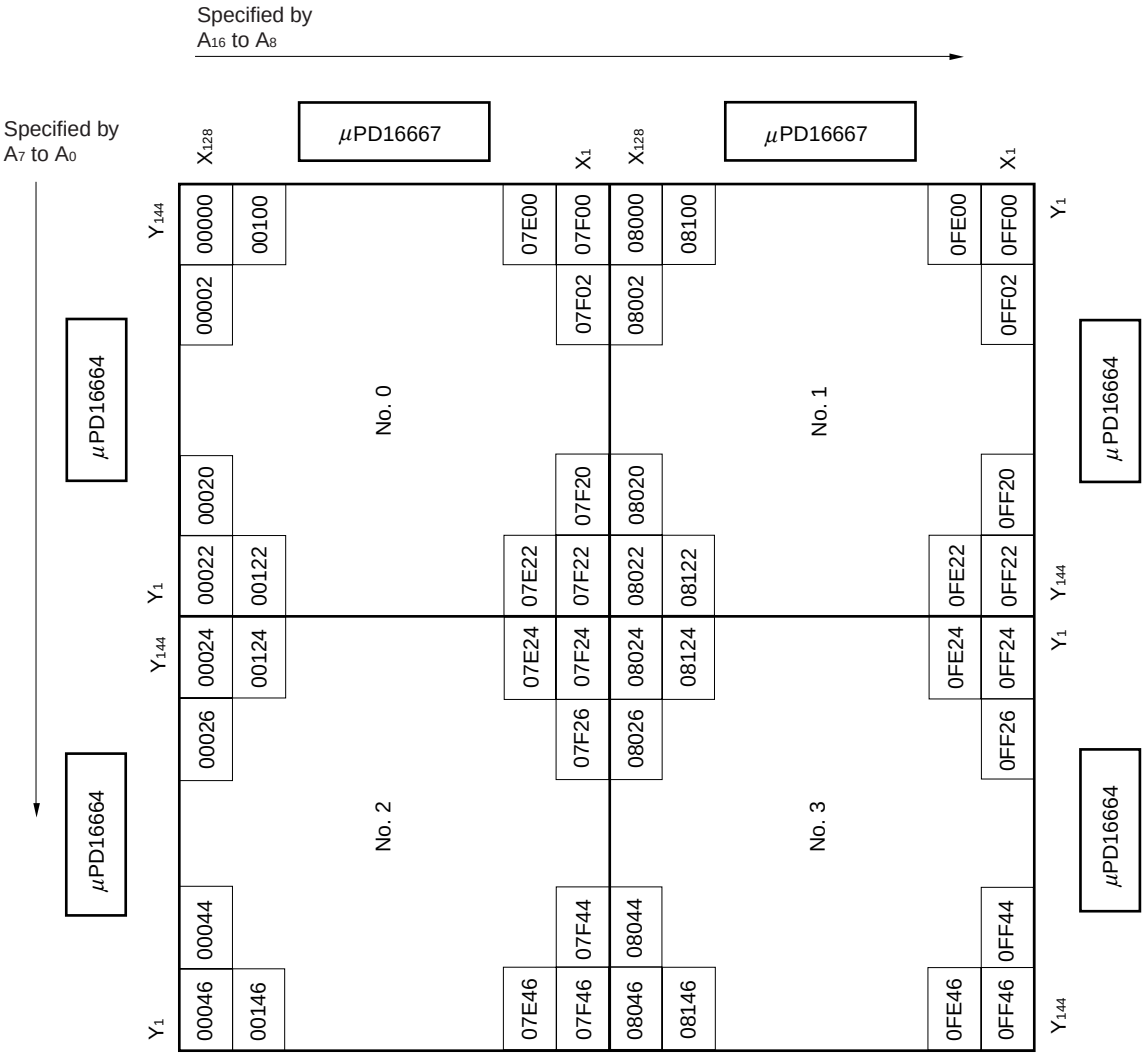


• 208-output Mode

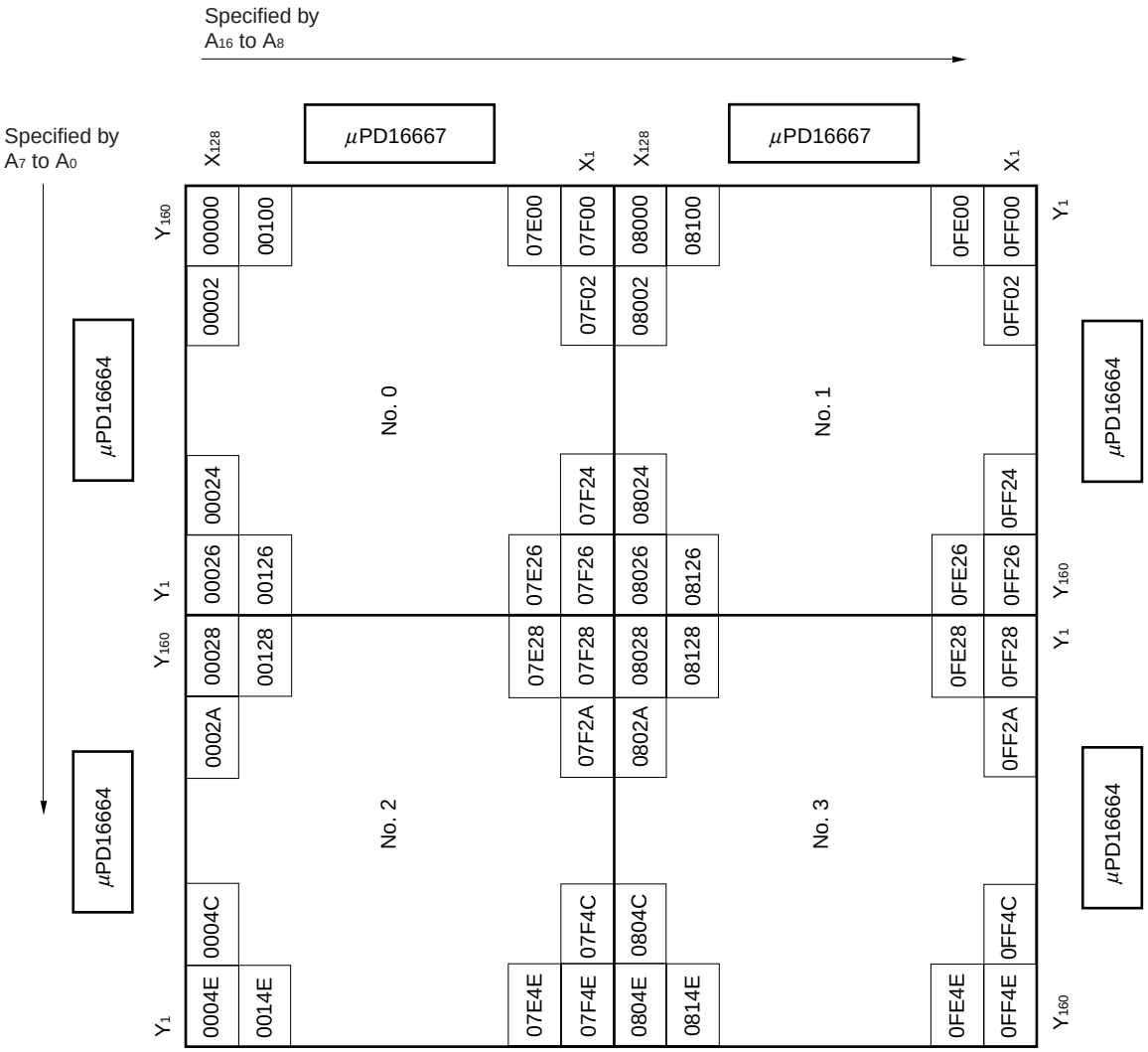


★ **Vertically Long Address** **DIR = H, DMODE = H**

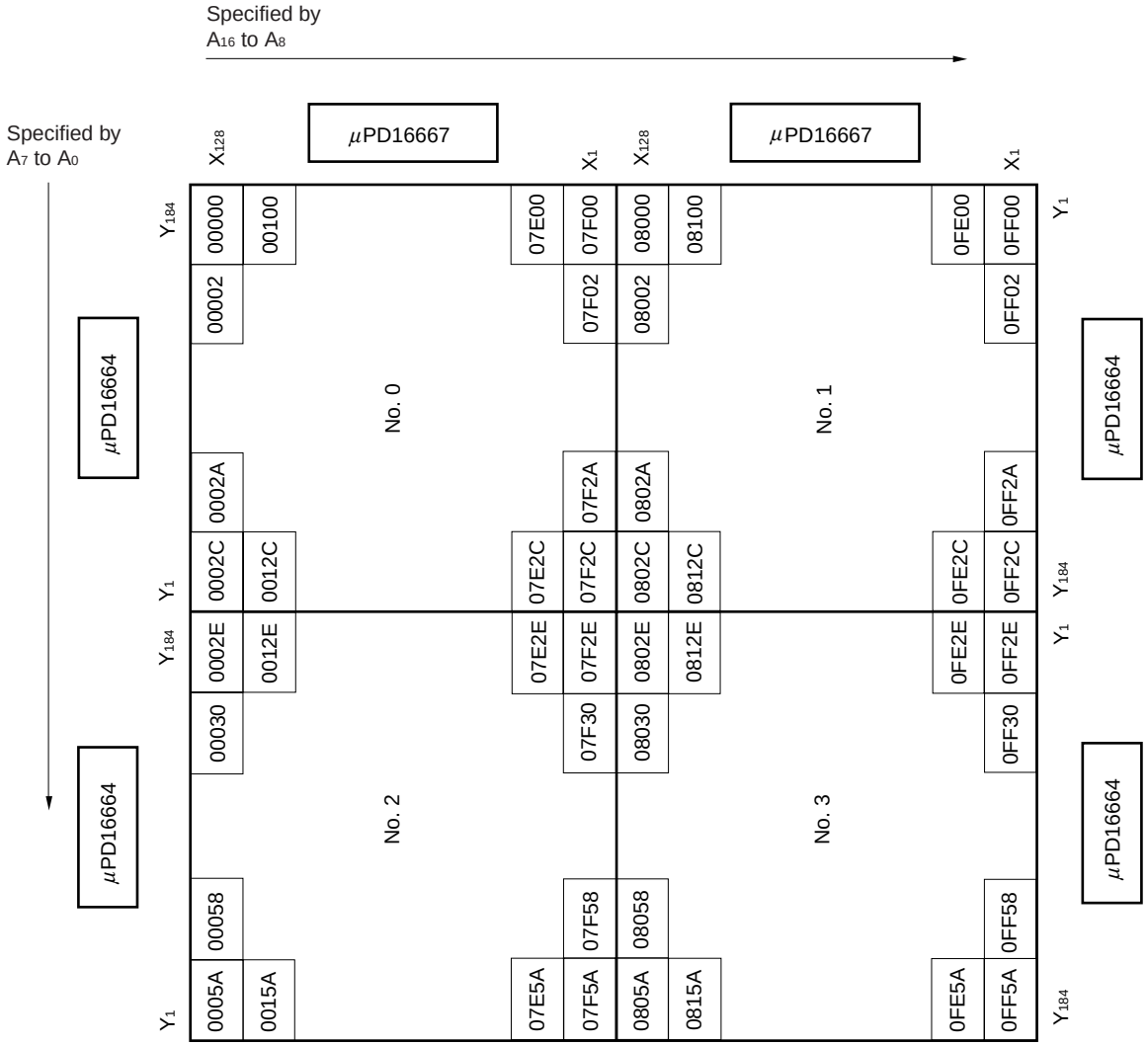
• 144-output Mode



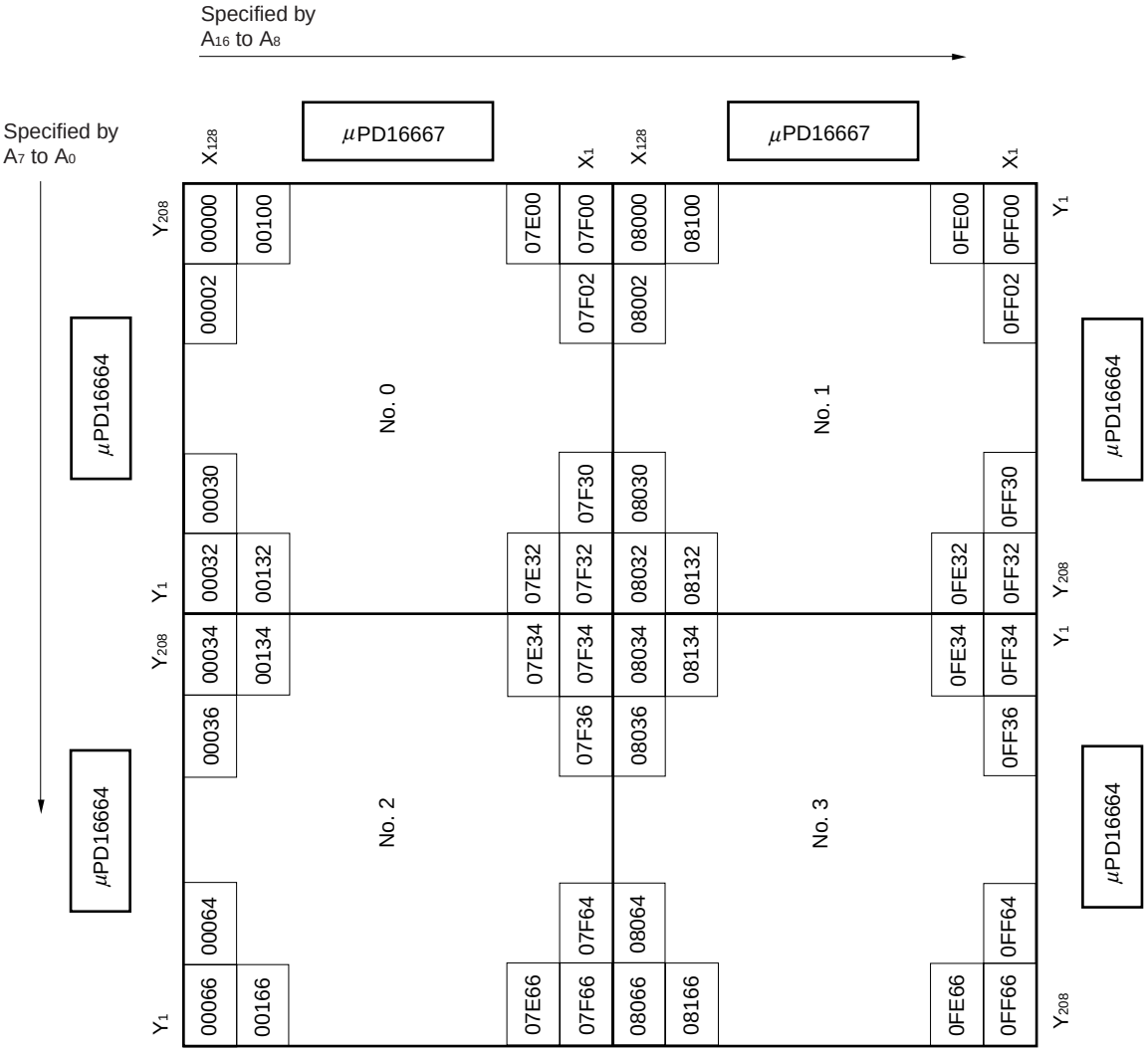
● 160-output Mode



● 184-output Mode



● 208-output Mode

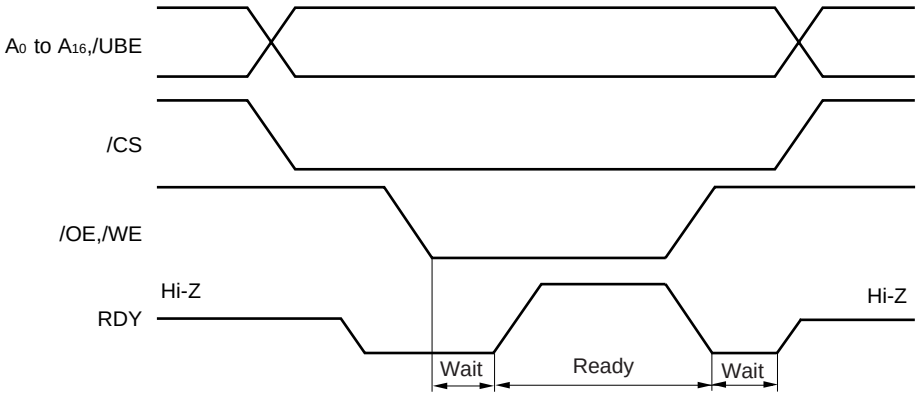


12. CPU INTERFACE

12.1 Function of RDY(ready) Pin

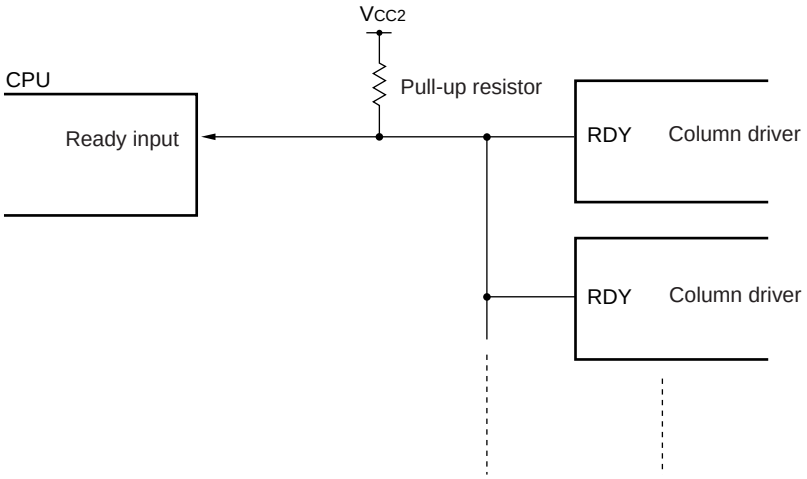
The internal RAM is a single-port RAM. The CPU is kept waiting so that access from the CPU does not conflict with reading by the driver.

(1) Timing



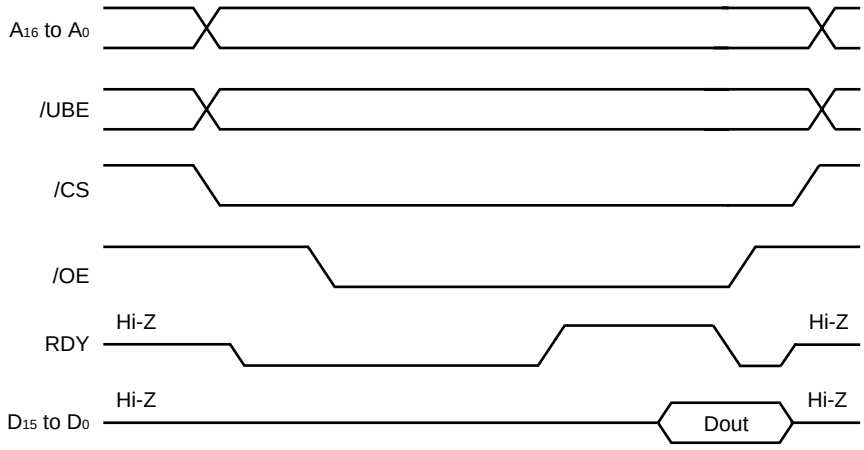
(2) Connection of RDY pin

The RDY pin uses a three-state buffer. The RDY pin should be connected to an external pull-up resistor. If more than one LSI are used, the RDY pins of each LSI are wired together.

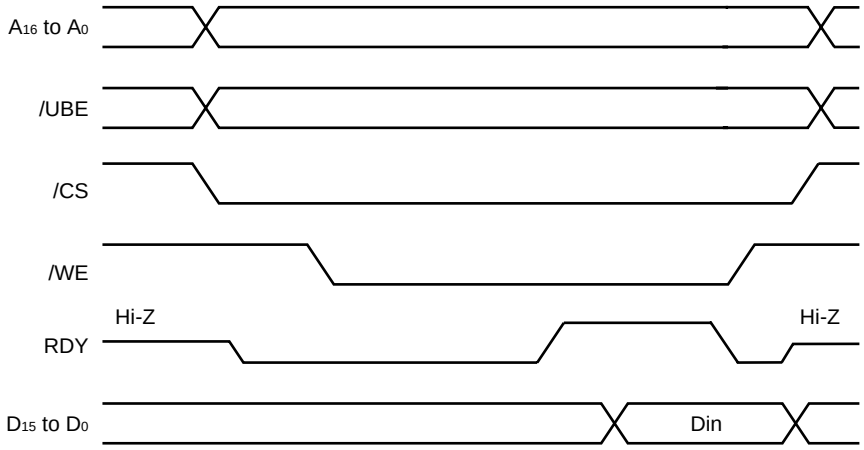


12.2 Access Timing

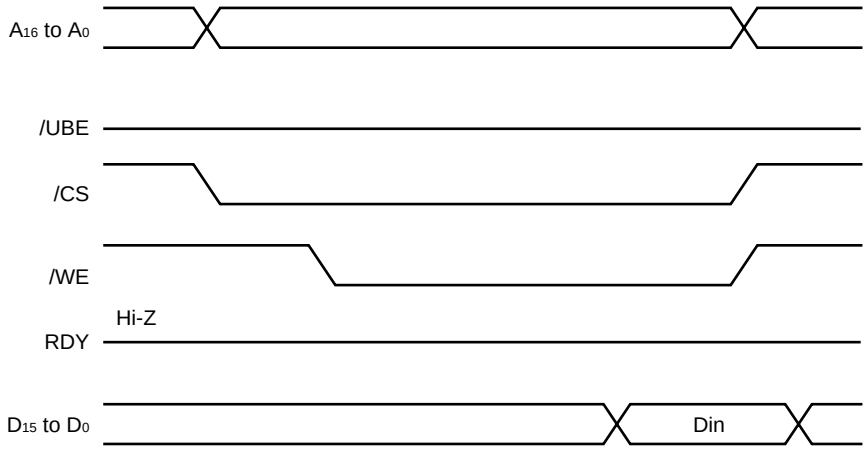
(1) Display data read timing



(2) Display data write timing



(3) Gray level palette data write timing



13. INITIALIZATIONAL FUNCTION

The μPD16664 has two types of initialization functions.

13.1 Initialization by /RESET

/RESET is the pin that is used to forcibly initialize the internal status of the IC from outside the IC. In the case of /RESET = L, the internal status of IC is as follows:

- Oscillator stopped.
- Liquid crystal timing generation circuit initialized.
- Internal timing generation circuit initialized.
- Self-diagnostic circuit initialized.

At power-on, be sure to perform initialization using /RESET.

13.2 Initialization by /REFRH

/REFRH is the pin that is used when the internal self-diagnostic circuit initializes the internal status of IC in cases when the timing of the column drivers deviate due to external noise, etc.

In the case of /REFRH = L, the internal status of IC is as follows:

- Oscillator stopped.
- Liquid crystal timing generation circuit initialized.
- Internal timing generation circuit initialized.

14. DISPLAY-OFF FUNCTION

When /DOFF = L, all column driver outputs Yn become V_1 level, and because the /DOUT output becomes L at the same time, the row driver will be /DOFF' = L and all row driver outputs Xn will also be V_1 level. Therefore, the display is forcibly turned off without regard to the display data. At power-on, be sure to make /DOFF = L until each power supply is stabilized.

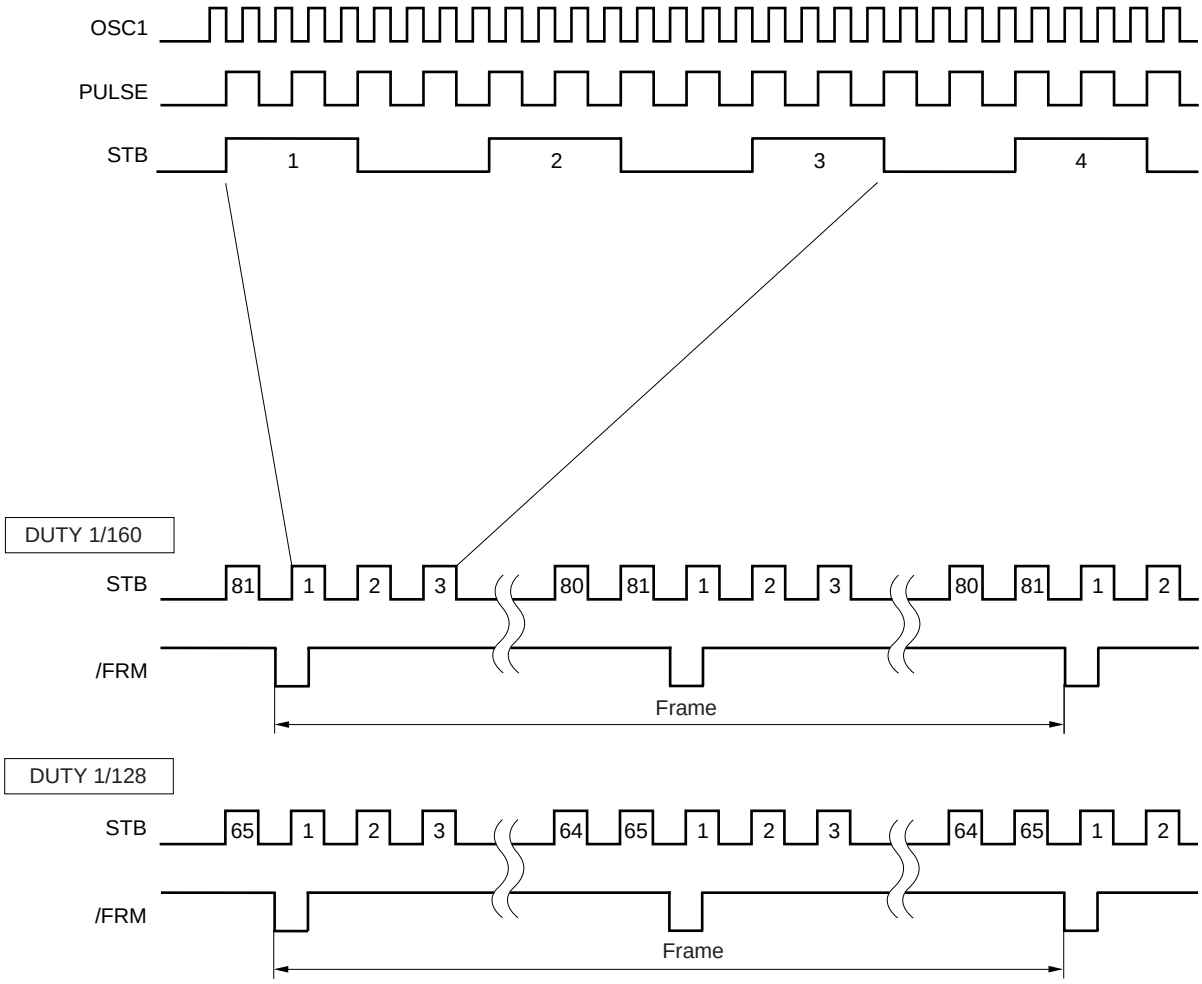
Remark /DOFF' is the input pin of the row driver.

15. LIQUID CRYSTAL TIMING GENERATION CIRCUIT

If the master mode is set by making MS high, /FRM and STB are generated at timing with a duty factor (1/128,1/160). Driver drive voltage select signals L1 and L2 are generated for a row driver.

/FRM is generated two times in 1 frame. When a duty rate is 1/160, STB is generated 81 times in 1/2 frame and 162 times in 1 frame. When a duty rate is 1/128, STB is generated 65 times in 1/2 frame and 130 times in 1 frame.

• /FRM and STB Signal Generation



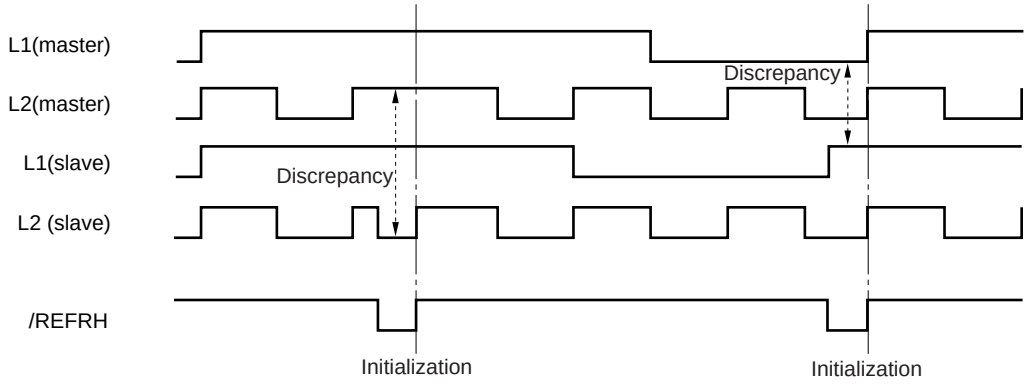
• L1 and L2 Signal Generation

STB	1	2	3	4	…	1	2	3	4	…	1	2	3	4	…	1	2	3	4	…
L1	1	1	1	1	…	1	1	1	1	…	0	0	0	0	…	0	0	0	0	…
L2	1	0	1	0	…	0	1	0	1	…	0	1	0	1	…	1	0	1	0	…

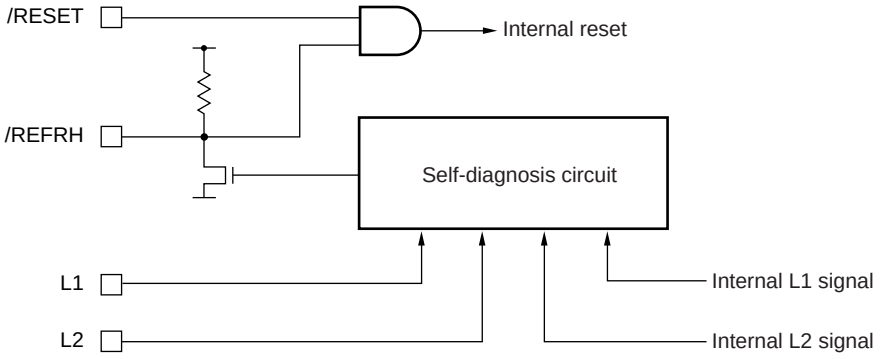
16. SELF-DIAGNOSIS FUNCTION

This function checks whether the timing of each column driver is different from that of the others due to external noise. A slave chip compares internally generated L1 and L2 with L1 and L2 of the master chip. If a discrepancy is found, a refresh signal is transmitted to all column drivers. On reception of the refresh signal, internal reset is effected, and timing is initialized. At this time, the display is turned OFF while /REFRH = L for 4 frame cycles.

Discrepancy between L1 and L2 is monitored at the rising edge of /FRM once in 1/2 frame.



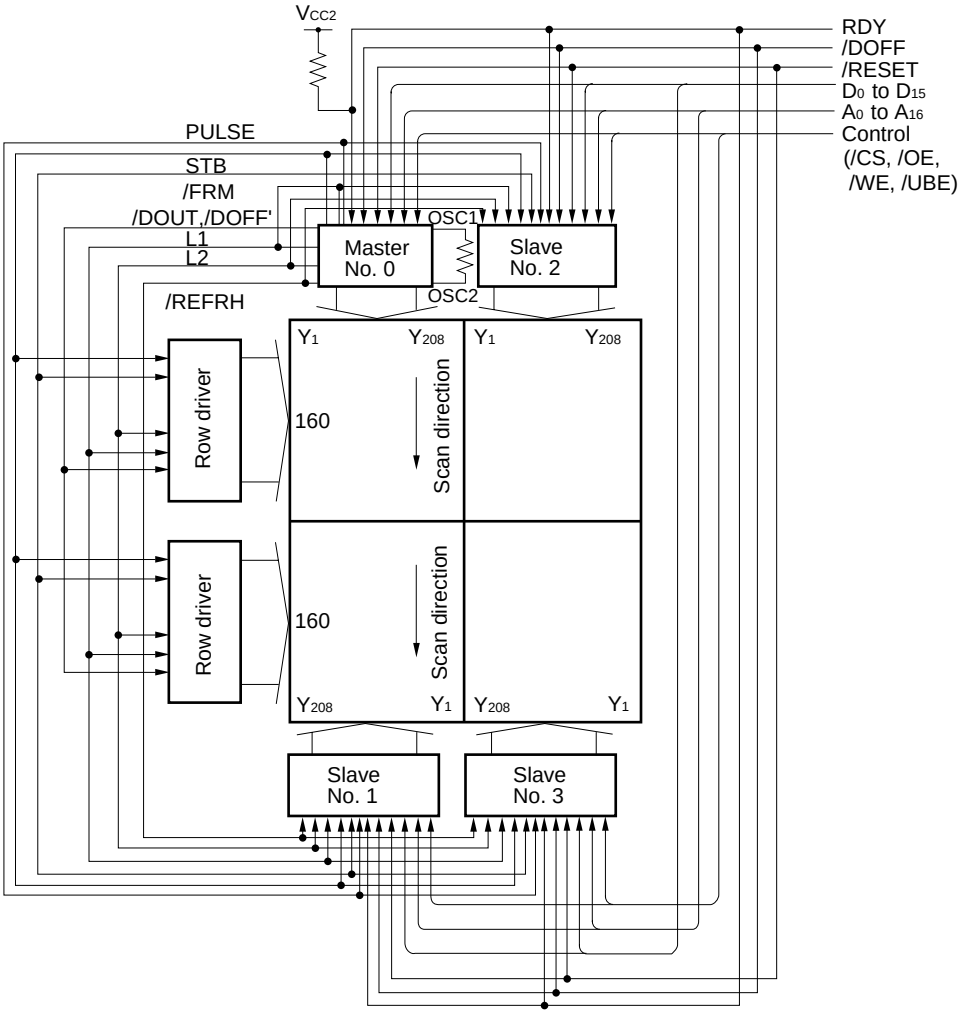
Block Configuration (slave side)



17. SYSTEM CONFIGURATION EXAMPLE

Here is an example using a liquid crystal panel of 416 x 320 pixels, horizontally long by using four μPD16664s and two row drivers.

- The LSI No. of each column driver is set by the PL0 and PL1 pins.
- The DIR pin of each column driver is set to low.
- The CMODE0, CMODE1 and DMODE pins of each column driver are set to low.
- One of the column drivers is set as a master and the others are set as slaves. The master column driver supplies signals to the slave column drivers and row drivers.
- A resistor for oscillation is connected to the OSC1 and OSC2 pins of the master. These pins of the slaves are left open.
- All the signals from the system (D_0 to D_{15}, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, /RESET, and /DOFF) are connected in parallel with the column drivers. A pull-up resistor is connected to the RDY pin.
- The TEST pin is used to test the LSI and is open or connected to GND when the system is constructed.

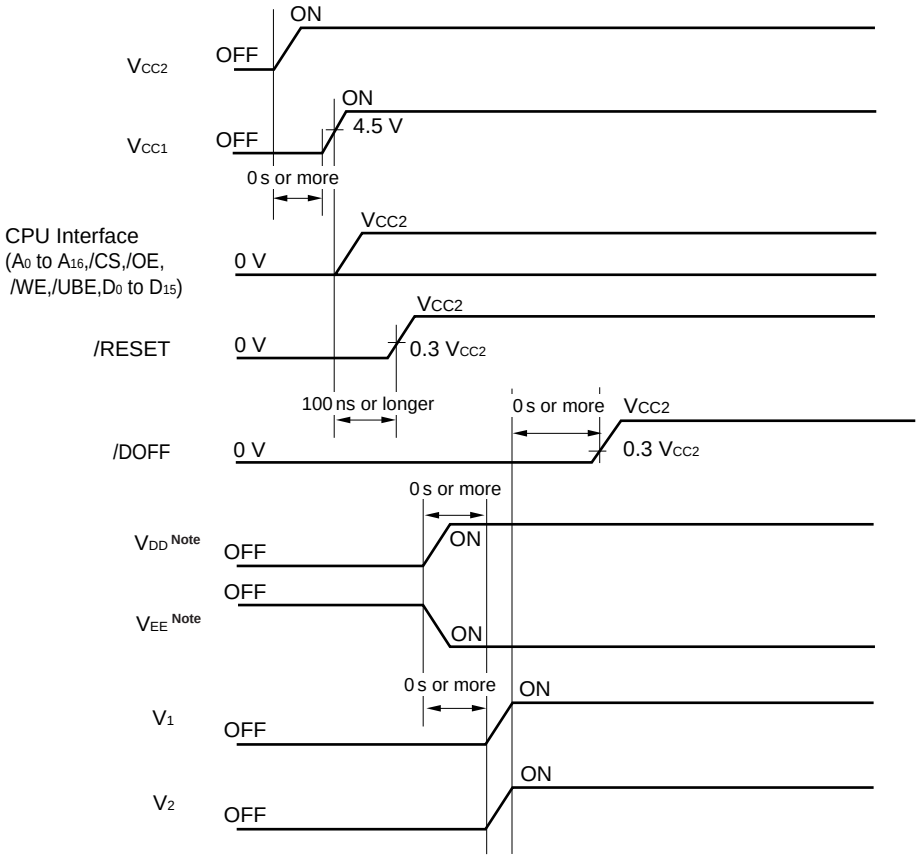


18. CHIP SET POWER-UP SEQUENCE

It is recommended to apply power in the following sequence:

$V_{CC2} \rightarrow V_{CC1} \rightarrow$ input $\rightarrow V_{DD}, V_{EE} \rightarrow V_1, V_2$

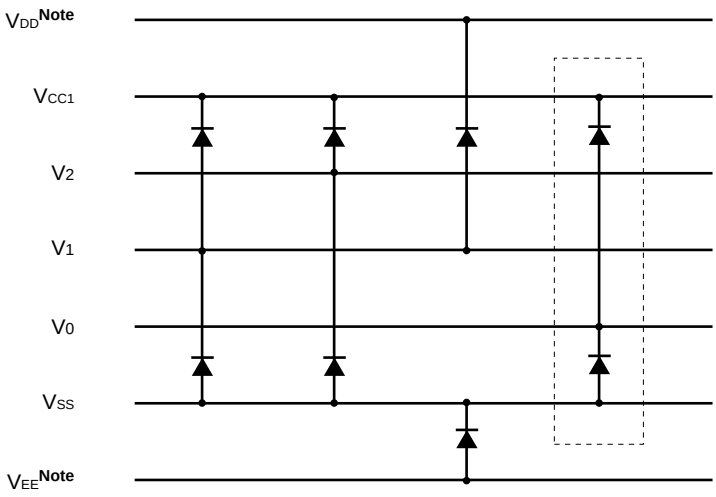
Be sure to apply LCD drive voltages V_1, V_2 in the end.



Note V_{DD} and V_{EE} do not have to be turned ON at the same time.

Caution Turn OFF power to the chip set in the sequence reverse to the above.

19. EXAMPLE OF CONNECTING OF INTERNAL SCHOTTKY BARRIER DIODE OF MODULE TO REINFORCE POWER SUPPLY PROTECTION



Diodes enclosed in a dotted line in the above figure must be connected when V_0 is other than 0 V (GND).

Note V_{DD} and V_{EE} are LCD power supply lines of row driver.

Remark Use schottky barrier diodes with V_f = 0.5 V or less.

20. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage (1) Note1	V_{CC1}	–0.5 to +6.5	V
Supply voltage (2) Note2	V_{CC2}	–0.5 to +4.5	V
Input/output voltage (1) Note1	$V_{I/O1}$	–0.5 to V_{CC1} + 0.5	V
Input/output voltage (2) Note2	$V_{I/O2}$	–0.5 to V_{CC2} + 0.5	V
Input/output voltage (3) Note3	$V_{I/O3}$	–0.5 to V_{CC1} + 0.5	V
Operating ambient temperature	T_A	–20 to +70	°C
Storage temperature	T_{stg}	–40 to +125	°C

Notes 1. V_{CC1} signals (/FRM, STB, /DOUT, L1, L2, PULSE)

2. V_{CC2} signals (MS, DIR, PL0 and PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, OSC1, OSC2, /DOFF, TEST, BMODE, /REFRH, CMODE0, CMODE1, DMODE)

3. Liquid crystal power (V_0, V_1, V_2, Y_1 to Y_{208})

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Conditions (T_A = –20 to +70°C, V_0 = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage (1)	V_{CC1}	4.5	5.0	5.5	V
Supply voltage (2)	V_{CC2}	2.4		3.6	V
Input voltage (1) Note1	V_{I1}	0		V_{CC1}	V
Input voltage (2) Note2	V_{I2}	0		V_{CC2}	V
V_1 input voltage	V_1	V_0		V_2	V
V_2 input voltage	V_2	V_1		V_{CC1}	V
External resistor for OSC	R_{OSC}	75		270	kΩ

Notes 1. V_{CC1} signals (/FRM, STB, L1, L2, PULSE)

2. V_{CC2} signals (MS, DIR, PL0 and PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, OSC1, OSC2, /DOFF, TEST, BMODE, /REFRH, CMODE0, CMODE1, DMODE)

DC Characteristics (Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70°C)

○V_{CC2} = 3.0 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage (1), V_{CC1} Note1	V_{IH1}		0.7 V_{CC1}			V
Low-level input voltage (1), V_{CC1} Note1	V_{IL1}				0.3 V_{CC1}	V
High-level input voltage (2), V_{CC2} Note2	V_{IH2}		0.7 V_{CC2}			V
Low-level input voltage (2), V_{CC2} Note2	V_{IL2}				0.3 V_{CC2}	V
High-level input voltage (2), V_{CC2} Note3	V_{IH3}		0.8 V_{CC2}			V
Low-level input voltage (2), V_{CC2} Note3	V_{IL3}				0.2 V_{CC2}	V
High-level output voltage (1), V_{CC1} Note4	V_{OH1}	I_{OH} = –1 mA	V_{CC1} – 0.4			V
Low-level output voltage (1), V_{CC1} Note4	V_{OL1}	I_{OL} = 2 mA			0.4	V
High-level output voltage (2), V_{CC1} Note1	V_{OH2}	I_{OH} = –2 mA	V_{CC1} – 0.4			V
Low-level output voltage (2), V_{CC1} Note1,3	V_{OL2}	I_{OL} = 4 mA			0.4	V
High-level output voltage (3), V_{CC2} Note5	V_{OH3}	I_{OH} = –1 mA	V_{CC2} – 0.4			V
Low-level output voltage (3), V_{CC2} Note5	V_{OL3}	I_{OL} = 2 mA			0.4	V
Input leakage current (1)	I_{I1}	Other than TEST pin, V_1 = V_{CC2} or GND			±10	μA
Input leakage current (2)	I_{I2}	Pull down (TEST pin), V_1 = V_{CC2}	10	40	100	μA
★ Display operating current consumption (1) Note6	I_{MAS1}	Master, V_{CC1}			80	μA
★ Display operating current consumption (2) Note6	I_{MAS2}	Master, V_{CC2}			200	μA
★ Display operating current consumption (3) Note6	I_{SLV1}	Slave, V_{CC1}			50	μA
★ Display operating current consumption (4) Note6	I_{SLV2}	Slave, V_{CC2}			130	μA
Liquid crystal driver output ON resistance Note7	R_{ON}			1	2	kΩ

Notes 1. V_{CC1} signal (/FRM, STB, L1, L2, PULSE)

2. V_{CC2} signal (MS, DIR, PL0 and PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, /DOFF, TEST, BMODE, CMODE0, CMODE1, DMODE)

3. /REFRH pin

4. /DOUT pin

5. D_0 to D_{15}, RDY, OSC2 pins

6. Frame frequency: 70 Hz, output: no load, not accessed by CPU
(D_0 to D_{15}, A_0 to A_{16}, /UBE = GND, /CS, /OE, /WE = V_{CC2})

7. Resistance between Y and V pins (any of V_0, V_1, and V_2) when a load current (I_{ON} = 100 μA) flows through one pin of Y_1 to Y_{208}.

○ V_{CC2} = 2.4 to 3.0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage (1), V_{CC1} Note1	V_{IH1}		0.7 V_{CC1}			V
Low-level input voltage (1), V_{CC1} Note1	V_{IL1}				0.3 V_{CC1}	V
High-level input voltage (2), V_{CC2} Note2	V_{IH2}		0.7 V_{CC2}			V
Low-level input voltage (2), V_{CC2} Note2	V_{IL2}				0.3 V_{CC2}	V
High-level input voltage (2), V_{CC2} Note3	V_{IH3}		0.8 V_{CC2}			V
Low-level input voltage (2), V_{CC2} Note3	V_{IL3}				0.2 V_{CC2}	V
High-level output voltage (1), V_{CC1} Note4	V_{OH1}	I_{OH} = –1 mA	V_{CC1} – 0.4			V
Low-level output voltage (1), V_{CC1} Note4	V_{OL1}	I_{OL} = 2 mA			0.4	V
High-level output voltage (2), V_{CC1} Note1	V_{OH2}	I_{OH} = –2 mA	V_{CC1} – 0.4			V
Low-level output voltage (2), V_{CC1} Note1,3	V_{OL2}	I_{OL} = 4 mA			0.4	V
High-level output voltage (3), V_{CC2} Note5	V_{OH3}	I_{OH} = –1 mA	V_{CC2} – 0.4			V
Low-level output voltage (3), V_{CC2} Note5	V_{OL3}	I_{OL} = 2 mA			0.4	V
Input leakage current (1)	I_{I1}	Other than TEST pin, V_I = V_{CC2} or GND			±10	μA
Input leakage current (2)	I_{I2}	Pull down (TEST pin), V_I = V_{CC2}	10	40	100	μA
★ Display operating current consumption (1) Note6	I_{MAS1}	Master, V_{CC1}			100	μA
★ Display operating current consumption (2) Note6	I_{MAS2}	Master, V_{CC2}			150	μA
★ Display operating current consumption (3) Note6	I_{SLV1}	Slave, V_{CC1}			60	μA
★ Display operating current consumption (4) Note6	I_{SLV2}	Slave, V_{CC2}			100	μA
Liquid crystal driver output ON resistance Note7	R_{ON}			1.2	2.4	kΩ

Notes 1. V_{CC1} signal (/FRM, STB, L1, L2, PULSE)

2. V_{CC2} signal (MS, DIR, PL0 and PL1, A_0 to A_{16}, /CS, /OE, /WE, /UBE, RDY, D_0 to D_{15}, /RESET, /DOFF, TEST, BMODE, CMODE0, CMODE1, DMODE)

3. /REFRH pin

4. /DOUT pin

5. D_0 to D_{15}, RDY, OSC2 pins

6. Frame frequency: 70 Hz, output: no load, not accessed by CPU (D_0 to D_{15}, A_0 to A_{16}, /UBE = GND, /CS, /OE, /WE = V_{CC2})

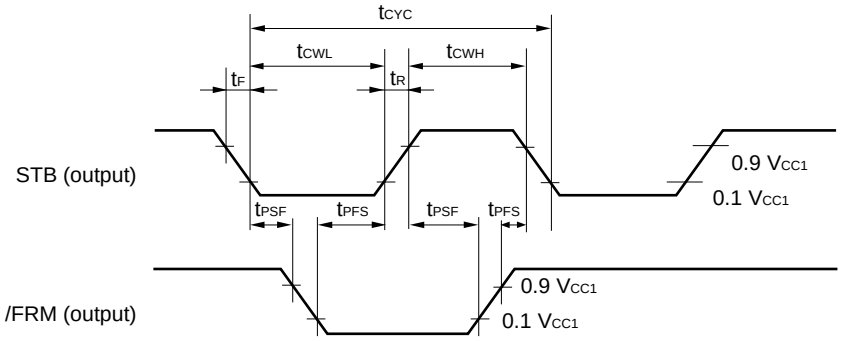
7. Resistance between Y and V pins (any of V_0, V_1, and V_2) when a load current (I_{ON} = 100 μA) flows through one pin of Y_1 to Y_{208}.

AC Characteristics 1 Display Data Transfer Timing

(1) Master Mode

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 2.4 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70°C, frame frequency: 70 Hz (f_{OSC} = 90.72 kHz at 1/160 duty, 72.8 kHz at 1/128 duty), output load: 100 pF)

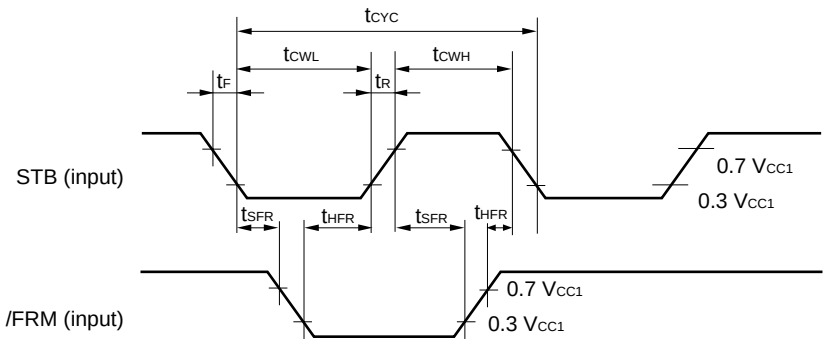
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
STB clock cycle time	t_{CYC}	1/160 duty	87	8/f_{OSC}		μs
		1/128 duty	108	8/f_{OSC}		μs
STB high-level width	t_{CWH}	1/160 duty	43	4/f_{OSC}		μs
		1/128 duty	54	4/f_{OSC}		μs
STB low-level width	t_{CWL}	1/160 duty	43	4/f_{OSC}		μs
		1/128 duty	54	4/f_{OSC}		μs
STB rise time	t_R				100	ns
STB fall time	t_F				100	ns
STB - /FRM delay time	t_{PSF}		20			μs
/FRM - STB delay time	t_{PFS}		20			μs



(2) Slave mode

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 2.4 to 3.6 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
STB clock cycle time	t_{CYC}		10			μs
STB high-level width	t_{CWH}		4			μs
STB low-level width	t_{CWL}		4			μs
STB rise time	t_R				150	ns
STB fall time	t_F				150	ns
/FRM setup time	t_{SFR}		1			μs
/FRM hold time	t_{HFR}		1			μs



(3) Parameters Common to Master/Slave

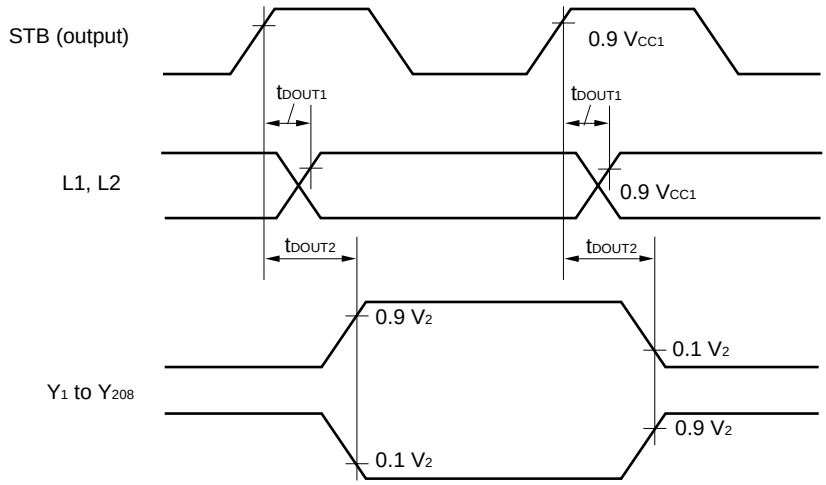
(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70°C)

○V_{CC2} = 3.0 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output delay time (L1, L2)	t_{DOUT1}	No output load		50	100	ns
Output delay time (Y_1 to Y_{208})	t_{DOUT2}	No output load		90	150	ns

○V_{CC2} = 2.4 to 3.0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output delay time (L1, L2)	t_{DOUT1}	No output load			120	ns
Output delay time (Y_1 to Y_{208})	t_{DOUT2}	No output load			180	ns



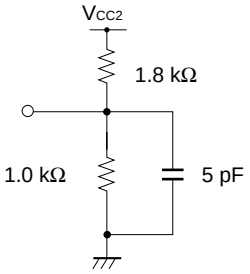
AC Characteristics 2 Drawing Access Timing

(Unless otherwise specified, V_{CC1} = 4.5 to 5.5 V, V_0 = 0 V, V_1 = 1.4 to 2.0 V, V_2 = 2.8 to 4.0 V, T_A = –20 to +70°C, $t_r = t_f$ = 5 ns)

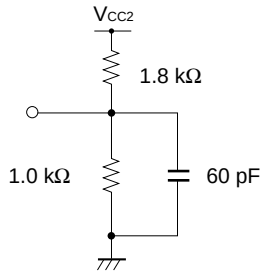
○ V_{CC2} = 3.0 to 3.6 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
/OE,/WE recovery time	t_{RY}		30			ns
Address setup time	t_{AS}		10			ns
Address hold time	t_{AH}		20			ns
RDY output delay time	t_{RYR}	C_L = 15 pF			30	ns
RDY float time Note 1	t_{RYZ}				30	ns
Wait status time Note 2	t_{RYW}				35	ns
Ready status time (without conflict) Note 2	t_{RYF1}			60	100	ns
Ready status time (with conflict) Note 2	t_{RYF2}			650	1200	ns
Data access time (read cycle) Note 3	t_{ACS}				100	ns
Data float time (read cycle) Note 1	t_{HZ}				40	ns
/CS - /OE time (read cycle)	t_{CSOE}		10			ns
/OE - /CS time (read cycle)	t_{OECS}		20			ns
Write pulse width 1 (write cycle 1) Note 2	t_{WP1}		50			ns
Write pulse width 2 (write cycle 2) Note 2	t_{WP2}		50			ns
Data setup time (write cycles 1, 2)	t_{DW}		20			ns
Data hold time (write cycles 1, 2)	t_{DH}		20			ns
/CS - /WE time (write cycles 1, 2)	t_{CSWE}		10			ns
/WE - /CS time (write cycles 1, 2)	t_{WECS}		20			ns
Reset pulse width	t_{WRES}		100			ns
RDY - /OE time	t_{RDOE}				**Note 4**	–
RDY - /WE time	t_{RDWE}				**Note 4**	–

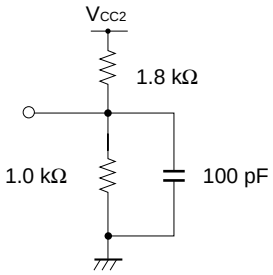
Notes 1. Load circuit



2. Load circuit



3. Load circuit

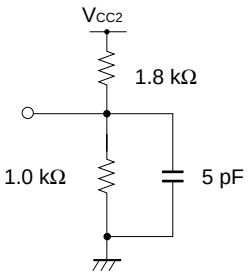


4. The display may be affected if the time from the rising of RDY to /OE or /WE is too long. It is recommended that t_{RDOE} and t_{RDWE} be 1000 ns or less.

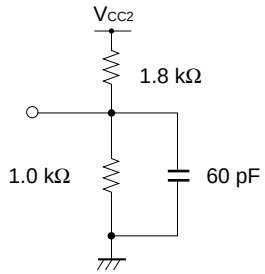
○V_{CC2} = 2.4 to 3.0 V

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
/OE,/WE recovery time	t_{RY}		40			ns
Address setup time	t_{AS}		20			ns
Address hold time	t_{AH}		30			ns
RDY output delay time	t_{RYR}	C_L = 15 pF			40	ns
RDY float time Note 1	t_{RYZ}				40	ns
Wait status time Note 2	t_{RYW}				50	ns
Ready status time (without conflict) Note 2	t_{RYF1}				120	ns
Ready status time (with conflict) Note 2	t_{RYF2}				1600	ns
Data access time (read cycle) Note 3	t_{ACS}				120	ns
Data float time (read cycle) Note 1	t_{HZ}				50	ns
/CS - /OE time (read cycle)	t_{CSOE}		20			ns
/OE - /CS time (read cycle)	t_{OECS}		30			ns
Write pulse width 1 (write cycle 1) Note 2	t_{WP1}		60			ns
Write pulse width 2 (write cycle 2) Note 2	t_{WP2}		60			ns
Data setup time (write cycles 1, 2)	t_{DW}		30			ns
Data hold time (write cycles 1, 2)	t_{DH}		30			ns
/CS - /WE time (write cycles 1, 2)	t_{CSWE}		20			ns
/WE - /CS time (write cycles 1, 2)	t_{WECS}		30			ns
Reset pulse width	t_{WRES}		120			ns
RDY - /OE time	t_{RDOE}				**Note 4**	–
RDY - /WE time	t_{RDWE}				**Note 4**	–

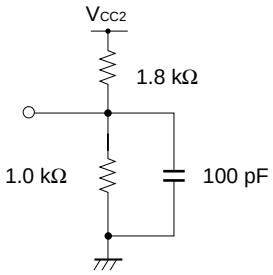
Notes 1. Load circuit



2. Load circuit

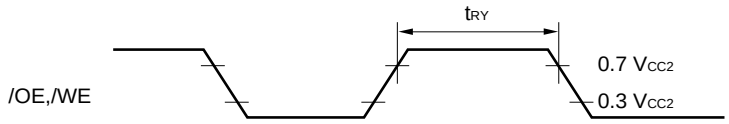


3. Load circuit

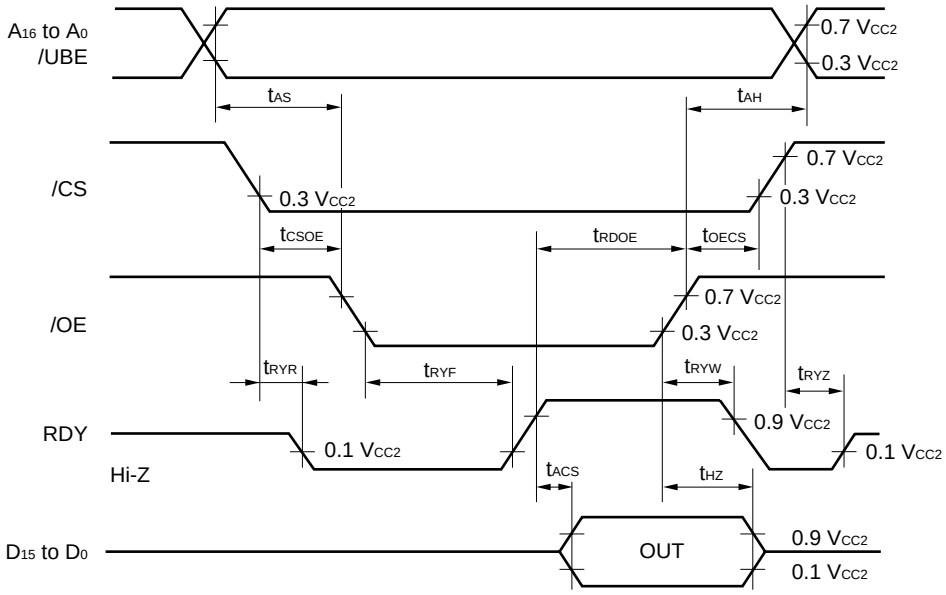


4. The display may be affected if the time from the rising of RDY to /OE or /WE is too long. It is recommended that t_{RDOE} and t_{RDWE} be 1000 ns or less.

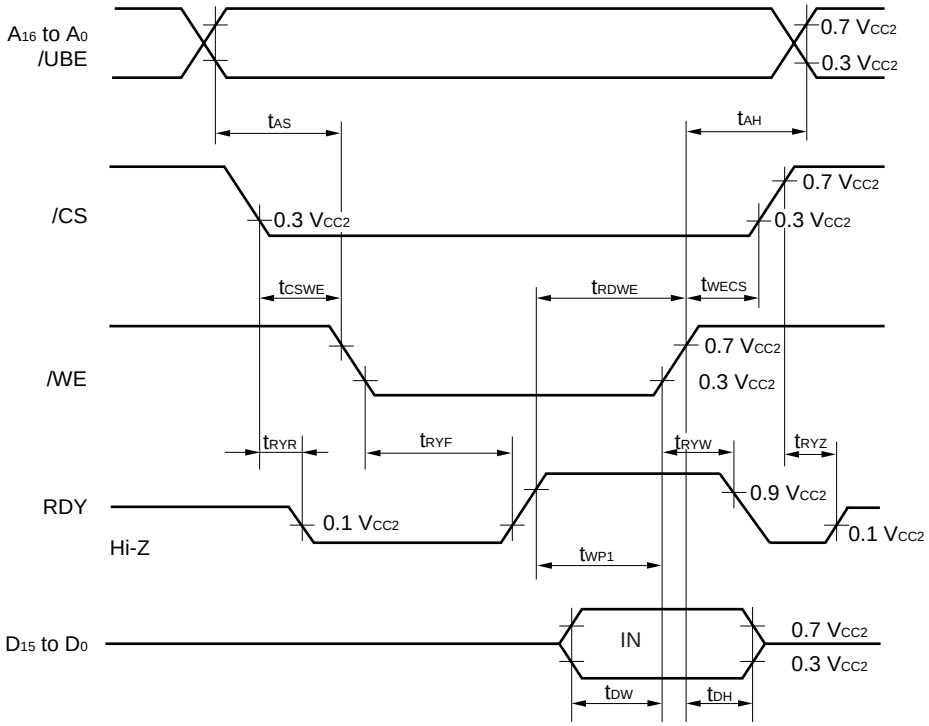
/OE,/WE Recovery Time



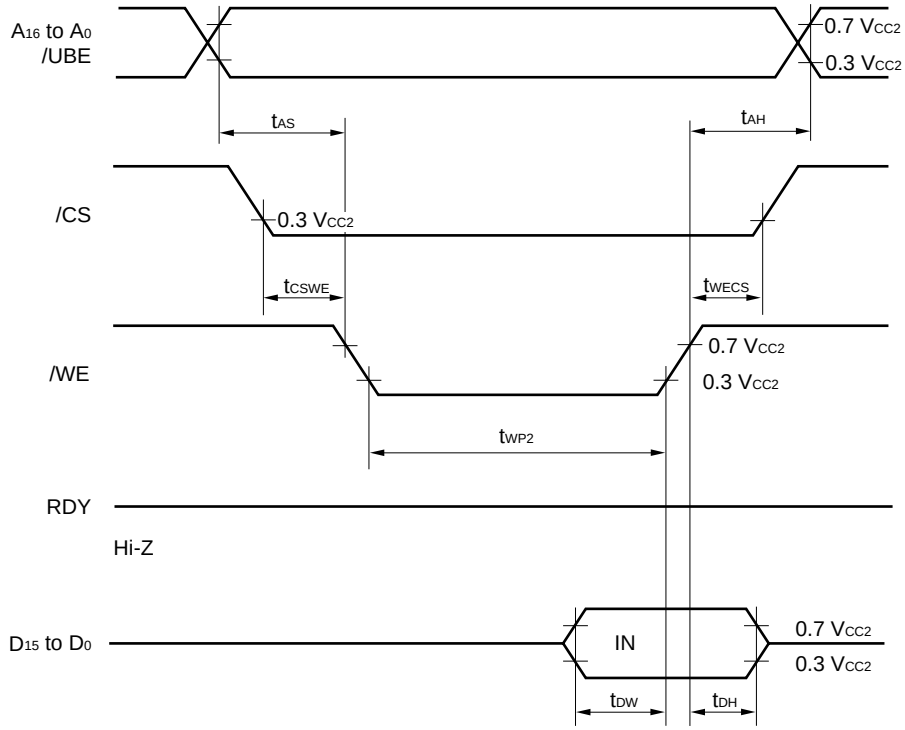
Read Cycle



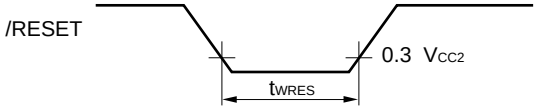
Write Cycle 1 (on writing display data)



Write Cycle 2 (on writing gray level palette)



Reset Pulse Width



AC Characteristics 3 CR Oscillation

○V_{CC2} = 2.4 to 3.6 V, T_A = –20 to +70 °C, 1/160 duty

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	External resistor: 130 kΩ	80	95	110	kHz
Frame frequency	–	External resistor: 130 kΩ	61.7	73.3	84.9	Hz

○V_{CC2} = 2.4 to 3.6 V, T_A = –20 to +70 °C, 1/128 duty

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Oscillation frequency	f_{OSC}	External resistor: 160 kΩ	64	76	88	kHz
★ Frame frequency	–	External resistor: 160 kΩ	61.5	73.1	84.6	Hz

21. RELATION BETWEEN OSCILLATION FREQUENCY, FRAME FREQUENCY, AND STB FREQUENCY

The relation between the oscillation frequency, frame frequency, and STB frequency is as follows:

1/160 duty

$$\text{Frame frequency} = \frac{1}{162 \times 2 \times 4} \times \text{Oscillation frequency}$$

$$\text{STB frequency} = \frac{1}{2 \times 4} \times \text{Oscillation frequency}$$

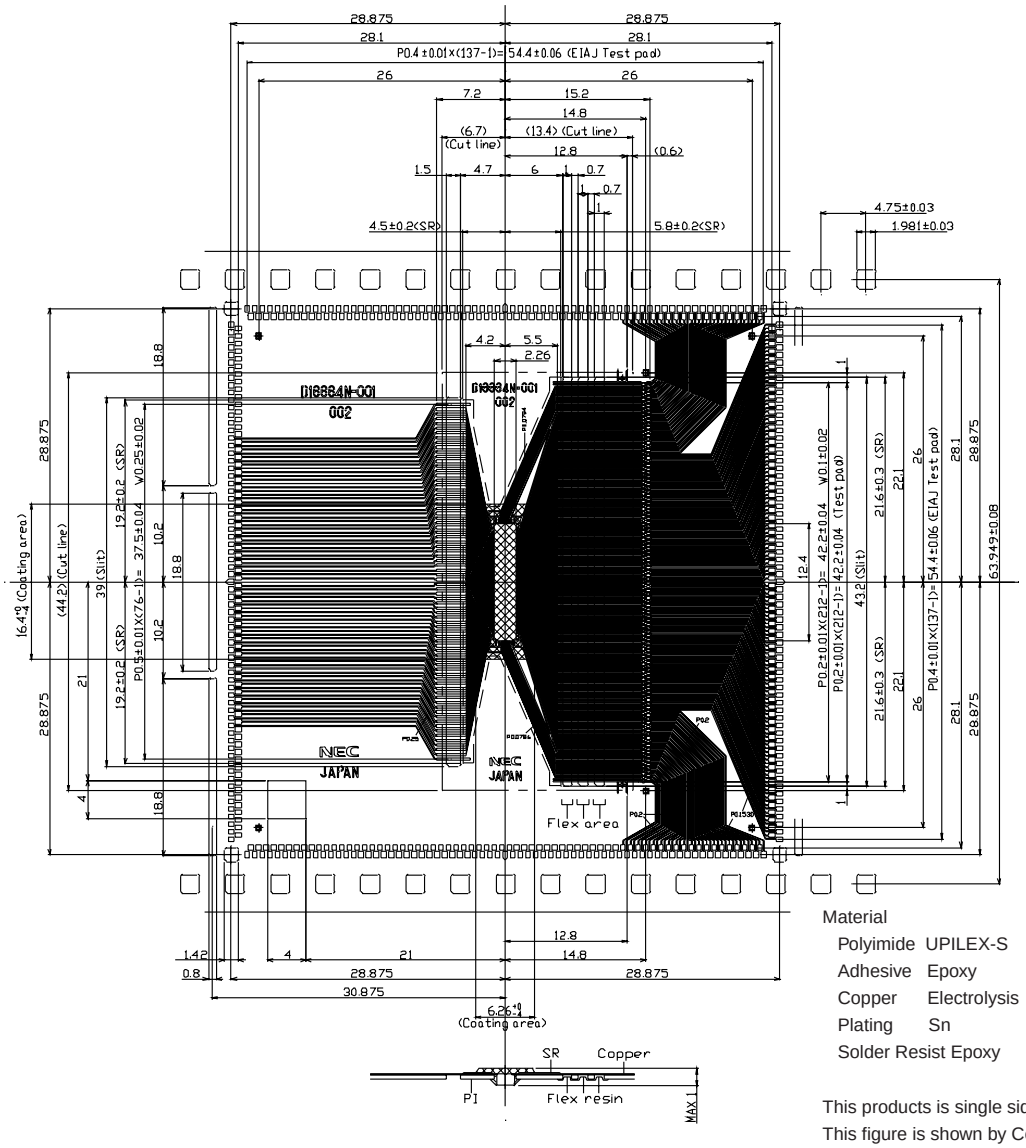
1/128 duty

$$\text{Frame frequency} = \frac{1}{130 \times 2 \times 4} \times \text{Oscillation frequency}$$

$$\text{STB frequency} = \frac{1}{2 \times 4} \times \text{Oscillation frequency}$$

22. PACKAGE DRAWINGS

Standard TCP Package Drawing (μPD16664N-001) (1/3)



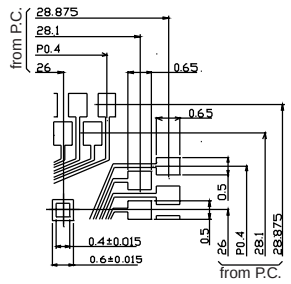
Material

Polyimide	UPILEX-S	t = 75 μm
Adhesive	Epoxy	t = 12 μm
Copper	Electrolysis Cu	t = 18 μm
Plating	Sn	t = 0.15 μm min
Solder Resist	Epoxy	t = 25 μm

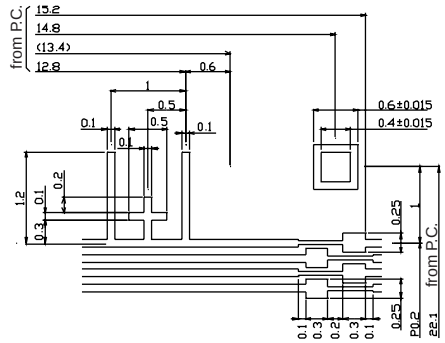
This products is single side Flex type.
This figure is shown by Copper side over Polymide.
All tolerances unless otherwise specified 0.05 mm.
Corner radius is 0.30 mm MAX.
13 Sprocket holes (61.75 mm) for 1 Pattern.

Standard TCP Package Drawing (μPD16664N-001) (2/3)

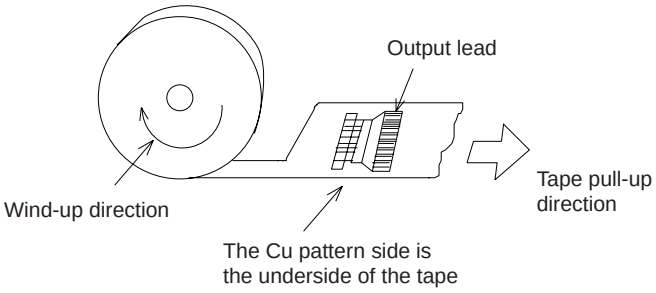
EIAJ test pad details



Alignment details

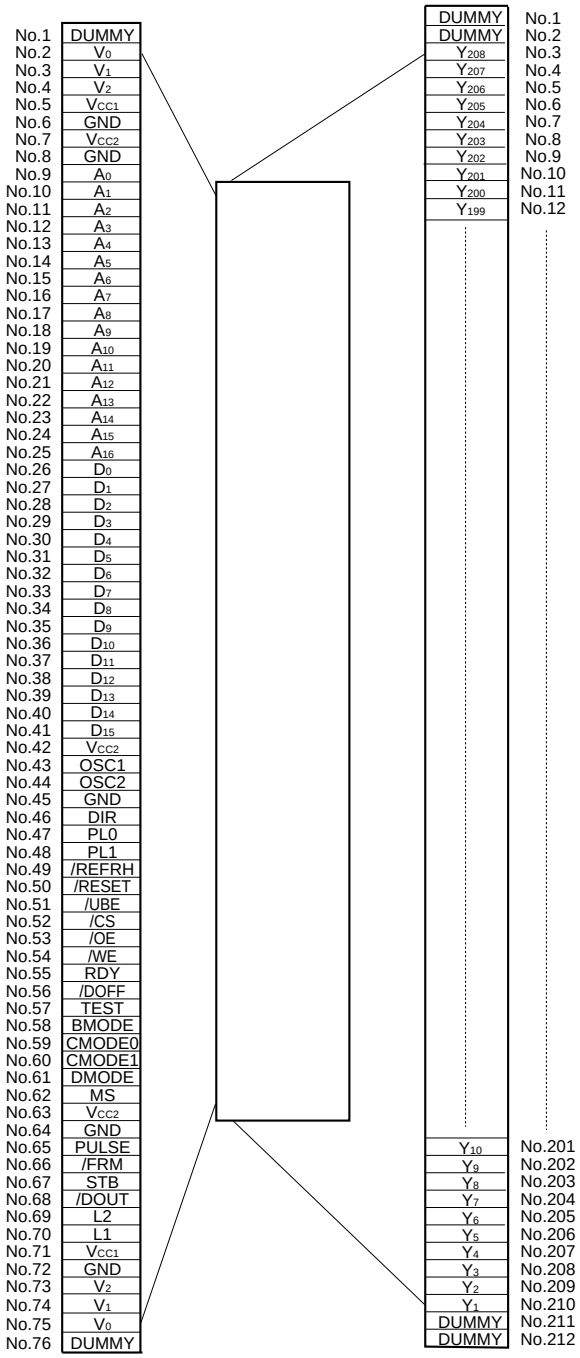


TCP tape winding direction



Standard TCP Package Drawing (μPD16664N-001) (3/3)

Pin configuration



[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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