NEC

MOS INTEGRATED CIRCUIT

μPD16454A

The μPD16454A is a single-chip controller/driver for dot matrix LCD, enabling the display of up to 48 alphanumerical and kana characters and symbols (24 characters × 2 lines) each of which is composed of 5 × 7 dots. On-chip charge pump-type DC/DC converter that enables the μPD16454A to operate on a single 5-V power supply and the chip design aiming at tape carrier package (TCP) mounting make the μPD16454A ideal for portable equipment and all kinds of data terminals for which downsizing is an important consideration.

FEATURES

- 5 × 7 dot matrix LCD display controller/driver
- 24 characters × 2 lines, 1/14 duty display
- Interface with CPU 4 bits wise
- On-chip ROM and RAM
  - Display data RAM (8 × 48 bits)
  - Character generator RAM (8 user-defined characters; 5 × 7 × 8 bits)
  - Character generator ROM (160 characters; 5 × 7 × 160 bits)
- On-chip LCD driver
  - 120 segment signals
  - 14 common signals
- Single 5-V power supply
  - Doubling DC/DC booster generating 10 V for driving LCDs
  - Total power dissipation: 2 mA max.
- On-chip temperature compensation circuit
- TCP mounting enabled

ORDERING INFORMATION

Part number	Available as
μPD16454AN-XXX	TCP (TAB)
μPD16454AP	Chip

TPC formats are created on a custom-made basis. For additional information, contact an NEC sales representative.

For purchases of chips only, additional documents on quality are required. Contact an NEC sales representative.

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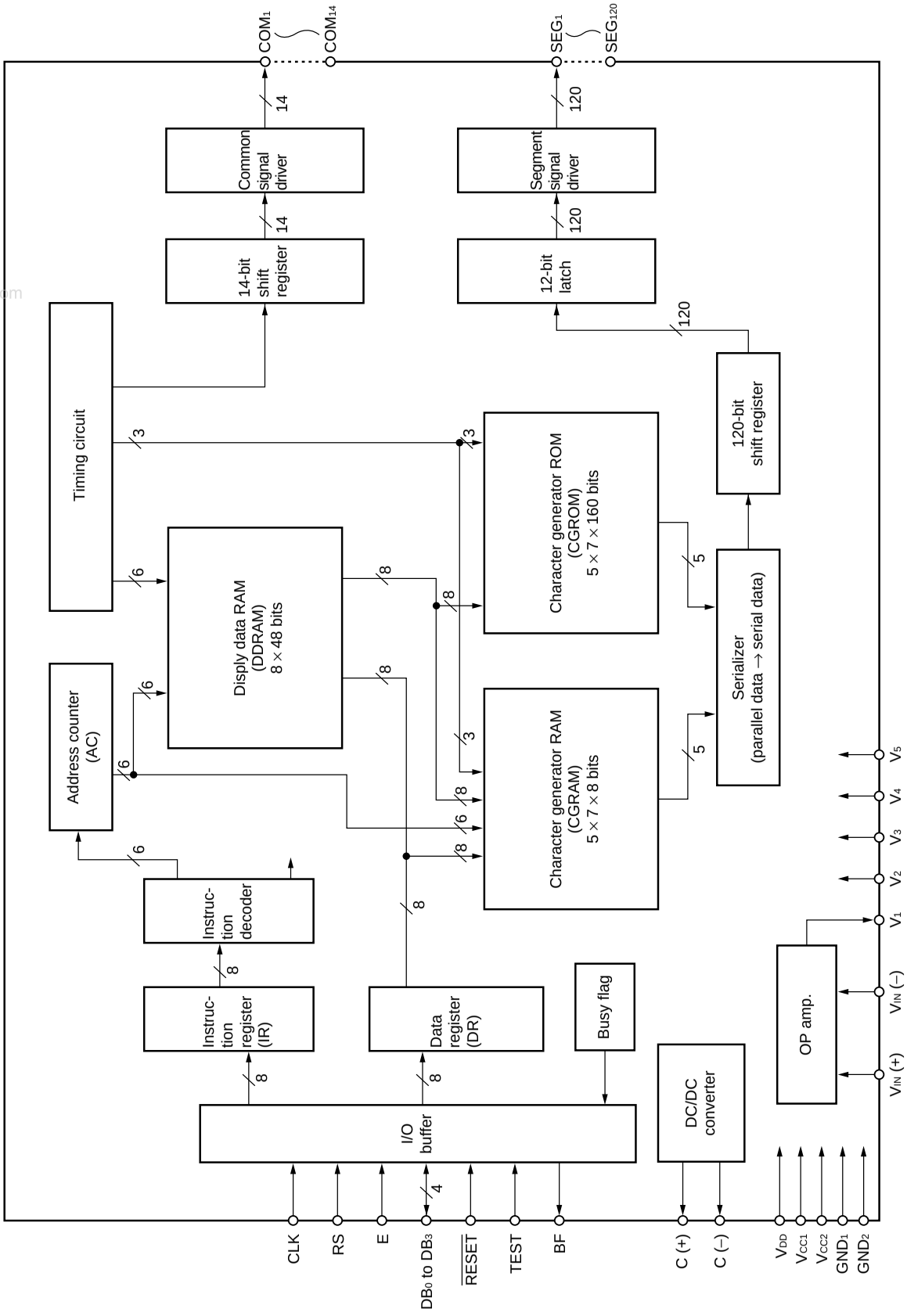
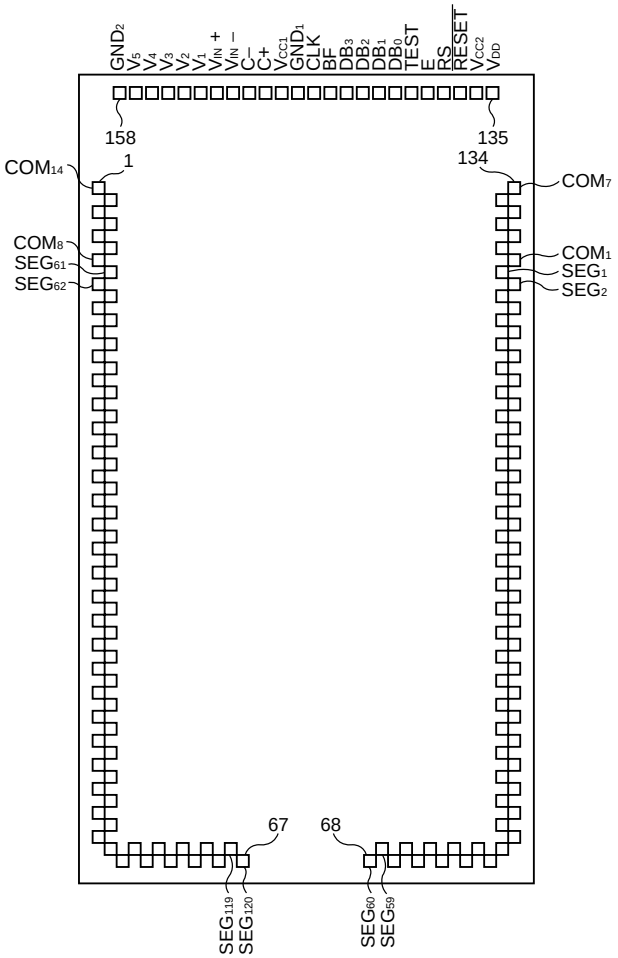
BLOCK DIAGRAM



PIN FUNCTION

Symbol	Pin No.	Input/Output	Connect to	Function
RS	138	Input	CPU	Register selection signal '0' instruction register (IR) '1' data register (DR)
E	139	Input	CPU	Data reading signal Reads data at the falling edge.
TEST	140	Input		Test pin '1' = test mode '0' or open = normal operation
BF	145	Output	CPU	When busy flag is '1', indicates that internal part of LCD is currently operating. In test mode, functions as test output.
$DB_{0 \text{ to } 3}$	141 to 144	Input/Output	CPU	Data input signals In test mode, function as output pin.
$\overline{RESET}$	137	Input	CPU	Reset is performed with reset signal '0'
CLK	146	Input	CPU	LCD-driving clock
$COM_{1 \text{ to } 14}$	128 to 134, 7 to 1	Output	LCD	Common signals
$SEG_{1 \text{ to } 120}$	127 to 68, 8 to 67	Output	LCD	Segment signal outputs
$V_{1 \text{ to } 5}$	153 to 157		Power supply	LCD-driving supply voltages
V_{CC1}	148		Power supply	Power supply for logic circuits
V_{CC2}	136		Power supply	Power supply for logic circuits
V_{DD}	135		Power supply	Boosted power supply
GND1	147		Power supply	Ground for logic circuit
GND2	158		Power supply	Ground for high-voltage circuit
V_{IN} (+)	151		Power supply	Reference voltage supply
V_{IN} (–)	152			LCD-driving supply voltage adjustment input
C (+)	149		Capacitor	Capacitor connection pin for booster
C (–)	150		Capaditor	Capacitor connection pin for booster

PIN CONFIGURATION (Pad Configuration)



BLOCK FUNCTIONS

(1) Registers (IR, DR)

This LCD contains both an 8-bit instruction register (IR) and an 8-bit data register (DR).

The IR register stores display clear instruction codes and display data RAM (DDRAM) and character generaotor RAM (CGRAM) addresses.

The DR register temporarily stores data to be transferred to DDRAM and CGRAM.

The IR and DR registers are selected with the register selector (RS) bit.

RS	Register selector
0	IR
1	DR

(2) Busy flag (BF)

When BF = '1', this indicates that the LCD's internal circuit is currently operating. Therefore, after ascertaining that BF = '0', it is necessary to read the next instruction or display data.

(3) Address counter (AC)

The AC is a counter that sets addresses in DDRAM and CGRAM. When an address-setting instruction is written to the IR, the address value is set from the IR to the address counter. At the same time, which of DDRAM and CGRAM is selected is also determined.

After display data is written in DDRAM or CGRAM, the address counter's address value is automatically incremented by 1. Nevertheless, since data in CGRAM consists of 7 bytes characters, the address value is incremented by 2 only when display data has been written to the 7th line.

(4) Display data RAM (DDRAM)

DDRAM is a RAM that stores display data consisting of 8-bit character codes. The capacity is 8×48 bits so that 48 characters can be stored. The correspondence between DDRAM addresses and display position on LCD is shown in Fig. 1.

Fig.1 Correspondence of DDRAM address and display position on LCD

1st digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
2nd line	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F

DDRAM address (hexadecimal)

(5) Character generator ROM (CGROM)

CGROM is a ROM that generates 5 × 7-dot character patterns from 8-bit character codes, and can generate 160 different characters in total. The correspondence of CGROM addresses and character patterns to the ASCII code is shown in Fig.2.

Fig.2 Correspondence of CGROM address data (character codes) and character patterns (00110010 → "2")

CGROM address											ROM output data				
A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	04	03	02	01	00
Character code (DDRAM output data)								Line position							
								0	0	0	0	1	1	1	0
								0	0	1	1	0	0	0	1
								0	1	0	0	0	0	0	1
0	0	1	1	0	0	1	0	0	1	1	0	0	0	1	0
								1	0	0	0	0	1	0	0
								1	0	1	0	1	0	0	0
								1	1	0	1	1	1	1	1

Character code and character pattern correspondence is shown in Fig.3.

Fig.3. Character Code and Character Pattern Correspondence

Upper 4 bits / Lower 4 bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101
XXXX0000	CG RAM (1)										
XXXX0001	(2)										
XXXX0010	(3)										
XXXX0011	(4)										
XXXX0100	(5)										
XXXX0101	(6)										
XXXX0110	(7)										
XXXX0111	(8)										
XXXX1000	(1)										
XXXX1001	(2)										
XXXX1010	(3)										
XXXX1011	(4)										
XXXX1100	(5)										
XXXX1101	(6)										
XXXX1110	(7)										
XXXX1111	(8)										

(6) Character generator RAM (CGRAM)

CGRAM is a RAM that the user can use to freely define character patterns. Eight types of 5 × 7-dot character pattern definitions are possible. The CGRAM address values (character codes) of A10 to A3 in Fig.2 are 00H to 17H (8 types). Other values (line position, output data, etc.) are the same as in Fig.2.

(7) Timing circuit

The timing circuit generates timing signals to activate internal circuits. Retrieve timing of RAM needed for display and internal operation timing through access from the CPU are performed on a time-share basis and thus do not interfere with each other. Therefore, to change display characters on the LCD panel, even if DDRAM has been accessed, characters other than those that have been accessed do not flicker.

(8) LCD-related circuit

The LCD driver circuit consists of 14 common signal drivers and 120 segment signal drivers. Each driver is automatically controlled by an internal control circuit, and outputs a driving waveform corresponding to the character pattern.

Serial data is always sent from the character pattern of the display data corresponding to the last DDRAM address, and the character pattern of the display data corresponding to the first DDRAM address (00H) is latched when inpout in the 120-bit shift register. LCD display positions are shown in Fig.1 of section **(4) Display data RAM (DDRAM).**

Interface with CPU (data transfer)

This LSI interfaces (transfers data) with CPU in 4-bit units (DB0 to DB3), but the internal register circuits (IR and DR) have 8-bit paths, therefore making it necessary to transfer 4-bit data twice.

Assuming that the 8 bits of data are numbered D0 to D7, this data is transferred in the following sequence: first the upper 4 bits (D4 to D7), then the lower 4 bits (D0 to D3). The busy flag check is performed before the upper 4 bits are transferred, and is not necessary before transferring the 4 lower bits.

If data is transferred without checking BF, taking 10 CLK cycles or more is necessary between previous 8-bit data transfer and next transfer (CLK = 1/fc).

INSTRUCTIONS

The instructions for this LSI are shown in Table 1 below.

Table 1 Instruction List

Instruction	Code									Description
	RS	D7	D6	D5	D4	D3	D2	D1	D0	
Display On/Off	0	0	0	0	0	1	D	*	*	Full display On/Off D : '1' (ON), '0' (OFF)
CGRAM Address Set	0	0	0	CGRAM address						CGRAM address set. Transfer of subsequent data is of CGRAM.
DDRAM Address Set	0	1	*	DDRAM address						DDRAM address set. Transfer of subsequent data is of DDRAM data.
CGRAM/DDRAM Data Write	1	Write data However, because CGRAM data occupies D0 to D4, D5 to D7 are ignored.								Data is written in CGRAM or DDRAM. The internal address counter (AC) is automatically incremented by one following data write.

Remark * in the above table indicates that the value may be either 0 to 1.

Initialization using the reset signal ($\overline{\text{RESET}}$)

When the reset signal ($\overline{\text{RESET}}$) is activated ($\overline{\text{RESET}}$ = 0) for 10 CLK cycles (CLK = 1/fc) or more, initialization is performed as follows.

(1) Display ON/OFF

Set to OFF (D = 0)

(2) DDRAM address set

Set to DDRAM address 00H

When data write is performed under this condition, data is written to DDRAM address 00H.

ABSOLUTE MAXIMUM RATINGS (T_a = +25 °C, GND_1 = GND_2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{CC}	–0.3 to +7.0	V
Driver Input Voltage	V_I	–0.3 to V_{CC} +0.3	V
Logic Output Voltage	V_{O1}	–0.3 to V_{CC} +0.3	V
Driver Supply Voltage	V_{DD}	–0.3 to +15	V
Driver's Driver Input Voltage	V_2 to V_5	–0.3 to V_{DD} +0.3	V
Driver's Driver Output Voltage	V_1	–0.3 to V_{DD} +0.3	V
Driver Output Voltage	V_{O2}	–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{stg}	–40 to +125	°C

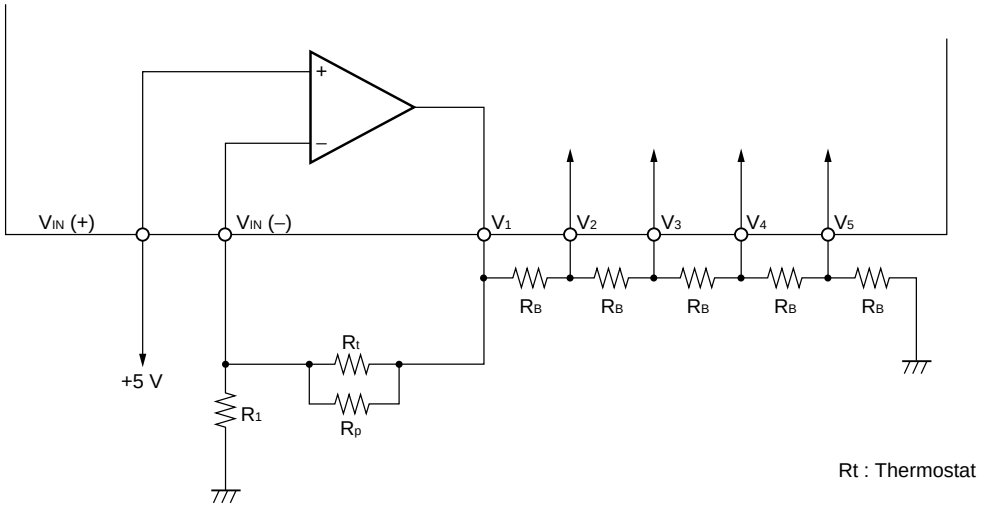
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{CC}	4.75	5	5.25	V
Operating Ambient Temperature	T_{opt}	–30	25	85	°C

DC CHARACTERISTICS (T_a = –30 to +85 °C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-Level Input Voltage 1	V_{IH1}	E, $\overline{RESET}$, CLK, input excluded	0.7 V_{CC}			V
Low-Level Input Voltage 1	V_{IL1}				0.3 V_{CC}	V
High-Level Input Voltage 2	V_{IH2}	E, $\overline{RESET}$, CLK input	0.8 V_{CC}			V
Low-Level Input Voltage 2	V_{IL2}				0.2 V_{CC}	V
Hysteresis voltage	V_H			0.1		V
High-Level Output Voltage	V_{OH}	I_{OH} = –1 mA	0.9 V_{DD}			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1 mA			0.1 V_{CC}	V
High-Level Input Leak Current	I_{IH1}	TEST excluded, V_{IN} = V_{CC}			1	μA
High-Level Input Leak Current	I_{IH2}	TEST, V_{IN} = V_{CC}			6	mA
Low-Level Input Lead Current	I_{IL}	V_{IN} = 0 V	–1			μA
Common Output Impedance	R_{COM}	$\lvert I_O \rvert$ = 50 μA		1.5	58	kΩ
Segment Output Impedance	R_{SEG}	$\lvert I_O \rvert$ = 50 μA		1.5	76	kΩ
Logic Supply Voltage (Total consumption)	I_{CC}	R_1 = 33 kΩ R_P = 27 kΩ R_B = 22 kΩ f_C = 250 kHz		1	2	mA
Driver Supply Voltage (Boosted voltage)	V_{DD}	R_1 = 33 kΩ R_P = 27 kΩ R_B = 22 kΩ External capacitor of 1 μF	1.9 V_{CC}		2 V_{CC}	V
High-Level Output Voltage (V_1 pin)	V_{OH2}	I_{OH} = –1 mA V_{IN} (+) = V_{DD} V_{IN} (–) = 0 V	0.9 V_{DD}			V
Low-Level Output Voltage (V_1 pin)	V_{OL2}	I_{OL} = 10 μA V_{IN} (+) = 0 V V_{IN} (–) = V_{DD}			0.1 V_{DD}	V

∗ TYP. is reference value at T_a = +25 °C.



Rt : Thermostat

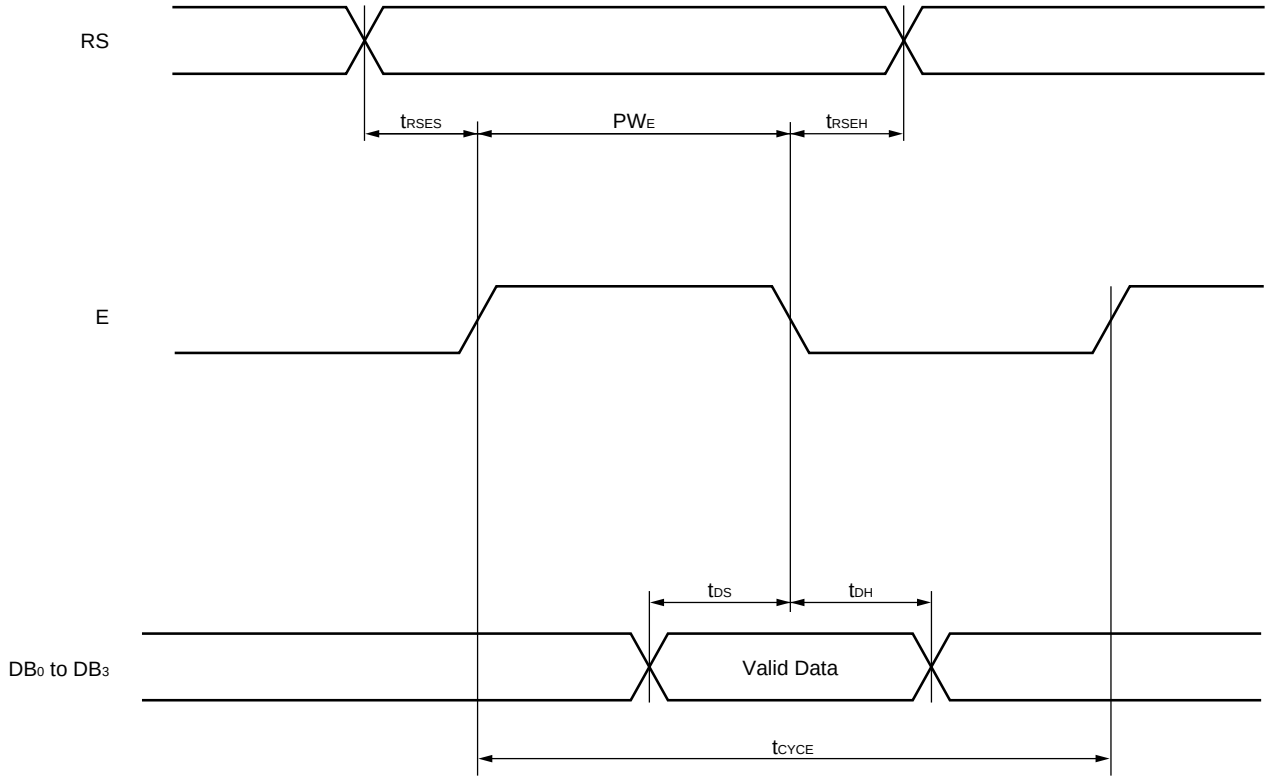
AC CHARACTERISTICS (T_a = –30 to +85 °C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	f_C		160	250	500	kHz
Enable Cycle Time	t_{CYCE}		1 000			ns
Enable Pulse Width	PW_E		450			ns
RS • E Setup Time	t_{RSES}		100			ns
RS • E Hold Time	t_{RSEH}		100			ns
Data Setup Time	t_{DS}		100			ns
Data Hold Time	t_{DH}		100			ns

∗ TYP. is reference value at T_a = +25 °C.

AC CHARACTERISTIC WAVEFORM

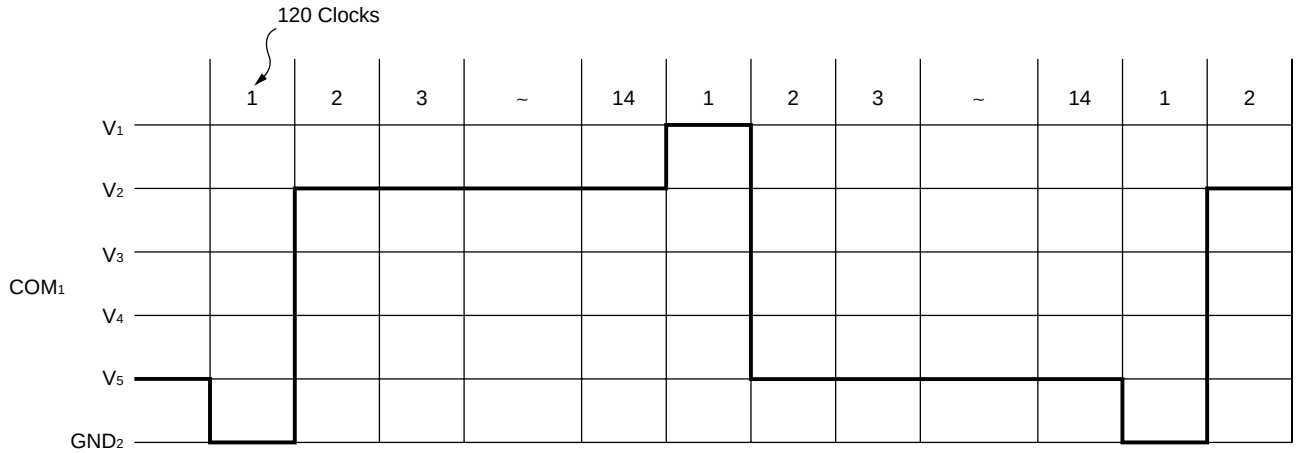
Write Operation



OSCILLATION FREQUENCY and LCD FRAME FREQUENCY CORRESPONDENCE

The correspondence between the oscillation frequency of 250 kHz and the LCD frame frequency is shown in Fig.4 below.

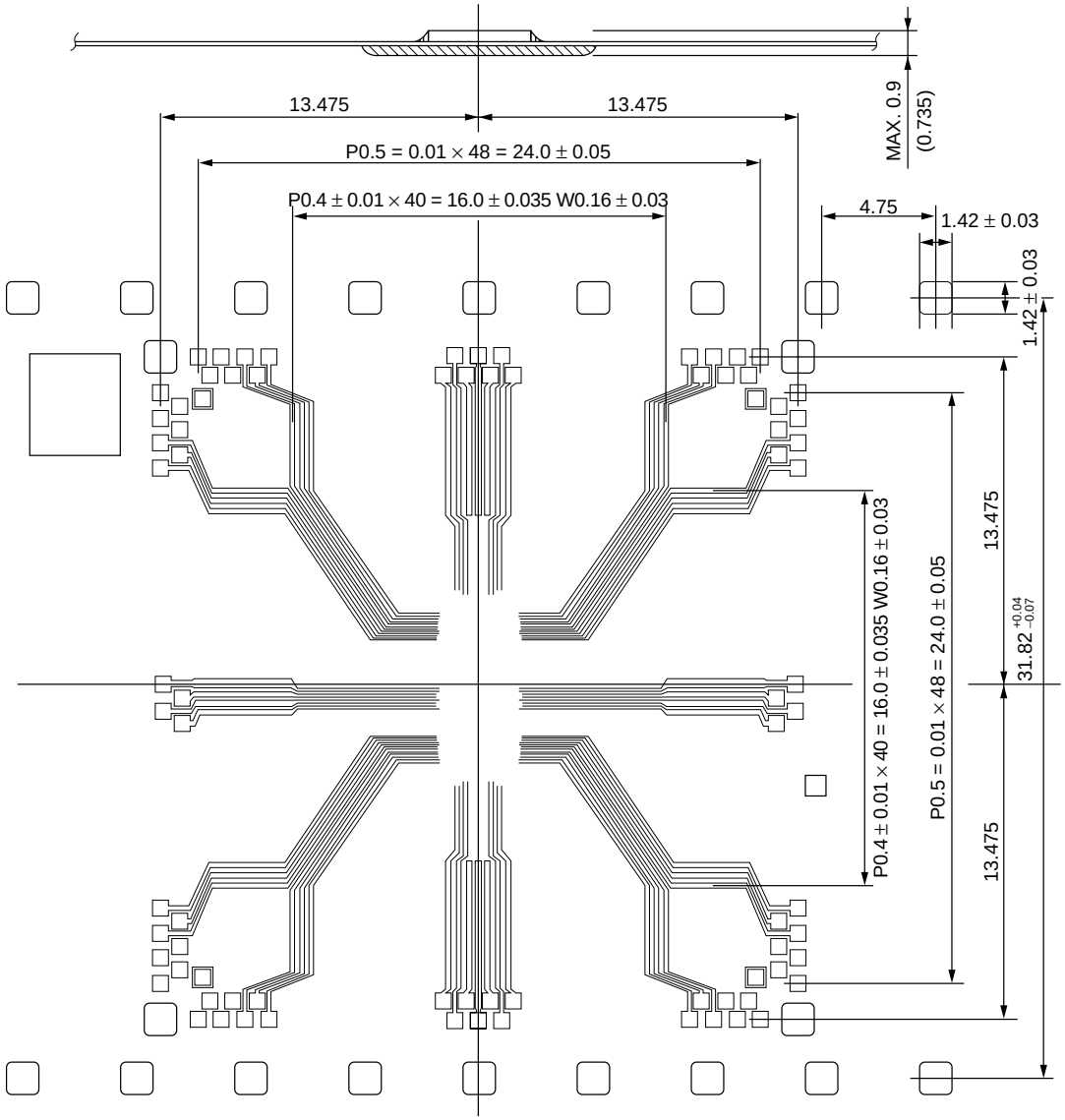
Fig.4 Oscillation Frequency and LCD Frame Frequency Correspondence



1 frame = 4 μs × 120 × 14 = 6 720 μs = 6.72 ms

Signal	Display Mode	+	−
COM	Lit	GND_2	V_1
	Not lit	V_2	V_5
SEG	Lit	GND_2	V_1
	Not lit	V_4	V_3

REFERENCE 1 : STANDARD TCP DRAWING (μPD16454AN-051)

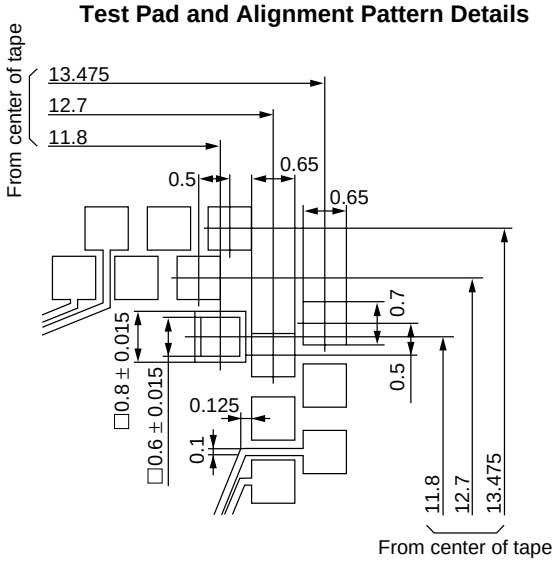


Note 1. Measurements between brackets are for referency only.

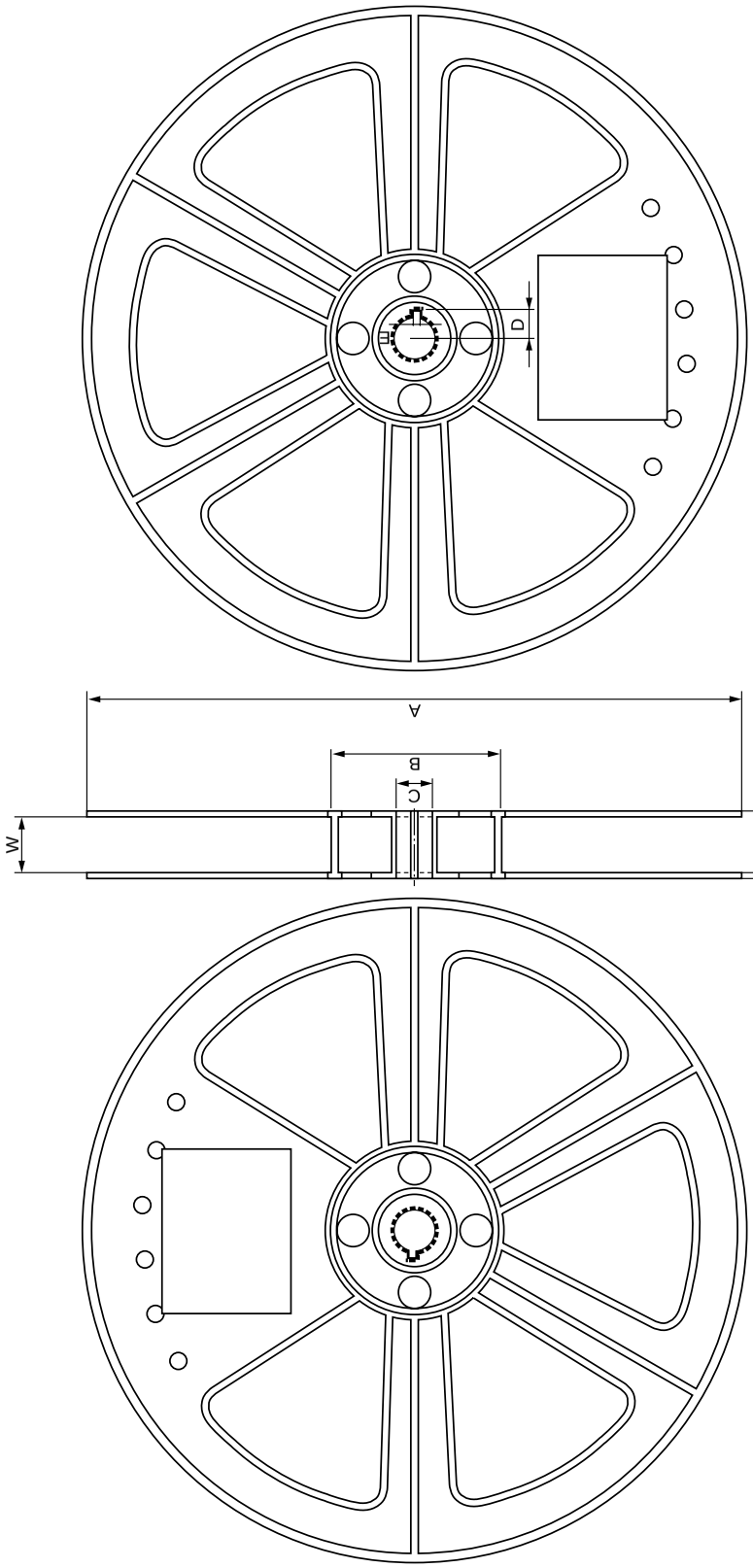
2. Non-specified tolerances are ± 0.05 mm.

3. This drawing is viewed from wire-patterned face.

Test Pad and Alignment Pattern Details



REFERENCE 2 : TCP SHIPPING RELL (φ 405 mm)



*:Tape width

Symbol	Size (mm)		
A	φ405 ± 2.0		
B	φ105		
C	φ25.9 ± 0.5		
D	φ17.9 ± 0.5		
E	$50^{+1.0}_{-0}$		
W	(35)*	37 ± 1.5	
W	(48)*	50 ± 1.5	
W	(70)*	72 ± 1.5	
W_1	3 ± 0.5		
W_2	W + 2W_1		

[MEMO]

M4 96.5