NEC

MOS INTEGRATED CIRCUIT

μPD16326A

32-BIT FLUORESCENT DISPLAY TUBE DRIVER

The μPD16326A is a fluorescent display tube driver using a high breakdown voltage CMOS process. It consists of 32-bit bidirectional shift registers, a latch circuit, and a high breakdown voltage CMOS driver block. The logic block operates on a 5 V power supply designed to be connected directly to a microcontroller (CMOS level input). The driver block has a 150 V and 20 mA high breakdown voltage output, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

FEATURES

- High breakdown voltage CMOS structure
- High breakdown voltage, high current output (150 V, 20 mA)
- 32-bit bidirectional shift registers on chip
- Data control by transfer clock (external) and latch
- High-speed data transfer capability (f_{max} = 8.0 MHz MIN)
- Wide operating temperature range (T_A = –40 to 85 ˚C)

ORDERING INFORMATION

Part Number	Package
μPD16326AGB-3B4	44-pin plastic QFP (4-direction leads)

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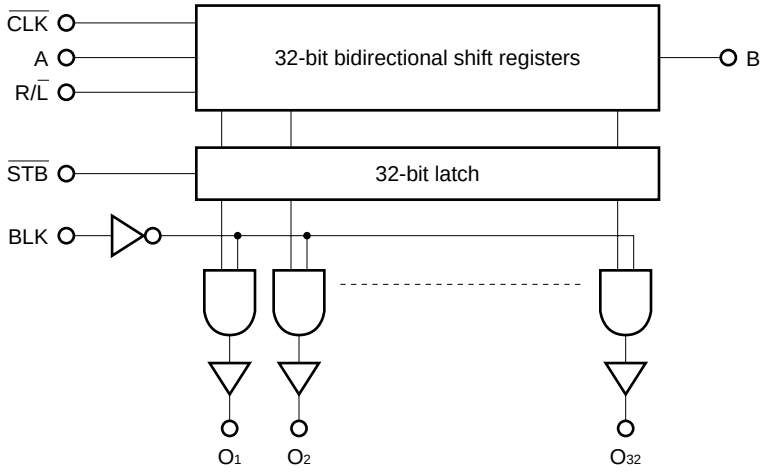
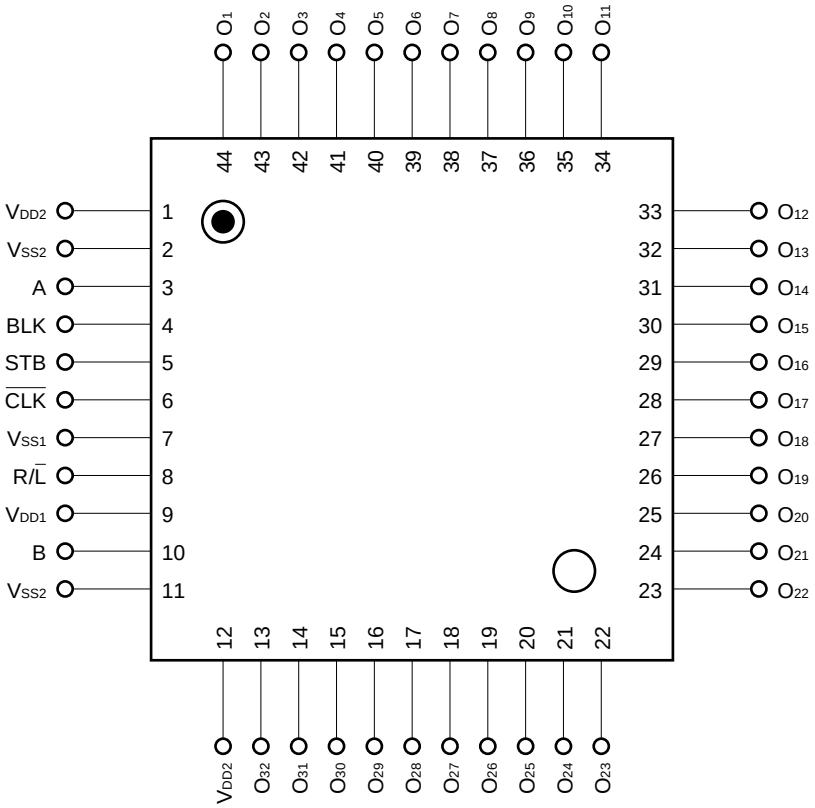
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



Remark Be sure to enter the power to V_{DD1}, logic signal, and V_{DD2}, in that order, and turn off the power in the reverse order.

PIN DESCRIPTION

Pin Symbol	Pin Name	Pin Number	Description
STB	Latch strobe input	5	H: Data through L: Data retention
A	RIGHT data input	3	When R/$\overline{L}$ = H, A: Input B: Output When R/$\overline{L}$ = L, A: Output B: Input
B	LEFT data input	10	
$\overline{CLK}$	Clock input	6	Shift is executed on a fall.
BLK	Blanking input	4	H: O_1 to O_{32}: ALL "L"
R/$\overline{L}$	Shift control input	8	H: Right shift mode A → O_1 ... O_{32} → B L: Left shift mode B → O_{32} ... O_1 → A
O_1 to O_{32}	High breakdown voltage output	13 - 44	130 V, 20 mA MAX
V_{DD1}	Logic block power supply	9	5 V ±10 %
V_{DD2}	Driver block power supply	1, 12	30 to 130 V
V_{SS1}	Logic ground	5	Connected to system GND
V_{SS2}	Driver ground	2, 11	Connected to system GND

TRUTH TABLE 1 (SHIFT REGISTER BLOCK)

Input		Output		Shift Register
R/$\overline{L}$	$\overline{CLK}$	A	B	
H	↓	Input	Output[Note 1]	Execution of right shift
H	H or L		Output	Retained
L	↓	Output[Note 2]	Input	Execution of left shift
L	H or L	Output		Retained

Notes 1. On a clock fall, the data items of S_{31} are shifted to S_{32}, and output from B.

2. On a clock fall, the data items of S_2 are shifted to S_1, and output from A.

TRUTH TABLE 2 (LATCH BLOCK)

STB	Operation
L	Retains S_n data immediately before $\overline{STB}$ becomes L.
H	Outputs shift register data.

TRUTH TABLE 3 (DRIVER BLOCK)

L_n[Note]	STB	BLK	Driver output state
×	×	H	L (all driver outputs: L)
×	L	L	Outputs S_n data on STB fall.
L	H	L	L
H	H	L	H

Note L_n: Latch output

Remark × = H or L, H = high level, L = Low level

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS} = 0 V)

Item	Symbol	Rating	Unit
Logic block supply voltage	V_{DD1}	–0.5 to +7.0	V
Driver block supply voltage	V_{DD2}	–0.5 to +150	V
Logic block input voltage	V_I	–0.5 to V_{DD1} + 0.5	V
Driver block output current	I_O	20	mA
Package allowable power dissipation	P_D	800[Note]	mW
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Note When $T_A \geq 25$ °C, load should be alleviated at a rate of –8.0 mW/°C. (T_j = 125 °C (MAX.))

RECOMMENDED OPERATING RANGE (T_A = –40 to +85 °C, V_{SS} = 0 V)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Logic block supply voltage	V_{DD1}	4.5	5.0	5.5	V
Driver block supply voltage	V_{DD2}	30		130	V
Input voltage high	V_{IH}	0.7·V_{DD1}		V_{DD1}	V
Input voltage low	V_{IL}	0		0.2·V_{DD1}	V
Driver output current	I_{OH}			–10	mA
	I_{OL}			+2.5	mA

ELECTRICAL SPECIFICATIONS (T_A = 25 °C, V_{DD1} = 4.5 to 5.5 V, V_{DD2} = 130 V, V_{SS} = 0 V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V_{OH1}	Logic, I_{OH} = –1.0 mA	0.9·V_{DD1}		V_{DD1}	V
Output voltage low	V_{OL1}	Logic, I_{OL} = 1.0 mA	0		0.1·V_{DD1}	V
Output voltage high	V_{OH21}	O_1 to O_{40}, I_{OH} = –0.5 mA	126			V
	V_{OH22}	O_1 to O_{40}, I_{OH} = –5.0 mA	120			V
Output voltage low	V_{OL2}	O_1 to O_{40}, I_{OL} = 0.5 mA			2.5	V
Input leakage current	I_{IL}	V_I = V_{DD1} or V_{SS1}			±1.0	μA
Input voltage high	V_{IH}		0.7·V_{DD1}		V_{DD1}	V
Input voltage low	V_{IL}		0		0.2·V_{DD1}	V
Static consumption current	I_{DD1}	Logic, T_A = –40 to +85 °C			1 000	μA
	I_{DD1}	Logic, T_A = 25 °C			100	μA
	I_{DD2}	Driver, T_A = –40 to +85 °C			1 000	μA
	I_{DD2}	Driver, T_A = 25 °C			100	μA

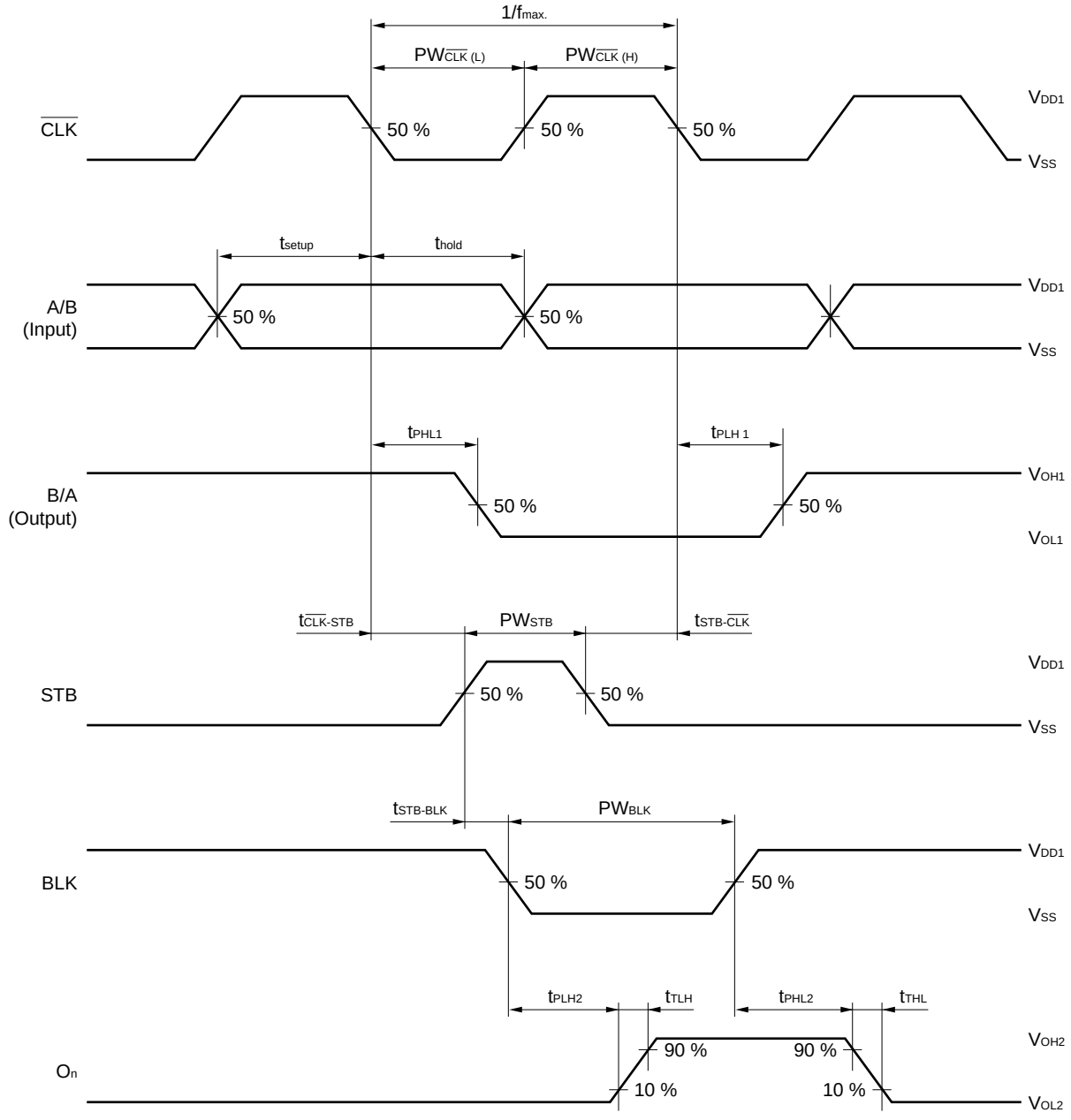
SWITCHING CHARACTERISTICS (T_A = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 130 V, V_{SS} = 0 V, logic C_L = 15 pF, driver C_L = 50 pF, driver R_L = 220 kΩ, $t_r = t_f$ = 10 ns)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission delay time	t_{PHL1}	$\overline{CLK}$ ↓→ A/B			110	ns
	t_{PLH1}				110	ns
	t_{PHL2}	$\overline{BLK}$ ↓→ O_1 to O_{32}			300	ns
	t_{PLH2}				300	ns
Fall time	t_{THL}	O_1 to O_{32}			600	ns
Rise time	t_{TLH}	O_1 to O_{32}			500	ns
Maximum clock frequency	f_{max}	With cascading, Duty = 50 %	8.0			MHz
Input capacitance	C_I				15	pF

TIMING REQUIREMENTS (T_A = –40 to +85 °C, V_{DD1} = 4.5 to 5.5 V, V_{SS} = 0 V, $t_r = t_f$ = 10 ns)

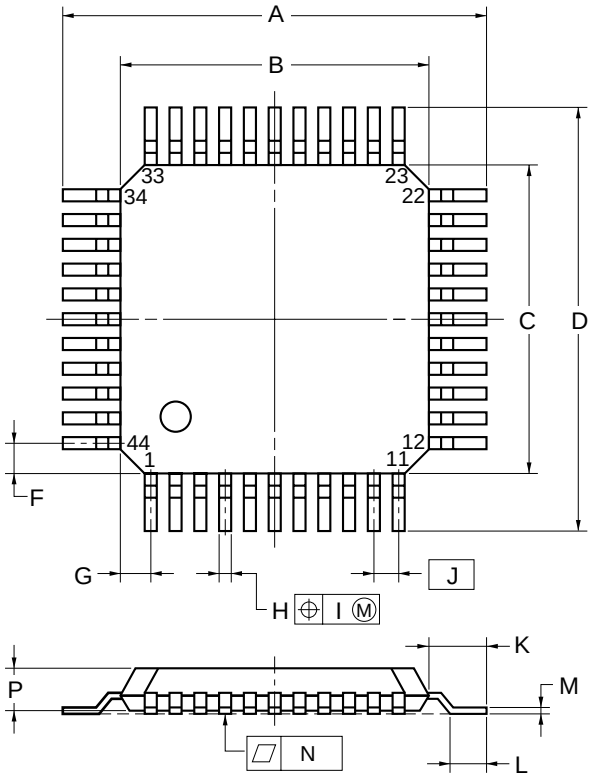
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		40			ns
Strobe pulse width	PW_{STB}		80			ns
Blank pulse width	PW_{BLK}		1 500			ns
Data setup time	t_{setup}		15			ns
Data hold time	t_{hold}		30			ns
Clock-strobe time	$t_{\overline{CLK}\text{-}STB}$	$\overline{CLK}$ ↓→ STB ↑	45			ns
Strobe-clock time	$t_{STB\text{-}\overline{CLK}}$	STB ↓→ $\overline{CLK}$ ↓	45			ns
Strobe-blank time	$t_{STB\text{-}BLK}$	STB ↑→ BLK ↓	80			ns

SWITCHING CHARACTERISTIC WAVEFORM (R/$\overline{L}$ = H)

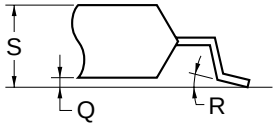


PACKAGE DRAWINGS

44 PIN PLASTIC QFP (Unit: mm)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P44GB-80-3B4-3

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

SURFACE MOUNT TYPE

For details of recommended soldering conditions, refer to the information document "**Semiconductor Device Mounting Technology Manual**" **(C10535E)**.

μPD16326GB-3B4

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 ˚C, Duration: 30 sec. MAX. (at 210 ˚C or above), Number of times: Twice, Time limit: None**Note**	IR35-00-2
VPS	Package peak temperature: 215 ˚C, Duration: 40 sec. MAX. (at 200 ˚C or above), Number of times: Twice, Time limit: None**Note**	VP15-00-2
Wave soldering	Solder bath temperature: 260 ˚C MAX., Duration: 10 sec. MAX., Number of times: Once, Time limit: None**Note**	WS60-00-1
Pin partial heating	Pin partial temperature: 300 ˚C MAX., Duration: 10 sec. MAX., Time limit: None**Note**	

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25 ˚C, 65 % RH.

Caution Use of more than one soldering method should be avoided (except in the case of pin partial heating).

REFERENCES

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grade on NEC Semiconductor Devices (C11531E)

[MEMO]

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M4 96.5