NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD16302

40 BIT ROW DRIVER FOR EL PANEL

DESCRIPTION

The μPD16302 is a ROW driver utilized high voltage CMOS for EL Panel. It consists of a 40bit bidirectional shift register and high voltage CMOS drivers.

It operates at 5 V (CMOS input level) and provides low power dissipation because the driver is full CMOS construction, 250 V and 100 mA max.

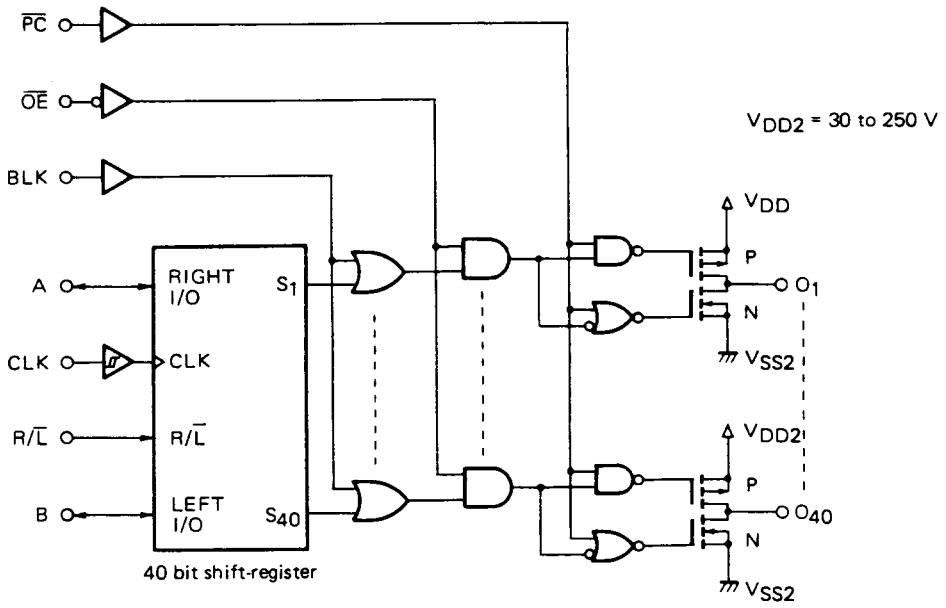
FEATURES

- High voltage CMOS construction
- High voltage Output (250 V, 100 mA max.)
- Built-in 40bit bidirectional shift register
- Capable of reversing a driver output polarity by PC terminal
- Low power dissipation (1 mA max., T_a = −40 to +85 °C)
- Symmetry pin configuration by tridirectional lead quad flat package

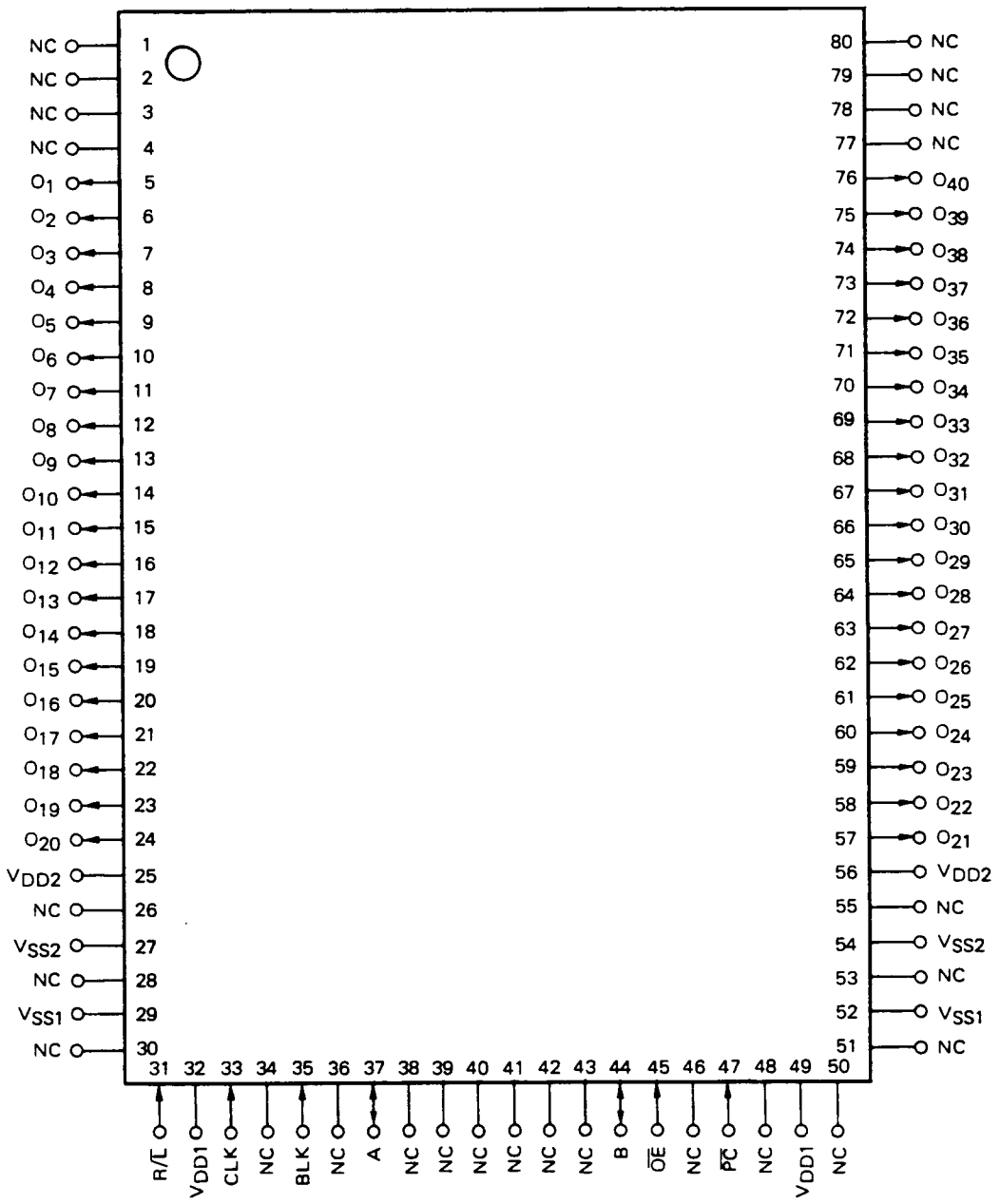
ORDERING INFORMATION

Part No.	Package
μPD16302GF-3LA	100pin Plastic QFP (3 direction lead)

BLOCK DIAGRAM



PIN CONNECTION (Top View)



* Please open No. 40 pin to be connected with lead frame.
* The all power supply terminals (ex V_{DD1}, V_{DD2}, V_{SS1}, and V_{SS2}) should be used. V_{SS1} and V_{SS2} should be respectively connected with themselves outside.

PIN CONFIGURATION

SYMBOL	PIN NAME	PIN NO.	FUNCTION
BLK	Blank Input	35	Refer to below Table 2
$\overline{OE}$	Output Enable Input	45	Refer to below Table 2
$\overline{PC}$	Polarity Change Input	47	$\overline{PC}$ = L: All driver output invert
A	Right Data I/O	37	R/$\overline{L}$ = H: A = IN, B = OUT R/$\overline{L}$ = L: B = IN, A = OUT
B	Left Data I/O	44	
CLK	Shift Clock Input	33	Positive edge active
R/$\overline{L}$	Shift Direction Control Input	31	H: Right shift mode A → O_1 to O_{40} → B L: Left shift mode B → O_{40} to O_1 → A
O_1 to O_{40}	High Voltage Output	5-24, 57-76	250 V 100 mA max.
V_{DD1}	Logic Power Supply	32, 49	5 V ± 10 %
V_{DD2}	Driver Power Supply	25, 56	30 to 240 V
V_{SS1}	Ground (Logic)	29, 52	–
V_{SS2}	Ground (Driver)	27, 54	–
NC	No Connection	1-4, 26, 28, 30, 34, 36, 38-43, 46, 48, 50, 51, 53, 55, 77-80	No connection Please open No. 40 pin.

TRUTH TABLE 1 (Shift Register)

R/L	CLK	A	B	SHIFT REGISTER
H	↑	S_1 input	S_{40} output	Data are shifted (to Right)
H	H or L			No change
L	↑	S_1 output	S_{40} input	Data are shifted (to Left)
L	H or L			No change

TRUTH TABLE 2 (Driver)

DATA	BLK	$\overline{OE}$	$\overline{PC}$	O_n	NOTE
X	H	L	H	H	All drivers = H
X	H	L	L	L	All drivers = L
X	X	H	X	Z	All drivers = Z
L	L	L	X	Z	
H	L	L	H	H	
H	L	L	L	L	

H = High level, L = Low level, X = H or L, Z = High Impedance, DATA = Contents of Shift Register

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Logic Power Supply	V_{DD1}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to V_{DD1} + 0.5	V
Logic Output Voltage	V_{O1}	−0.5 to V_{DD1} + 0.5	V
Driver Power Supply	V_{DD2}	−0.5 to 250	V
Driver Output Voltage	V_{O2}	−0.5 to V_{DD2} + 0.5	V
Driver Output Current	I_{O2}	±100	mA
Power Dissipation/Package	P_D	1000	mW
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS1} = V_{SS2} = 0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Logic Power Supply	V_{DD1}	4.5	5	5.5	V
High Level Input Voltage	V_{IH}	0.7 V_{DD1}		V_{DD1}	V
Low Level Input Voltage	V_{IL}	0		0.2 V_{DD1}	V
Driver Power Supply	V_{DD2}	80		250	V
Driver Output Current	I_{O2}			±70	mA

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD1} = 5.0 V, V_{DD2} = 250 V, V_{SS1} = V_{SS2} = 0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Output Voltage	V_{OH1}	0.9 V_{DD1}			V	Logic I_{OH1} = 1 mA
Low Level Output Voltage	V_{OL1}			0.1 V_{DD1}	V	Logic I_{OL1} = 1 mA
High Level Output Voltage	V_{OH21}	230	248		V	$O_{1\text{-}40}$, I_{OH2} = −10 mA
	V_{OH22}	200	240		V	$O_{1\text{-}40}$, I_{OH2} = −70 mA
Low Level Output Voltage	V_{OL21}		2	20	V	$O_{1\text{-}40}$, I_{OL2} = 10 mA
	V_{OL22}		35	50	V	$O_{1\text{-}40}$, I_{OH2} = 70 mA
3 State Output Current	I_{TL}			±10	μA	V_{O2} = V_{DD2} or V_{SS2}
3 State Input Current	I_I			±1	μA	V_I = V_{DD1} or V_{SS1}
High Level Input Voltage	V_{IH}	0.7 V_{DD1}			V	
Low Level Input Voltage	V_{IL}			0.2 V_{DD1}	V	
Stand by Current	I_{DD1}			100	μA	Logic
	I_{DD1}			1.0	mA	Logic: T_a = −40 to +85 °C
	I_{DD2}			100	μA	Driver
	I_{DD2}			1.0	mA	Driver: T_a = −40 to +85 °C

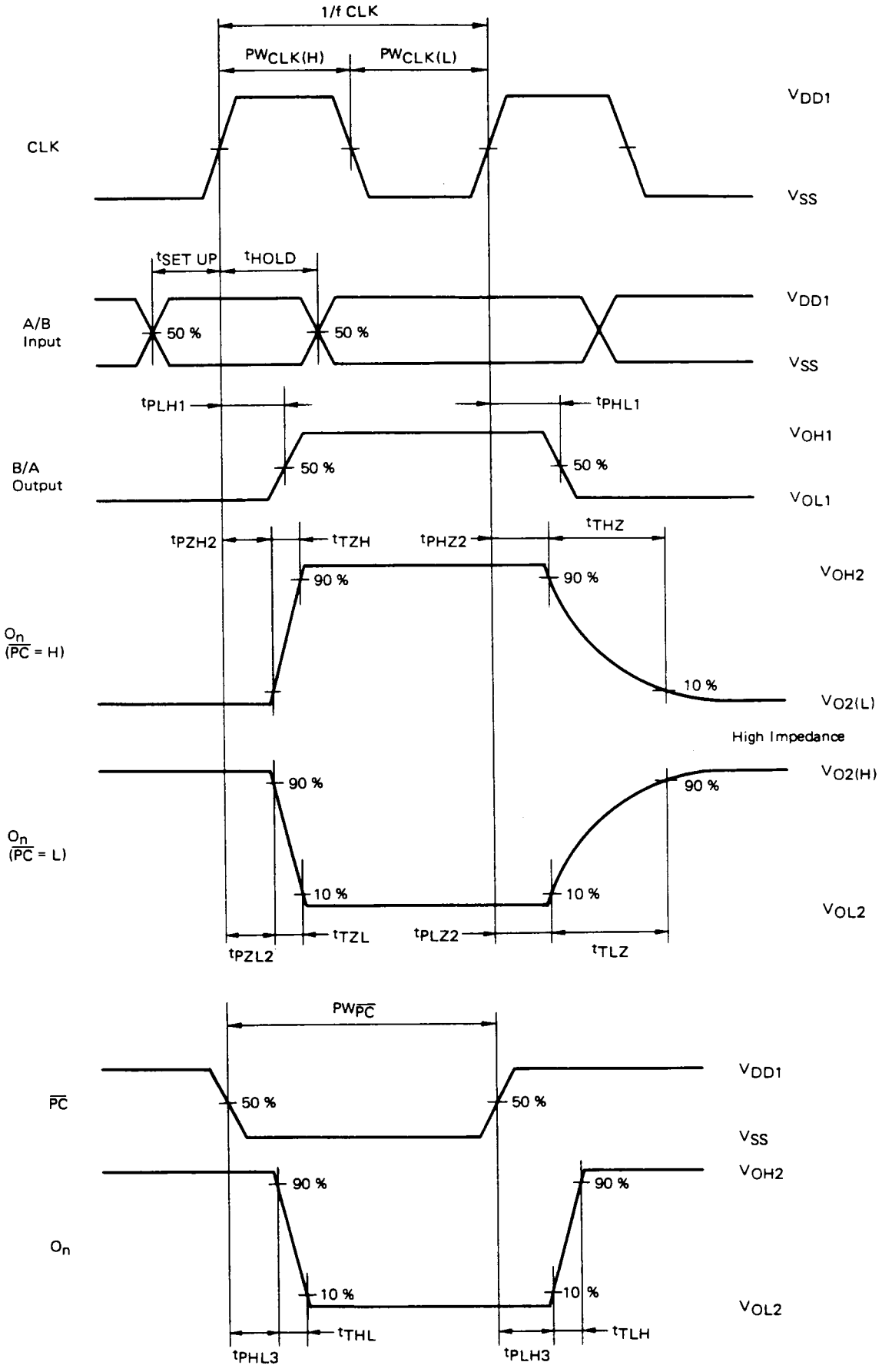
SWITCHING CHARACTERISTICS (T_a = 25 °C, V_{DD1} = 5 V, V_{DD2} = 250 V, V_{SS} = 0 V, C_L (LOGIC) = 15 pF, C_L (DRIVER) = 330 pF, R_L = 10 kΩ)

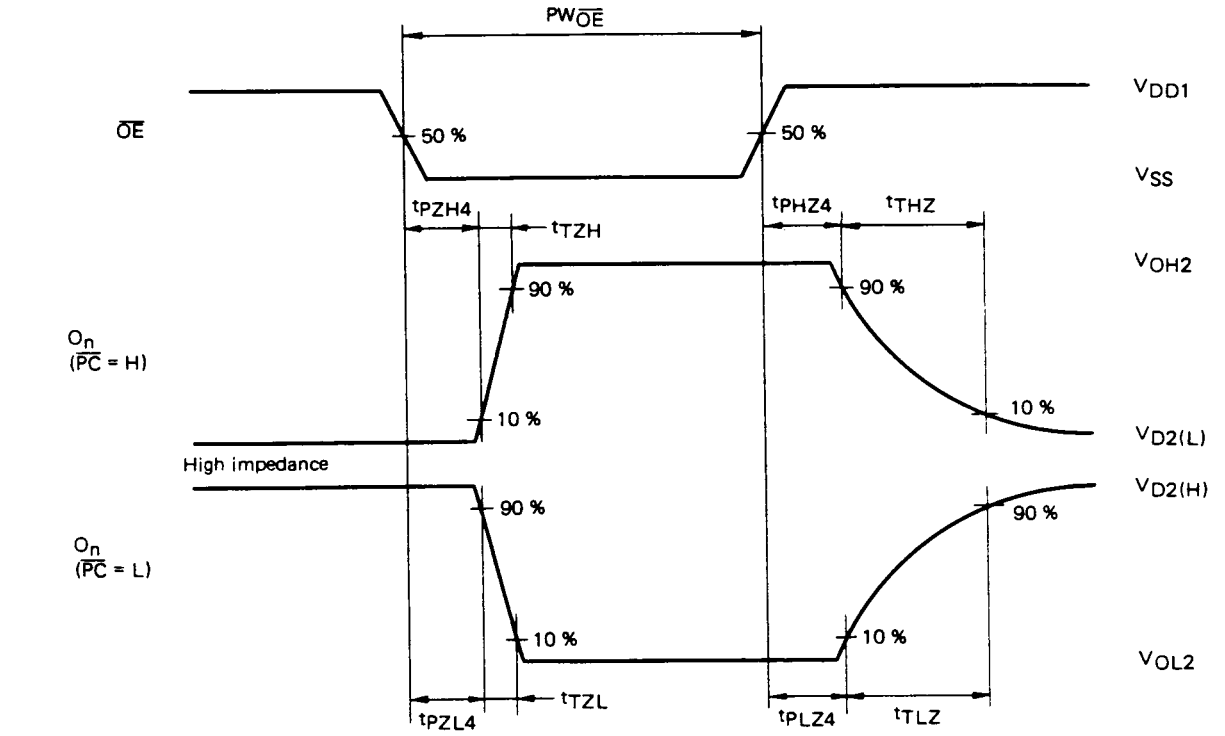
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Output Delay Time	t_{PHL1}		60	100	ns	CLK → A/B
	t_{PLH1}		60	100	ns	
	t_{PZH2}			500	ns	CLK → O_1 to O_{40}
	t_{PZL2}			500	ns	
	t_{PHZ2}			1	μs	
	t_{PLZ2}			1	μs	
	t_{PHL3}			1	μs	$\overline{PC}$ → O_1 to O_{40}
	t_{PLH3}			1	μs	
	t_{PZH4}			500	ns	$\overline{OE}$ → O_1 to O_{40}
	t_{PZL4}			500	ns	
	t_{PHZ4}			1	μs	
	t_{PLZ4}			1	μs	
	t_{PZH5}			500	ns	BLK → O_1 to O_{40}
	t_{PZL5}			500	ns	
	t_{PHZ5}			1	μs	
	t_{PLZ5}			1	μs	
Output Rise Time	t_{TZH}			2	μs	O_1 to O_{40}
	t_{TLH}			2	μs	
	t_{TLZ}			15	μs	
Output Fall Time	t_{TZL}			2	μs	O_1 to O_{40}
	t_{THL}			2	μs	
	t_{THZ}			15	μs	
Maximum Clock Frequency	f_{max}	10	15		MHz	Duty = 50 %
Input Capacitance	C_I		10	15	pF	

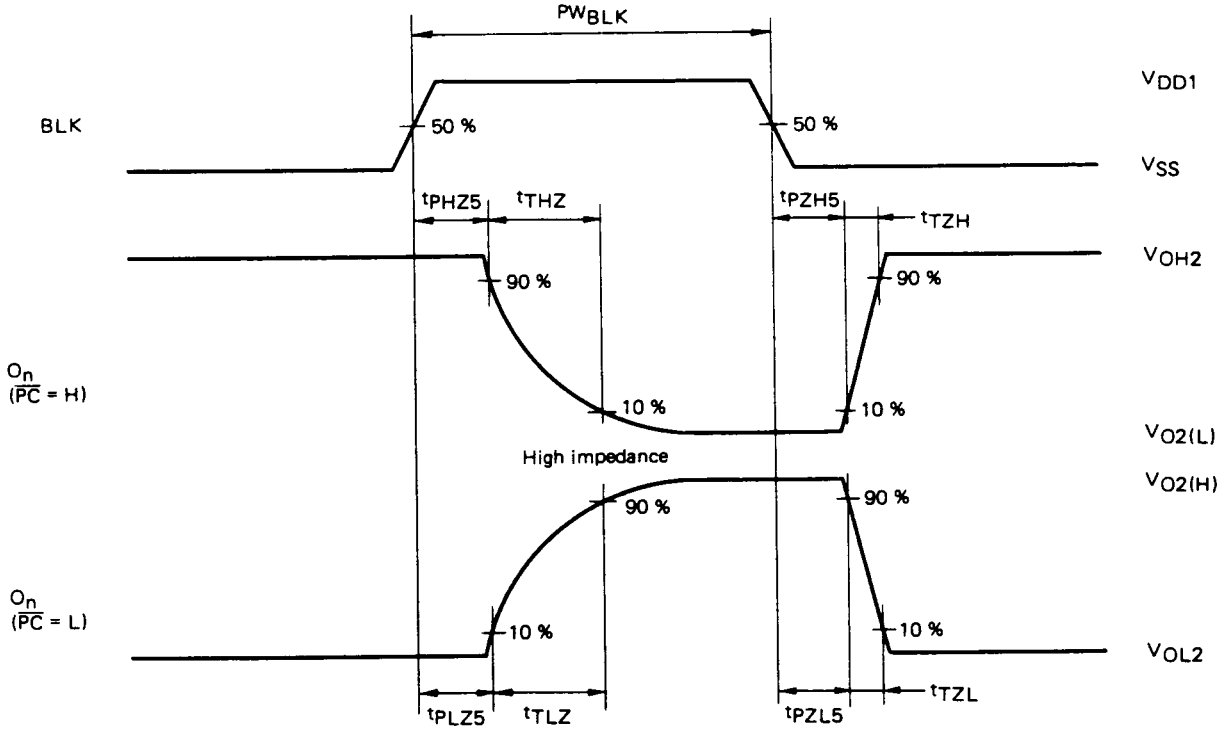
AC TIMING REQUIREMENT (T_a = −40 to +85 °C, V_{DD1} = 4.5 V to 5.5 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock Pulse Width	PW_{CLK}	50			ns	
Blank Pulse Width	PW_{BLK}	3			μs	
$\overline{PC}$ Pulse Width	$PW_{\overline{PC}}$	3			μs	
Enable Pulse Width	$PW_{\overline{OE}}$	3			μs	
Data Setup Time	t_{SETUP}	50			ns	
Data Hold Time	t_{HOLD}	50			ns	

AC CHARACTERISTICS WAVEFORM

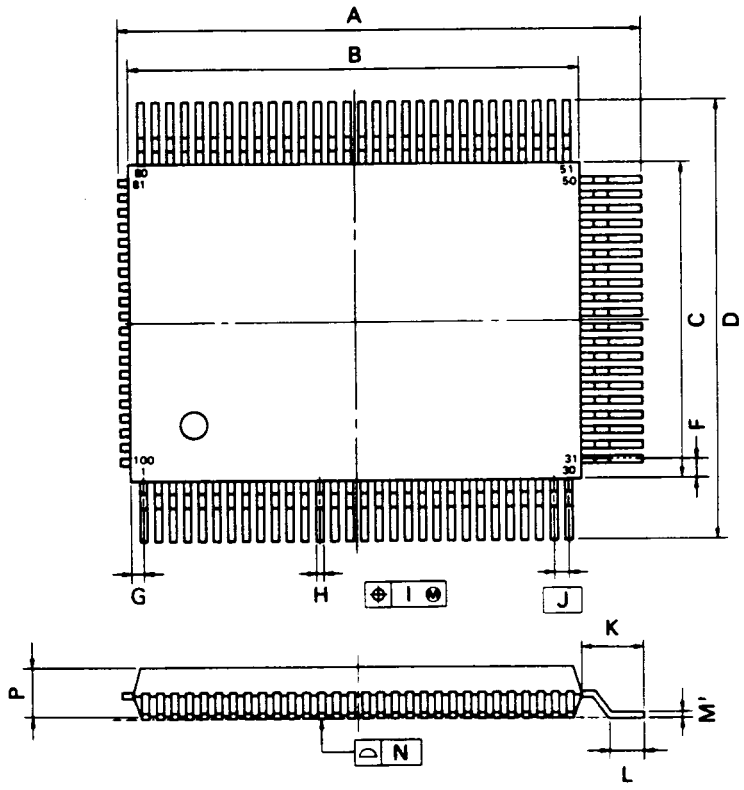



PW$\overline{OE}$
$\overline{OE}$
50 %
50 %
V_{DD1}
V_{SS}
t_{PZH4}
t_{TZH}
t_{PHZ4}
t_{THZ}
V_{OH2}
90 %
90 %
O_n ($\overline{PC}$ = H)
10 %
10 %
$V_{D2(L)}$
High impedance
$V_{D2(H)}$
90 %
90 %
O_n ($\overline{PC}$ = L)
10 %
10 %
V_{OL2}
t_{PZL4}
t_{TZL}
t_{PLZ4}
t_{TLZ}


PW$_{BLK}$
BLK
50 %
50 %
V_{DD1}
V_{SS}
t_{PHZ5}
t_{THZ}
t_{PZH5}
t_{TZH}
V_{OH2}
90 %
90 %
O_n ($\overline{PC}$ = H)
10 %
10 %
$V_{O2(L)}$
High impedance
$V_{O2(H)}$
90 %
90 %
O_n ($\overline{PC}$ = L)
10 %
10 %
V_{OL2}
t_{PLZ5}
t_{TLZ}
t_{PZL5}
t_{TZL}

PACKAGE DIMENSION

100 pin plastic QFP (3 directions leads)



P100GF-65-3LA

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$22.3^{\pm 0.4}$	$0.878^{\pm 0.016}$
B	$20.0^{\pm 0.2}$	$0.795^{+0.008}_{-0.009}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$17.6^{\pm 0.4}$	$0.693^{\pm 0.016}$
F	0.8	0.031
G	0.6	0.024
H	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.