Preliminary Specification

N E C
ELECTRON DEVICE

MOS INTEGRATED CIRCUITS

μPD16301GF

64bit DC • PDP DRIVER

DESCRIPTION

The μPD16301 is a column driver utilized high voltage CMOS process, for DC plasma display panel. It consists of a 64bit bidirectional shift register (32bit shift register×2), latch circuit and high voltage Pch MOS FET.

The logic part operates at 5V (CMOS input level) and the driver part is Pch open drain output, 200V,3mA, MAX..

Features

- High speed CMOS + high voltage Pch MOS structure
- High voltage/current output (-200V, -3mA max.)
- Built-in 2×32bit bidirectional shift register
- Capable of high speed transmission to input even and odd bit separately
- Low power dissipation (1mA max., Ta = -40 ~ +85℃)
- Wide operating temperature (-40 ~ +85℃)

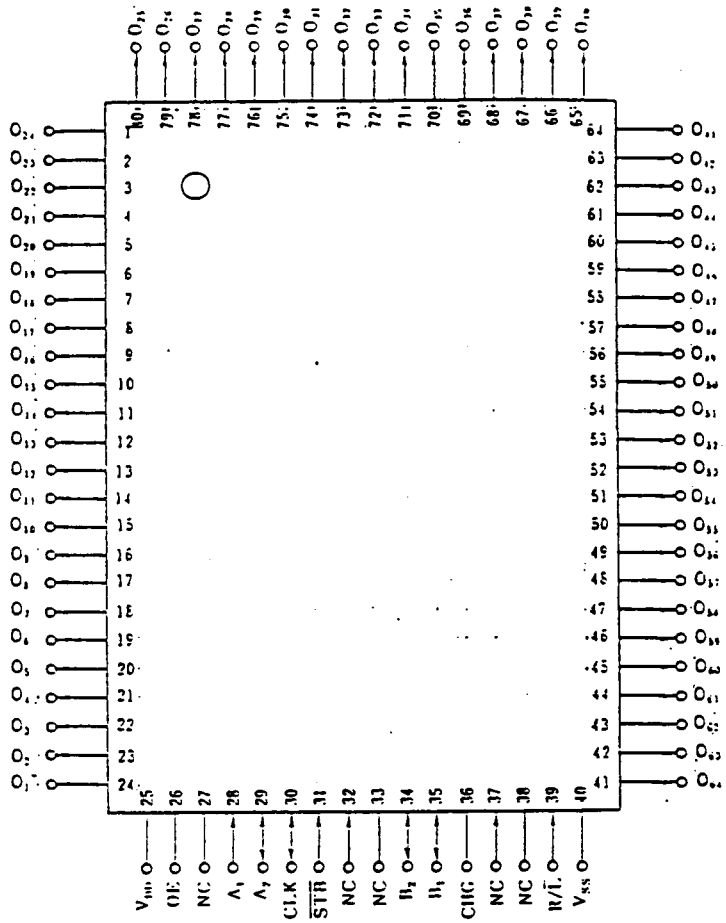
- ORDERING INFORMATION :

  μPD16301GF-3B9 : 80pin Plastic QFP

NEC reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

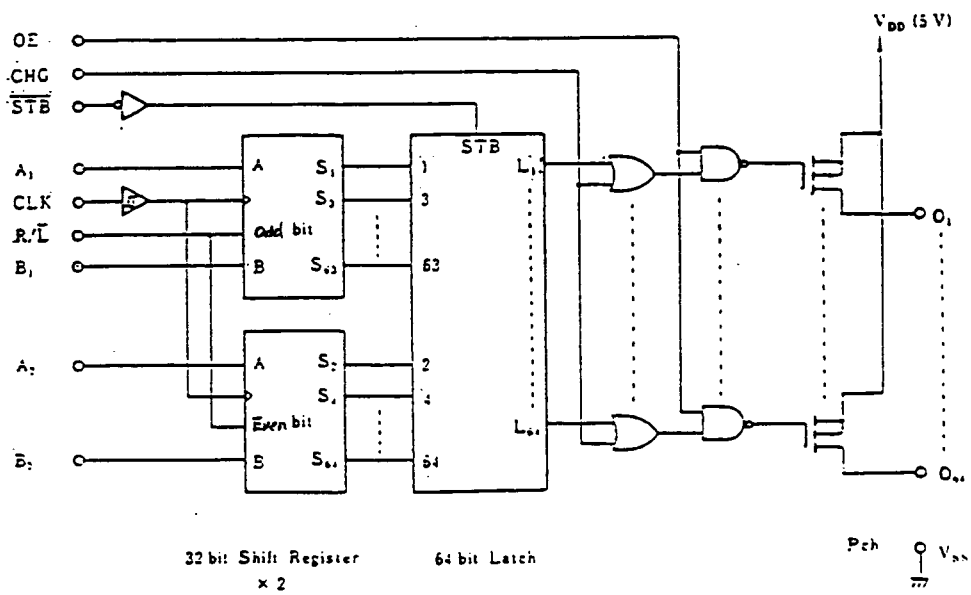
1988, 10th June

(TOP VIEW)



Please open 33pin because of connecting lead frame.

(BLOCK DIAGRAM)



Pin Configuration

SYMBOL	Pin Name	Pin No.	Function
OE	Output Enable Input	26	H : O1-64 Data Output L : O1-64 High Impedance
CHG	CHG Input	36	H : All Output H
A1	Right odd Data I/O	28	Serial data Input/Output A1,B1 : Odd bit A2,B2 : Even bit R/$\overline{L}$=H : A→B R/L=L : B→A
A2	Right even Data I/O	29	
B1	Left odd Data I/O	35	
B2	Left even Data I/O	34	
CLK	Shift Clock Input	30	Positive edge active
$\overline{STB}$	Latch strobe input	31	L : Data through H : Data hold
R/$\overline{L}$	Shift Direction Control Input	39	H : Right shift mode A→O1～O64→B L : Left shift mode B→O64～O1→A
O1 ～O64	High Voltage Output	1-24,41-80	-250V -3mA max.
VDD	Power Supply	25	5V±10%
VSS	Ground	40	—
NC	No Connection	27,32,33,37,38	No connection Please open 33 pin.

Truth Table 1 (Shift Register)

R/L	CLK	A	B	SHIFT REGISTER
H	↑	Input	Output ×1	Data is shifted. (Right shift)
H	H OR L		Output	No change
L	↑	Output ×2	Input	Data is shifted. (Left shift)
L	H OR L	Output		No change

×1 ····· When CLK is positive edge active, S61 shifts to S63 and appears to be B1, and S62 shifts to S64 and appears to be B2.

×2 ····· When CLK is positive edge active, S3 shifts to S1 and appears to be A1, and S4 shifts to S2 and appears to be A2.

Truth Table 2 (Latch, Driver)

DATA	$\overline{STB}$	CHG	OE	Driver Output (O1-64)
×	×	×	L	Z (all driver off)
×	×	H	H	H (all driver on)
L	L	L	H	Z (Driver off)
H	L	L	H	H (Driver on)
×	H	L	H	Data are held just before STB turns H.

DATA = Contents of Shift Register

× = H or L, H = High Level, L = Low Level

Z = High Impedance

Absolute Maximum Ratings
(Ta=25℃, Vss = 0V)

ITEMS	SYMBOL	RATINGS	UNIT
Logic Power Supply	VDD	-0.5～+7.0	V
Input Voltage	VI	-0.5～VDD+0.5	V
Logic Output Voltage	VO1	-0.5～VDD+0.5	V
Driver Output Voltage	VO2	-200～VDD+0.5	V
Driver Maximum current	IO2	-3	mA
Power Dissipation/Package	PD	1000	mW
Operating Temperature	Topt	-40～+85	℃
Storage Temperature	Tstg	-65～+150	℃

Recommended Operating Conditions
(Ta = -40 ～ +85℃, Vss = 0V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.
Logic Power Supply	VDD	4.5	5	5.5	V
High Level Input Voltage	VIH	0.7 VDD		VDD	V
Low Level Input Voltage	VIL	0		0.2 VDD	V
Driver Output Voltage	VO2	VDD		-150	V
Driver Output Current	IO2			-1.2	mA

Electrical Characteristics
(Ta = 25℃, VDD = 4.5~5.5V, Vss = 0V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Output Voltage	VOH1	Logic IOH1=-1mA	0.9 VDD			V
Low Level Output Voltage	VOL1	Logic IOL1=1mA			0.1 VDD	V
Low Level Output Voltage	VOL2	O1-64, IOL2=-1.2mA			VDD-2	V
Output leak current	ITL	VO2=-150V, OE=Vss			-10	μA
Input current	II	VI=VDD or Vss			±1	μA
High Level Input Voltage	VIH		0.7 VDD			V
Low Level Input Voltage	VIL				0.2 VDD	V
Stand by Current	IDD	No Load Ta=-40 ~ +85℃			1.0	mA
		No Load Ta=25℃			100	μA

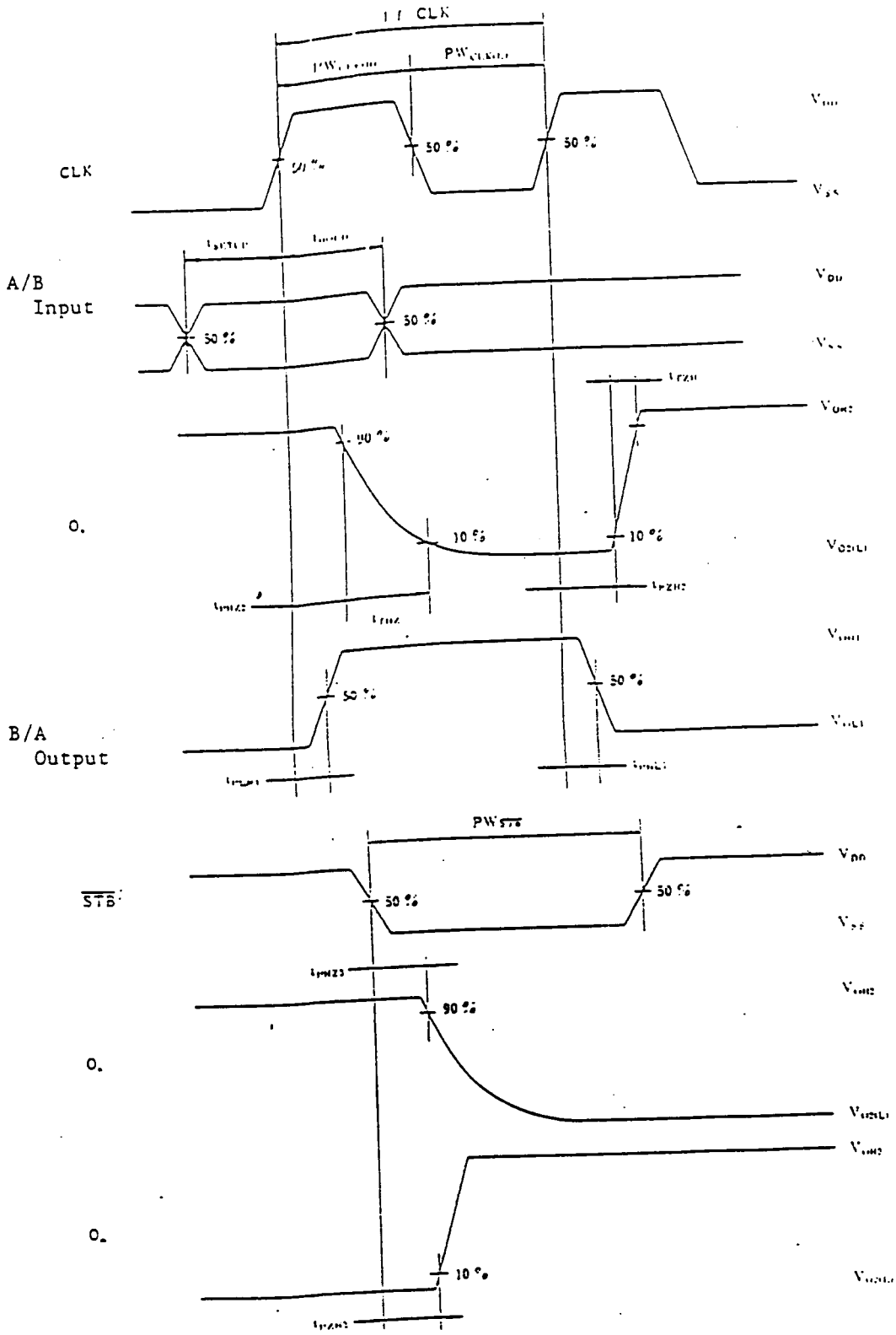
Switching Characteristics
(Ta = 25℃, VDD = 4.5 ~ 5.5V, VO2(L) = −200V
CL=15pF, RL=91KΩ)

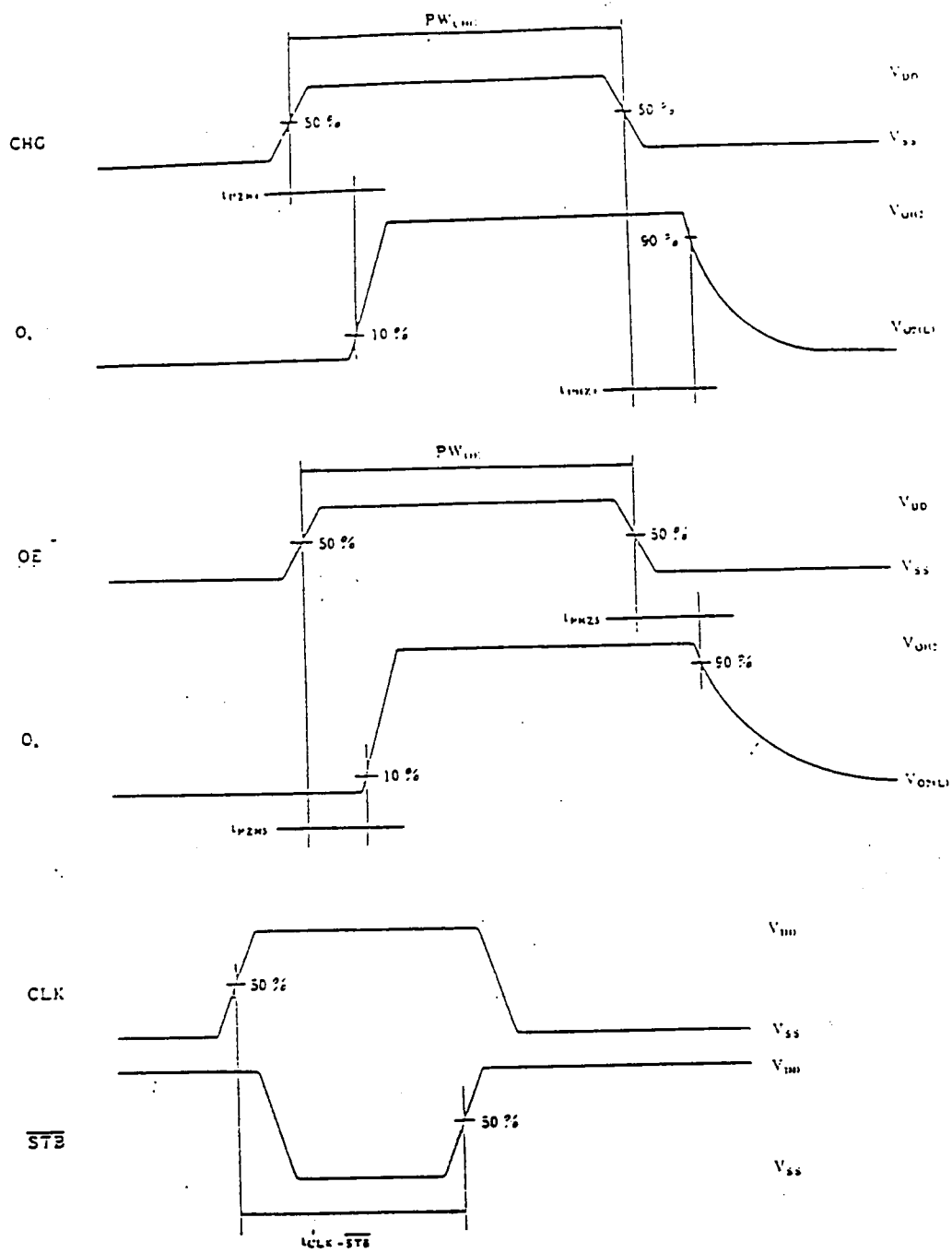
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Delay time	t PHL1	CLK→A/B			100	ns
	t PLH1				100	ns
	t PHZ2	CLK→O1~O64			2.0	μs
	t PZH2				0.8	μs
	t PHZ3	$\overline{STB}$→O1~O64			2.0	μs
	t PZH3				0.75	μs
	t PHZ4	CHG→O1~O64			2.0	μs
	t PZH4				0.7	μs
	t PHZ5	OE→O1~O64			2.0	μs
	t PZH5				0.6	μs
Output Transient Time	t TZH	O1-64			2.0	μs
	t THZ				20	μs
Maximum Clock Frequency	f MAX	Duty=50%	10			MHz
Input Capasitance	CI				10	pF

Timing Requirement Conditions
(Ta = −40 ~ +85℃, VDD1 = 4.5 ~ 5.5V)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	PWCLK		50			ns
OE Pulse Width	PWOE		2.0			μs
Strobe Pulse Width	PW$\overline{STB}$		50			ns
Charge Pulse Width	PWCHG		2.0			μs
Data Setup Time	t SETUP		20			ns
Data Hold Time	t HOLD		10			ns
Setup time	t CLK-STB		100			ns

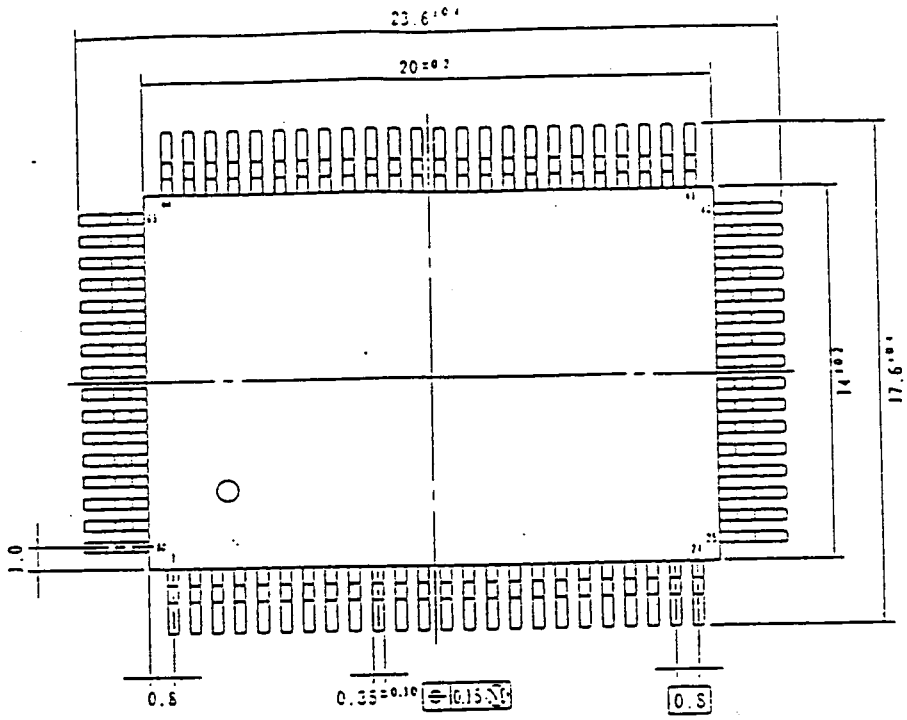
(AC Characteristics Wave Chart)

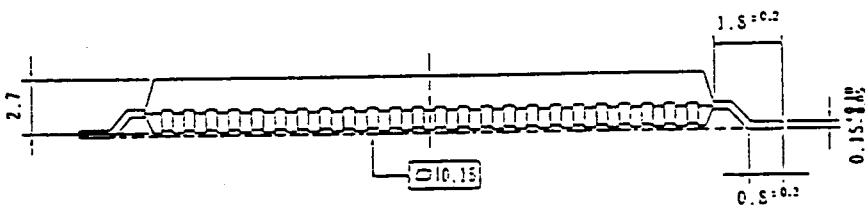


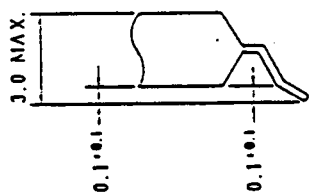

CHG
O.
OE
O.
CLK
STB
50 %
10 %
90 %

=== Out Line ===

(80pin Plastic QFP) unit:mm







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