RENESAS

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD160010

384-/360-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256 GRAY SCALES, mini-LVDS INTERFACE SUPPORTED)

DESCRIPTION

The μPD160010 is a source driver for TFT-LCDS that supports the display of 256 gray scales and employs mini-LVDS interface. Which can realize a full-color display of 16,777,216 colors by output of 256 values γ-corrected by an internal D/A converter and 10-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.2 V to V_{DD2} – 0.2 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Because of the incorporation of mini-LVDS interface, the data transfer speed has improved and the amount of wiring on the PCB has been significantly reduced.

Remark "mini-LVDS" is the technology with Texas Instruments applied LVDS technology and developed.
(LVDS: Low Voltage Differential Signaling)

FEATURES

- Differential interface: CLK, gray scale data,
- CMOS interface: STHR(L), R,/L, STB, SB, POL, O_{sel}, V_{sel1}, V_{sel2}, SRC, ORC, RxBIAS1, RxBIAS2
- 384/360 outputs (O_{sel})
- Capable of outputting 256 values by means of 10-by-2 external power modules (20 units) and a D/A converter
- Logic power supply voltage (V_{DD1}): 2.7 to 3.6V
- Driver power supply voltage (V_{DD2}): 10.0 to 16.5V
- High-speed data transfer: f_{CLK} = 190 MHz MAX. (internal data transfer speed when operating at V_{DD1} = 2.7 V)
- Output dynamic range: V_{SS2} + 0.2 V to V_{DD2} – 0.2 V
- Apply for dot-line inversion, n-line inversion
- Output voltage polarity inversion function (POL)

★ ORDERING INFORMATION

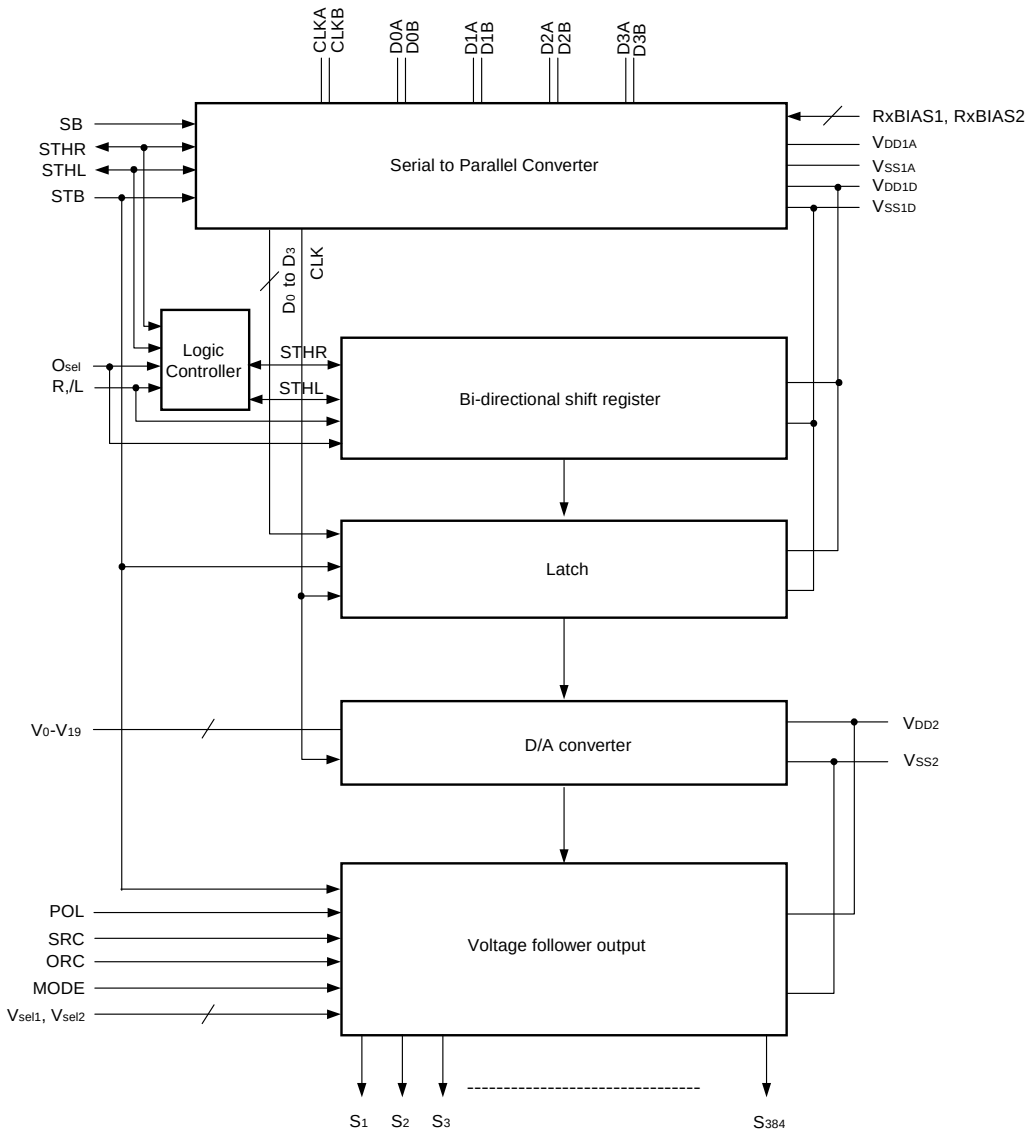
Part Number	Package
μPD160010N-xxx	TCP (TAB package)
μPD160010NL-xxx	COF (COF package)

Remark The TCP/COF's external shape is customized. To order the required shape, please contact one of our sales representatives.

Document No. S16316EJ2V0DS00 (2nd edition)
Date Published March 2004 NS CP (K)
Printed in Japan

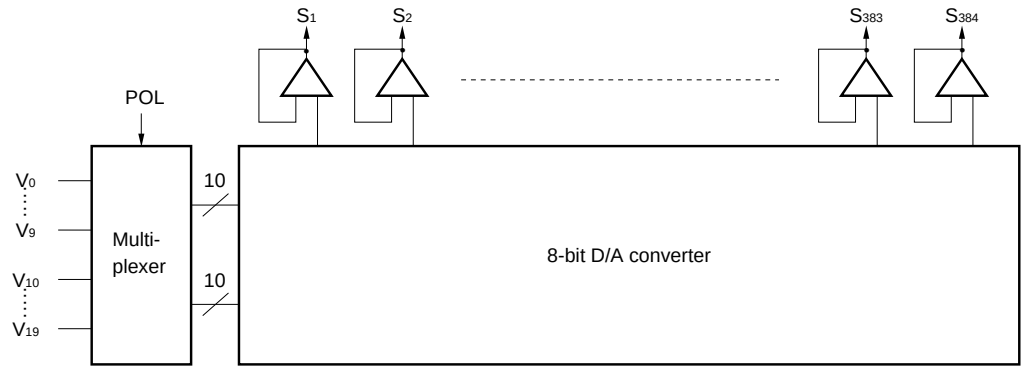
The mark ★ shows major revised points.

★ 1. BLOCK DIAGRAM

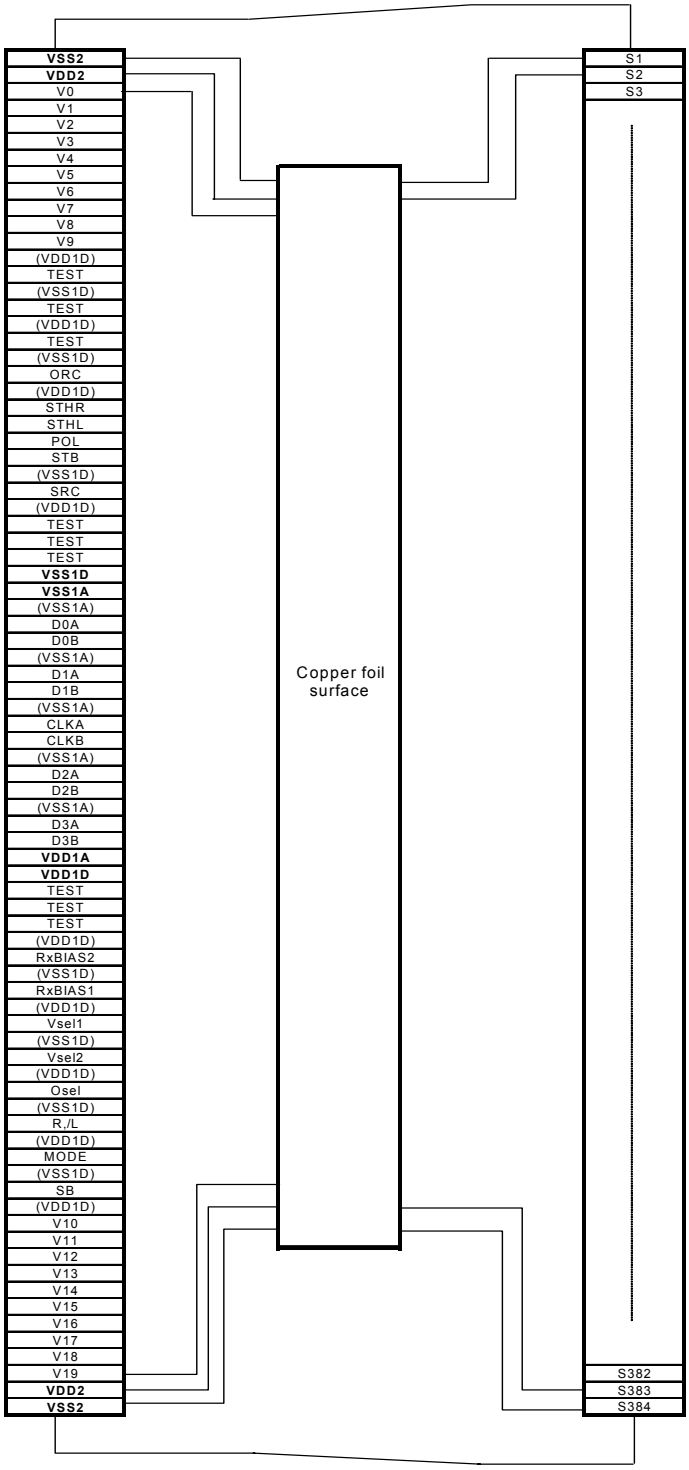


Remark /xxx indicates active low signals.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (μPD160010NL-xxx:COF, Copper Foil Surface, Face-down)



Remarks 1. This figure does not specify the COF package.

2. (V_{DD1D}) and (V_{SS1D}) is available for supply to logic input terminal. Please don't use these pins for power supply terminal with current.

(V_{SS1A}) must be connected to analog GND on PCB.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S_1 to S_{384}	Driver	Output	The D/A converted 256-gray-scale analog voltage is output.
D0A, D0B D1A, D1B D2A, D2B D3A, D3B	Gray scale data	Input (mini-LVDS)	Display data with gray-scale data (8-bit) and control signal (RST = reset). Refer to **Table 4–1**.
CLKA, CLKB	Shift clock	Input (mini-LVDS)	Shift clock. Refer to **Table 4–1**.
R,/L	Shift direction control	Input (CMOS)	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR input, $S_1 \rightarrow S_{384}$, STHL output R,/L = L (left shift): STHL input, $S_{384} \rightarrow S_1$, STHR output
STHR	Right shift start pulse	I/O (CMOS)	This is the start pulse I/O pin when connected in cascade. Loading of display data starts when a high level is read. For right shift, STHR is input and STHL is output. For left shift, STHL is input and STHR is output.
STHL	Left shift start pulse		
STB	Latch	Input (CMOS)	Change the input mode, latched the registered data and transfer to DAC at the rising edge. And supplied voltage to LCD pixel is output at falling edge.
POL	Polarity	Input (CMOS)	Control the polarity of the output. Input of the POL signal is allowed the setup time (t_{14}) with respect to STB's rising edge. Refer to **Table 4–3**.
SB	Bus-line set-back	Input (CMOS)	Change the data order of mini-LVDS input. Refer to **Table 4–1**. Input "L" level to this pin.
RxBIAS1, RxBIAS2	mini-LVDS receiver bias voltage control	Input (CMOS)	This pin controls the bias current of mini-LVDS receiver circuit. Please refer to the following table.
O_{sel}	Number of output pins select pin	Input (CMOS)	This pin selects the number of output pins. O_{sel} = L: 384-output mode O_{sel} = H: 360-output mode Output pins S_{181} through S_{204} are invalid in 360-output mode.
SRC	Slew-rate control	Input (CMOS)	SRC = H: High-slew-rate mode (large current consumption) SRC = L: Low-slew-rate mode (small current consumption)
ORC	Output resistance control	Input (CMOS)	ORC = H: Low output resistance mode ORC = L: High output resistance mode
MODE	Output reset control	Input (CMOS)	MODE = H: Output reset MODE = L: No output reset

RxBIAS1	RxBIAS2	I_{BIAS}
L	L	I_1 (Low power)
L	H	I_2
H	L	I_3
H	H	I_4 (High power)

(2/2)

Pin Symbol	Pin Name	I/O	Description
V_{sel1}, V_{sel2}	V_{DD2} selector	Input (CMOS)	This pin controls the bias current of output amplifier. Logic input to V_{sel1} and V_{sel2} have a dependence on V_{DD2} and load condition and so on. Output waveform simulation should be done before decision. V_{sel1} / V_{sel2} / V_{DD2} Range (reference) L / L / 10.5 V TYP. L / H / 12.5 V TYP. H / L / 16.0 V TYP. H / H / Non-assign
V_0 to V_{19}	γ -corrected power supplies	–	Input the γ -corrected power supplies from outside. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq 0.5\ V_{DD2}$ $0.5\ V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2} + 0.2\ V$
V_{DD1D}	Low-voltage logic power supply	–	2.7 to 3.6 V V_{DD1D} and V_{DD1A} should be same electric potential.
V_{DD1A}	Low-voltage analog power supply	–	2.7 to 3.6 V V_{DD1D} and V_{DD1A} should be same electric potential.
V_{DD2}	Driver power supply	–	10.0 to 16.5 V
V_{SS1D}	Low-voltage logic ground	–	Ground for internal logic circuit. Please wire V_{SS1D} and V_{SS1A} in external circuit boards.
V_{SS1A}	Low-voltage analog ground	–	Ground for internal mini-LVDS receiver circuit. Please wire V_{SS1D} and V_{SS1A} in external circuit boards.
V_{SS2}	Driver ground	–	Ground for internal high voltage circuit.
TEST	TEST	Input (CMOS)	Please leave these pins open in normal operation mode.

Cautions 1. The power start sequence must be V_{DD1}, logic input, and V_{DD2} & V_0-V_{19} in that order. Reverse this sequence to shut down.

2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals (V_0, V_1, V_2,....., V_{19}) and V_{SS2}.

Table 4–1. Function (Bus-line Set-Back)

Pin Name	SB = L
D0A	$D_{0(+)}$
D0B	$D_{0(-)}$
D1A	$D_{1(+)}$
D1B	$D_{1(-)}$
CLKA	$CLK_{(+)}$
CLKB	$CLK_{(-)}$
D2A	$D_{2(+)}$
D2B	$D_{2(-)}$
D3A	$D_{3(+)}$
D3B	$D_{3(-)}$

Remark Suffix "+" indicates positive polarity and "–" indicates negative polarity at each differential signal input pair.

Table 4–2. Function (R,/L and STHR(L))

R,/L	STHR	STHL	Shift Direction
H (Right shift)	IN	OUT	$S_1 \rightarrow S_{384}$
L (Left shift)	OUT	IN	$S_{384} \rightarrow S_1$

Table 4–3. Function (POL and γ-corrected power supplies)

POL	Odd Numbered Output	Even Numbered Output
H	V_{10}-V_{19}	V_0-V_9
L	V_0-V_9	V_{10}-V_{19}

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

μPD160010 incorporates a 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2}, V_{SS2} and common electrode potential V_{COM}, and γ -corrected voltages V_0-V_{19} and the input data. Be sure to maintain the voltage relationships of below.

$$V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq 0.5\ V_{DD2}$$

$$0.5\ V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2} + 0.2\ V$$

Figures 5–2 shows γ-corrected power supply and ladder resistors ratio and figure 5–3 shows the relationship between the input data and the output data.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

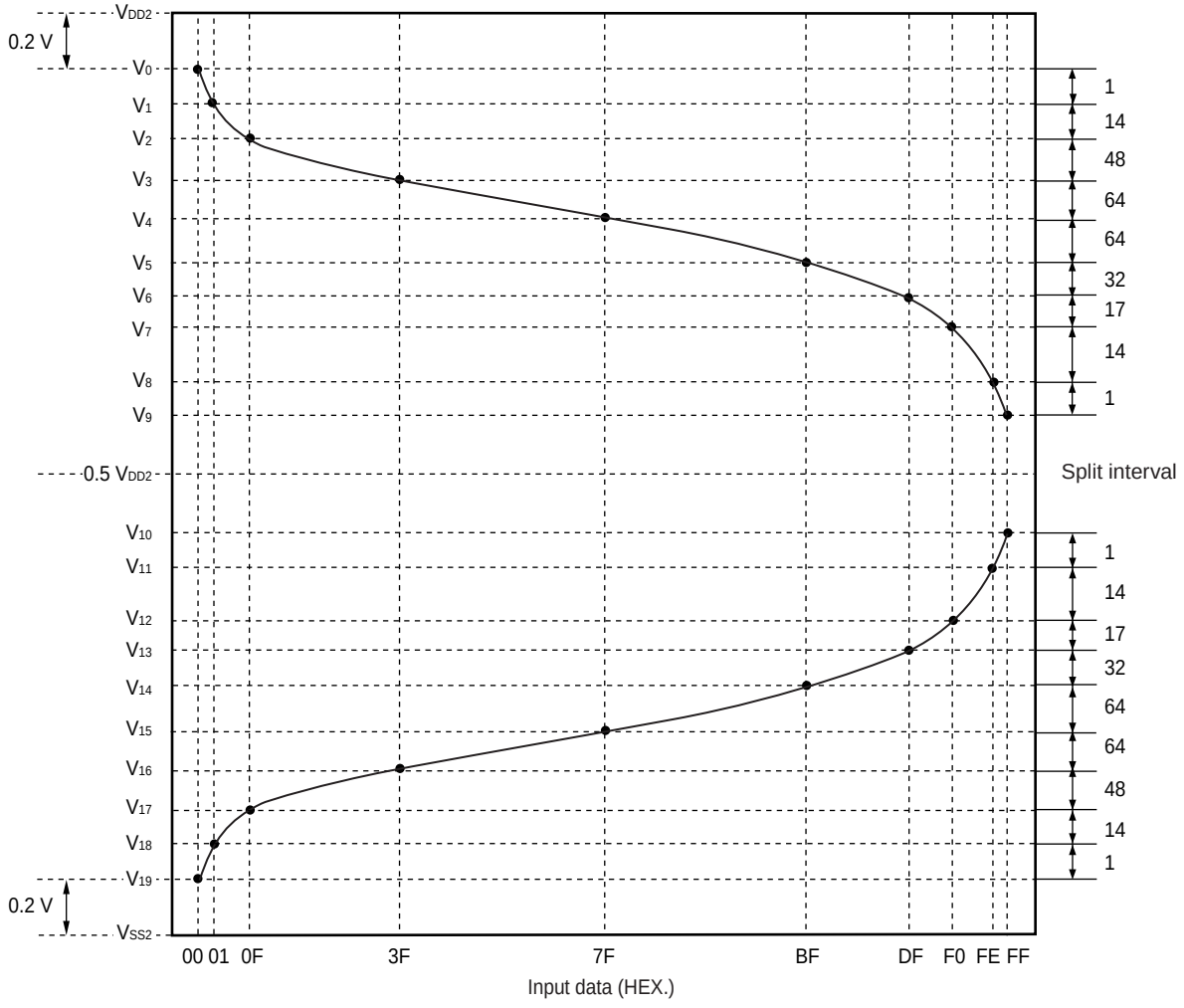
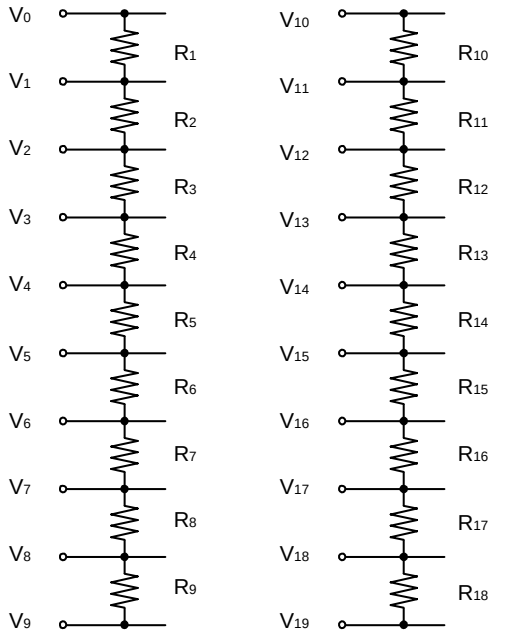


Figure 5–2. γ-corrected Power Supply and Ladder Resistors Ratio



Positive Polarity Negative Polarity

R_1, R_{18}: r_0

R_2, R_{17}: r_1 to r_{14}

R_3, R_{16}: r_{15} to r_{62}

R_4, R_{15}: r_{63} to r_{126}

R_5, R_{14}: r_{127} to r_{190}

R_6, R_{13}: r_{191} to r_{222}

R_7, R_{12}: r_{223} to r_{239}

R_8, R_{11}: r_{240} to r_{253}

R_9, R_{10}: r_{254}

R_n	Ratio
R_1, R_{18}	173
R_2, R_{17}	1475
R_3, R_{16}	2419
R_4, R_{15}	2083
R_5, R_{14}	1940
R_6, R_{13}	1219
R_7, R_{12}	794
R_8, R_{13}	1373
R_9, R_{10}	525

rn	Ratio	rn	Ratio	rn	Ratio	rn	Ratio
r0	173	r64	38	r128	29	r192	34
r1	155	r65	37	r129	29	r193	34
r2	142	r66	37	r130	29	r194	35
r3	131	r67	37	r131	29	r195	35
r4	122	r68	37	r132	29	r196	35
r5	114	r69	36	r133	29	r197	35
r6	107	r70	36	r134	29	r198	35
r7	102	r71	36	r135	29	r199	36
r8	97	r72	36	r136	29	r200	36
r9	93	r73	35	r137	29	r201	36
r10	89	r74	35	r138	29	r202	37
r11	85	r75	35	r139	29	r203	37
r12	82	r76	35	r140	29	r204	37
r13	79	r77	35	r141	29	r205	37
r14	77	r78	34	r142	29	r206	38
r15	74	r79	34	r143	29	r207	38
r16	72	r80	34	r144	29	r208	38
r17	70	r81	34	r145	29	r209	39
r18	69	r82	34	r146	29	r210	39
r19	67	r83	34	r147	29	r211	39
r20	65	r84	33	r148	29	r212	40
r21	64	r85	33	r149	29	r213	40
r22	62	r86	33	r150	29	r214	40
r23	61	r87	33	r151	29	r215	41
r24	60	r88	33	r152	30	r216	41
r25	59	r89	33	r153	30	r217	41
r26	58	r90	33	r154	30	r218	42
r27	57	r91	32	r155	30	r219	42
r28	56	r92	32	r156	30	r220	42
r29	55	r93	32	r157	30	r221	43
r30	54	r94	32	r158	30	r222	43
r31	53	r95	32	r159	30	r223	43
r32	52	r96	32	r160	30	r224	44
r33	51	r97	32	r161	30	r225	44
r34	51	r98	32	r162	30	r226	44
r35	50	r99	31	r163	30	r227	45
r36	49	r100	31	r164	30	r228	45
r37	49	r101	31	r165	30	r229	46
r38	48	r102	31	r166	30	r230	46
r39	47	r103	31	r167	30	r231	46
r40	47	r104	31	r168	31	r232	47
r41	46	r105	31	r169	31	r233	47
r42	46	r106	31	r170	31	r234	48
r43	45	r107	31	r171	31	r235	48
r44	45	r108	31	r172	31	r236	49
r45	44	r109	30	r173	31	r237	50
r46	44	r110	30	r174	31	r238	50
r47	43	r111	30	r175	31	r239	52
r48	43	r112	30	r176	31	r240	53
r49	43	r113	30	r177	32	r241	55
r50	42	r114	30	r178	32	r242	57
r51	42	r115	30	r179	32	r243	59
r52	41	r116	30	r180	32	r244	62
r53	41	r117	30	r181	32	r245	66
r54	41	r118	30	r182	32	r246	71
r55	40	r119	30	r183	32	r247	78
r56	40	r120	30	r184	33	r248	86
r57	40	r121	30	r185	33	r249	98
r58	39	r122	30	r186	33	r250	114
r59	39	r123	30	r187	33	r251	138
r60	39	r124	30	r188	33	r252	178
r61	38	r125	30	r189	33	r253	258
r62	38	r126	29	r190	34	r254	525
r63	38	r127	29	r191	34		

Figure 5–3. Relationship between Input Data and Output Voltage (1/2)

(Output voltage) $V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq 0.5\ V_{DD2}$

Data	Output Voltage		Data	Output Voltage		Data	Output Voltage		Data	Output Voltage	
00H	V0	V0	40H	V64'	V4+(V3-V4) X 2045 / 2083	80H	V128	V5+(V4-V5) X 1911 / 1940	C0H	V192	V6+(V5-V6) X 1185 / 1219
01H	V1'	V1	41H	V65	V4+(V3-V4) X 2007 / 2083	81H	V129	V5+(V4-V5) X 1882 / 1940	C1H	V193	V6+(V5-V6) X 1151 / 1219
02H	V2	V2+(V1-V2) X 1320 / 1475	42H	V66	V4+(V3-V4) X 1970 / 2083	82H	V130	V5+(V4-V5) X 1853 / 1940	C2H	V194'	V6+(V5-V6) X 1117 / 1219
03H	V3	V2+(V1-V2) X 1178 / 1475	43H	V67	V4+(V3-V4) X 1933 / 2083	83H	V131'	V5+(V4-V5) X 1824 / 1940	C3H	V195	V6+(V5-V6) X 1082 / 1219
04H	V4'	V2+(V1-V2) X 1047 / 1475	44H	V68	V4+(V3-V4) X 1896 / 2083	84H	V132	V5+(V4-V5) X 1795 / 1940	C4H	V196	V6+(V5-V6) X 1047 / 1219
05H	V5	V2+(V1-V2) X 925 / 1475	45H	V69	V4+(V3-V4) X 1859 / 2083	85H	V133	V5+(V4-V5) X 1766 / 1940	C5H	V197	V6+(V5-V6) X 1012 / 1219
06H	V6	V2+(V1-V2) X 811 / 1475	46H	V70	V4+(V3-V4) X 1823 / 2083	86H	V134'	V5+(V4-V5) X 1737 / 1940	C6H	V198	V6+(V5-V6) X 977 / 1219
07H	V7	V2+(V1-V2) X 704 / 1475	47H	V71'	V4+(V3-V4) X 1787 / 2083	87H	V135	V5+(V4-V5) X 1708 / 1940	C7H	V199	V6+(V5-V6) X 942 / 1219
08H	V8	V2+(V1-V2) X 602 / 1475	48H	V72	V4+(V3-V4) X 1751 / 2083	88H	V136	V5+(V4-V5) X 1679 / 1940	C8H	V200	V6+(V5-V6) X 906 / 1219
09H	V9	V2+(V1-V2) X 505 / 1475	49H	V73	V4+(V3-V4) X 1715 / 2083	89H	V137	V5+(V4-V5) X 1650 / 1940	C9H	V201'	V6+(V5-V6) X 870 / 1219
0AH	V10'	V2+(V1-V2) X 412 / 1475	4AH	V74'	V4+(V3-V4) X 1680 / 2083	8AH	V138	V5+(V4-V5) X 1621 / 1940	CAH	V202	V6+(V5-V6) X 834 / 1219
0BH	V11'	V2+(V1-V2) X 323 / 1475	4BH	V75	V4+(V3-V4) X 1645 / 2083	8BH	V139	V5+(V4-V5) X 1592 / 1940	CBH	V203	V6+(V5-V6) X 797 / 1219
0CH	V12	V2+(V1-V2) X 238 / 1475	4CH	V76	V4+(V3-V4) X 1610 / 2083	8CH	V140	V5+(V4-V5) X 1563 / 1940	CCH	V204'	V6+(V5-V6) X 760 / 1219
0DH	V13	V2+(V1-V2) X 156 / 1475	4DH	V77	V4+(V3-V4) X 1575 / 2083	8DH	V141'	V5+(V4-V5) X 1534 / 1940	CDH	V205	V6+(V5-V6) X 723 / 1219
0EH	V14'	V2+(V1-V2) X 77 / 1475	4EH	V78	V4+(V3-V4) X 1540 / 2083	8EH	V142	V5+(V4-V5) X 1505 / 1940	CEH	V206	V6+(V5-V6) X 686 / 1219
0FH	V15'	V2	4FH	V79	V4+(V3-V4) X 1506 / 2083	8FH	V143	V5+(V4-V5) X 1476 / 1940	CFH	V207'	V6+(V5-V6) X 648 / 1219
10H	V16	V3+(V2-V3) X 2345 / 2419	50H	V80	V4+(V3-V4) X 1472 / 2083	90H	V144'	V5+(V4-V5) X 1447 / 1940	D0H	V208	V6+(V5-V6) X 610 / 1219
11H	V17	V3+(V2-V3) X 2273 / 2419	51H	V81'	V4+(V3-V4) X 1438 / 2083	91H	V145	V5+(V4-V5) X 1418 / 1940	D1H	V209	V6+(V5-V6) X 572 / 1219
12H	V18	V3+(V2-V3) X 2203 / 2419	52H	V82	V4+(V3-V4) X 1404 / 2083	92H	V146	V5+(V4-V5) X 1389 / 1940	D2H	V210	V6+(V5-V6) X 533 / 1219
13H	V19	V3+(V2-V3) X 2134 / 2419	53H	V83	V4+(V3-V4) X 1370 / 2083	93H	V147	V5+(V4-V5) X 1360 / 1940	D3H	V211'	V6+(V5-V6) X 494 / 1219
14H	V20	V3+(V2-V3) X 2067 / 2419	54H	V84'	V4+(V3-V4) X 1336 / 2083	94H	V148	V5+(V4-V5) X 1331 / 1940	D4H	V212	V6+(V5-V6) X 455 / 1219
15H	V21'	V3+(V2-V3) X 2002 / 2419	55H	V85	V4+(V3-V4) X 1303 / 2083	95H	V149	V5+(V4-V5) X 1302 / 1940	D5H	V213	V6+(V5-V6) X 415 / 1219
16H	V22	V3+(V2-V3) X 1938 / 2419	56H	V86	V4+(V3-V4) X 1270 / 2083	96H	V150	V5+(V4-V5) X 1273 / 1940	D6H	V214'	V6+(V5-V6) X 375 / 1219
17H	V23	V3+(V2-V3) X 1876 / 2419	57H	V87	V4+(V3-V4) X 1237 / 2083	97H	V151'	V5+(V4-V5) X 1244 / 1940	D7H	V215	V6+(V5-V6) X 335 / 1219
18H	V24'	V3+(V2-V3) X 1815 / 2419	58H	V88	V4+(V3-V4) X 1204 / 2083	98H	V152	V5+(V4-V5) X 1215 / 1940	D8H	V216	V6+(V5-V6) X 294 / 1219
19H	V25	V3+(V2-V3) X 1755 / 2419	59H	V89	V4+(V3-V4) X 1171 / 2083	99H	V153	V5+(V4-V5) X 1185 / 1940	D9H	V217	V6+(V5-V6) X 253 / 1219
1AH	V26	V3+(V2-V3) X 1696 / 2419	5AH	V90	V4+(V3-V4) X 1138 / 2083	9AH	V154'	V5+(V4-V5) X 1155 / 1940	DAH	V218	V6+(V5-V6) X 212 / 1219
1BH	V27	V3+(V2-V3) X 1638 / 2419	5BH	V91'	V4+(V3-V4) X 1105 / 2083	9BH	V155	V5+(V4-V5) X 1125 / 1940	DBH	V219	V6+(V5-V6) X 170 / 1219
1CH	V28	V3+(V2-V3) X 1581 / 2419	5CH	V92	V4+(V3-V4) X 1073 / 2083	9CH	V156	V5+(V4-V5) X 1095 / 1940	DCH	V220	V6+(V5-V6) X 128 / 1219
1DH	V29	V3+(V2-V3) X 1525 / 2419	5DH	V93	V4+(V3-V4) X 1041 / 2083	9DH	V157	V5+(V4-V5) X 1065 / 1940	DDH	V221'	V6+(V5-V6) X 86 / 1219
1EH	V30	V3+(V2-V3) X 1470 / 2419	5EH	V94'	V4+(V3-V4) X 1009 / 2083	9EH	V158	V5+(V4-V5) X 1035 / 1940	DEH	V222	V6+(V5-V6) X 43 / 1219
1FH	V31'	V3+(V2-V3) X 1416 / 2419	5FH	V95	V4+(V3-V4) X 977 / 2083	9FH	V159	V5+(V4-V5) X 1005 / 1940	DFH	V223	V6
20H	V32	V3+(V2-V3) X 1363 / 2419	60H	V96	V4+(V3-V4) X 945 / 2083	A0H	V160	V5+(V4-V5) X 975 / 1940	E0H	V224'	V7+(V6-V7) X 751 / 794
21H	V33	V3+(V2-V3) X 1311 / 2419	61H	V97	V4+(V3-V4) X 913 / 2083	A1H	V161'	V5+(V4-V5) X 945 / 1940	E1H	V225	V7+(V6-V7) X 707 / 794
22H	V34'	V3+(V2-V3) X 1260 / 2419	62H	V98	V4+(V3-V4) X 881 / 2083	A2H	V162	V5+(V4-V5) X 915 / 1940	E2H	V226	V7+(V6-V7) X 663 / 794
23H	V35	V3+(V2-V3) X 1209 / 2419	63H	V99	V4+(V3-V4) X 849 / 2083	A3H	V163'	V5+(V4-V5) X 885 / 1940	E3H	V227'	V7+(V6-V7) X 619 / 794
24H	V36	V3+(V2-V3) X 1159 / 2419	64H	V100	V4+(V3-V4) X 818 / 2083	A4H	V164'	V5+(V4-V5) X 855 / 1940	E4H	V228	V7+(V6-V7) X 574 / 794
25H	V37	V3+(V2-V3) X 1110 / 2419	65H	V101'	V4+(V3-V4) X 787 / 2083	A5H	V165	V5+(V4-V5) X 825 / 1940	E5H	V229	V7+(V6-V7) X 529 / 794
26H	V38	V3+(V2-V3) X 1061 / 2419	66H	V102	V4+(V3-V4) X 756 / 2083	A6H	V166	V5+(V4-V5) X 795 / 1940	E6H	V230	V7+(V6-V7) X 483 / 794
27H	V39	V3+(V2-V3) X 1013 / 2419	67H	V103	V4+(V3-V4) X 725 / 2083	A7H	V167	V5+(V4-V5) X 765 / 1940	E7H	V231'	V7+(V6-V7) X 437 / 794
28H	V40	V3+(V2-V3) X 966 / 2419	68H	V104'	V4+(V3-V4) X 694 / 2083	A8H	V168	V5+(V4-V5) X 735 / 1940	E8H	V232	V7+(V6-V7) X 391 / 794
29H	V41'	V3+(V2-V3) X 919 / 2419	69H	V105	V4+(V3-V4) X 663 / 2083	A9H	V169	V5+(V4-V5) X 704 / 1940	E9H	V233	V7+(V6-V7) X 344 / 794
2AH	V42	V3+(V2-V3) X 873 / 2419	6AH	V106	V4+(V3-V4) X 632 / 2083	AAH	V170	V5+(V4-V5) X 673 / 1940	EAH	V234'	V7+(V6-V7) X 297 / 794
2BH	V43	V3+(V2-V3) X 827 / 2419	6BH	V107	V4+(V3-V4) X 601 / 2083	ABH	V171'	V5+(V4-V5) X 642 / 1940	EBH	V235	V7+(V6-V7) X 249 / 794
2CH	V44'	V3+(V2-V3) X 782 / 2419	6CH	V108	V4+(V3-V4) X 570 / 2083	ACH	V172	V5+(V4-V5) X 611 / 1940	ECH	V236	V7+(V6-V7) X 201 / 794
2DH	V45	V3+(V2-V3) X 737 / 2419	6DH	V109	V4+(V3-V4) X 539 / 2083	ADH	V173	V5+(V4-V5) X 580 / 1940	EDH	V237	V7+(V6-V7) X 152 / 794
2EH	V46	V3+(V2-V3) X 693 / 2419	6EH	V110	V4+(V3-V4) X 509 / 2083	AEH	V174'	V5+(V4-V5) X 549 / 1940	EEH	V238	V7+(V6-V7) X 102 / 794
2FH	V47	V3+(V2-V3) X 649 / 2419	6FH	V111'	V4+(V3-V4) X 479 / 2083	AFH	V175	V5+(V4-V5) X 518 / 1940	EFH	V239	V7+(V6-V7) X 52 / 794
30H	V48	V3+(V2-V3) X 606 / 2419	70H	V112	V4+(V3-V4) X 449 / 2083	B0H	V176	V5+(V4-V5) X 487 / 1940	F0H	V240	V7
31H	V49	V3+(V2-V3) X 563 / 2419	71H	V113	V4+(V3-V4) X 419 / 2083	B1H	V177	V5+(V4-V5) X 456 / 1940	F1H	V241'	V8+(V7-V8) X 1320 / 1373
32H	V50	V3+(V2-V3) X 520 / 2419	72H	V114'	V4+(V3-V4) X 389 / 2083	B2H	V178	V5+(V4-V5) X 424 / 1940	F2H	V242	V8+(V7-V8) X 1265 / 1373
33H	V51'	V3+(V2-V3) X 478 / 2419	73H	V115	V4+(V3-V4) X 359 / 2083	B3H	V179	V5+(V4-V5) X 392 / 1940	F3H	V243	V8+(V7-V8) X 1208 / 1373
34H	V52	V3+(V2-V3) X 436 / 2419	74H	V116	V4+(V3-V4) X 329 / 2083	B4H	V180	V5+(V4-V5) X 360 / 1940	F4H	V244'	V8+(V7-V8) X 1149 / 1373
35H	V53	V3+(V2-V3) X 395 / 2419	75H	V117	V4+(V3-V4) X 299 / 2083	B5H	V181'	V5+(V4-V5) X 328 / 1940	F5H	V245	V8+(V7-V8) X 1087 / 1373
36H	V54'	V3+(V2-V3) X 354 / 2419	76H	V118	V4+(V3-V4) X 269 / 2083	B6H	V182	V5+(V4-V5) X 296 / 1940	F6H	V246	V8+(V7-V8) X 1021 / 1373
37H	V55	V3+(V2-V3) X 313 / 2419	77H	V119	V4+(V3-V4) X 239 / 2083	B7H	V183	V5+(V4-V5) X 264 / 1940	F7H	V247	V8+(V7-V8) X 960 / 1373
38H	V56	V3+(V2-V3) X 273 / 2419	78H	V120	V4+(V3-V4) X 209 / 2083	B8H	V184'	V5+(V4-V5) X 232 / 1940	F8H	V248	V8+(V7-V8) X 872 / 1373
39H	V57	V3+(V2-V3) X 233 / 2419	79H	V121'	V4+(V3-V4) X 179 / 2083	B9H	V185	V5+(V4-V5) X 199 / 1940	F9H	V249	V8+(V7-V8) X 786 / 1373
3AH	V58	V3+(V2-V3) X 193 / 2419	7AH	V122	V4+(V3-V4) X 149 / 2083	BAH	V186	V5+(V4-V5) X 166 / 1940	FAH	V250	V8+(V7-V8) X 688 / 1373
3BH	V59	V3+(V2-V3) X 154 / 2419	7BH	V123	V4+(V3-V4) X 119 / 2083	BBH	V187'	V5+(V4-V5) X 133 / 1940	FBH	V251'	V8+(V7-V8) X 574 / 1373
3CH	V60	V3+(V2-V3) X 115 / 2419	7CH	V124'	V4+(V3-V4) X 89 / 2083	BCH	V188	V5+(V4-V5) X 100 / 1940	FCH	V252	V8+(V7-V8) X 436 / 1373
3DH	V61'	V3+(V2-V3) X 76 / 2419	7DH	V125	V4+(V3-V4) X 59 / 2083	BDH	V189	V5+(V4-V5) X 67 / 1940	FDH	V253	V8+(V7-V8) X 258 / 1373
3EH	V62	V3+(V2-V3) X 38 / 2419	7EH	V126	V4+(V3-V4) X 29 / 2083	BEH	V190	V5+(V4-V5) X 34 / 1940	FEH	V254'	V8
3FH	V63	V3	7FH	V127	V4	BFH	V191'	V5	FFH	V255	V9

Figure 5–3. Relationship between Input Data and Output Voltage (2/2)

(Output voltage) 0.5 $V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2}$ + 0.2 V

Data	Output Voltage	Data	Output Voltage	Data	Output Voltage	Data	Output Voltage
00H	\V0" V19	40H	\V64" V16+(V15-V16) X 38 / 2083	80H	V128" V15+(V14-V15) X 29 / 1940	C0H	V192" V14+(V13-V14) X 34 / 1219
01H	\V1" V18	41H	\V65" V16+(V15-V16) X 76 / 2083	81H	V129" V15+(V14-V15) X 58 / 1940	C1H	V193" V14+(V13-V14) X 68 / 1219
02H	\V2" V18+(V17-V18) X 155 / 1475	42H	\V66" V16+(V15-V16) X 113 / 2083	82H	V130" V15+(V14-V15) X 87 / 1940	C2H	V194" V14+(V13-V14) X 102 / 1219
03H	\V3" V18+(V17-V18) X 297 / 1475	43H	\V67" V16+(V15-V16) X 150 / 2083	83H	V131" V15+(V14-V15) X 116 / 1940	C3H	V195" V14+(V13-V14) X 137 / 1219
04H	\V4" V18+(V17-V18) X 428 / 1475	44H	\V68" V16+(V15-V16) X 187 / 2083	84H	V132" V15+(V14-V15) X 145 / 1940	C4H	V196" V14+(V13-V14) X 172 / 1219
05H	\V5" V18+(V17-V18) X 550 / 1475	45H	\V69" V16+(V15-V16) X 224 / 2083	85H	V133" V15+(V14-V15) X 174 / 1940	C5H	V197" V14+(V13-V14) X 207 / 1219
06H	\V6" V18+(V17-V18) X 664 / 1475	46H	\V70" V16+(V15-V16) X 260 / 2083	86H	V134" V15+(V14-V15) X 203 / 1940	C6H	V198" V14+(V13-V14) X 242 / 1219
07H	\V7" V18+(V17-V18) X 771 / 1475	47H	\V71" V16+(V15-V16) X 296 / 2083	87H	V135" V15+(V14-V15) X 232 / 1940	C7H	V199" V14+(V13-V14) X 277 / 1219
08H	\V8" V18+(V17-V18) X 873 / 1475	48H	\V72" V16+(V15-V16) X 332 / 2083	88H	V136" V15+(V14-V15) X 261 / 1940	C8H	V200" V14+(V13-V14) X 313 / 1219
09H	\V9" V18+(V17-V18) X 970 / 1475	49H	\V73" V16+(V15-V16) X 368 / 2083	89H	V137" V15+(V14-V15) X 290 / 1940	C9H	V201" V14+(V13-V14) X 349 / 1219
0AH	\V10" V18+(V17-V18) X 1063 / 1475	4AH	\V74" V16+(V15-V16) X 403 / 2083	8AH	V138" V15+(V14-V15) X 319 / 1940	CAH	V202" V14+(V13-V14) X 385 / 1219
0BH	\V11" V18+(V17-V18) X 1152 / 1475	4BH	\V75" V16+(V15-V16) X 438 / 2083	8BH	V139" V15+(V14-V15) X 348 / 1940	CBH	V203" V14+(V13-V14) X 422 / 1219
0CH	\V12" V18+(V17-V18) X 1237 / 1475	4CH	\V76" V16+(V15-V16) X 473 / 2083	8CH	V140" V15+(V14-V15) X 377 / 1940	CCH	V204" V14+(V13-V14) X 459 / 1219
0DH	\V13" V18+(V17-V18) X 1319 / 1475	4DH	\V77" V16+(V15-V16) X 508 / 2083	8DH	V141" V15+(V14-V15) X 406 / 1940	CDH	V205" V14+(V13-V14) X 496 / 1219
0EH	\V14" V18+(V17-V18) X 1398 / 1475	4EH	\V78" V16+(V15-V16) X 543 / 2083	8EH	V142" V15+(V14-V15) X 435 / 1940	CEH	V206" V14+(V13-V14) X 533 / 1219
0FH	\V15" V17	4FH	\V79" V16+(V15-V16) X 577 / 2083	8FH	V143" V15+(V14-V15) X 464 / 1940	CFH	V207" V14+(V13-V14) X 571 / 1219
10H	\V16" V17+(V16-V17) X 74 / 2419	50H	\V80" V16+(V15-V16) X 611 / 2083	90H	V144" V15+(V14-V15) X 493 / 1940	D0H	V208" V14+(V13-V14) X 609 / 1219
11H	\V17" V17+(V16-V17) X 146 / 2419	51H	\V81" V16+(V15-V16) X 645 / 2083	91H	V145" V15+(V14-V15) X 522 / 1940	D1H	V209" V14+(V13-V14) X 647 / 1219
12H	\V18" V17+(V16-V17) X 216 / 2419	52H	\V82" V16+(V15-V16) X 679 / 2083	92H	V146" V15+(V14-V15) X 551 / 1940	D2H	V210" V14+(V13-V14) X 686 / 1219
13H	\V19" V17+(V16-V17) X 285 / 2419	53H	\V83" V16+(V15-V16) X 713 / 2083	93H	V147" V15+(V14-V15) X 580 / 1940	D3H	V211" V14+(V13-V14) X 725 / 1219
14H	\V20" V17+(V16-V17) X 352 / 2419	54H	\V84" V16+(V15-V16) X 747 / 2083	94H	V148" V15+(V14-V15) X 609 / 1940	D4H	V212" V14+(V13-V14) X 764 / 1219
15H	\V21" V17+(V16-V17) X 417 / 2419	55H	\V85" V16+(V15-V16) X 780 / 2083	95H	V149" V15+(V14-V15) X 638 / 1940	D5H	V213" V14+(V13-V14) X 804 / 1219
16H	\V22" V17+(V16-V17) X 481 / 2419	56H	\V86" V16+(V15-V16) X 813 / 2083	96H	V150" V15+(V14-V15) X 667 / 1940	D6H	V214" V14+(V13-V14) X 844 / 1219
17H	\V23" V17+(V16-V17) X 543 / 2419	57H	\V87" V16+(V15-V16) X 846 / 2083	97H	V151" V15+(V14-V15) X 696 / 1940	D7H	V215" V14+(V13-V14) X 884 / 1219
18H	\V24" V17+(V16-V17) X 604 / 2419	58H	\V88" V16+(V15-V16) X 879 / 2083	98H	V152" V15+(V14-V15) X 725 / 1940	D8H	V216" V14+(V13-V14) X 925 / 1219
19H	\V25" V17+(V16-V17) X 664 / 2419	59H	\V89" V16+(V15-V16) X 912 / 2083	99H	V153" V15+(V14-V15) X 755 / 1940	D9H	V217" V14+(V13-V14) X 966 / 1219
1AH	\V26" V17+(V16-V17) X 723 / 2419	5AH	\V90" V16+(V15-V16) X 945 / 2083	9AH	V154" V15+(V14-V15) X 785 / 1940	DAH	V218" V14+(V13-V14) X 1007 / 1219
1BH	\V27" V17+(V16-V17) X 781 / 2419	5BH	\V91" V16+(V15-V16) X 978 / 2083	9BH	V155" V15+(V14-V15) X 815 / 1940	DBH	V219" V14+(V13-V14) X 1049 / 1219
1CH	\V28" V17+(V16-V17) X 838 / 2419	5CH	\V92" V16+(V15-V16) X 1010 / 2083	9CH	V156" V15+(V14-V15) X 845 / 1940	DCH	V220" V14+(V13-V14) X 1091 / 1219
1DH	\V29" V17+(V16-V17) X 894 / 2419	5DH	\V93" V16+(V15-V16) X 1042 / 2083	9DH	V157" V15+(V14-V15) X 875 / 1940	DDH	V221" V14+(V13-V14) X 1133 / 1219
1EH	\V30" V17+(V16-V17) X 949 / 2419	5EH	\V94" V16+(V15-V16) X 1074 / 2083	9EH	V158" V15+(V14-V15) X 905 / 1940	DEH	V222" V14+(V13-V14) X 1176 / 1219
1FH	\V31" V17+(V16-V17) X 1003 / 2419	5FH	\V95" V16+(V15-V16) X 1106 / 2083	9FH	V159" V15+(V14-V15) X 935 / 1940	DFH	V223" V13
20H	\V32" V17+(V16-V17) X 1056 / 2419	60H	\V96" V16+(V15-V16) X 1138 / 2083	A0H	V160" V15+(V14-V15) X 965 / 1940	E0H	V224" V13+(V12-V13) X 43 / 794
21H	\V33" V17+(V16-V17) X 1108 / 2419	61H	\V97" V16+(V15-V16) X 1170 / 2083	A1H	V161" V15+(V14-V15) X 995 / 1940	E1H	V225" V13+(V12-V13) X 87 / 794
22H	\V34" V17+(V16-V17) X 1159 / 2419	62H	\V98" V16+(V15-V16) X 1202 / 2083	A2H	V162" V15+(V14-V15) X 1025 / 1940	E2H	V226" V13+(V12-V13) X 131 / 794
23H	\V35" V17+(V16-V17) X 1210 / 2419	63H	\V99" V16+(V15-V16) X 1234 / 2083	A3H	V163" V15+(V14-V15) X 1055 / 1940	E3H	V227" V13+(V12-V13) X 175 / 794
24H	\V36" V17+(V16-V17) X 1260 / 2419	64H	\V100" V16+(V15-V16) X 1265 / 2083	A4H	V164" V15+(V14-V15) X 1085 / 1940	E4H	V228" V13+(V12-V13) X 220 / 794
25H	\V37" V17+(V16-V17) X 1309 / 2419	65H	\V101" V16+(V15-V16) X 1296 / 2083	A5H	V165" V15+(V14-V15) X 1115 / 1940	E5H	V229" V13+(V12-V13) X 265 / 794
26H	\V38" V17+(V16-V17) X 1358 / 2419	66H	\V102" V16+(V15-V16) X 1327 / 2083	A6H	V166" V15+(V14-V15) X 1145 / 1940	E6H	V230" V13+(V12-V13) X 311 / 794
27H	\V39" V17+(V16-V17) X 1406 / 2419	67H	\V103" V16+(V15-V16) X 1358 / 2083	A7H	V167" V15+(V14-V15) X 1175 / 1940	E7H	V231" V13+(V12-V13) X 357 / 794
28H	\V40" V17+(V16-V17) X 1453 / 2419	68H	\V104" V16+(V15-V16) X 1389 / 2083	A8H	V168" V15+(V14-V15) X 1205 / 1940	E8H	V232" V13+(V12-V13) X 403 / 794
29H	\V41" V17+(V16-V17) X 1500 / 2419	69H	\V105" V16+(V15-V16) X 1420 / 2083	A9H	V169" V15+(V14-V15) X 1236 / 1940	E9H	V233" V13+(V12-V13) X 450 / 794
2AH	\V42" V17+(V16-V17) X 1546 / 2419	6AH	\V106" V16+(V15-V16) X 1451 / 2083	AAH	V170" V15+(V14-V15) X 1267 / 1940	EAH	V234" V13+(V12-V13) X 497 / 794
2BH	\V43" V17+(V16-V17) X 1592 / 2419	6BH	\V107" V16+(V15-V16) X 1482 / 2083	ABH	V171" V15+(V14-V15) X 1298 / 1940	EBH	V235" V13+(V12-V13) X 545 / 794
2CH	\V44" V17+(V16-V17) X 1637 / 2419	6CH	\V108" V16+(V15-V16) X 1513 / 2083	ACH	V172" V15+(V14-V15) X 1329 / 1940	ECH	V236" V13+(V12-V13) X 593 / 794
2DH	\V45" V17+(V16-V17) X 1682 / 2419	6DH	\V109" V16+(V15-V16) X 1544 / 2083	ADH	V173" V15+(V14-V15) X 1360 / 1940	EDH	V237" V13+(V12-V13) X 642 / 794
2EH	\V46" V17+(V16-V17) X 1726 / 2419	6EH	\V110" V16+(V15-V16) X 1574 / 2083	AEH	V174" V15+(V14-V15) X 1391 / 1940	EEH	V238" V13+(V12-V13) X 692 / 794
2FH	\V47" V17+(V16-V17) X 1770 / 2419	6FH	\V111" V16+(V15-V16) X 1604 / 2083	AFH	V175" V15+(V14-V15) X 1422 / 1940	EFH	V239" V13+(V12-V13) X 742 / 794
30H	\V48" V17+(V16-V17) X 1813 / 2419	70H	\V112" V16+(V15-V16) X 1634 / 2083	B0H	V176" V15+(V14-V15) X 1453 / 1940	F0H	V240" V12
31H	\V49" V17+(V16-V17) X 1856 / 2419	71H	\V113" V16+(V15-V16) X 1664 / 2083	B1H	V177" V15+(V14-V15) X 1484 / 1940	F1H	V241" V12+(V11-V12) X 53 / 1373
32H	\V50" V17+(V16-V17) X 1899 / 2419	72H	\V114" V16+(V15-V16) X 1694 / 2083	B2H	V178" V15+(V14-V15) X 1516 / 1940	F2H	V242" V12+(V11-V12) X 108 / 1373
33H	\V51" V17+(V16-V17) X 1941 / 2419	73H	\V115" V16+(V15-V16) X 1724 / 2083	B3H	V179" V15+(V14-V15) X 1548 / 1940	F3H	V243" V12+(V11-V12) X 165 / 1373
34H	\V52" V17+(V16-V17) X 1983 / 2419	74H	\V116" V16+(V15-V16) X 1754 / 2083	B4H	V180" V15+(V14-V15) X 1580 / 1940	F4H	V244" V12+(V11-V12) X 224 / 1373
35H	\V53" V17+(V16-V17) X 2024 / 2419	75H	\V117" V16+(V15-V16) X 1784 / 2083	B5H	V181" V15+(V14-V15) X 1612 / 1940	F5H	V245" V12+(V11-V12) X 286 / 1373
36H	\V54" V17+(V16-V17) X 2065 / 2419	76H	\V118" V16+(V15-V16) X 1814 / 2083	B6H	V182" V15+(V14-V15) X 1644 / 1940	F6H	V246" V12+(V11-V12) X 352 / 1373
37H	\V55" V17+(V16-V17) X 2106 / 2419	77H	\V119" V16+(V15-V16) X 1844 / 2083	B7H	V183" V15+(V14-V15) X 1676 / 1940	F7H	V247" V12+(V11-V12) X 423 / 1373
38H	\V56" V17+(V16-V17) X 2146 / 2419	78H	\V120" V16+(V15-V16) X 1874 / 2083	B8H	V184" V15+(V14-V15) X 1708 / 1940	F8H	V248" V12+(V11-V12) X 501 / 1373
39H	\V57" V17+(V16-V17) X 2186 / 2419	79H	\V121" V16+(V15-V16) X 1904 / 2083	B9H	V185" V15+(V14-V15) X 1741 / 1940	F9H	V249" V12+(V11-V12) X 587 / 1373
3AH	\V58" V17+(V16-V17) X 2226 / 2419	7AH	\V122" V16+(V15-V16) X 1934 / 2083	BAH	V186" V15+(V14-V15) X 1774 / 1940	FAH	V250" V12+(V11-V12) X 685 / 1373
3BH	\V59" V17+(V16-V17) X 2265 / 2419	7BH	\V123" V16+(V15-V16) X 1964 / 2083	BBH	V187" V15+(V14-V15) X 1807 / 1940	FBH	V251" V12+(V11-V12) X 799 / 1373
3CH	\V60" V17+(V16-V17) X 2304 / 2419	7CH	\V124" V16+(V15-V16) X 1994 / 2083	BCH	V188" V15+(V14-V15) X 1840 / 1940	FCH	V252" V12+(V11-V12) X 937 / 1373
3DH	\V61" V17+(V16-V17) X 2343 / 2419	7DH	\V125" V16+(V15-V16) X 2024 / 2083	BDH	V189" V15+(V14-V15) X 1873 / 1940	FDH	V253" V12+(V11-V12) X 1115 / 1373
3EH	\V62" V17+(V16-V17) X 2381 / 2419	7EH	\V126" V16+(V15-V16) X 2054 / 2083	BEH	V190" V15+(V14-V15) X 1906 / 1940	FEH	V254" V11
3FH	\V63" V16	7FH	\V127" V15	BFH	V191" V14	FFH	V255" V10

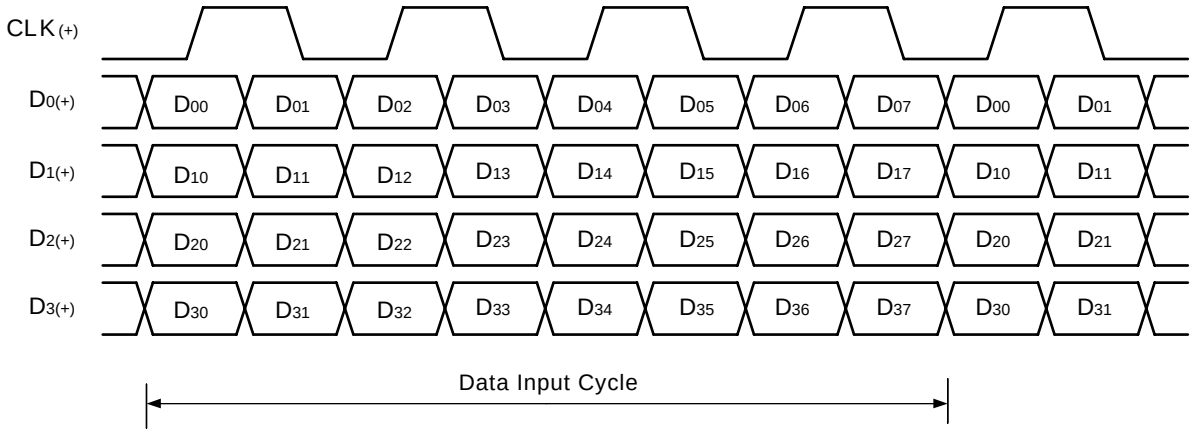
6. FUNCTION DESCRIPTION

6.1 Input Data Mapping

Display data and control data (RST) are input to $D_{0(+/-)}$ to $D_{3(+/-)}$.

Data mapping is changed in response to the mode, and the mode is changed by STB.

<Data Input Mode>



6.2 Composition of Display Data

MSB							LSB
Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0

Remark n = 0 to 3

6.3 Relation between Display Data and Output Number

This relationship is irrespective of R,/L condition.

(1) In case of 384 channel output

(a) Right shift (R,/L = H)

Output	S_1	S_2	S_3	→	S_{382}	S_{383}	S_{384}
Display Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	→	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}

(b) Left shift (R,/L = L)

Output	S_{384}	S_{383}	S_{382}	→	S_3	S_2	S_1
Display Data	D_{30} to D_{37}	D_{20} to D_{27}	D_{10} to D_{17}	→	D_{20} to D_{27}	D_{10} to D_{17}	D_{00} to D_{07}

(2) In case of 360 channel output

(a) Right shift (R,/L = H)

Output	S_1	S_2	S_3	→	S_{180}	S_{181} to S_{204}	S_{205}	→	S_{382}	S_{383}	S_{384}
Display Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	→	D_{30} to D_{37}	NA	D_{00} to D_{07}	→	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}

Remark NA: Non-assign

(b) Left shift (R,/L = L)

Output	S_{384}	S_{383}	S_{382}	→	S_{205}	S_{204} to S_{181}	S_{180}	→	S_3	S_2	S_1
Display Data	D_{30} to D_{37}	D_{20} to D_{27}	D_{10} to D_{17}	→	D_{00} to D_{07}	NA	D_{30} to D_{37}	→	D_{20} to D_{27}	D_{10} to D_{17}	D_{00} to D_{07}

Remark NA: Non-assign

6.4 Cascade

Multiple chips can be used in a cascade connection.

- Input STHR(L) pad at lead (head) chip is fixed to H.
- Input STHR(L) after secondary chips are connected from output STHR(L) at foregoing chip.
- Output STHR(L) of final stage driver IC can support current load up to ±1.0 mA (MAX.) by using pull-up or pull-down resistor.

6.5 Taking in the Display Data

(1) The lead (head) chip is set to control signal input mode (so called control mode),
and the receivers at $D_{0(+/-)}$ and $CLK_{(+/-)}$ of all chips are activated by rising edge of STB.

(2) Input the reset (RST) signal as L to $D_{0(+/-)}$. This RST should be kept over 200 ns after rising of STB.

(3) RST as H is input to $D_{0(+/-)}$ and H width should be over 50 ns and also over 3 CLK cycles.

(4) Input the RST as L to $D_{0(+/-)}$ and then changed to the data input mode function.
By the way, input STB again when a second RST is necessary.

(5) Data sampling starts at the rising edge of CLK after reading of "RST = L".

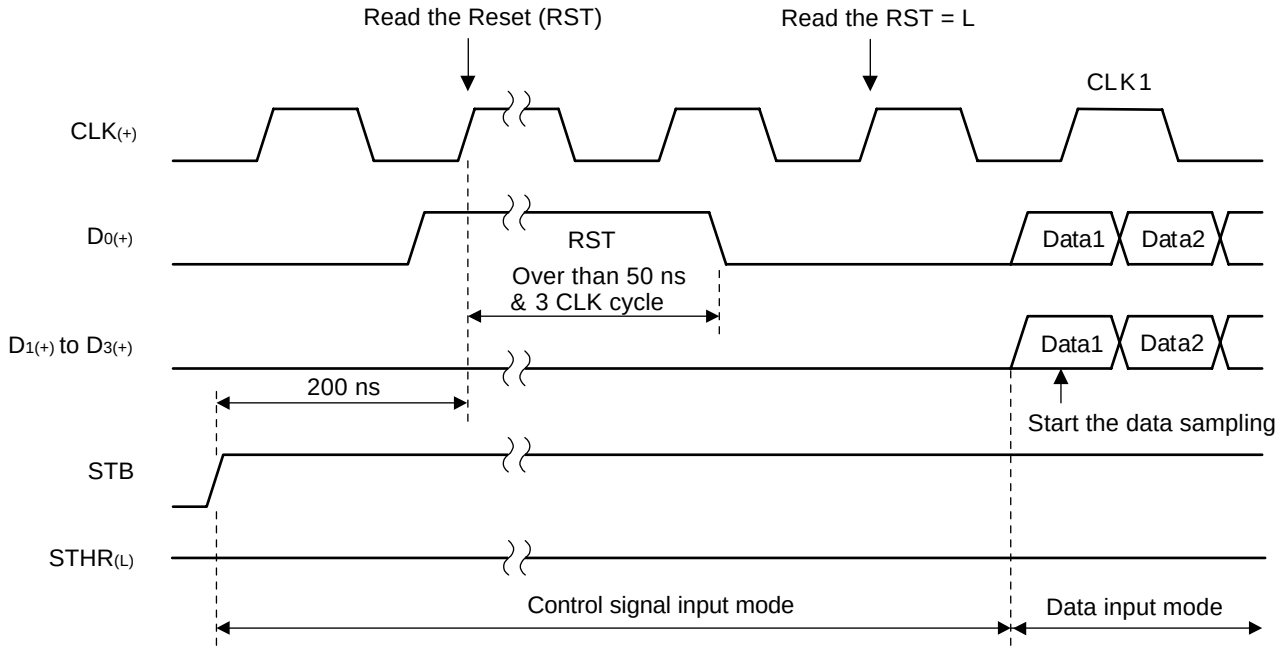
(6) At the same time data sampling starts, internal counter starts counting the data cycle for STHR(L) signal generation.

(7) After data sampling is finished, the receivers turn OFF.

(8) After the receivers turn OFF, keep the timing for more than 5 CLK cycles until STB is applied.

(9) Figure 6–1 shows the rough timing chart from application of STB to the start of data sampling.

Figure 6–1 Timing from Start to Sampling (reference)



7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic power supply voltage	V_{DD1}	−0.5 to +4.0	V
Driver power supply voltage	V_{DD2}	−0.5 to +18.0	V
Logic input voltage	V_{I1}	−0.5 to V_{DD1} + 0.5	V
Logic output voltage	V_{O1}	−0.5 to V_{DD1} + 0.5	V
Logic output current	I_O	± 1.0	mA
Driver input voltage	V_{I2}	−0.5 to V_{DD2} + 0.5	V
Driver output voltage	V_{O2}	−0.5 to V_{DD2} + 0.5	V
Operating ambient temperature	T_A	−10 to +90	°C
Storage temperature	T_{stg}	−55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +90 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic power supply voltage	V_{DD1}		2.7	3.0	3.6	V
Driver power supply voltage	V_{DD2}		10.0	15.4	16.5	V
CMOS high-level input voltage	V_{IH}	STHR(L), R,/L, STB, SB, POL, O_{sel}, RxBIAS1, RxBIAS2, SRC, ORC, V_{sel1}, V_{sel2}	0.7 V_{DD1}		V_{DD1}	V
CMOS low-level input voltage	V_{IL}		0		0.3 V_{DD1}	V
mini-LVDS input voltage (Center)	V_I	V_{DD1} =3.0 V, V_{ID} = 200 mV	0.3 + (V_{ID}/2)		(V_{DD1}–1.2) – (V_{ID}/2)	V
mini-LVDS differential voltage range (Amplitude: peak to peak)	V_{ID}	V_{DD1} = 3.0 V, V_I = 1.7 V	200		600	mV
γ- corrected voltage	V_0-V_9		0.5 V_{DD2}		V_{DD2} – 0.2	V
	V_{10}-V_{19}		0.2		0.5 V_{DD2}	V
Driver output voltage	V_{OUT}		0.2		V_{DD2} – 0.2	V
Clock frequency	f_{CLK}	CLKA, CLKB, T_A = 25°C, V_{DD1} = 3.0 V, V_{ID} = 200 mV, V_I = 1.7 V		159	190	MHz

Electrical Characteristics (T_A = 25 °C, V_{DD1} = 3.0 V, V_{DD2} = 13.0 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	STHR(L), R,/L, STB, SB, POL, O_{sel}, RxBIAS1, RxBIAS2, SRC, ORC, V_{sel1}, V_{sel2}, CLKA, CLKB, D0A, D0B to D3A, D3B			± 1.0	μA
γ-corrected resistor value	R_γ	V_0-V_9 = V_{10} -V_{19}	7.8	12.0	16.3	kΩ
Driver output current	I_{VOH}	V_X = V_{DD2} – 0.2 V, V_{OUT} = V_X – 1.0 V Note1, low output resistance mode (ORC = H)		– 334	– 200	μA
	I_{VOL}	V_X = V_{SS2} + 0.2 V, V_{OUT} = V_X + 1.0 V Note1, low output resistance mode (ORC = H)	360	527		μA
Output swing voltage difference deviation Note2	ΔV_{P-P1}	Input: 00H to 3FH		± 10	± 20	mV
	ΔV_{P-P2}	Input: 40H to 7FH, 80H to BFH		± 7	± 15	mV
	ΔV_{P-P3}	Input: C0H to FFH		± 4	± 10	mV
Output swing voltage average deviation Note3	AV_O	Input: 3FH, 7FH, BFH		± 16	± 20	mV
Logic dynamic current consumption	I_{DD11}	Checkered, f_{STB} = 100 kHz (PW = 500 ns), f_{CLK} =159 MHz, V_{DD1} = 3.6 V			7.50	mA
Logic static current consumption	I_{DD12}	No CLK & Input, V_{DD1} = 3.6 V			4.50	mA
Driver dynamic current consumption	I_{DD21}	Raster pattern, V_{DD2} = 16.5 V, f_{STB} = 100 kHz (PW = 500 ns), with no load			30.0	mA
Driver static current consumption	I_{DD22}	Raster pattern, V_{DD2} = 16.5 V, Input: FFH, with no load			30.0	mA

★ **Notes1.** V_X refers to the output voltage of analog output pins S_1 to S_{384}.
V_{OUT} refers to the voltage applied to analog output pins S_1 to S_{384}.

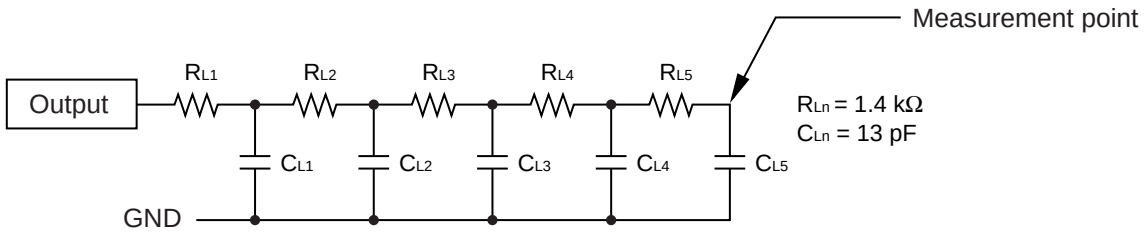
2. Amplitude offset when all of output ports out same data.

3. Deviation of averaged amplitude offset value between chips.

Switching Characteristics (T_A = 25 °C, V_{DD1} = 3.0 V, V_{DD2} = 13.0 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_1	C_L = 50 pF	6	15	22	ns
Driver output delay time	t_2	R_L = 7 kΩ, C_L = 65 pF		2.1	2.5	μs
	t_3	Refer to <Test Condition >		3.9	5.0	μs
	t_4			1.3	2.5	μs
	t_5			3.4	5.0	μs
Input capacitance	C_{I1}	CMOS interface, STHR(L)		10	15	pF
	C_{I2}	mini-LVDS interface, Except STHR(L), V_0-V_{19}		5	10	pF

<Test Condition>



Timing Requirements (T_A = 25 °C, V_{DD1} = 3.0 V, V_{SS1} = 0 V, t_r = t_f = 0.5 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	t_6		5.2	6.2		ns
Clock pulse high period	t_7		2.1	2.6		ns
Clock pulse low period	t_8		2.1	2.6		ns
Data setup time	t_9		1.0			ns
Data hold time	t_{10}		1.0			ns
Start pulse setup time	t_{11}		0			ns
STB pulse width	t_{13}		200			ns
POL setup time	t_{14}		–5.0			ns
RST high period	t_{16}		50.0			ns
			3			CLK
Receiver OFF to STB timing	t_{17}		5			CLK
STB to RST input time	t_{18}		200			ns

Remark Unless otherwise specified, V_{IH} and V_{IL} of the CMOS signals are defined as V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

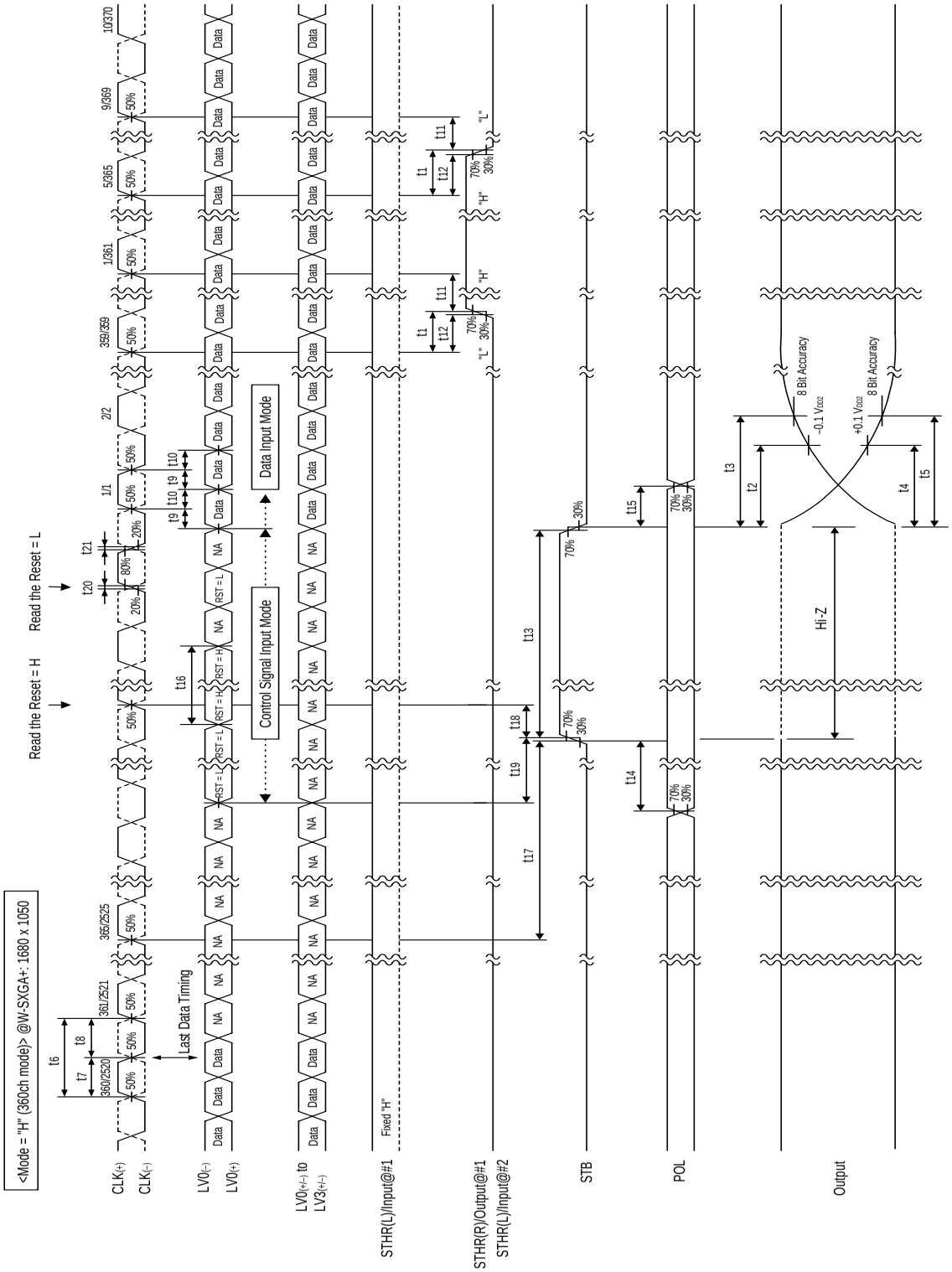
Phase-out/Discontinued

Switching Characteristic Waveform (R,/L = H)

Unless otherwise specified, V_{IH} and V_{IL} of the CMOS signals are defined as V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Also, unless otherwise specified, V_{IH} and V_{IL} of the mini-LVDS signals are defined as V_{IH} = V_{IL} = V_I (Center of V_{ID}).

(Clock and display data numbers are examples when W-SXGA+ is used.)



★ 8. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD160010.

For more details, refer to the

[Semiconductor Device Mount Manual] (http://www.necel.com/pkg/en/mount/index.html)

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD160010N-xxx: TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100g (per solder).
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm^2, time 3 to 5 sec. Real bonding 165 to 180°C pressure 25 to 45 kg/cm^2, time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)