μPA2763

MOS FIELD EFFECT TRANSISTOR

R07DS0003EJ0100
Rev.1.00
May 31, 2010

Description

The μPA2763 is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications.

Features

- Low on-state resistance
  - $R_{DS(on)1}$ = 23.0 mΩ MAX. (V_{GS} = 10 V, I_D = 21 A)
  - $R_{DS(on)2}$ = 28.0 mΩ MAX. (V_{GS} = 8 V, I_D = 21 A)
- Low C_{iss} 2100 pF TYP.
- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±42	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±84	A
Total Power Dissipation*2	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	4.6	W
Total Power Dissipation (T_C = 25°C)	P_{T3}	83	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C
Single Avalanche Current *3	I_{AS}	24.7	A
Single Avalanche Energy *3	E_{AS}	61.0	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	1.5	°C/W

Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

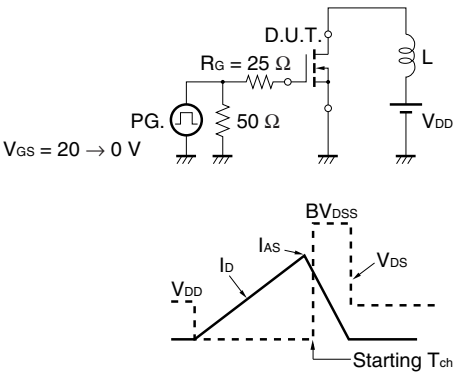
*3. Starting T_{ch} = 25°C, V_{DD} = 50 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20→0 V

Electrical Characteristics (T_A = 25°C)

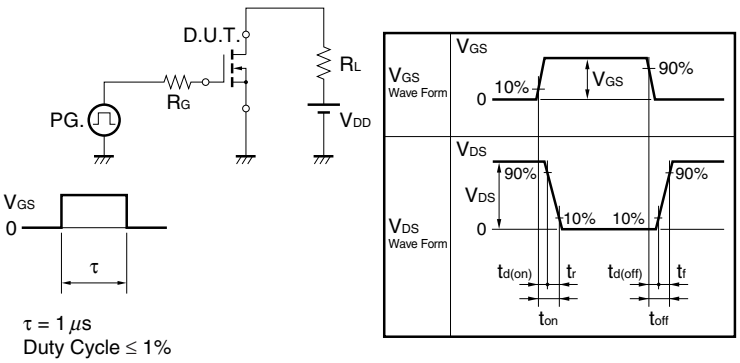
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			10	μA	V_{DS} = 100 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance *1	$\|y_{fs}\|$	10			S	V_{DS} = 10 V, I_D = 21 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		18.0	23.0	mΩ	V_{GS} = 10 V, I_D = 21 A
	$R_{DS(on)2}$		19.0	28.0	mΩ	V_{GS} = 8 V, I_D = 21 A
Input Capacitance	C_{iss}		2100		pF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz
Output Capacitance	C_{oss}		350		pF	
Reverse Transfer Capacitance	C_{rss}		130		pF	
Turn-on Delay Time	$t_{d(on)}$		28		ns	V_{DD} = 50 V, I_D = 21 A, V_{GS} = 10 V, R_G = 10 Ω
Rise Time	t_r		13		ns	
Turn-off Delay Time	$t_{d(off)}$		73		ns	
Fall Time	t_f		11		ns	
Total Gate Charge	Q_G		40		nC	V_{DD} = 50 V, V_{GS} = 10 V, I_D = 42 A
Gate to Source Charge	Q_{GS}		11		nC	
Gate to Drain Charge	Q_{GD}		13		nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.88		V	I_F = 42 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		59		ns	I_F = 42A, V_{GS} = 0 V, di/dt = 100A/μs
Reverse Recovery Charge	Q_{rr}		152		nC	
Gate Resistance	R_G		2.1		Ω	f = 1 MHz

Note: *1. Pulsed

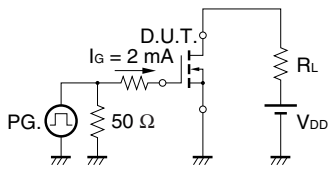
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

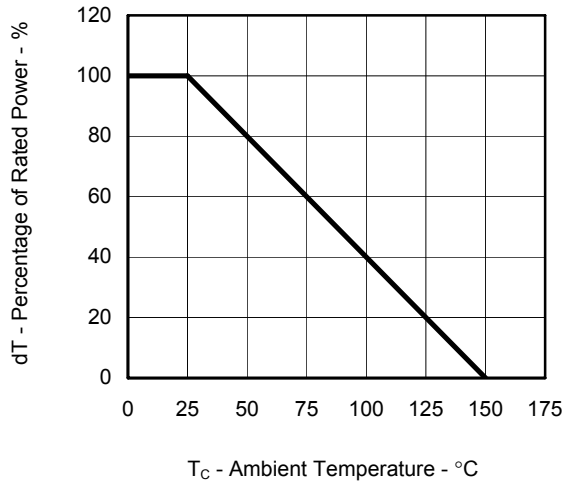


TEST CIRCUIT 3 GATE CHARGE

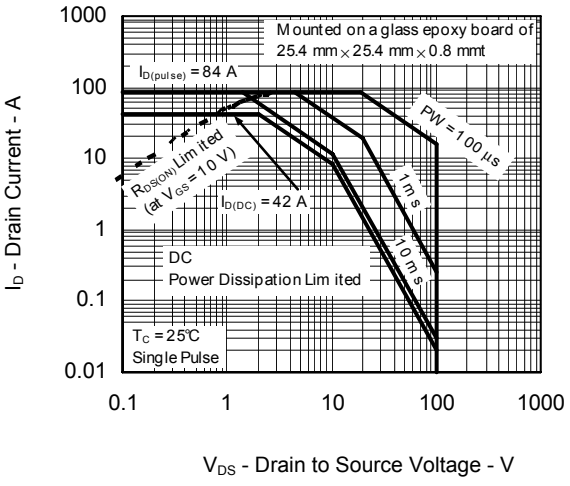


Typical Characteristics (T_A = 25°C)

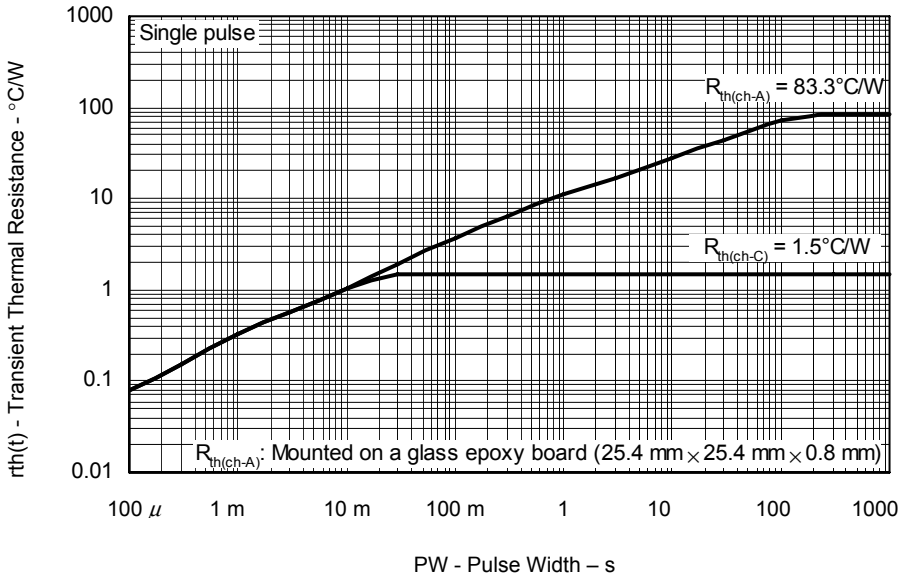
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



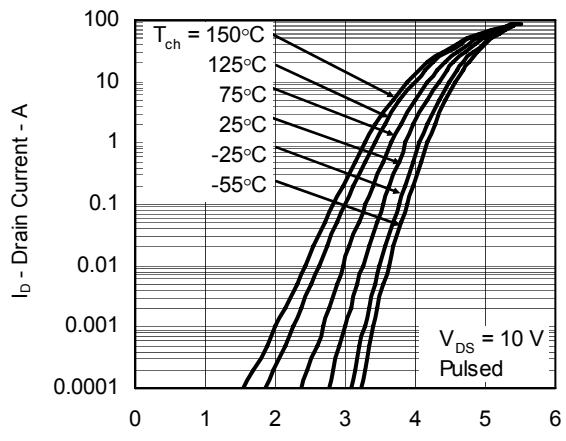
FORWARD BIAS SAFE OPERATING AREA



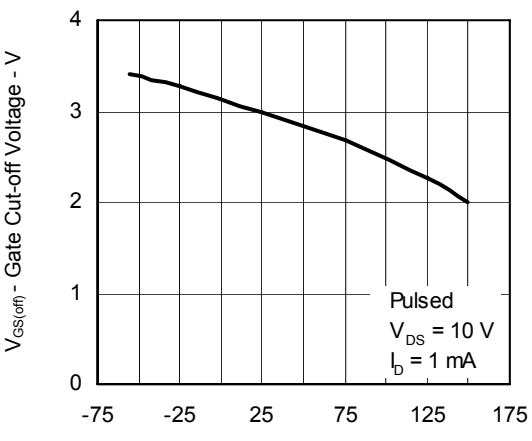
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



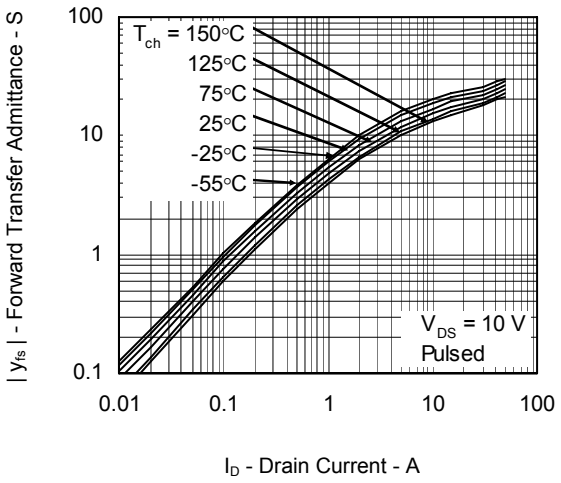
FORWARD TRANSFER CHARACTERISTICS



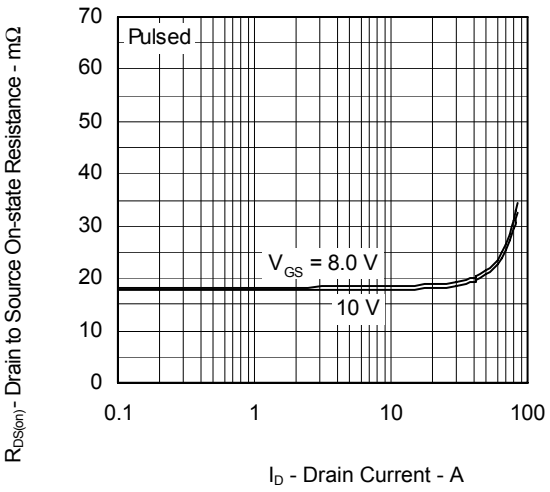
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



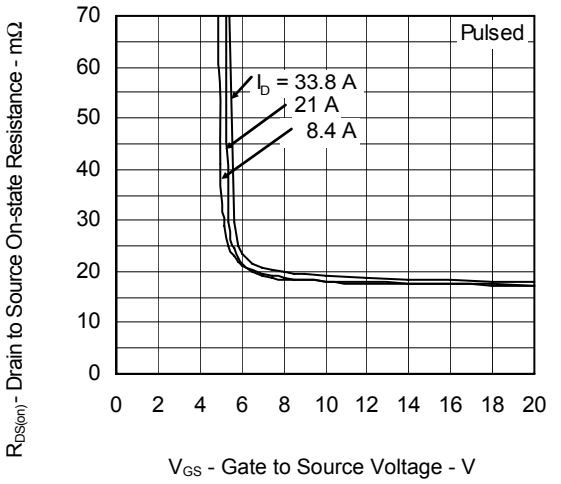
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



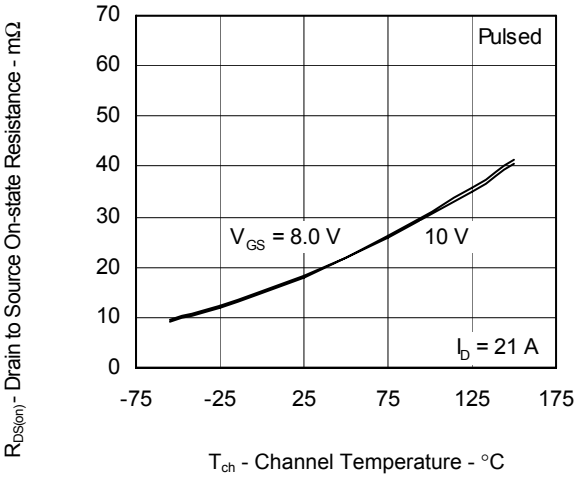
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



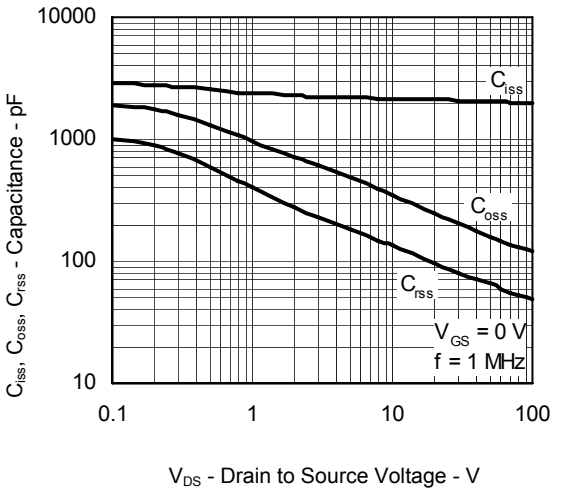
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



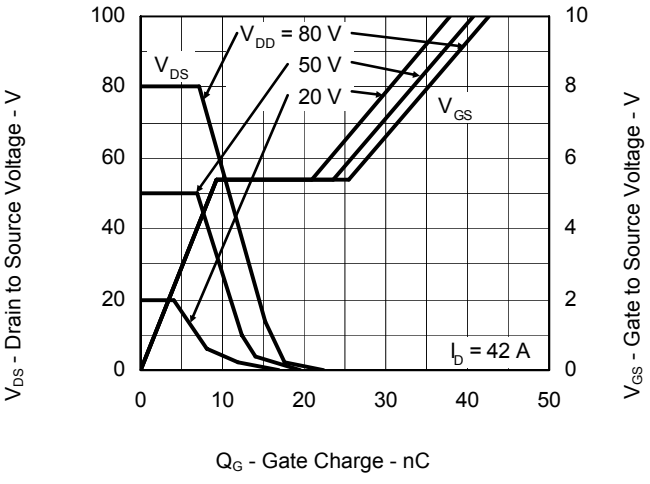
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



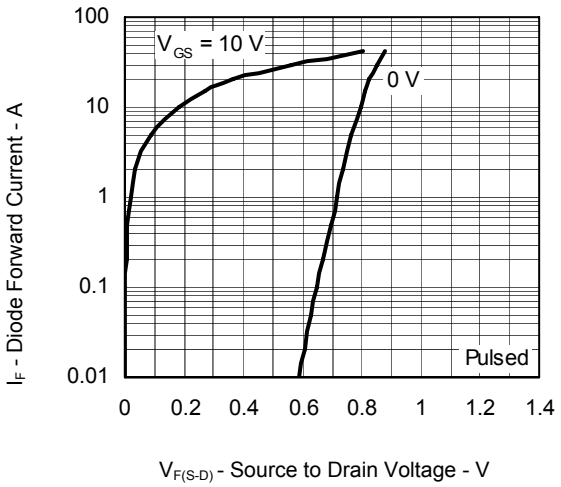
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



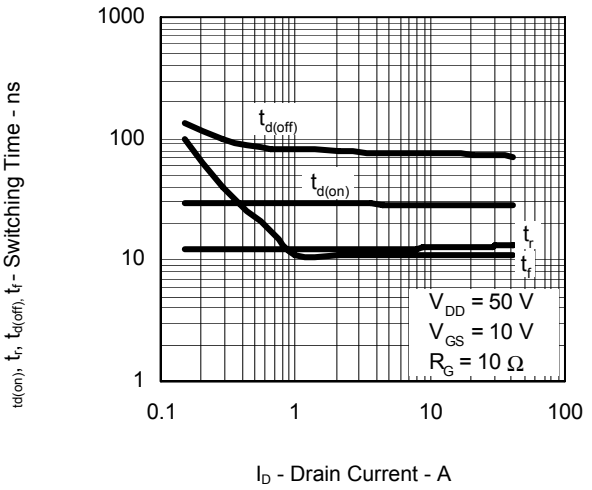
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



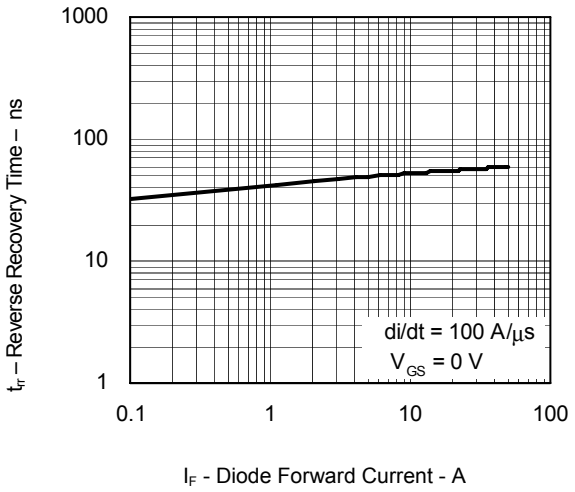
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



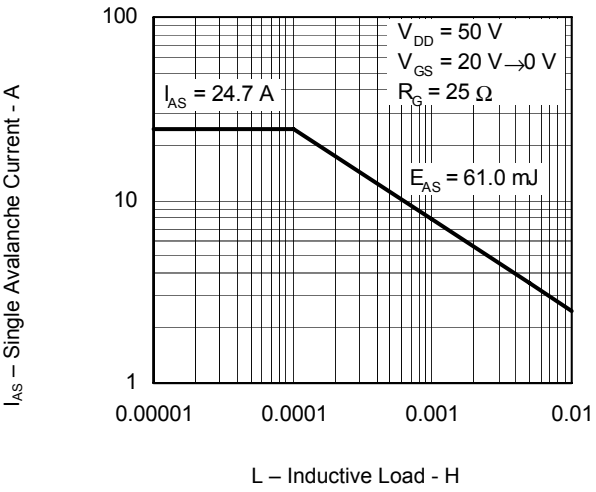
SWITCHING CHARACTERISTICS



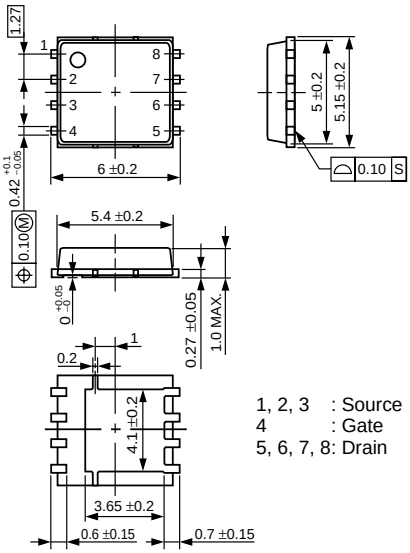
REVERSE RECOVERY TIME vs DIODE FORWARD CURRENT



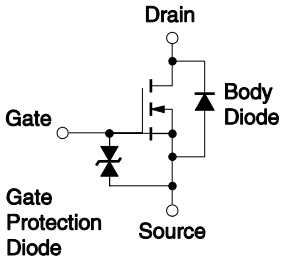
SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



Package Drawing (Unit: mm)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device

Ordering Information

Part No.	Lead Plating	Packing	Package
μPA2763T1A-E1-AY *1	Pure Sn	Tape 3000 p/reel	8-pin HVSON (0.1 g TYP.)
μPA2763T1A-E2-AY *1			

Note: *1. This product does not contain Pb in the external electrode.

Revision History	μPA2763

Rev.	Date	Description	
		Page	Summary
1.00	May 31, 2010	-	First Edition issued

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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