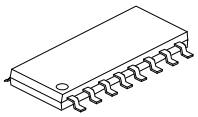
3 CHANNEL CONSTANT-CURRENT DRIVER AND GREY-LEVEL MODULATE OUTPUT



SOP-16

■ DESCRIPTION

UTC **UL1030** is designed for driving chip of LED lighting system design, it uses advanced high voltage CMOS technology, provide 3 channel constant current drive and gray scale modulation output, especially in the dissociation with mutual grey level in the full-color lighting system.

UTC **UL1030** includes serial shift register and concatenation driver circuit, grey level data shift into serial shift register in the clock, and transfer saving, it transfer to interface 3 after pulse-width modulate, then output, serial shift register and grey-level counter can be controlled by different clock signal. In the meantime, UTC **UL1030** driver data signal and control signal, and output next circuit.

■ FEATURES

* 3 channel driver output, maxim current per channel is 45mA, LED light voltage can reach 12V
* Output adopt In-Rush online feedback constant-current driver structure, compatible with constant-voltage module, it also can contact outside equipment and transfer to higher voltage or current output driver
* Built-in LDO voltage-stabilizing circuit, voltage range : 3~8V, and have 5V stabilizing voltage output
* Adopt self-add token ring technology dual shift line, shift clock can reach 25MHz
* Directly input grey-level data, it is transfer to 256 output with reverse-gamma regulator after inside SUPER-PWM technology, e. g, adopt built-in oscillator as grey-level clock, it support FREE-RUN module output, especially can be used in low-cost controller
* Data clock signal is drived strongly to next chip to enhance level after built-in phase-lock circuit
* High-voltage CMOS technology, industrial design, with extra-good interference immunity

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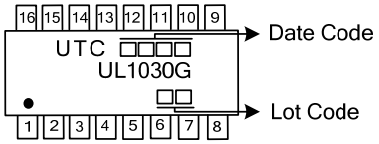
■ ORDERING INFORMATION

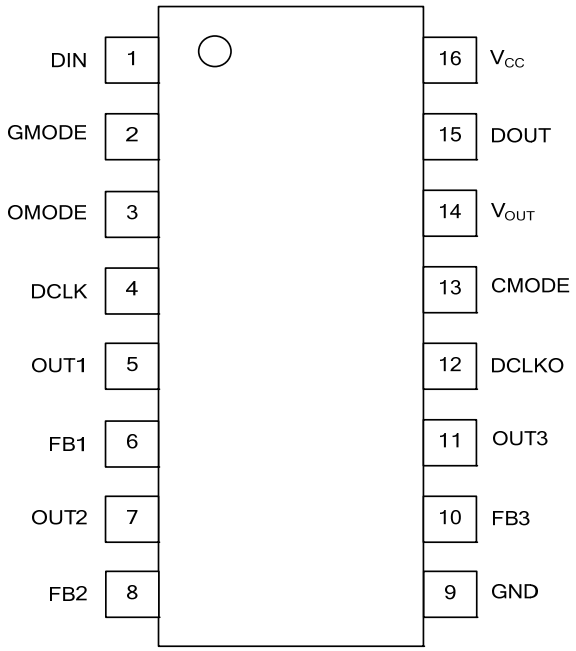
Ordering Number	Package	Packing
UL1030G-S16-R	SOP-16	Tape Reel

UL1030G-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free

■ MARKING



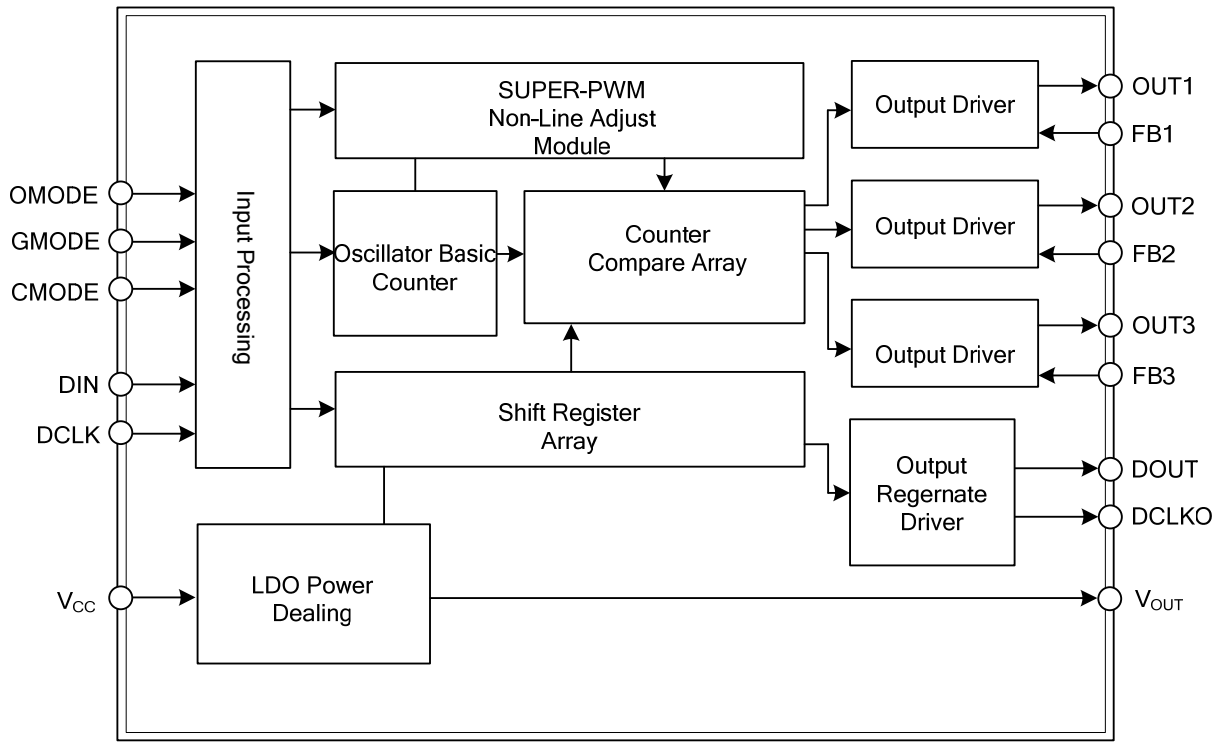
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	DIN	Serial data input, built-in pull-up
2	GMODE	Grey-level regulate mode: GMODE=1, adapt line modulate, GMODE=0, adapt reverse-gamma 256 grade non-line regulate, built-in pull-up
3	OMODE	Control output polarity: OMODE=1, output is in-constant current/voltage drive mode, OMODE=0, output is out drive mode, voltage built-in pull-up
4	DCLK	Serial data clock input, built-in pull-up
5, 7 ,11	OUT1, OUT2, OUT3	3 channel driver output
6, 8, 10	FB1, FB2, FB3	Feedback input in constant current state
9	GND	Ground
12	DCLKO	Serial clock output, after inside phase locked loop and strong drive output
13	CMODE	Choose inside grey clock GCLK, CMODE=0, GCLK=DCLK, CMODE=1, GCLK=inside oscillator output, built-in pull-up
14	V_{OUT}	When VCC>5V, 5V stable voltage output, when VCC>5V, VOUT=VCC, can be used as inside working voltage, suggest outside contact a 0.01μF-0.1μF capacity
15	DOUT	Serial data output, after inside strongly drive
16	V_{CC}	LDO power, range: 4.5V~8V

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{DD}	3~8	V
LED Light Voltage		V_{LED}	3~12	V
Data Clock Frequency	Compatible with Grey Level at 10	F_{CLK}	25	MHz
Maxim Driver Current	at Constant Voltage	I_{OMAX}	45	mA
	at Constant Current		30	mA
Channel Current Error	Chip Inside	D_{IO}	<5	%
	Between Chip		<6	%
Power Consumption		P_{DMAX}	600	mW
Soldering Temperature (8S)		T_M	300	°C
Operating Temperature		T_{OPR}	-40~+80	°C
Storage Temperature		T_{STG}	-65~+120	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

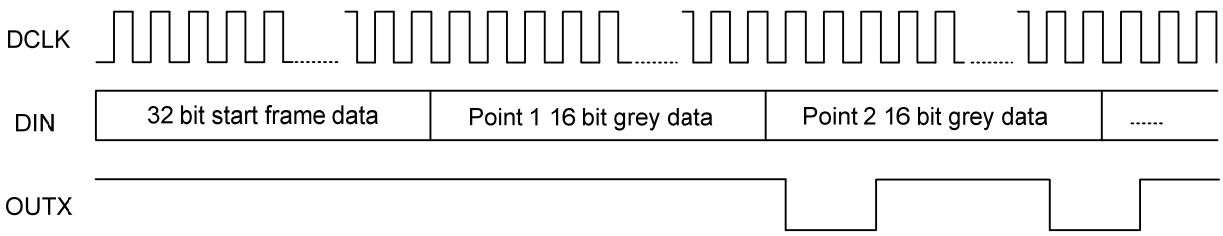
■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	5 ~ 7.5	V
Typical Voltage-Stabilizing Output Voltage	V_{OUT}	5±5%	V
Input Voltage	V_{IN}	-0.4 ~ V_{OUT}+0.4	V
Data Clock Frequency	F_{CLK}	0~15	MHz
Clock High-Level Voltage Width	T_{CLKH}	>30	ns
Clock Low-Level Voltage Width	T_{CLKL}	>30	ns
Data Build Time	T_{SETUP}	>10	ns
Data Keep Time	T_{HOLD}	>5	ns
Power Comsumption	P_D	<350	mW
Operating Temperature	T_{OP}	-30 ~ +60	°C

■ TIMING SEQUENCE PARAMETER (T=25°C, V_{DD}=5V, OMODE=1, GMODE=0, CMODE=1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maxim Up and Down Time of Input Signal	T_R	V_{DD}=5V		400		ns
	T_F			300		ns
Up and Down Time of Concatenation Output Signal	T_{TLH}	C_L=30pF, R_L=1K		12		ns
	T_{THL}			12		ns
Maxim Delay Time of Concatenation Output	T_{PD}	C_L=30pF, R_L=1K		10		ns
	T_{CO}			10		ns
Min PWM Width of Driver Output	T_{ONMIN}	I_{OUT}=20mA		200		ns
Maxim Open and Close Time of Driver Output Signal	T_{ON}	I_{OUT}=20mA		60		ns
	T_{OFF}			60		ns

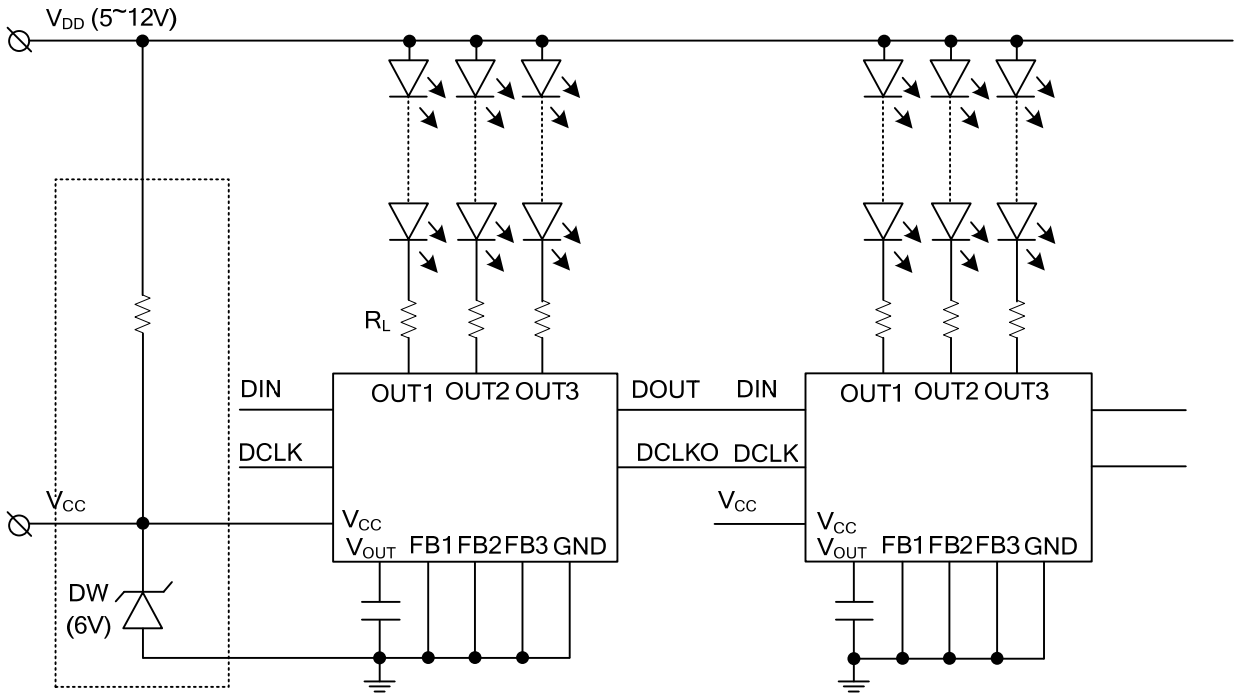
■ BASIC TIMING SEQUENCE



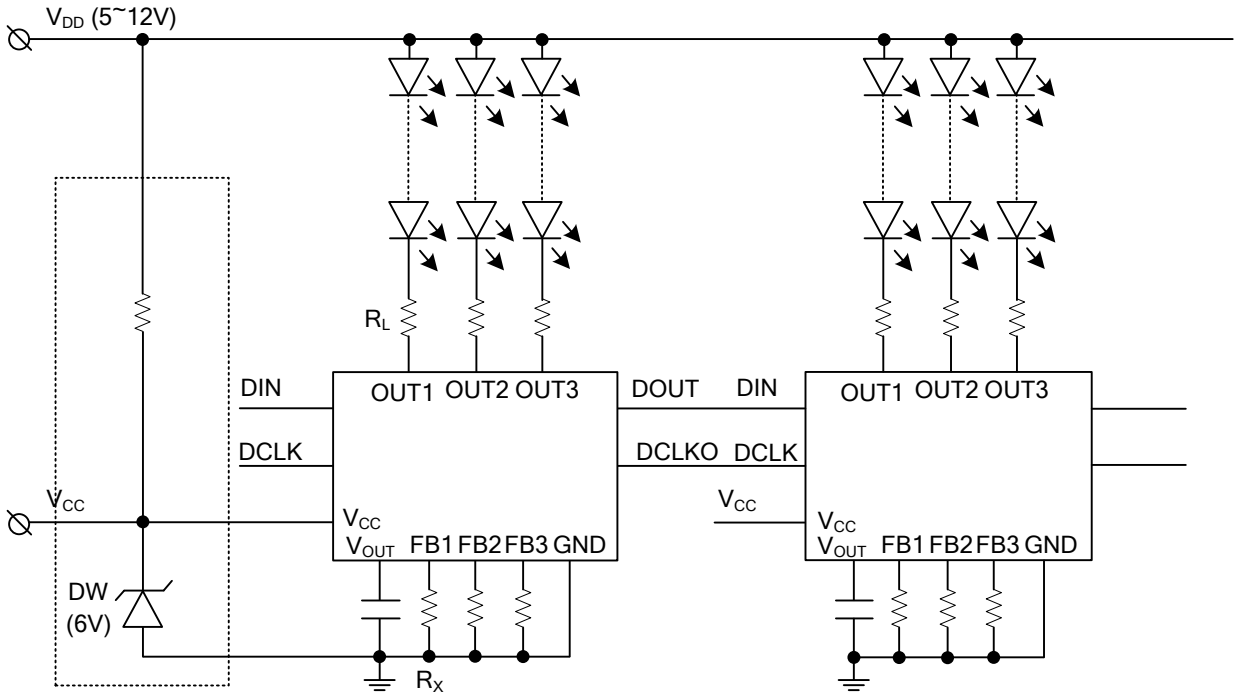
A. First shift in 32bit “0” as start frame, then shift in all data frame, start frame and data frame both are shift by high-bit, every data is input on DCLK rising edge.
B. The first data frame is corresponding LED light nearest from shift-in polar, its format includes 1bit as start “1” plus 3 groups 5bits grey level.
C. Turn shift in all data, add append pulse of corresponding point, new data start valid.

■ TYPICAL APPLICATION CIRCUIT

Inside constant voltage driver mode:

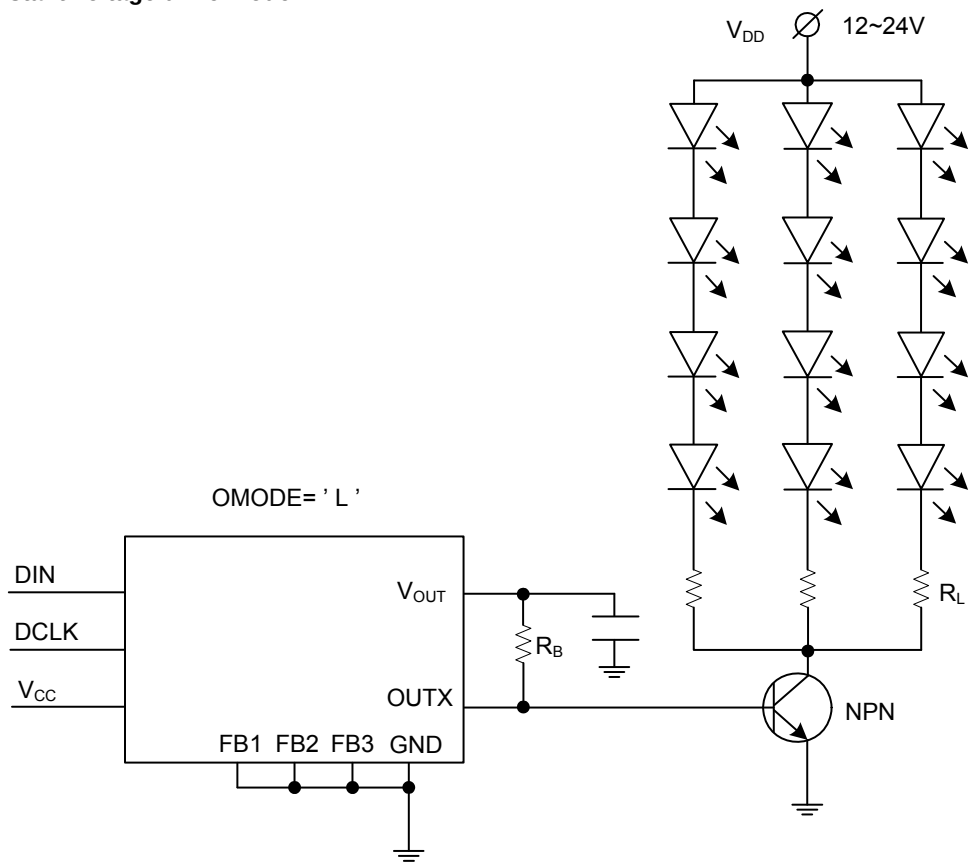


Inside constant current driver mode:

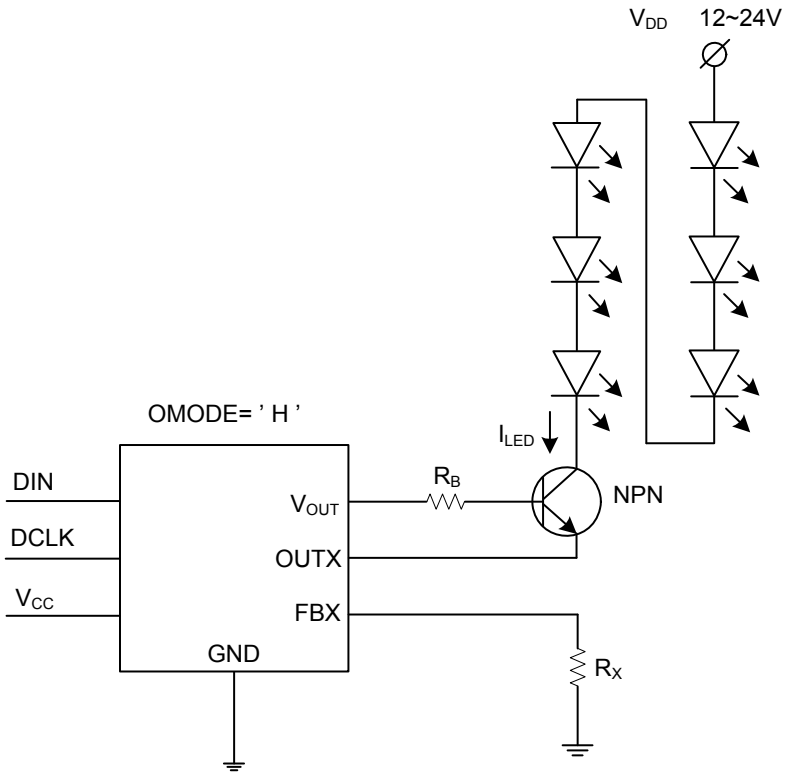


■ TYPICAL APPLICATION CIRCUIT (Cont.)

Outside constant voltage drive mode:



Outside constant current drive mode:



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