





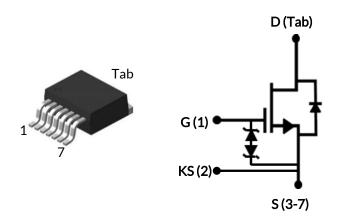








UJ4C075044B7S



| Part Number | Package | Marking |
|---------------|-----------------------|---------------|
| UJ4C075044B7S | D ² PAK-7L | UJ4C075044B7S |







Silicon Carbide (SiC) Cascode JFET -EliteSiC, Power N-Channel, D2PAK-7L, 750 V, 44 mohm

Rev. C, January 2025

Description

The UJ4C075044B7S is a 750V, $44m\Omega$ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-7L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance R_{DS(on)}: 44mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 55nC
- Low body diode V_{FSD}: 1.2V
- ◆ Low gate charge: Q_G = 37.8nC
- Threshold voltage V_{G(th)}: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- D²PAK-7L package for faster switching, clean gate waveforms

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating













Maximum Ratings

| Parameter | Symbol | Test Conditions | Value | Units |
|---|------------------|-------------------------------|------------|-------|
| Drain-source voltage | V_{DS} | | 750 | V |
| Gate-source voltage | V | DC | -20 to +20 | V |
| Gate-Source voltage | V_{GS} | AC (f > 1Hz) | -25 to +25 | V |
| Continuous drain current ¹ | | T _C =25°C | 35.6 | Α |
| Continuous drain current | I _D | T _C =100°C | 26 | Α |
| Pulsed drain current ² | I _{DM} | T _C = 25°C | 110 | Α |
| Single pulsed avalanche energy ³ | E _{AS} | L=15mH, I _{AS} =2.1A | 33 | mJ |
| SiC FET dv/dt ruggedness | dv/dt | $V_{DS} \le 500V$ | 200 | V/ns |
| Power dissipation | P _{tot} | T _C = 25°C | 181 | W |
| Maximum junction temperature | $T_{J,max}$ | | 175 | °C |
| Operating and storage temperature | T_J,T_STG | | -55 to 175 | °C |
| Reflow soldering temperature | T_{solder} | reflow MSL 1 | 245 | °C |

- 1. Limited by $T_{J,max}$
- 2. Pulse width t_p limited by $T_{J,max}$
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

| Parameter | Symbol | Test Conditions | Value | | | Linite |
|--------------------------------------|-----------------|-----------------|-------|------|------|---------|
| | | | Min | Тур | Max | - Units |
| Thermal resistance, junction-to-case | $R_{\theta JC}$ | | | 0.64 | 0.83 | °C/W |













Electrical Characteristics ($T_J = +25^{\circ}C$ unless otherwise specified)

Typical Performance - Static

| Parameter | Symbol Test Conditions | | Value | | | Units | |
|--------------------------------|------------------------|--|-------|-----|-----|--------|--|
| Parameter | Зуппоп | rest Conditions | Min | Тур | Max | Offics | |
| Drain-source breakdown voltage | BV_{DS} | V_{GS} =0V, I_D =1mA | 750 | | | V | |
| Total duois lockers summent | | V _{DS} =750V, V _{GS} =0V, T _J =25°C | 1.5 | | 15 | | |
| Total drain leakage current | I _{DSS} | V _{DS} =750V, V _{GS} =0V, T _J =175°C | | 15 | | – μΑ | |
| Total gate leakage current | I _{GSS} | V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V | | 6 | ±20 | μΑ | |
| | R _{DS(on)} | V _{GS} =12V, I _D =25A, T _J =25°C | | 44 | 56 | | |
| Drain-source on-resistance | | V _{GS} =12V, I _D =25A, T _J =125°C | | 75 | | mΩ | |
| | | V_{GS} =12V, I_{D} =25A, T_{J} =175°C | | 101 | | | |
| Gate threshold voltage | $V_{G(th)}$ | V_{DS} =5V, I_{D} =10mA | 4 | 4.8 | 6 | V | |
| Gate resistance | R_{G} | f=1MHz, open drain | | 4.5 | | Ω | |

Typical Performance - Reverse Diode

| Parameter | Symbol | Test Conditions | Value | | | Units | |
|---|----------------------|--|-------|------|------|--------|--|
| Parameter | Syllibol | Test Conditions | Min | Тур | Max | Offics | |
| Diode continuous forward current ¹ | I _S | T _C = 25°C | | | 35.6 | Α | |
| Diode pulse current ² | I _{S,pulse} | T _C =25°C | | | 110 | Α | |
| Forward voltage | V_{FSD} | V _{GS} =0V, I _S =10A, T _J =25°C | | 1.2 | 1.36 | V | |
| 1 of ward voltage | * F5D | V _{GS} =0V, I _S =10A, T _J =175°C | | 1.42 | | | |
| Reverse recovery charge | Q _{rr} | V_R =400V, I_S =25A, V_{GS} =0V, R_{G_EXT} =50 Ω | | 55 | | nC | |
| Reverse recovery time | t _{rr} | di/dt=1000A/μs, T _J =25°C | | 10.4 | | ns | |
| Reverse recovery charge | Q _{rr} | V_R =400V, I_S =25A, V_{GS} =0V, R_{G_EXT} =50 Ω | | 60 | | nC | |
| Reverse recovery time | t _{rr} | di/dt=1000A/μs, Τ _J =150°C | | 11.2 | | ns | |













Typical Performance - Dynamic

| Developed | Cl. al | Took Counditions | Total Constitution | | Value | | |
|---|-------------------------------|--|--------------------|------|-------|-------|--|
| Parameter | Symbol | Test Conditions – | Min | Тур | Max | Units | |
| Input capacitance | C_{iss} | V _{DS} =400V, V _{GS} =0V | | 1400 | | | |
| Output capacitance | C_{oss} | f=100kHz | | 55 | | pF | |
| Reverse transfer capacitance | C_{rss} | 1-100K112 | | 2.5 | | | |
| Effective output capacitance, energy related | $C_{oss(er)}$ | V _{DS} =0V to 400V, V _{GS} =0V | | 66.4 | | pF | |
| Effective output capacitance, time related | C _{oss(tr)} | V_{DS} =0V to 400V, V_{GS} =0V | | 131 | | pF | |
| C _{OSS} stored energy | E _{oss} | V _{DS} =400V, V _{GS} =0V | | 5.3 | | μJ | |
| Total gate charge | Q_{G} | V _{DS} =400V, I _D =25A, | | 37.8 | | | |
| Gate-drain charge | Q_{GD} | $V_{DS} = 400 \text{ V}, I_D = 25 \text{ A},$ $V_{GS} = 0 \text{ V to } 15 \text{ V}$ | | 8 | | nC | |
| Gate-source charge | Q_{GS} | V _{GS} = 0V to 15V | | 11.8 | | | |
| Turn-on delay time | $t_{d(on)}$ | Notes 4, V_{DS} =400V, I_D =25A, Gate Driver =0V to +15V, Turn-on R_{GEXT} = 1 Ω , | | 11 | | ns | |
| Rise time | t _r | | | 23 | | | |
| Turn-off delay time | t _{d(off)} | | | 83 | | | |
| Fall time | t _f | Turn-off $R_{G,EXT}$ =50 Ω , | | 12 | | | |
| Turn-on energy including R _S energy | E _{ON} | inductive Load, FWD: same device with V _{GS} | | 131 | | μЈ | |
| Turn-off energy including R _S energy | E _{OFF} | = $0V$ and $R_G = 50\Omega$, | | 66 | | | |
| Total switching energy | E _{TOTAL} | T _J =25°C | | 197 | | | |
| Turn-on delay time | t _{d(on)} | Notes 4, | | 10.4 | | | |
| Rise time | t _r | V _{DS} =400V, I _D =25A, Gate | | 23 | | ns | |
| Turn-off delay time | $t_{d(off)}$ | Driver =0V to +15V, Turn-on $R_{G,EXT} = 1\Omega$, Turn-off $R_{G,EXT} = 50\Omega$, | | 164 | | | |
| Fall time | t _f | | | 14.4 | | | |
| Turn-on energy including R _S energy | E _{ON} | inductive Load, FWD: same device with V _{GS} | | 145 | | | |
| Turn-off energy including R _S energy | E _{OFF} | = $0V$ and $R_G = 50\Omega$, | | 96 | | μЈ | |
| Total switching energy | ing energy E _{TOTAL} | T _J =150°C | | 241 | | 1 | |

 $^{4.\,}Measured\,with\,the\,switching\,test\,circuit\,in\,Figure\,23.$













Typical Performance - Dynamic (continued)

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---------------------|---|-------|-----|-----|-------|
| Parameter | Зуппоп | rest Conditions | Min | Тур | Max | UTILS |
| Turn-on delay time | t _{d(on)} | Notes 5 and 6, | | 12 | | |
| Rise time | t _r | V _{DS} =400V, I _D =25A, Gate | | 23 | | nc |
| Turn-off delay time | t _{d(off)} | Driver =0V to +15V, Turn-on $R_{G,EXT} = 1\Omega$, Turn-off $R_{G,EXT} = 5\Omega$, | | 42 | | ns |
| Fall time | t _f | | | 5.6 | | |
| Turn-on energy including R _S energy | E _{ON} | inductive Load, | | 128 | | |
| Turn-off energy including R _S energy | E _{OFF} | FWD: same device with V_{GS} = 0V and R_G = 5Ω , RC snubber: R_S =15 Ω and C_S =68pF, T_I =25°C | | 18 | | |
| Total switching energy | E _{TOTAL} | | | 146 | | μJ |
| Snubber R _S energy during turn-on | E _{RS_ON} | | | 0.5 | | |
| Snubber R _S energy during turn-off | E _{RS_OFF} | I _J =25°C | | 0.7 | | |
| Turn-on delay time | t _{d(on)} | Notes 5 and 6. | | 12 | | |
| Rise time | t _r | V _{DS} =400V, I _D =25A, Gate | | 23 | | ns |
| Turn-off delay time | $t_{d(off)}$ | Driver =0V to +15V, Turn-on $R_{G,EXT} = 1\Omega$, | | 43 | | 115 |
| Fall time | t _f | Turn-off $R_{G,EXT} = 152$, | | 8 | | |
| Turn-on energy including R _S energy | E _{ON} | inductive Load, | | 140 | | |
| Turn-off energy including R_S energy | E _{OFF} | FWD: same device with V_{GS} = 0V and R_G = 5 Ω , RC | | 21 | | |
| Total switching energy | E _{TOTAL} | snubber: $R_S=15\Omega$ and | | 161 | | μJ |
| Snubber R _S energy during turn-on | E _{RS_ON} | C _s =68pF, T _J =150°C | | 0.5 | | |
| Snubber R _S energy during turn-off | E _{RS_OFF} | | | 0.6 | | |

^{5.} Measured with the switching test circuit in Figure 24.

^{6.} In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.





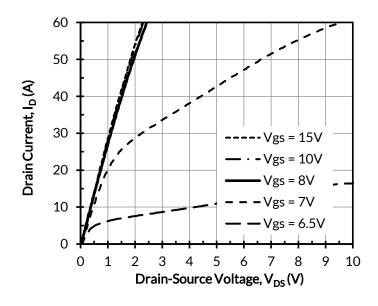








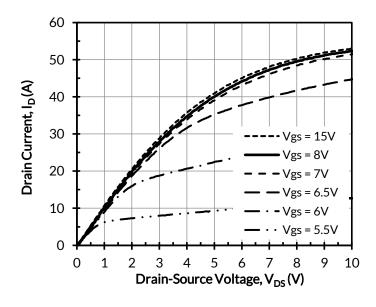
Typical Performance Diagrams



60 50 Drain Current, I_D (A) 40 30 Vgs = 15V Vgs = 8V 20 Vgs = 7V - Vgs = 6.5V 10 Vgs = 6V 0 1 2 3 5 10 Drain-Source Voltage, $V_{DS}(V)$

Figure 1. Typical output characteristics at $T_J = -55$ °C, tp < 250 μ s

Figure 2. Typical output characteristics at $T_J = 25$ °C, $tp < 250\mu s$



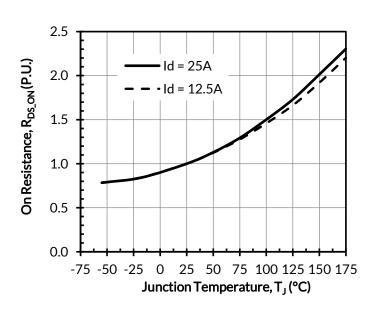


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V



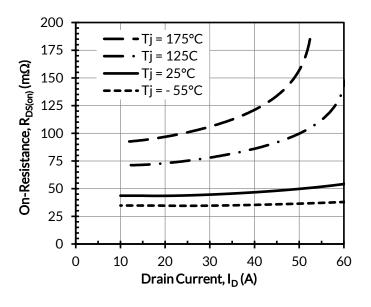








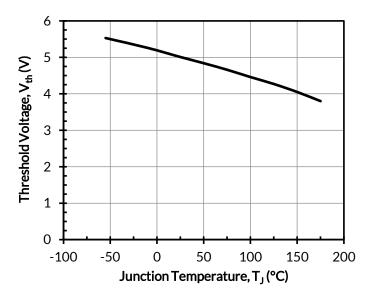




50 Tj = -55°C Tj = 25°C 40 Tj = 175°C Drain Current, I_D (A) 30 20 10 0 5 8 9 0 1 2 3 6 10 Gate-Source Voltage, $V_{GS}(V)$

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V



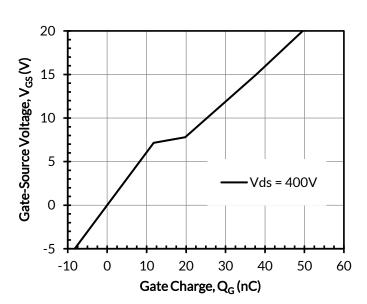


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

Figure 8. Typical gate charge at $I_D = 25A$













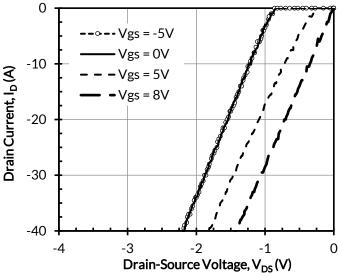


Figure 9. 3rd quadrant characteristics at $T_J = -55^{\circ}C$

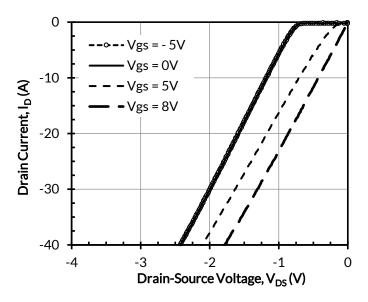


Figure 10. 3rd quadrant characteristics at T_J = 25°C

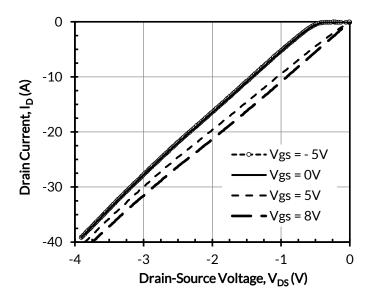


Figure 11. 3rd quadrant characteristics at $T_J = 175$ °C

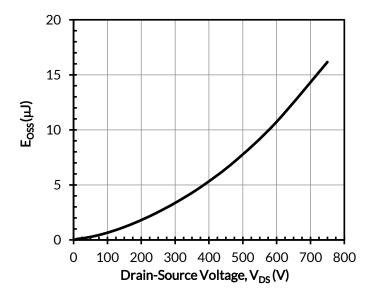


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$



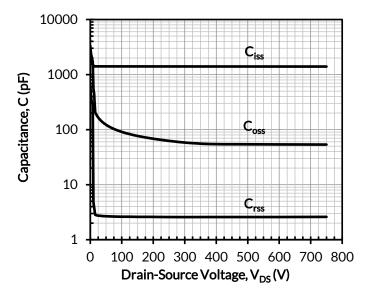












40 35 30 20 15 10 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T_c (°C)

Figure 13. Typical capacitances at f = 100kHz and $V_{GS} = 0V$

Figure 14. DC drain current derating

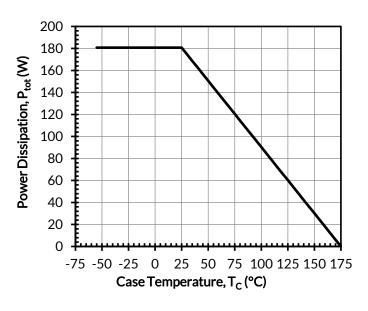


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













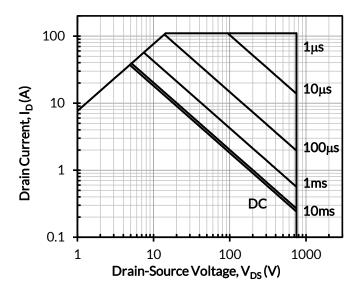


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_D

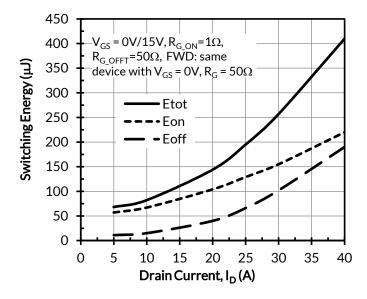


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 400V and T_J = 25°C

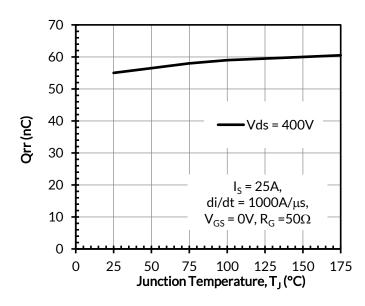


Figure 18. Reverse recovery charge Qrr vs. junction temperature

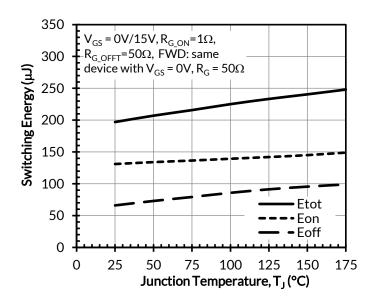


Figure 20. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_{D} = 25A













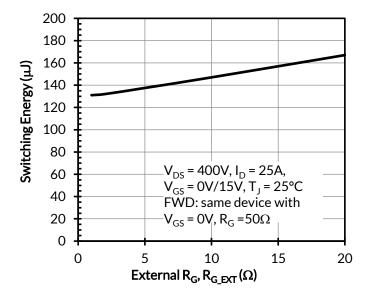


Figure 21. Clamped inductive switching turn-on energy vs. R_{G,EXT_ON}

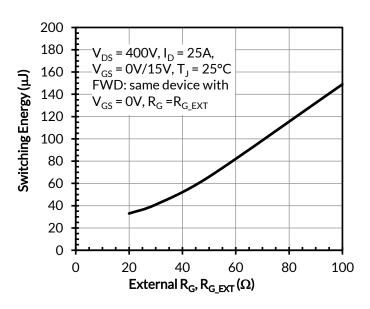


Figure 22. Clamped inductive switching turn-off energy vs. $R_{G.EXT\ OFF}$

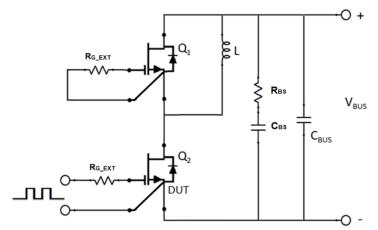


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5 Ω , C_{BS} =100nF) is used to reduce the power loop high frequency oscillations.

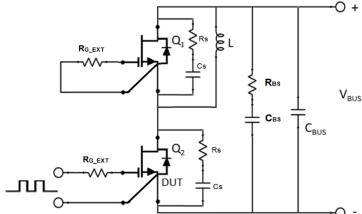


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers (R_s = 10 Ω , C_s = 68pF) and a bus RC snubber (R_{BS} = 2.5 Ω , C_{BS} =100nF).













Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode. Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

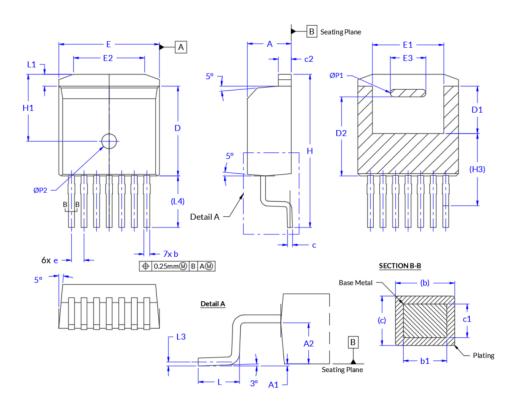
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| TO263-7L (D2PAK-7L) PACKAGE OUTLINE, MARKING, TAPE AND REEL SPECIFICATION | Page 1 of 4 |
|---|---------------------------|
| DS TO 263 71 | Rev D |

PACKAGE OUTLINE



| | 7L-D2PAK | | | | |
|-------|----------|-------|-----------|------|--|
| SYM | MM | | IN | CH | |
| 31141 | Min | Max | Min | Max | |
| Α | 4.30 | 4.56 | .169 | .180 | |
| A1 | 0.00 | 0.25 | .000 | .010 | |
| A2 | 2.45 | 2.75 | .096 | .108 | |
| b | 0.50 | 0.70 | .020 | .028 | |
| b1 | 0.50 | - | .020 | - | |
| С | 0.40 | 0.60 | .016 | .024 | |
| c1 | 0.40 | | .016 | | |
| c2 | 1.20 | 1.40 | .047 | .055 | |
| D | 8.93 | 9.23 | .352 | .363 | |
| D1 | 4.65 | 4.95 | .183 | .195 | |
| D2 | 7.90 | 8.10 | .311 | .319 | |
| e | 1.27 | BSC | .050 BSC | | |
| E | 10.08 | 10.28 | .397 | .405 | |
| E1 | 6.82 | 7.62 | .269 | .300 | |
| E2 | 6.50 | 8.60 | .256 | .339 | |
| E3 | 3.50 | 3.70 | .138 | .146 | |
| Н | 15.00 | 16.00 | .591 | .630 | |
| H1 | 6.68 | 6.88 | .263 | .271 | |
| H3 | 7.31 | REF. | .287 | REF | |
| L | 1.90 | 2.50 | .075 | .098 | |
| L1 | 0.98 | 1.42 | .039 | .056 | |
| L3 | 0.25 | BSC | .0098 BSC | | |
| L4 | 5.22 | REF | .205 | REF | |
| ØP1 | 0.65 | 0.85 | .026 | .033 | |
| ØP2 | 1.40 | 1.60 | .055 | .063 | |

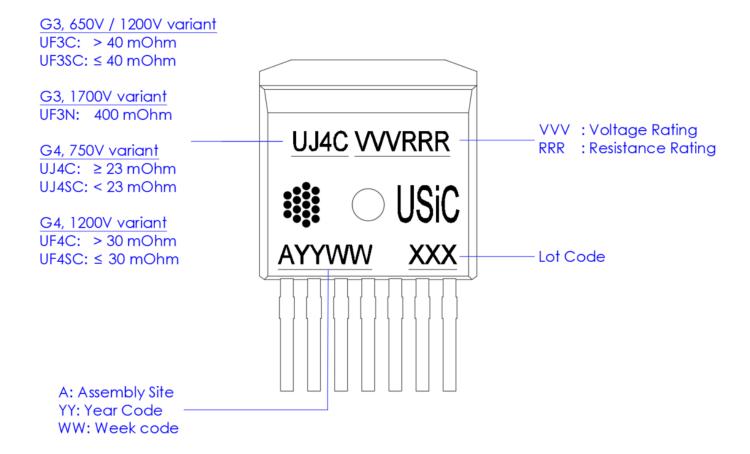
Notes:

- 1. GENERAL TOLERANCE: ±0.1 unless otherwise specified
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. PACKAGE BODY SIDES EXCLUDE MOLD FLASH AND GATE BURRS.
- 4. DIMENSION LIS MEASURED IN GAUGE LINE.
- 5. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
- 6. DIMENSION c1 AND b1 APPLIES TO BASE METAL ONLY



| TO263-7L (D2PAK-7L) PACKAGE OUTLINE, PART MARKING, TAPE AND REEL SPECIFICATION | Page 2 of 4 |
|--|---------------------------|
| DS_TO_263_7L | Rev D |

PART MARKING



Template: FOR-000530 Rev G



| TO263-7L | (D2PAK-7L) | PACKAGE | OUTLINE, | PART |
|----------|-------------|--------------------|----------|------|
| MARKING, | TAPE AND RE | EL SPECIFIC | ATION | |

TO 000 7

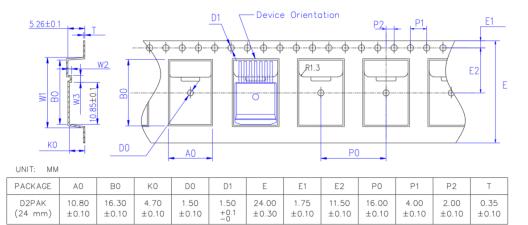
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Rev D

DS_TO_263_7L

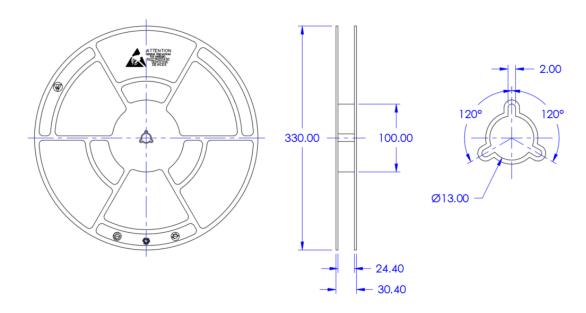
PACKING TYPE

Carrier Tape



| Ext | erior | size | |
|--------|-------|----------|------------|
| | W1 | 16.9±0.1 | |
| Spec | W2 | 1.3±0.1 | |
| ' | W3 | 1.0±0.1 | |
| | W1 | 17.2±0.1 | (1) |
| Spec 2 | W2 | 1.8±0.1 | (b) |
| | W3 | 0.85±0.1 | 0 |

Reel



All dimensions in millimeters Anti-Static Tape and Rell (T&R) Quantity per Reel: 800 units



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REVISION HISTORY

| Revision | Create Date (mm/dd/yyyy) | Description of Change | Initiator of Change |
|----------|--------------------------|---|------------------------|
| С | 11/06/2023 | Updated to Qorvo template Updated Package outline drawing based latest drawing revision | Glenn Galang |
| D | 05/21/2024 | Added illustration of device orientation on carrier tape (page 3) | Glenn Galang |
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