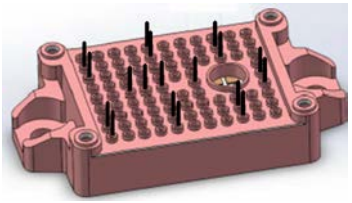
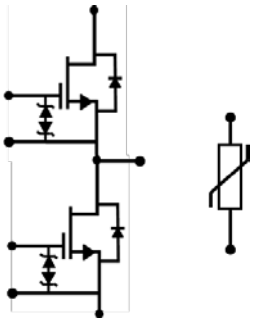
Description

United Silicon Carbide's SiC FET products feature a stacked cascode formed using its high-performance G3 Fast SiC JFETs with a optimized MOSFET to produce the only standard gate drive SiC device on the market today. This series exhibits ultra-low gate charge, but also the best reverse recovery characteristics of any device of similar ratings. These devices are excellent for switching inductive loads, and any application requiring standard gate drive.





Part Number	Package	Marking
UHB100SC12E1BC3-N	E1B	UHB100SC12E1BC3-N

Features

- Typical on-resistance $R_{DS(on),typ}$ of 9mΩ
- Maximum junction temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low C_{OSS}
- ESD protected, HBM class 2

Typical Applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Cascode Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current [1]	I_D	T_C=100°C	100	A
Pulsed drain current [2]	I_{DM}	T_C=25°C	200	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =TBD	TBD	mJ
Power dissipation	P_{tot}	T_C=25°C, Per switch	375	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C

1 Limited by package lead count
2 Pulse width t_p limited by $T_{J,max}$
3 Starting T_J = 25°C

Cascode Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V, T_J=25°C		40		μA
		V_{DS}=1200V, V_{GS}=0V, T_J=175°C		150		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_j=25°C, V_{GS}=-20V / +20V		24	80	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=100A, T_J=25°C		9	11	mΩ
		V_{GS}=12V, I_D=100A, T_J=175°C		19		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=40mA	4	5	6	V
Gate resistance	R_G	f=1MHz, open drain		1		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C=100°C			100	A
Diode pulse current [2]	$I_{S,pulse}$	T_C=25°C			200	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_F=80A, T_J=25°C		1.5	2	V
		V_{GS}=0V, I_F=80A, T_J=175°C		2		
Reverse recovery charge	Q_{rr}	V_R=800V, I_F=100A, V_{GS}=-5V, R_{G_EXT}=10Ω di/dt=2400A/μs, T_J=150°C		1040		nC
Reverse recovery time	t_{rr}			22		ns

Typical Performance - Dynamic

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=800V, V_{GS}=0V, f=100kHz		6,000		pF
Output capacitance	C_{oss}			380		
Reverse transfer capacitance	C_{rss}			2		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=0V		448		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 800V, V_{GS}=0V		1,120		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=0V		143		µJ
Total gate charge	Q_G	V_{DS}=800V, I_D=100A, V_{GS}=-5V to 15V		200		nC
Gate-drain charge	Q_{GD}			44		
Gate-source charge	Q_{GS}			76		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=100A, Gate Driver =-5V to +12V, Turn-on $R_{G,EXT}$=8.5Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: same device with V_{GS} = -5V, R_G = 20Ω T_J=25°C		TBD		ns
Rise time	t_r			TBD		
Turn-off delay time	$t_{d(off)}$			TBD		
Fall time	t_f			TBD		
Turn-on energy	E_{ON}			TBD		µJ
Turn-off energy	E_{OFF}			TBD		
Total switching energy	E_{TOTAL}			TBD		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=100A, Gate Driver =-5V to +12V, Turn-on $R_{G,EXT}$=8.5Ω, Turn-off $R_{G,EXT}$=20Ω Inductive Load, FWD: same device with V_{GS} = -5V, R_G = 20Ω T_J=150°C		TBD		ns
Rise time	t_r			TBD		
Turn-off delay time	$t_{d(off)}$			TBD		
Fall time	t_f			TBD		
Turn-on energy	E_{ON}			TBD		µJ
Turn-off energy	E_{OFF}			TBD		
Total switching energy	E_{TOTAL}			TBD		

Thermal Characteristics

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$	Per SiC FET			0.4	°C/W

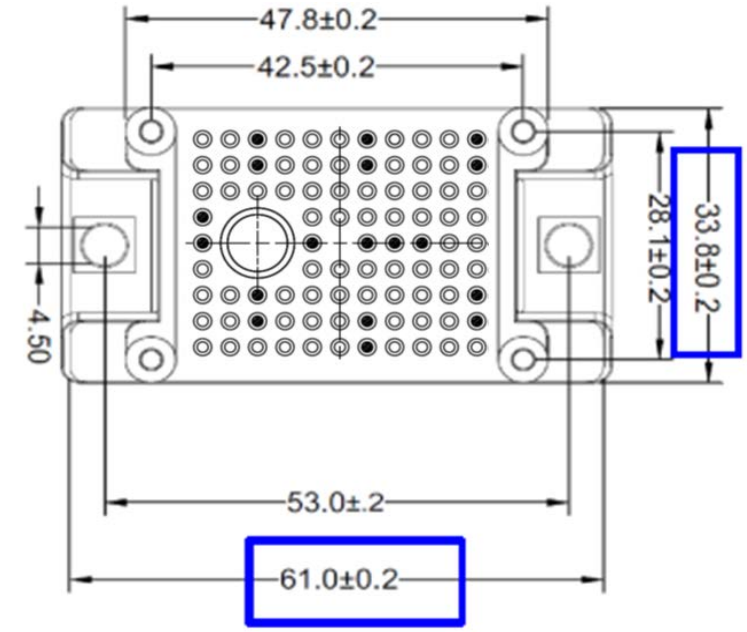
NTC Thermistor Characteristics

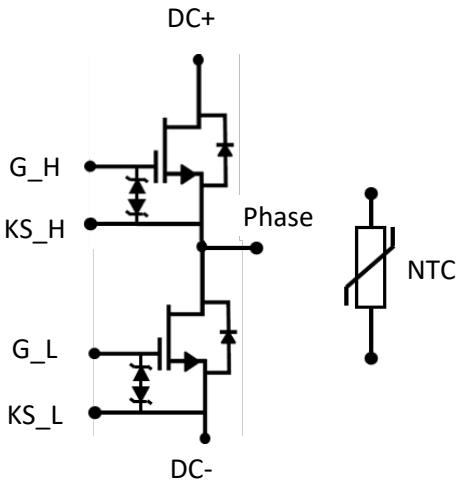
Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Rated resistance	R_{25}	T_C=25°C		TBD		kΩ
Deviation of R100	ΔR/R	T_C=25°C, R_{100}=493Ω		TBD		%
Power dissipation	P_{25}	T_C=25°C		TBD		mW
B-value	$B_{25/50}$	$R_2=R_{25}\exp[B_{25/50}(1/T_2 - 1/(298.15K))]$		TBD		K

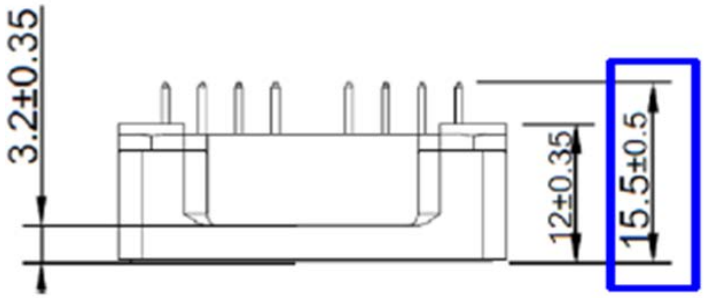
Module Characteristics

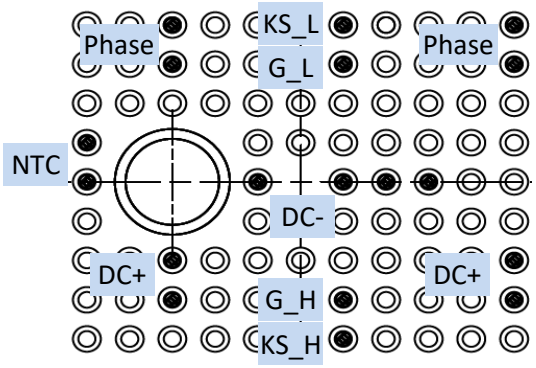
Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Isolation voltage	V_{ISOL}		TBD			kV
Internal isolation			TBD			
Stray inductance	L_{sDS}			TBD		nH
Operating and storage temperature	T_J, T_{STG}		-40		125	°C

Package Outline and Circuit Diagram









Unit: mm

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