Unigen Corp. Wireless Module Products

802.11b/g WiFi Radio Modules
UGWAS82BSM33 (APOLLO-USB-SMT)
UGWAS82GSM33 (APOLLO-SDIO-SMT)

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REVISION HISTORY

Rev. No.	History	Issue Date	Remarks
1.0	Draft	Dec. 5, 2008	Advanced information; Author: Allen B. Cabreros. FCC certificate pending. Needs Mechanical Review.

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PRODUCT INTRODUCTION

Unigen's Apollo module supports 802.11b/g radio technology. 802.11 Wireless Ethernet standards known as WLAN are currently the most popular, short range, unlicensed radio technology. With reliable transmissions, protocol stack with use of the OSI model, and over-the-air data throughput up to 54Mbps, WLAN is a radio technology for transferring large amounts of data within a short range and period of time reliably.

FEATURES AND BENEFITS

- 48-pin 20mm x 20mm module
- SDIO1.1 or USB2.0 interfaces
- Compliant to IEEE 802.11b/g standards
- Data rates up to 54Mbps
- WMM QoS
- IEEE 802.11i encryption, 64/128-bit WEP, TKIP, and AES
- WPA and WPA2 security
- Embedded LDOs, EEPROM, 40MHz and 32.768KHz crystals
- Supports antenna diversity
- Single 3.3V power supply
- Wake-On-LAN (WOL), remote wake-up
- Ready for embedded OS such as Windows CE, Linux, and more

APPLICATIONS

Personal computers, laptops, PDA's, mobile phones, portable devices, WLAN clients, embedded systems, robotics and remote controls.

PRODUCT DESCRIPTION

APOLLO Module

The Apollo family of wireless modules features the Realtek RTL8711 IEEE 802.11 b/g transceiver. Apollo modules support the 802.11b/g radio technology for wireless Ethernet transmissions and WLAN applications. The Apollo–SMT versions support either USB or SDIO interface for communications with a host controller. A host controller is required to support the full 802.11 protocol. Realtek supports protocol stacks for systems running Linux or Windows OS.

RealTek RTL8711 802.11b/g IC

The Realtek RTL 8711 chipset family is a highly integrated and cost-effective wireless LAN network interface controller that integrates an IEEE 802.11b/g Wireless LAN transceiver, PA, MAC and direct sequence spread spectrum baseband processor into one chip. RTL8711 family is fully compliant with IEEE 802.11b/g specifications.

With the help of an internal DSP-based processor, the RTL8711 family can handle on-field RF tuning, antenna select and power control. The internal DSP also assists with implementation of the IEEE 802.11 b/g MAC protocol, burst mode, block ACK, APSD, WMM management, WLAN exception handling and broadcast filtering with no interruption with the host. This greatly reduces the power consumption of the host to process the traffic from the WLAN interface.

The RTL8711 family implements a direct sequence spread spectrum (DSSS), complementary code keying (CCK) and orthogonal frequency division multiplexing (OFDM) baseband processing to support all IEEE 802.11b and 802.11b data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available along with complementary code keying to provide the data rates of 1, 2, 5.5, and 11Mbps with long or short preamble using DSSS. A high speed FFT/IFFT, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers using OFDM provides the data rate of 6, 9, 12, 18, 24, 36, 48 and 54Mbps with rate compatible punctured convolutional coding with a coding rate of 1/2, 2/3, and 3/4.

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The RTL8711 family builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate the severe multi-path effects. Efficient IQ-imbalance calibration, DC offset, phase noise, frequency offset and timing offset compensation are provided for the radio and frequency front-end impairments. Selectable digital transmit and receiver FIR filters are provided to meet he requirement of transmit spectrum mask and to reject the adjacent channel interference, respectively. Programmable scaling in the digital domain trades the quantization noise against the increasing probability of clipping in both the transmitter and receiver. Furthermore, robust signal detection, symbol boundary detection, and channel estimation are performed well at the minimum sensitivity.

The RTL8711 family support the fast receiver automatic gain control (AGC) and antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver. It also has on-chip digital-to-analog converters (DAC) and analog-to-digital (ADC, transmit TSSI and receiver RSSI input, and transmit and receiver AGC outputs. It also improves power efficiency when using the S-APSD and U-APSD. Moreover, the RTL8711 family's Smart Power Saving implementation can adapt clock rate (40MHz or 32KHz) based on dynamic traffic attribute.

The RTL8711 family supports SDIO and USB host interfaces. It also supports IEEE 802.11i security with hardware implementations of the Advanced Encryption Standard (AES) and Micro Integrity Check (MIC) for Counter Mode CBC-MAC Protocol, as well as Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP). For video, voice and multimedia applications, the RTL8711 family facilitates EDCA mechanisms compliant to WMM Quality of Service requirements.

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FUNCTIONAL BLOCK DIAGRAMS

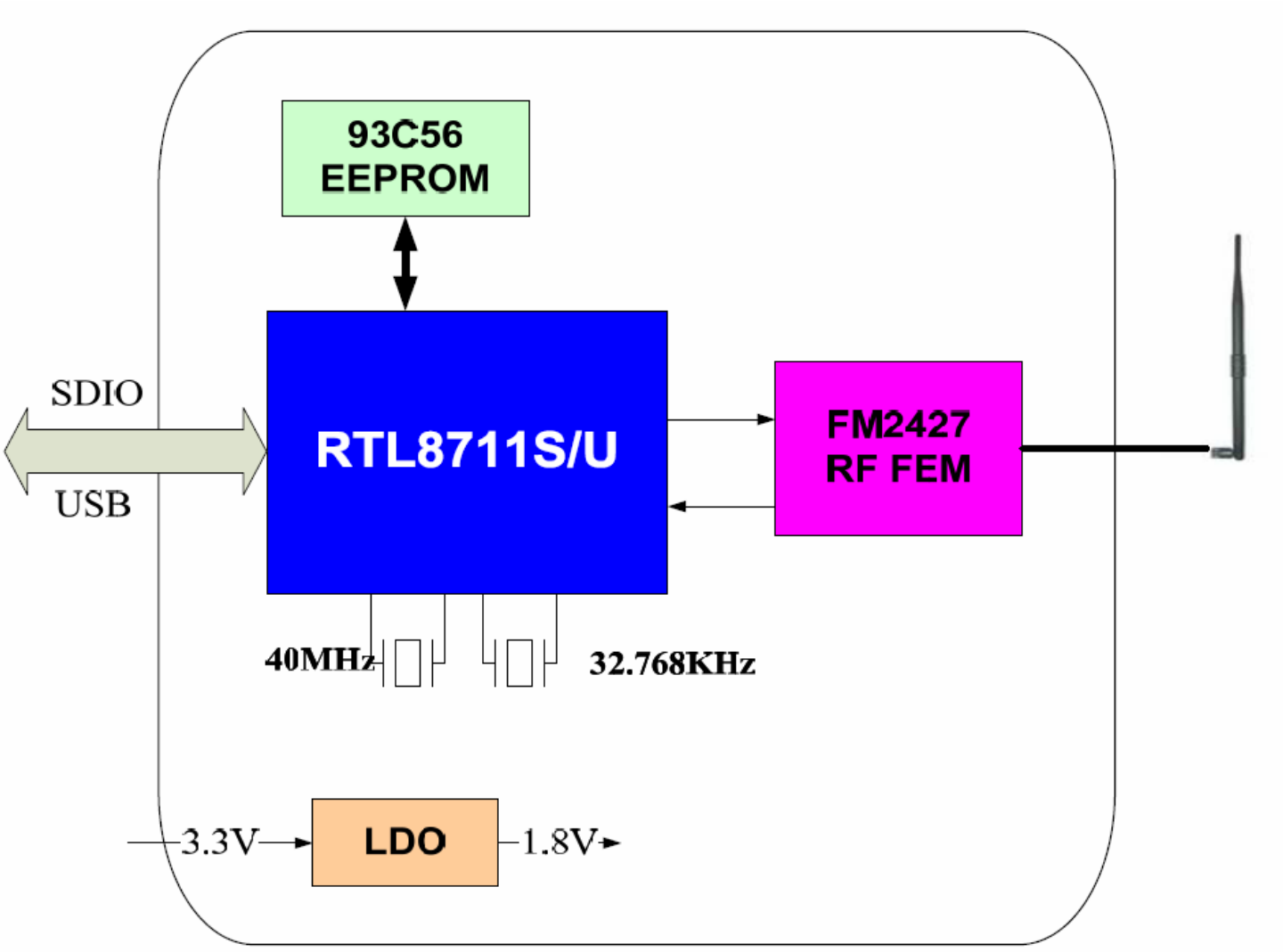

Figure 1: Module Block Diagram

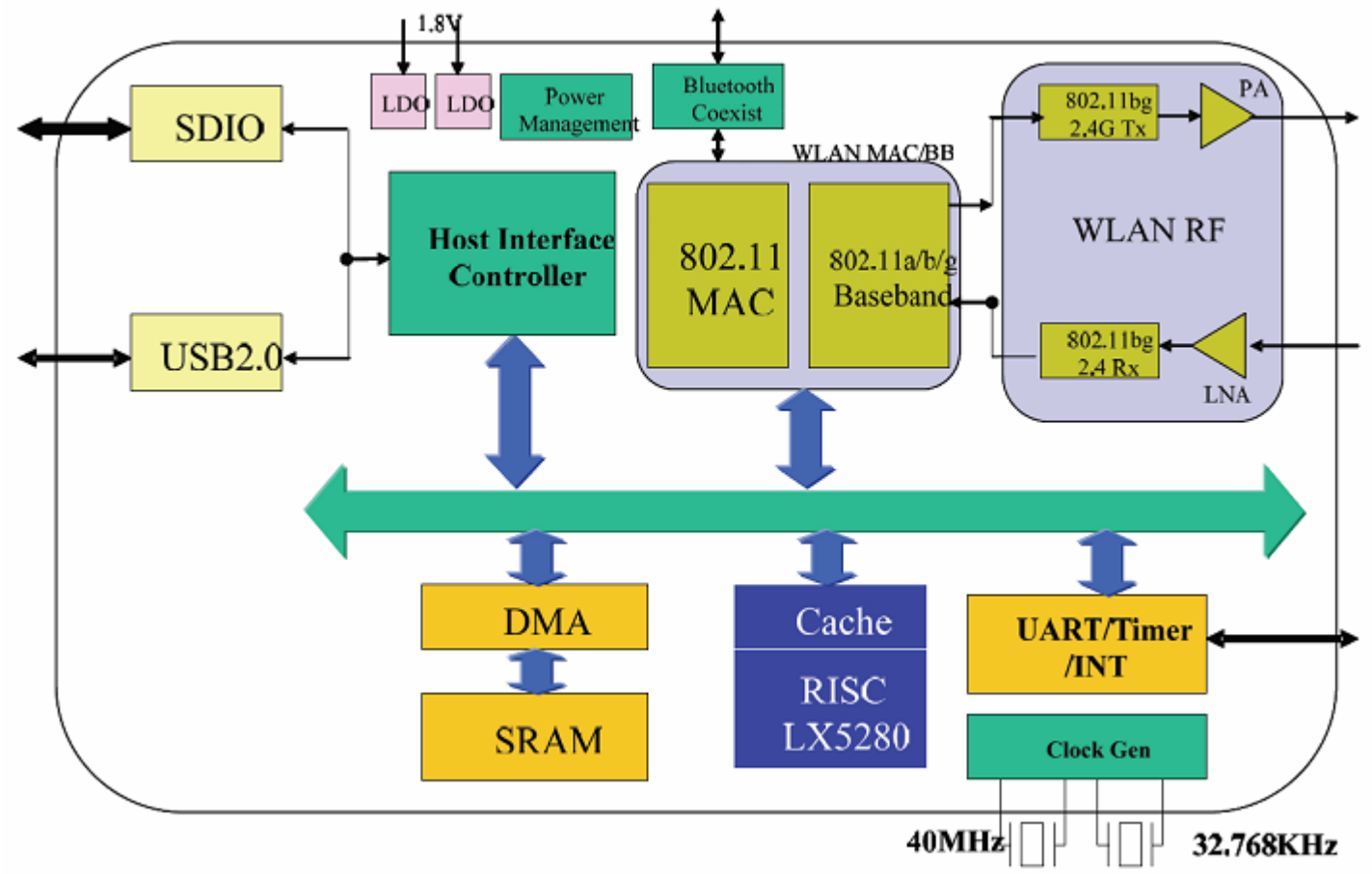

Figure 2: Component Block Diagram

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PIN ASSIGNMENT

UGWAS82GSM33 (APOLLO-SDIO-SMT)

Table 1: Pin Assignment SDIO

Pin No	Signal	Type	Description
1	VDD33	P	3.3V power supply to module
2	VDD33	P	3.3V power supply to module
3	GND	G	Module ground
4	GND	G	Module ground
5	GND	G	Module ground
6	ANT_SW-	DO	Antenna select. The antenna detects signal change states as the receiver switches from antenna to antenna during the acquisition process in antenna diversity mode. ANTSWP and ANTSWN are a pair of differential drive of antenna switches.
7	ANT_SW+	DO	Antenna select. The antenna detects signal change states as the receiver switches from antenna to antenna during the acquisition process in antenna diversity mode. ANTSWP and ANTSWN are a pair of differential drive of antenna switches.
8	GND	G	Module ground
9	ANT	RF	Antenna Port
10	GND	G	Module ground
11	BT_STA	DI	Bluetooth State. The Bluetooth state signal indicates when Bluetooth is either transmitting or receiving in the 2.4GHz ISM band.
12	BT_PRI	DI	Bluetooth Priority. The Bluetooth Priority signal is an optional signal that indicates when an important Bluetooth packet is being transmitted or received.
13	WL_ACT	DO	WLAN Active. The WLAN Active signal indicates when WLAN is either transmitting or receiving in the 2.4GHz ISM band.
14	WL_RX_IND	DO	WLAN Receive Indication. The WLAN Receive Indication signal indicates when 2.4GHz ISM band is being occupied for WLAN transmission.
15	GND	G	Module ground

16	XO_32.768K	XO	32.768KHz XTAL output pin. The module can optionally use an external 32.768KHz crystal if the crystal is available on the module.
Pin No	**Signal**	**Type**	**Description**
17	XI_32.768K	XI	32.768KHz XTAL input pin. The module can optionally use an external 32.768KHz crystal if the crystal is available on the module.
18	J_TMS	DI	For test purposes
19	J_TDI	DI	For test purposes
20	EESIZE	DI	EEPROM size selection 0: (pull low) 93C46 1: (pull high) 93C56 This pin was denoted as "J_TDO" on the schematics
21	J_RST_N	DI	For test purposes
22	GND	G	Module ground
23	J_CLK	DI	JTAG test clock
24	U_S_OUT	DO	USRT serial out
25	U_S_IN	DI	USRT serial in
26	EEDO	DI	For debug purposes
27	GND	G	G
28	HIFSEL1	DI	Host interface select. This pin must be tied high. This pin was denoted as "EEDI" on the schematics
29	HIFSEL0	DI	Host interface select. This pin must be tied high. This pin was denoted as "EECS" on the schematics
30	SD_D[1]	DI/O	SDIO data line 1 or interrupt output
31	SD_D[0]	DI/O	SDIO data line 0
32	VDD33	P	3.3V power supply to the module
33	GND	G	Module ground
34	GND	G	Module ground
35	SD_CLK	DI	SDIO clock
36	GND	G	Module ground
37	SD_CMD	DI/O	SDIO command line
38	SD_D[3]	DI/O	SDIO data line 3
39	GND	G	Module ground
40	SD_D[2]	DI/O	SDIO data line 2 or read wait
41	GND	G	Module ground

42	GND	G	Module ground
43	RX_I+	AI	For debug purposes
44	RX_Q+	AI	For debug purposes
45	GND	G	Module ground
46	GND	G	Module ground
Pin No	**Signal**	**Type**	**Description**
47	GND	G	Module ground
48	VDD33	P	3.3V power supply to the module

UGWAS82BSM33 (APOLLO-USB-SMT)

Table 2: Pin Assignment USB

Pin No	Signal	Type	Description
1	VDD33	P	3.3V power supply to module
2	VDD33	P	3.3V power supply to module
3	GND	G	Module ground
4	GND	G	Module ground
5	GND	G	Module ground
6	ANT_SW-	DO	Antenna select. The antenna detects signal change states as the receiver switches from antenna to antenna during the acquisition process in antenna diversity mode. ANTSWP and ANTSWN are a pair of differential drive of antenna switches.
7	ANT_SW+	DO	Antenna select. The antenna detects signal change states as the receiver switches from antenna to antenna during the acquisition process in antenna diversity mode. ANTSWP and ANTSWN are a pair of differential drive of antenna switches.
8	GND	G	Module ground
9	ANT	RF	Antenna Port
10	GND	G	Module ground
11	BT_STA	DI	Bluetooth State. The Bluetooth state signal indicates when Bluetooth is either transmitting or receiving in the 2.4GHz ISM band.
12	BT_PRI	DI	Bluetooth Priority. The Bluetooth Priority signal is an optional signal that indicates when an important Bluetooth packet is being transmitted or received.
			WLAN Active. The WLAN Active signal indicates

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13	WL_ACT	DO	when WLAN is either transmitting or receiving in the 2.4GHz ISM band.
14	WL_RX_IND	DO	WLAN Receive Indication. The WLAN Receive Indication signal indicates when 2.4GHz ISM band is being occupied for WLAN transmission.
15	GND	G	Module ground
16	XO_32.768K	XO	32.768KHz XTAL output pin. The module can optionally use an external 32.768KHz crystal if the crystal is available on the module.
Pin No	**Signal**	**Type**	**Description**
17	XI_32.768K	XI	32.768KHz XTAL input pin. The module can optionally use an external 32.768KHz crystal if the crystal is available on the module.
18	J_TMS	DI	For test purposes
19	J_TDI	DI	For test purposes
20	EESIZE	DI	EEPROM size selection 0: (pull low) 93C46 1: (pull high) 93C56 This pin was denoted as "J_TDO" on the schematics
21	J_RST_N	DI	For test purposes
22	GND	G	Module ground
23	J_CLK	DI	JTAG test clock
24	U_S_OUT	DO	USRT serial out
25	U_S_IN	DI	USRT serial in
26	EEDO	DI	For debug purposes
27	GND	G	G
28	HIFSEL1	DI	Host interface select. This pin must be tied high. This pin was denoted as "EEDI" on the schematics
29	HIFSEL0	DI	Host interface select. This pin must be tied high. This pin was denoted as "EECS" on the schematics
30	VDD33	P	3.3V power supply to the module
31	GND	G	Module ground
32	NC		No connection
33	GND	G	Module ground
34	GND	G	Module ground
35	GND	G	Module ground

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36	VDD33	P	3.3V power supply to the module
37	GND	G	Module ground
38	HSDP	AI/O	High Speed USB PHY differential IO pins
39	GND	G	Module ground
40	HSDM	AI/O	High Speed USB PHY differential IO pins
41	GND	G	Module ground
42	GND	G	Module ground
43	RX_I+	AI	For debug purposes
44	RX_Q+	AI	For debug purposes
45	GND	G	Module ground
46	GND	G	Module ground
Pin No	**Signal**	**Type**	**Description**
47	GND	G	Module ground
48	VDD33	P	3.3V power supply to the module

TEMPERATURE LIMIT RATINGS

Table 3: Temperature Limit Ratings

Symbol	Definition	Min.	Max.	Unit
Ts	Storage Temperature Range	-55	+125	°C
Tap	Ambient Operating Temperature	-10	+70	°C

DC ELECTRICAL CHARACTERISTICS

Table 4: DC Electrical Characteristics

Symbol	Description	Conditions	Value			
			Min	Typ	Max	Unit
VDD33	Supply Voltages		3.0	3.3	3.6	V
Voh	Min. high level output voltage	IOH = –8mA	0.9 * VDD33		VDD33	V
Vol	Max. low level output voltage	IOL = 8mA			0.1 * VDD33	V
Vih	Min. high level input voltage		0.5 * VDD33		VDD33 + 0.5	V
Vil	Max. low level		-0.5		0.3 *	V

	input voltage				VDD33	
Iin	Input current	Vin = VDD33 or GND	-1.0		+1.0	µA
Ioz	Tri-state output leakage current	Vout = VDD33 or GND	-10		10	mA
Icc	Average operating supply current	Iout = 0mA			160	mA

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POWER CONSUMPTION CHARACTERISTICS

Table 5: Power Consumption Characteristics

Parameter	Conditions	Specifications	Units
Transmit mode	Continuous Tx @ 14dBm	< 310	mA
Receive mode	Continuous RX	< 290	mA

RF CHARACTERISTICS

Table 6: RF Characteristics

Parameter	Conditions	Specifications	Units
RF channel support		2412, 2417, 2422, 2427, 2432, 2437, 2442, 2447, 2452, 2457, 2462, 2467, 2472, 2482	MHz
RF output power	OFDM, EVM<-25dBm	14	dBm
	CCK, EVM<10%	17	dBm
Receiver sensitivity	OFDM, 54Mbps	≤ -69	dBm
	CCK, 11Mbps	≤ -63	dBm
Transmit EVM	OFDM, 54Mbps	< -25	dBm
	CCK	≤ 10%	
Frequency offset		±25	ppm
Transmit Spectrum Mask		Conform to IEEE 802.11b/g Spectrum Mask	

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INTERFACE CHARACTERISTICS

SDIO Interface Timing

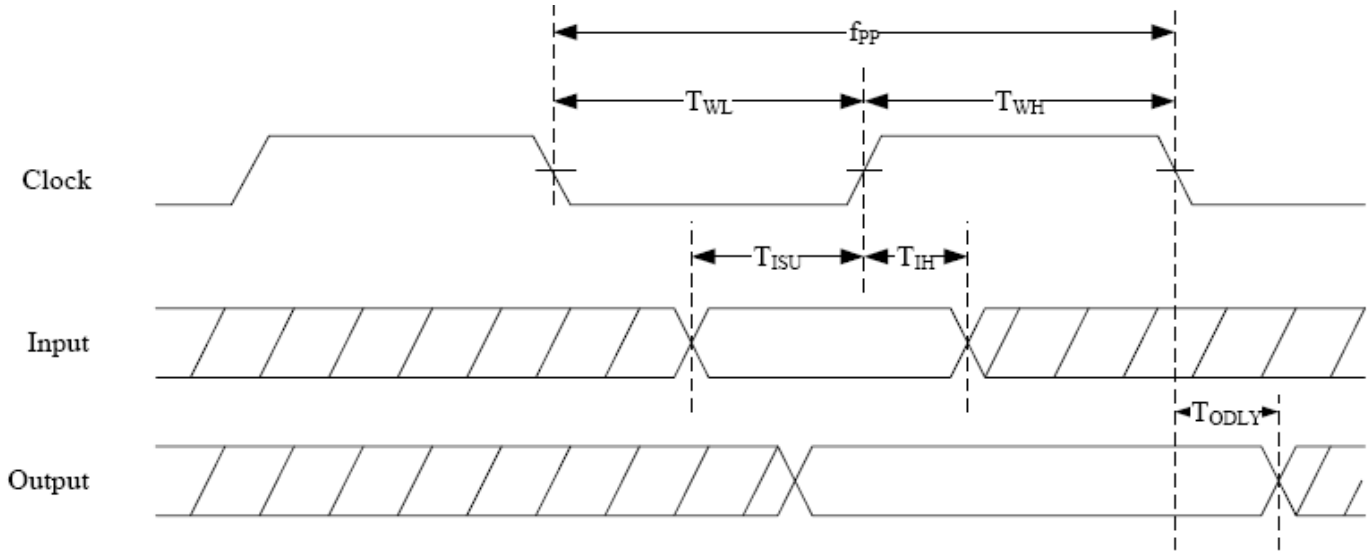

Figure 3: SDIO Interface Timing

Table 7: SDIO Timing

Symbol	Parameter	Mode	MIN	MAX	Unit
Fpp	Clock frequency		0	25	MHz
TWL	Clock low time		10		ns
					ns
TWH	Clock high time		10		ns
TISU	Input setup time		5		ns
TIH	Input hold time		5		ns
TODLY	Output delay time			14	ns

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SERIAL EEPROM CHARACTERISTICS

The Apollo modules come with an embedded serial EEPROM to hold register configuration settings that the RTL8711 will use during boot up. The APOLLO-USB-SMT modules use the 93C46 1K bits serial EEPROM. The APOLLO-SDIO-SMT modules use the 93C56 2K bits serial EEPROM. The RTL8711 will automatically load the system configuration data from the EEPROM after a power-on sequence. The host can recall these configurations anytime by issuing the software EEPROM auto-load command via the host interface. The host can read/write to the EEPROM using "bit banging" accesses via the 9346CR register.

Although the EEPROM contents are normally addressed by words, the contents are listed below by bytes for convenience. After the initial power-on the RTL8711 performs a series of read operations from the EEPROM addresses from 00h to 31h.

Note: It is suggested to obtain Realtek or Unigen approval before changing the default contents of the EEPROM.

APOLLO-USB-SMT

Table 8: EEPROM USB

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th></tr>
<tr><td>00h</td><td>11h</td><td>These two bytes contain the ID code word for the RTL8711. The RTL8711 will load the contents of the EEPROM into the corresponding location if the ID word (8711h) is correct</td></tr>
<tr><td>01h</td><td>87h</td><td></td></tr>
<tr><td>02h</td><td>SystemCfg</td><td>bit7-3: Reserved
bit2-0: System Configuration

<table><tr><th>Bit</th><th>Description</th></tr><tr><td>2</td><td>PA type select:
1: External PA
0: Internal PA</td></tr><tr><td>1</td><td>Band Select
1: A band exists
0: A band doesn't exist</td></tr><tr><td>0</td><td>Clock Source
1: XTAL mode
0: Oscillator mode</td></tr></table></td></tr>
</table>

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<table>
<tr><td>02h-08h</td><td>MAC Address</td><td>After the auto-load command or a hardware reset, the RTL8711 loads the MAC address to IDR0-IDR5 of the I/O registers of the RTL8711</td></tr>
<tr><td>09h</td><td>CONFIG0</td><td>Configuration Register 0 of WLAN registers</td></tr>
<tr><td>0Ah-0Bh</td><td>Version</td><td>The version of EEPROM contents</td></tr>
<tr><td>0Ch</td><td>HACR</td><td>Host Access Control Register

<table><tr><th>Bit</th><th>Description</th></tr><tr><td>7:4</td><td>Reserved</td></tr><tr><td>3</td><td>Half-Word Byte Swapping: Byte Swapping before data is written into LBA if data register is NOT auto-pending.
0: disable
1: Enable</td></tr><tr><td>2</td><td>Word Swapping: Byte Swapping before data is written into LBA register is NOT auto-pending
0: disable
1: Enable</td></tr><tr><td>1</td><td>Half Word Swapping: Byte swapping before data is written into LBA if data register is NOT auto-pending.
0: disable
1: Enable</td></tr><tr><td>0</td><td>Byte Swapping: Byte swapping before data is written into LBA if data register is auto-pending.
0: disable
1: Enable</td></tr></table>
Notes: Currently, SDIO, CF+ and Local Memory are Little Endian bus. Therefore, WSWAP=1, and BSWAP=, HWSWAP=0, and must be these “default values”</td></tr>
<tr><td>0Dh-0Eh</td><td>CRC</td><td>16-bit CRC value of EEPROM content</td></tr>
<tr><td>0Fh</td><td>ChannelPlan</td><td>Channel Plan: Map of channels to be scanned</td></tr>
<tr><td>10h</td><td>EnergyDetThr</td><td>Energy Detection threshold</td></tr>
<tr><td>11h</td><td>TxPowerb1</td><td>Transmit Power Level for 802.11b-defined channel_ID 1 (CCK)</td></tr>
<tr><td>12h</td><td>TxPowerb6</td><td>Transmit Power Level for 802.11b-defined channel_ID 6 (CCK)</td></tr>
<tr><td>13h</td><td>TxPowerb11</td><td>Transmit Power Level for 802.11b-defined channel_ID 11 (CCK)</td></tr>
<tr><td>14h</td><td>TxPowerb14</td><td>Transmit Power Level for 802.11b-defined channel_ID 14 (CCK)</td></tr>
<tr><td>15h</td><td>TxPower1</td><td>Transmit Power Level for 802.11g-defined channel_ID 1 (OFDM)</td></tr>
<tr><td>16h</td><td>TxPowerg6</td><td>Transmit Power Level for 802.11g-defined channel_ID 6 (OFDM)</td></tr>
<tr><td>17h</td><td>TxPowerg11</td><td>Transmit Power Level for 802.11g-defined channel_ID 11 (OFDM)</td></tr>
<tr><td>18h</td><td>TxPowerg14</td><td>Transmit Power Level for 802.11g-defined channel_ID 14 (OFDM)</td></tr>
<tr><td>19h</td><td>TSSI</td><td>TSSI for 802.11b channel 1</td></tr>
<tr><td>1Ah</td><td>TSSI</td><td>TSSI for 802.11b channel 6</td></tr>
<tr><td>1Bh</td><td>TSSI</td><td>TSSI for 802.11b channel 11</td></tr>
<tr><td>1Ch</td><td>TSSI</td><td>TSSI for 802.11b channel 14</td></tr>
<tr><td>1Dh</td><td>TSSI</td><td>TSSI for 802.11g channel 1</td></tr>
</table>

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<table>
<tr><td>1Eh</td><td>TSSI</td><td>TSSI for 802.11g channel 6</td></tr>
<tr><td>1Fh</td><td>TSSI</td><td>TSSI for 802.11g channel 11</td></tr>
<tr><td>20h</td><td>TSSI</td><td>TSSI for 802.11g channel 14</td></tr>
<tr><td>21h</td><td>TxPower100</td><td>Transmit Power Level for 802.11a-defined channel_ID 100 except Japan
Transmit Power Level for 802.11a-defined channel_ID 7 for Japan</td></tr>
<tr><td>22h</td><td>TxPower104</td><td>Transmit Power Level for 802.11a-defined channel_ID 104 except Japan
Transmit Power Level for 802.11a-defined channel_ID 8 for Japan</td></tr>
<tr><td>23h</td><td>TxPower108</td><td>Transmit Power Level for 802.11a-defined channel_ID 108 except Japan
Transmit Power Level for 802.11a-defined channel_ID 9 for Japan</td></tr>
<tr><td>24h-2Bh</td><td>Reserve</td><td>Reserve</td></tr>
<tr><td>2Ch</td><td>VID</td><td>USB Vendor ID High Byte</td></tr>
<tr><td>2Dh</td><td>VID</td><td>USB Vendor ID Low Byte</td></tr>
<tr><td>2Eh</td><td>PID</td><td>USB Product ID High Byte</td></tr>
<tr><td>2Fh</td><td>PID</td><td>USB Product ID Low Byte</td></tr>
<tr><td>30h</td><td>Manufacture String Length</td><td>Length of manufacture string in bytes. The encoding method of the manufacture string must be in UTF-8</td></tr>
<tr><td>31h</td><td>Product String Length</td><td>Length of product string in bytes. The encoding method of the product string must be in UTF-8</td></tr>
<tr><td>32h-5Fh</td><td>Manufacture String
&
Product String</td><td>Manufacture and Product String: These bits are specify both the Manufacture’s information and device information for the USB standard request. Maximum total length of these two strings is 48 bytes.</td></tr>
<tr><td>60h-62h</td><td>Country String</td><td>The Country String of Country Information Element. The Country String field of the element shall be 3 octets in length. The AP shall set this field to the value contained in the dot11CountryString attribute before transmission in a Beacon or Probe Response frame. Upon reception of this element, a STA shall set the value of the dot11CountryString to the value contained in this field.</td></tr>
<tr><td>63h</td><td>Frequency Offset</td><td>Tuning Cap for G mode</td></tr>
<tr><td>64h</td><td>TxPower153</td><td>Transmit Power Level for 802.11a-defined channel_ID 153 except Japan
Transmit Power Level for 802.11a-defined channel_ID 192 for Japan</td></tr>
<tr><td>65h</td><td>TxPower157</td><td>Transmit Power Level for 802.11a-defined channel_ID 157 except Japan
Transmit Power Level for 802.11a-defined channel_ID 196 for Japan</td></tr>
<tr><td>66h</td><td>TxPower161</td><td>Transmit Power Level for 802.11a-defined channel_ID 161</td></tr>
<tr><td>67h</td><td>TxPower165</td><td>Transmit Power Level for 802.11a-defined channel_ID 165</td></tr>
<tr><td>68h</td><td>USBCFG</td><td>
<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:2</td><td>Reserved</td></tr>
<tr><td>1</td><td>Using Bulk endpoints for Lexra Registers Read/Write/ This bit is used for 8051 firmware reporting the endpoint descriptors to hosts.
0: No (Using interrupt endpoints)
1: Yes</td></tr>
<tr><td>0</td><td>System Clock Setting when boot from NAND. This bit is for USB 8051 Firmware raising system clock to 40MHz or 60MHz.</td></tr>
</table>
</td></tr>
</table>

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		0: 40MHz 1: 60Mhz
78h	USBPHY_E0	RX Sensitivity Value for USB PHY Register 0xE0 (PLL Bandwidth). Default value 0x99
79h	USBPHY_E1	RX Sensitivity Value for USB PHY Register 0xE1 (PLL Bandwidth). Default value 0xAC
7Ah	USBPHY_E2	RX Sensitivity Value for USB PHY Register 0xE2 (HS RX Sensitivity & HS TX output swing). Default value 0x4F
7Bh	USBPHY_E3	RX Sensitivity Value for USB PHY Register 0xE3 (FS/LS TX output swing). Default value 0xE0
7Ch	USBPHY_E4	RX Sensitivity Value for USB PHY Register 0xE4 (HS Slew rate control). Default value 0x09
7Dh	USBPHY_E5	RX Sensitivity Value for USB PHY Register 0xE5 (impedance match). Default value 0x10
7Eh	USBPHY_E6	RX Sensitivity Value for USB PHY Register 0xE6 (impedance match & sensitivity for disconnect). Default value 0x98
7Fh	USBPHY_F0	RX Sensitivity Value for USB PHY Register 0xF0 (HS RX Sensitivity & HS TX output swing). Default value 0x4F

APOLLO-SDIO-MT

Table 9: EEPROM SDIO

<table>
<tr><th>Bytes</th><th>Contents</th><th>Description</th></tr>
<tr><td>00h</td><td>11h</td><td>These two bytes contain the ID code word for the RTL8711. The RTL8711 will load the contents of the EEPROM into the corresponding location if the ID word (8711h) is correct</td></tr>
<tr><td>01h</td><td>87h</td><td></td></tr>
<tr><td>02h</td><td>SystemCfg</td><td>bit7-3: Reserved
bit2-0: System Configuration

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>2</td><td>PA type select:
1: External PA
0: Internal PA</td></tr>
<tr><td>1</td><td>Band Select
1: A band exists
0: A band doesn’t exist</td></tr>
<tr><td>0</td><td>Clock Source
1: XTAL mode</td></tr>
</table>
</td></tr>
</table>

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<table>
<tr><td></td><td></td><td><table><tr><td></td><td>0: Oscillator mode</td></tr></table></td></tr>
<tr><td>02h-08h</td><td>MAC Address</td><td>After the auto-load command or a hardware reset, the RTL8711 loads the MAC address to IDR0-IDR5 of the I/O registers of the RTL8711</td></tr>
<tr><td>09h</td><td>CONFIG0</td><td>Configuration Register 0 of WLAN registers</td></tr>
<tr><td>0Ah-0Bh</td><td>Version</td><td>The version of EEPROM contents</td></tr>
<tr><td>0Ch</td><td>HACR</td><td>Host Access Control Register

<table><tr><th>Bit</th><th>Description</th></tr><tr><td>7:4</td><td>Reserved</td></tr><tr><td>3</td><td>Half-Word Byte Swapping: Byte Swapping before data is written into LBA if data register is NOT auto-pending.
0: disable
1: Enable</td></tr><tr><td>2</td><td>Word Swapping: Byte Swapping before data is written into LBA register is NOT auto-pending
0: disable
1: Enable</td></tr><tr><td>1</td><td>Half Word Swapping: Byte swapping before data is written into LBA if data register is NOT auto-pending.
0: disable
1: Enable</td></tr><tr><td>0</td><td>Byte Swapping: Byte swapping before data is written into LBA if data register is auto-pending.
0: disable
1: Enable</td></tr></table>
Notes: Currently, SDIO, CF+ and Local Memory are Little Endian bus. Therefore, WSWAP=1, and BSWAP=, HWSWAP=0, and must be these “default values”</td></tr>
<tr><td>0Dh-0Eh</td><td>CRC</td><td>16-bit CRC value of EEPROM content</td></tr>
<tr><td>0Fh</td><td>ChannelPlan</td><td>Channel Plan: Map of channels to be scanned</td></tr>
<tr><td>10h</td><td>EnergyDetThr</td><td>Energy Detection threshold</td></tr>
<tr><td>11h</td><td>TxPowerb1</td><td>Transmit Power Level for 802.11b-defined channel_ID 1 (CCK)</td></tr>
<tr><td>12h</td><td>TxPowerb6</td><td>Transmit Power Level for 802.11b-defined channel_ID 6 (CCK)</td></tr>
<tr><td>13h</td><td>TxPowerb11</td><td>Transmit Power Level for 802.11b-defined channel_ID 11 (CCK)</td></tr>
<tr><td>14h</td><td>TxPowerb14</td><td>Transmit Power Level for 802.11b-defined channel_ID 14 (CCK)</td></tr>
<tr><td>15h</td><td>TxPower1</td><td>Transmit Power Level for 802.11g-defined channel_ID 1 (OFDM)</td></tr>
<tr><td>16h</td><td>TxPowerg6</td><td>Transmit Power Level for 802.11g-defined channel_ID 6 (OFDM)</td></tr>
<tr><td>17h</td><td>TxPowerg11</td><td>Transmit Power Level for 802.11g-defined channel_ID 11 (OFDM)</td></tr>
<tr><td>18h</td><td>TxPowerg14</td><td>Transmit Power Level for 802.11g-defined channel_ID 14 (OFDM)</td></tr>
<tr><td>19h</td><td>TSSI</td><td>TSSI for 802.11b channel 1</td></tr>
<tr><td>1Ah</td><td>TSSI</td><td>TSSI for 802.11b channel 6</td></tr>
<tr><td>1Bh</td><td>TSSI</td><td>TSSI for 802.11b channel 11</td></tr>
<tr><td>1Ch</td><td>TSSI</td><td>TSSI for 802.11b channel 14</td></tr>
</table>

<table>
<tr><td>1Dh</td><td>TSSI</td><td>TSSI for 802.11g channel 1</td></tr>
<tr><td>1Eh</td><td>TSSI</td><td>TSSI for 802.11g channel 6</td></tr>
<tr><td>1Fh</td><td>TSSI</td><td>TSSI for 802.11g channel 11</td></tr>
<tr><td>20h</td><td>TSSI</td><td>TSSI for 802.11g channel 14</td></tr>
<tr><td>21h</td><td>TxPower100</td><td>Transmit Power Level for 802.11a-defined channel_ID 100 except Japan
Transmit Power Level for 802.11a-defined channel_ID 7 for Japan</td></tr>
<tr><td>22h</td><td>TxPower104</td><td>Transmit Power Level for 802.11a-defined channel_ID 104 except Japan
Transmit Power Level for 802.11a-defined channel_ID 8 for Japan</td></tr>
<tr><td>23h</td><td>TxPower108</td><td>Transmit Power Level for 802.11a-defined channel_ID 108 except Japan
Transmit Power Level for 802.11a-defined channel_ID 9 for Japan</td></tr>
<tr><td>24h-2Bh</td><td>Reserve</td><td>Reserve</td></tr>
<tr><td>2Ch</td><td>SDIO Setting</td><td>SDIO Function Register
<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>7:4</td><td>Reserved</td></tr>
<tr><td>3</td><td>SCSI: Support Continuous SPI Interrupt.
0: Disable
1: Enable
Default Enable</td></tr>
<tr><td>2</td><td>S4MI: Support Interrupts between blocks of data in 4-bit SD mode.
0: Disable
1: Enable
Default Enable</td></tr>
<tr><td>1</td><td>SMB: Support Multi-Block.
0: Disable
1: Enable
Default Enable</td></tr>
<tr><td>0</td><td>SDC: Support Direct Commands.
0: Disable
1: Enable
Default Enable</td></tr>
</table>
Note: SCSI, SDC, SMB, and S4MI are in CCCR register.</td></tr>
<tr><td>2Dh-2Fh</td><td>OCR</td><td>OCR Value. Little Endian order. This value must be consistent with CIS tuple value.</td></tr>
<tr><td>30h</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>31h-41h</td><td>Common CIS Data</td><td>20 04 4C 02 00 00 //CISTPL_MANFID
21 02 0C 00 //CISTPL_FUNCID
22 04 00 08 00 32 FF //CISTPL_FUNCE</td></tr>
<tr><td>42h-AFh</td><td>Function 1 CIS Data</td><td>21 02 0C 00 //CISTPL_FUNCID
22 2A //CISTPL_FUNCE
01 01 00 00 00 00 00 00 – 00 00 00 00 00 02 00 FF
FF 00 00 00 00 00 00 00 – 00 00 00 00 00 00 00 00
00 00 EB 00 6E 01 00 00 – 00 00
22 08 04 06 00 E0 4C 87 11 01 // MAC ADDRESS</td></tr>
</table>

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		15 35 //CISTPL_VERS_1 87 11 …(46 Bytes Product String)… FF FF
B0h-B2h	Country String	The Country String of Country Information Element. The Country String field of the element shall be 3 octets in length. The AP shall set this field to the value contained in the dot11CountryString attribute before transmission in a Beacon or Probe Response frame. Upon reception of this element, a STA shall set the value of the dot11CountryString to the value contained in this field.
B3h	TxPower149	Transmit Power Level for 802.11a-defined channel_ID 149 except Japan Transmit Power Level for 802.11a-defined channel_ID 189 for Japan
B4h	TxPower153	Transmit Power Level for 802.11a-defined channel_ID 153 except Japan Transmit Power Level for 802.11a-defined channel_ID 192 for Japan
B5h	TxPower157	Transmit Power Level for 802.11a-defined channel_ID 157 except Japan Transmit Power Level for 802.11a-defined channel_ID 196 for Japan
B6h	TxPower161	Transmit Power Level for 802.11a-defined channel_ID 161
B7h	TxPower165	Transmit Power Level for 802.11a-defined channel_ID 165
B8h	Reserved	Reserved
B9h	Frequency Offset	Tuning Cap for G mode

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APPLICATION SCHEMATIC

UGWAS82GSM33 (APOLLO-SDIO-SMT)

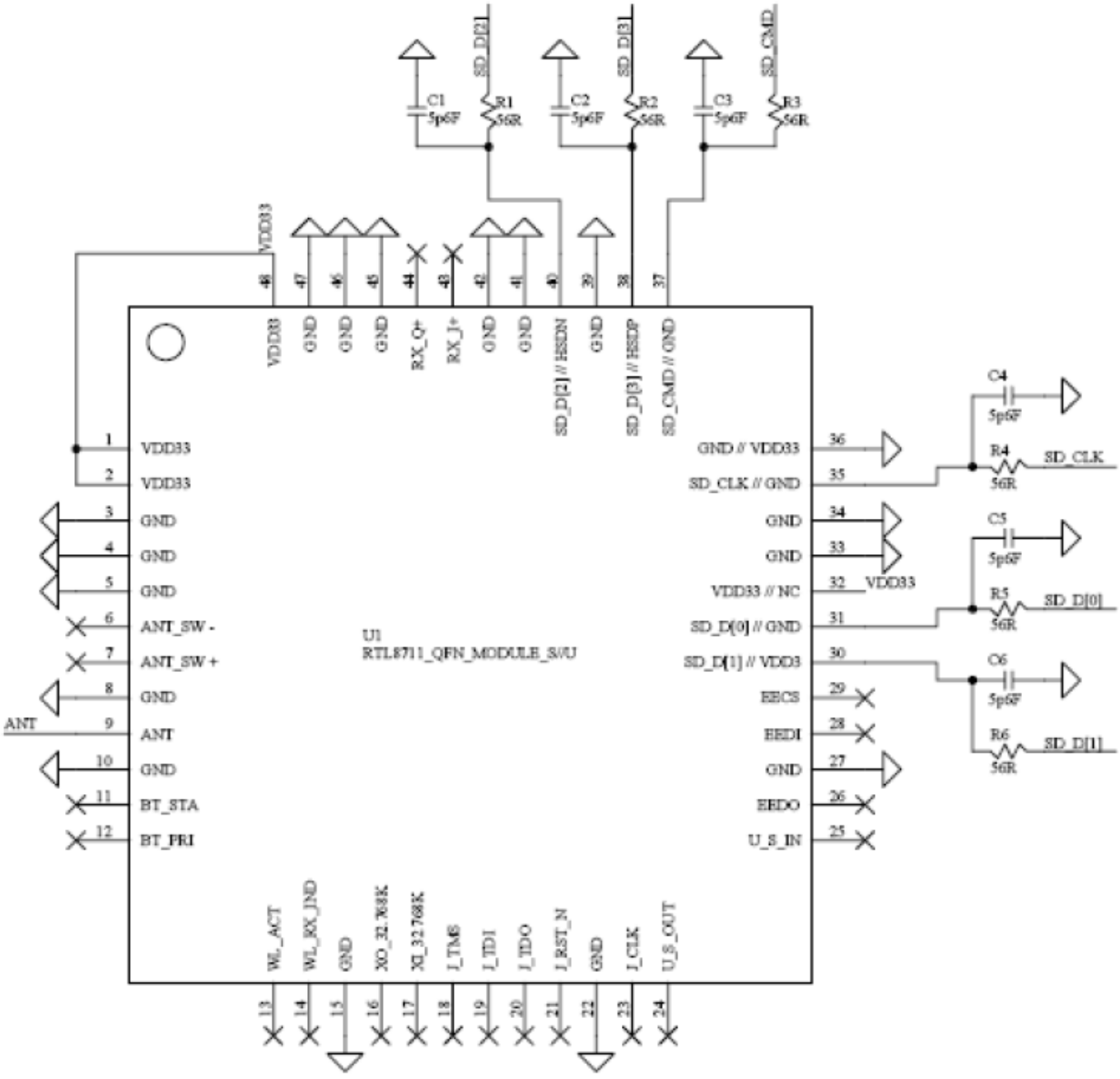

Figure 4: Application Schematic SDIO

APPLICATIONS SCHEMATIC

UGWAS82BSM33 (APOLLO-USB-SMT)

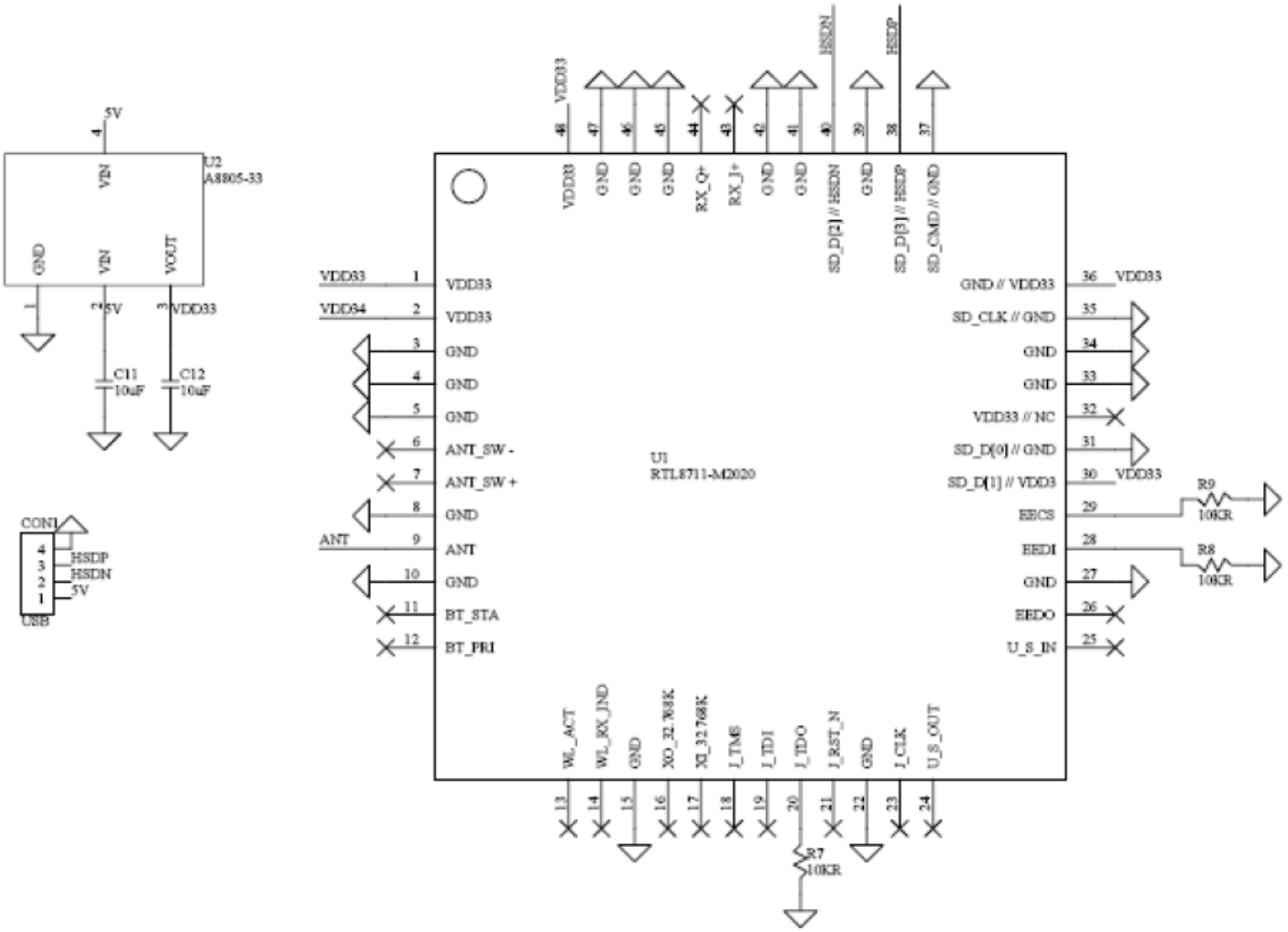

Figure 5: Application Schematic USB

AGENCY CERTIFICATIONS (PRE-SCAN)

TBD

REGULATORY COMPLIANCE STATEMENT

TBD

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MECHANICAL CHARACTERISTICS

Table 10: Mechanical Characteristics

Item	Description	Specification
1	PCB Material	FR-4
2	PCB Layers	TBD
3	Connector Type	Surface Mount
4	PCB Number	TBD
5	Flammability Rating	TBD
6	UGWAS82 Dimensions	22mm x 22mm x 1mm
8	Antenna Cable Connector	SMT

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MECHANICAL DRAWINGS

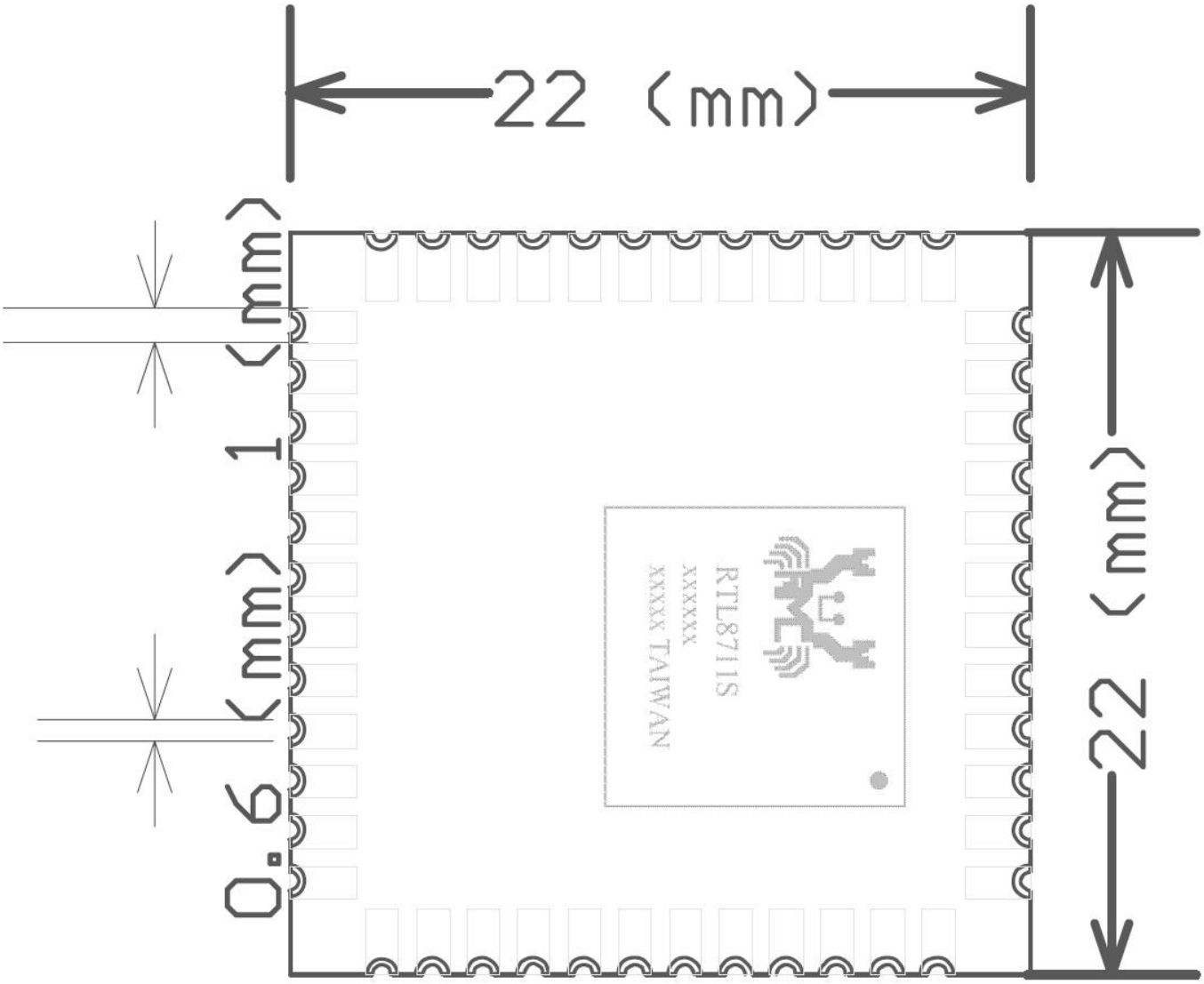

Figure 6: Mechanical Drawing 1

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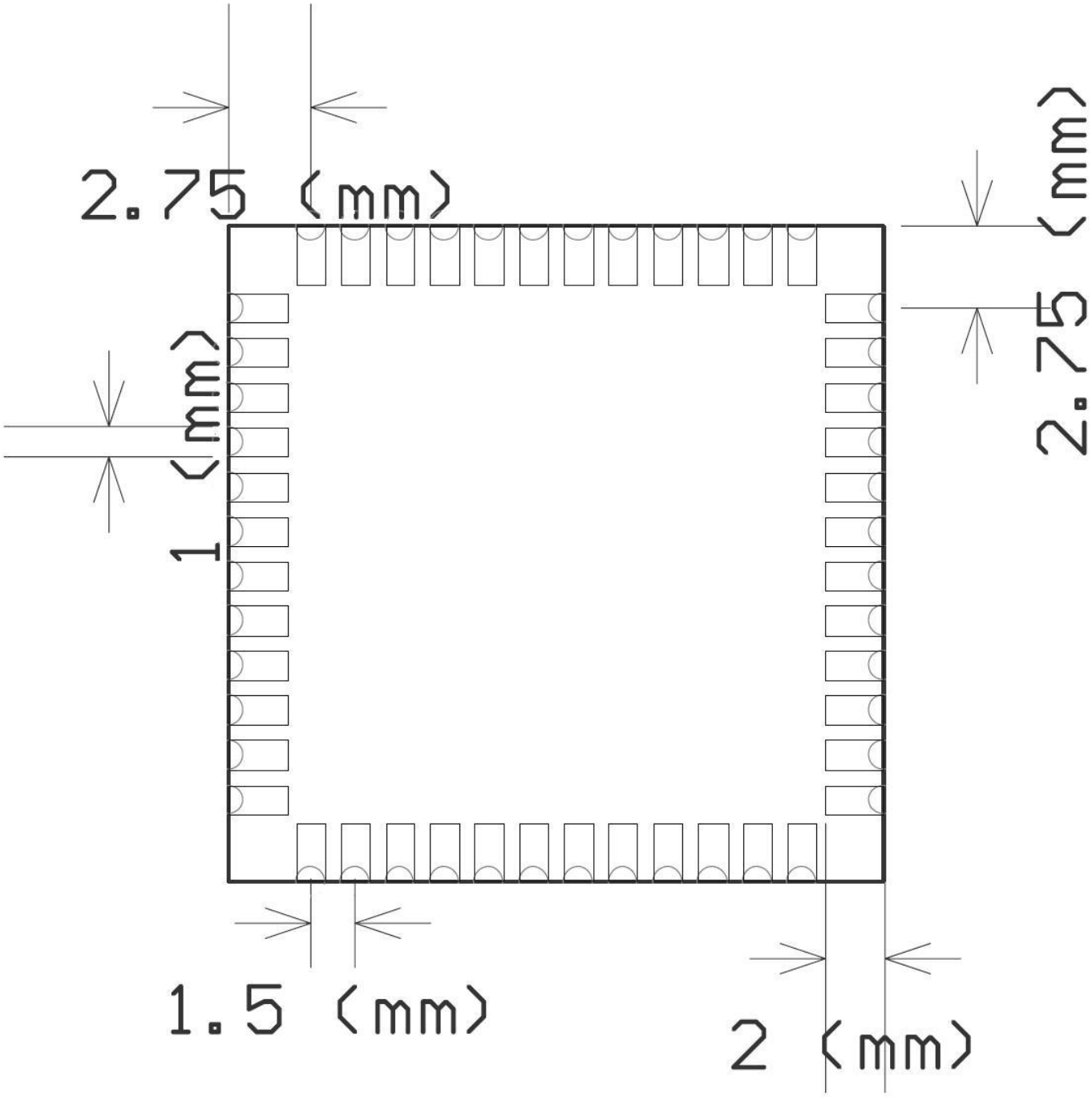

Figure 7: Mechanical Drawing 2

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RECOMMENDED PAD PLACEMENT DRAWING

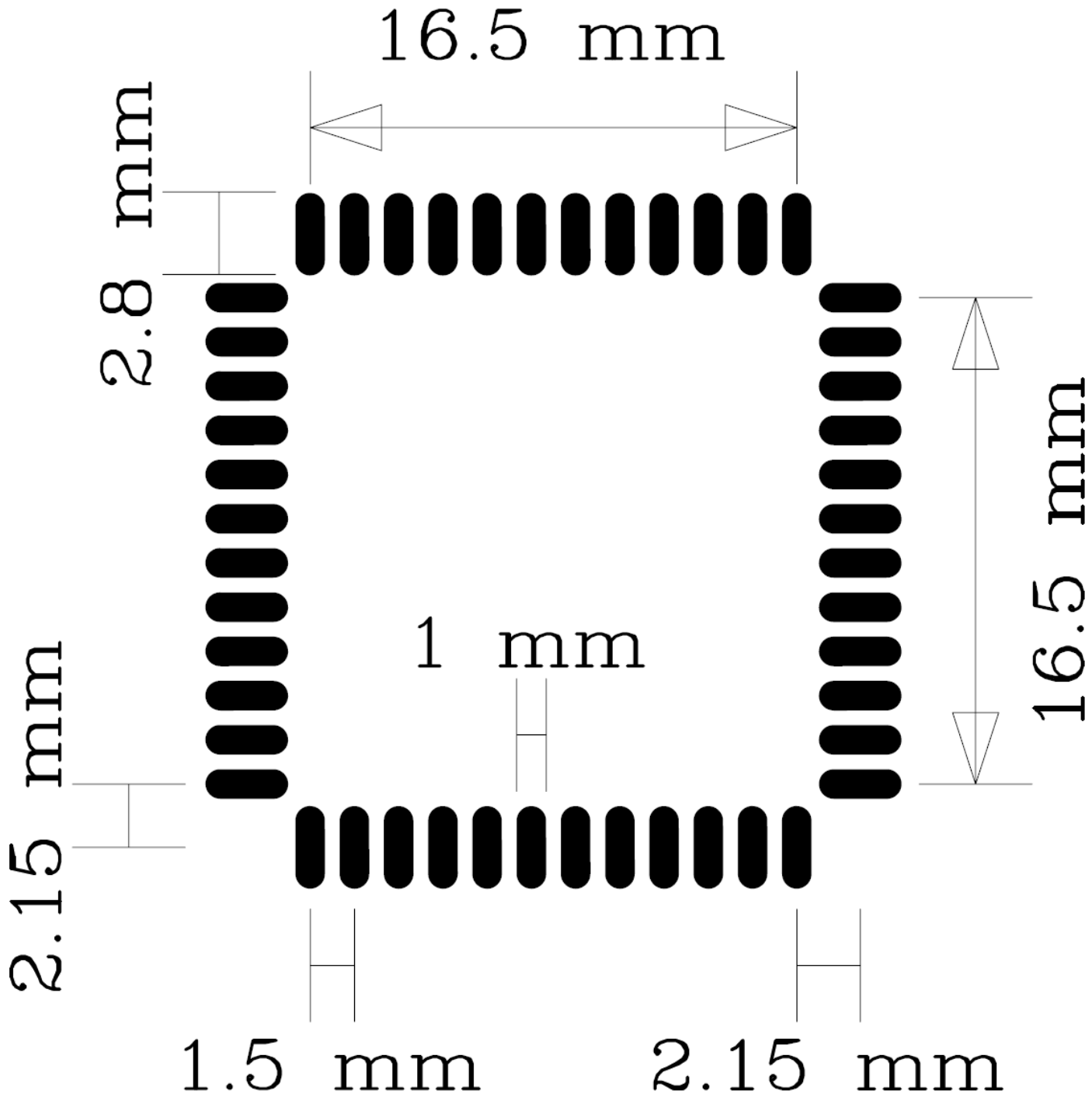

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Figure 8: Recommended Pad Placement Drawing

ORDERING INFORMATION

CONTACT INFORMATION

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REFERENCE DOCUMENTATION

Realtek RTL8711 Datasheet Rev 1.0 17 March 2008