DATASHEET

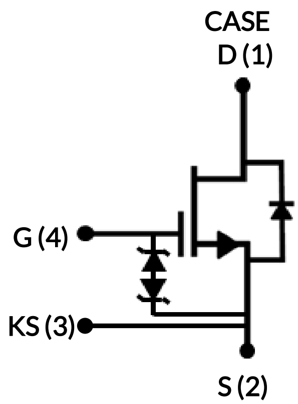
UF4SC120030K4S

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO-247-4L, 1200 V, 30 mohm

Rev. B, January 2025

Description

The UF4SC120030K4S is a 1200V, 30mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.



Part Number	Package	Marking
UF4SC120030K4S	TO-247-4L	UF4SC120030K4S

RoHS COMPLIANT · Pb LEAD FREE · HF HALOGEN FREE

Features

- On-resistance $R_{DS(on)}$: 30mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 277nC
- Low body diode V_{FSD}: 1.22V
- Low gate charge: Q_G = 37.8nC
- Threshold voltage $V_{G(th)}$: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3
- TO-247-4L package for faster switching, clean gate waveforms

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [1]	I_D	$T_C \leq 40°C$	53	A
		$T_C = 100°C$	41	A
Pulsed drain current [2]	I_{DM}	$T_C = 25°C$	164	A
Single pulsed avalanche energy [3]	E_{AS}	L=15mH, I_{AS} =3.6A	97	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 800V$	200	V/ns
Power dissipation	P_{tot}	$T_C = 25°C$	341	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8” from case for 5 seconds	T_L		250	°C

1. Limited by bondwires
2. Pulse width t_p limited by $T_{J,max}$
3. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.34	0.44	°C/W

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=0V, I_D=1mA	1200			V
Total drain leakage current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V, T_J=25°C		1	50	μA
		V_{DS}=1200V, V_{GS}=0V, T_J=175°C		15		
Total gate leakage current	I_{GSS}	V_{DS}=0V, T_J=25°C, V_{GS}=-20V / +20V		6	20	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V, I_D=20A, T_J=25°C		30	39	mΩ
		V_{GS}=12V, I_D=20A, T_J=125°C		56		
		V_{GS}=12V, I_D=20A, T_J=175°C		77		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=10mA	4	4.8	6	V
Gate resistance	R_G	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C ≤ 40°C			53	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			164	A
Forward voltage	V_{FSD}	V_{GS}=0V, I_S=15A, T_J=25°C		1.22	1.35	V
		V_{GS}=0V, I_S=15A, T_J=175°C		1.68		
Reverse recovery charge	Q_{rr}	V_R=800V, I_S=30A, V_{GS}=0V, R_G=18Ω di/dt=1840A/μs, T_J=25°C		277		nC
Reverse recovery time	t_{rr}			14		ns
Reverse recovery charge	Q_{rr}	V_R=800V, I_S=30A, V_{GS}=0V, R_G=18Ω di/dt=1840A/μs, T_J=150°C		298		nC
Reverse recovery time	t_{rr}			12.8		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=800V, V_{GS}=0V f=100kHz		1450		pF
Output capacitance	C_{oss}			65		
Reverse transfer capacitance	C_{rss}			2		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 800V, V_{GS}=0V		82		pF
Effective output capacitance, time related	$C_{oss(tr)}$	V_{DS}=0V to 800V, V_{GS}=0V		150		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=800V, V_{GS}=0V		26		μJ
Total gate charge	Q_G	V_{DS}=800V, I_D=30A, V_{GS} = 0V to 15V		37.8		nC
Gate-drain charge	Q_{GD}			8		
Gate-source charge	Q_{GS}			11.8		
Turn-on delay time	$t_{d(on)}$	Note 4 and 5, V_{DS}=800V, I_D=30A, Gate Driver =0V to +15V, R_{G_ON}=1Ω, R_{G_OFF}=18Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_G =18Ω, Snubber: R_s=10Ω, C_s=47pF T_J=25°C		12		ns
Rise time	t_r			19		
Turn-off delay time	$t_{d(off)}$			77		
Fall time	t_f			11		
Turn-on energy including R_S energy	E_{ON}			423		μJ
Turn-off energy including R_S energy	E_{OFF}			73		
Total switching energy	E_{TOTAL}			496		
Snubber R_S energy during turn-on	E_{RS_ON}			1.7		
Snubber R_S energy during turn-off	E_{RS_OFF}			1.5		
Turn-on delay time	$t_{d(on)}$	Note 4 and 5, V_{DS}=800V, I_D=30A, Gate Driver =0V to +15V, R_{G_ON}=1Ω, R_{G_OFF}=18Ω, inductive Load, FWD: same device with V_{GS} = 0V and R_G =18Ω, Snubber: R_s=10Ω, C_s=47pF T_J=150°C		13		ns
Rise time	t_r			20		
Turn-off delay time	$t_{d(off)}$			85		
Fall time	t_f			12		
Turn-on energy including R_S energy	E_{ON}			500		μJ
Turn-off energy including R_S energy	E_{OFF}			97		
Total switching energy	E_{TOTAL}			597		
Snubber R_S energy during turn-on	E_{RS_ON}			1.6		
Snubber R_S energy during turn-off	E_{RS_OFF}			1.4		

4. Measured with the switching test circuit in Figure 26.
5. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance Diagrams

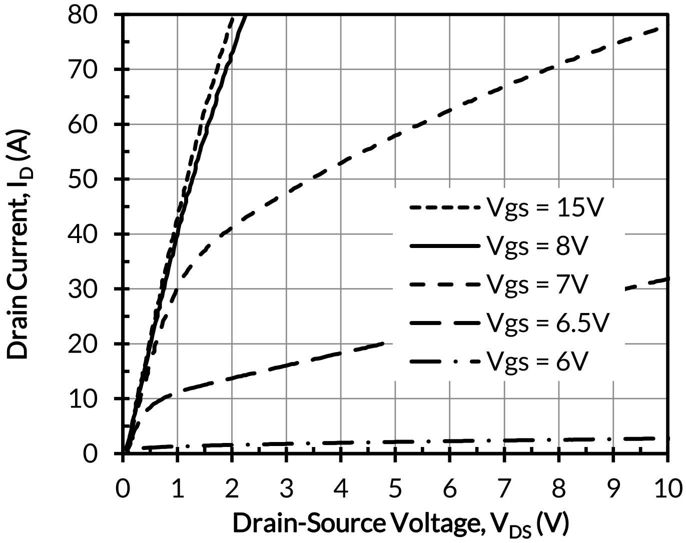


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250μs

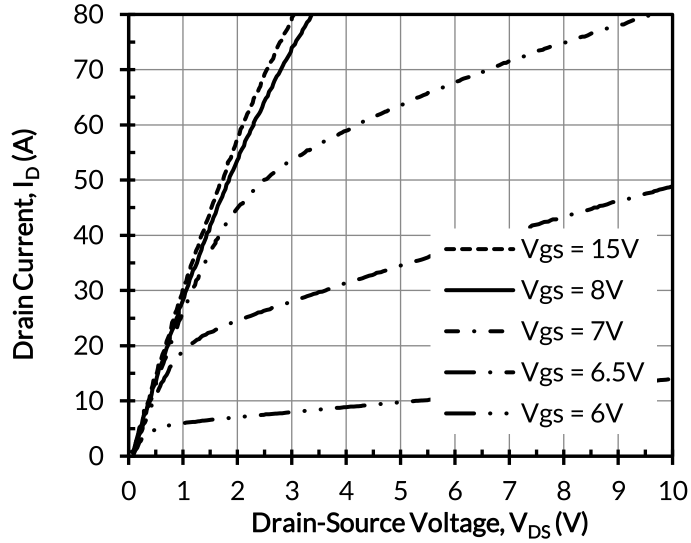


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250μs

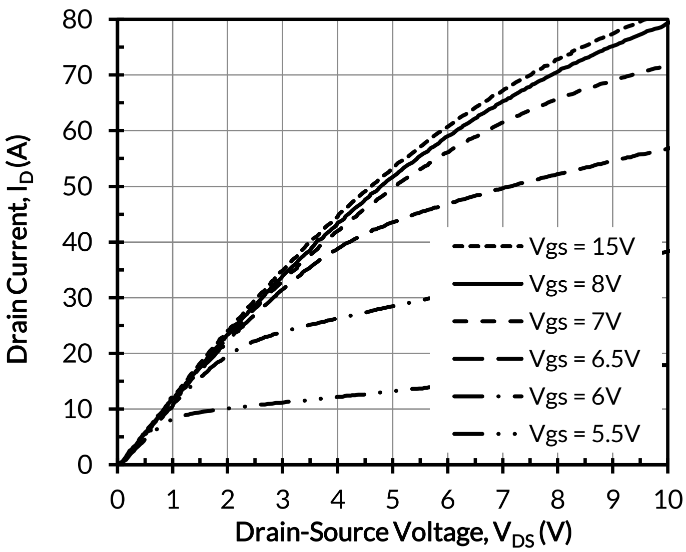


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250μs

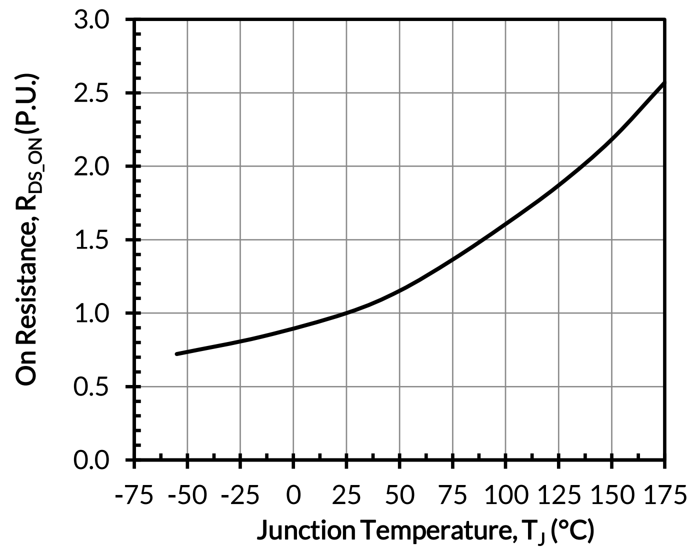


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V at I_D = 30A

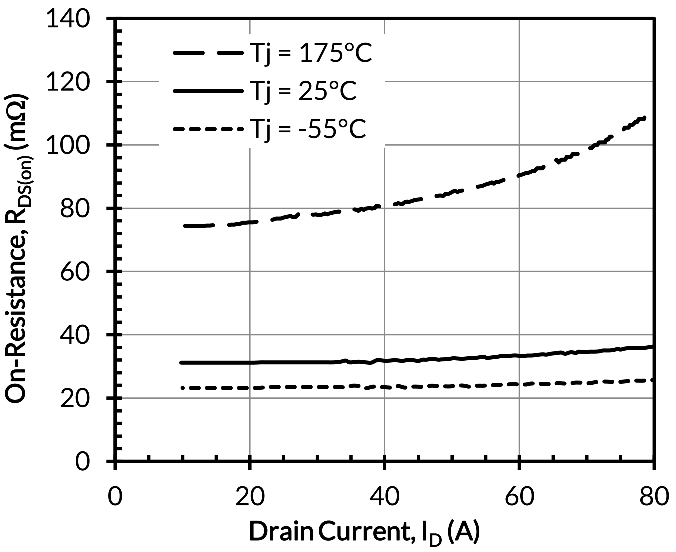


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

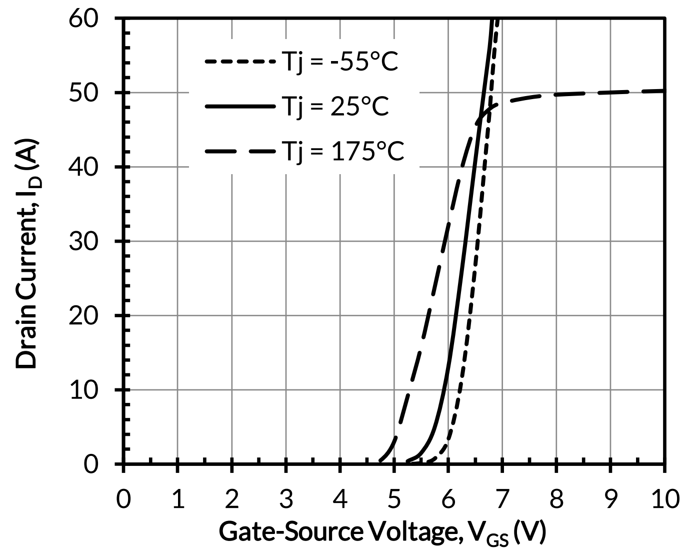


Figure 6. Typical transfer characteristics at V_{DS} = 5V

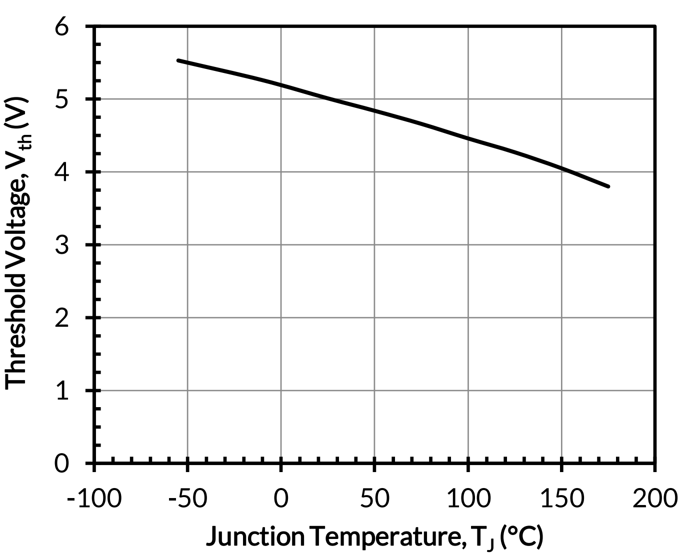


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

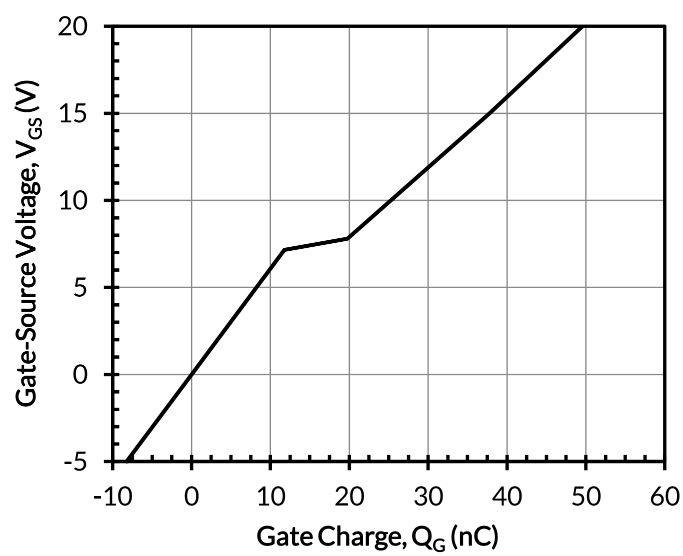


Figure 8. Typical gate charge at V_{DS} = 5V and I_D = 30A

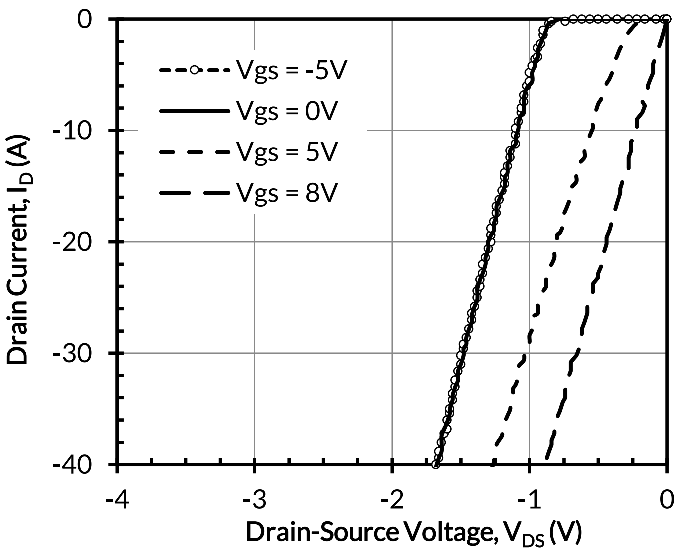


Figure 9. 3rd quadrant characteristics at T_J = -55°C

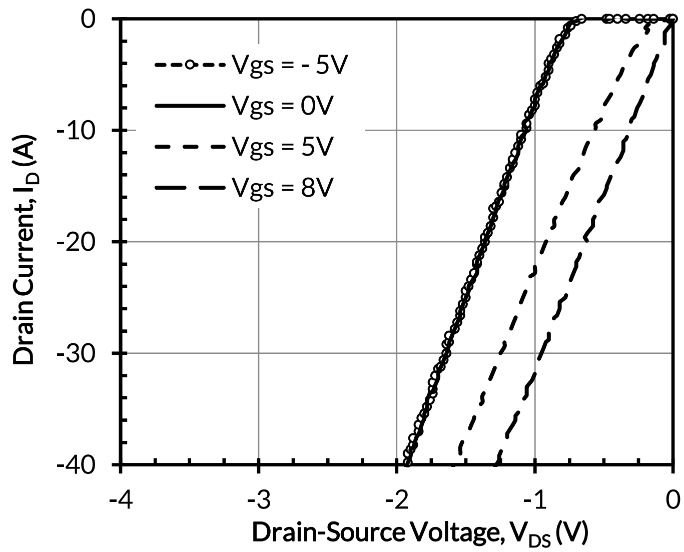


Figure 10. 3rd quadrant characteristics at T_J = 25°C

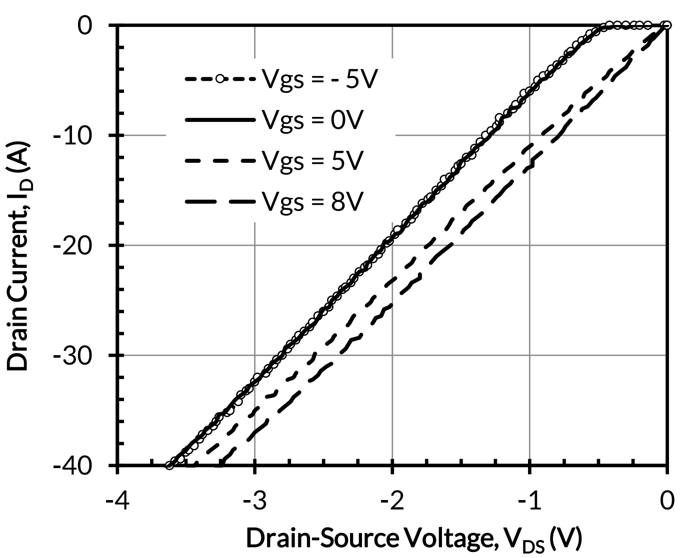


Figure 11. 3rd quadrant characteristics at T_J = 175°C

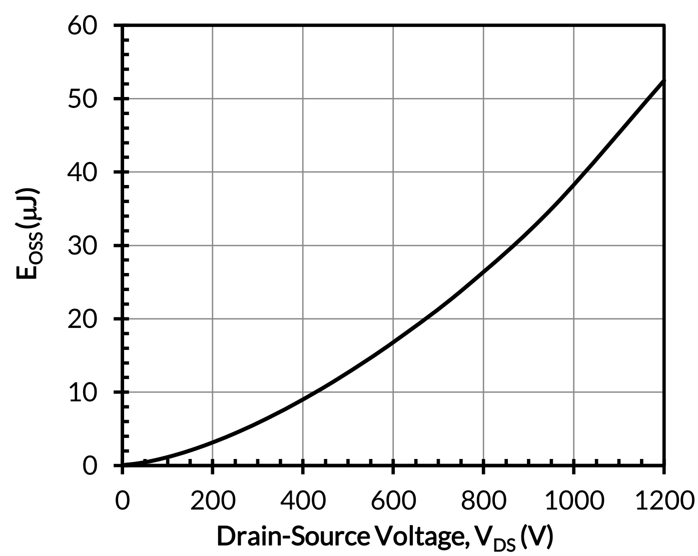


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

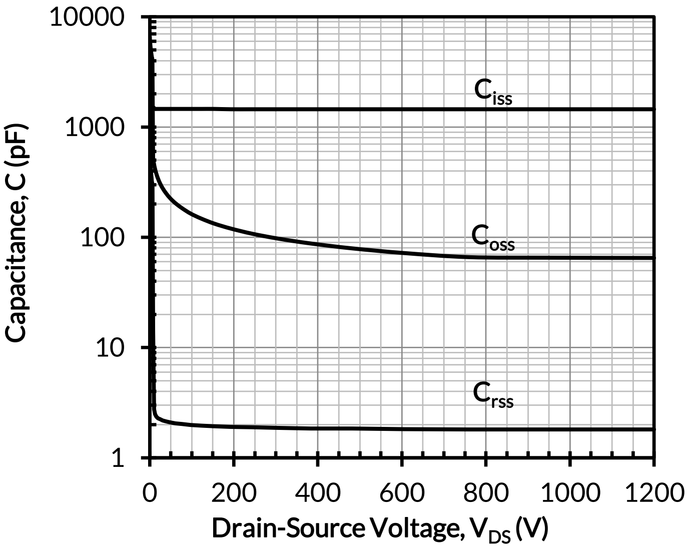


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

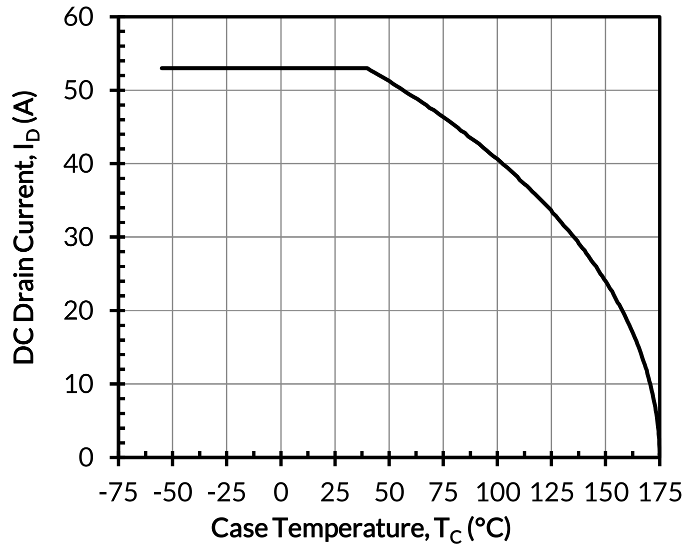


Figure 14. DC drain current derating

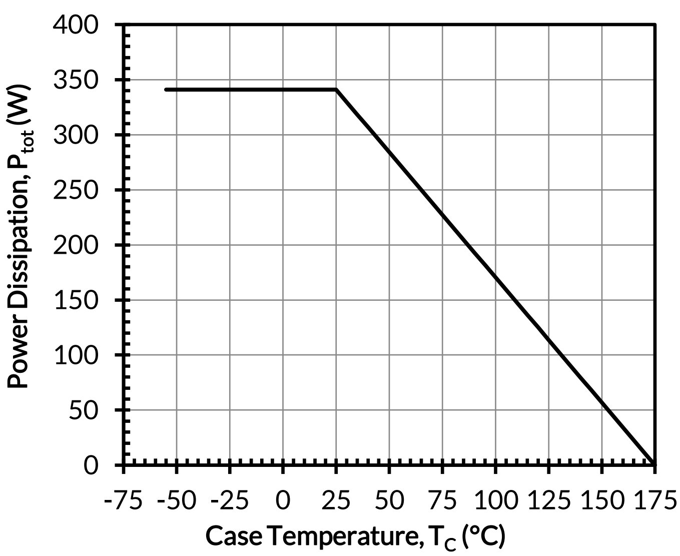


Figure 15. Total power dissipation

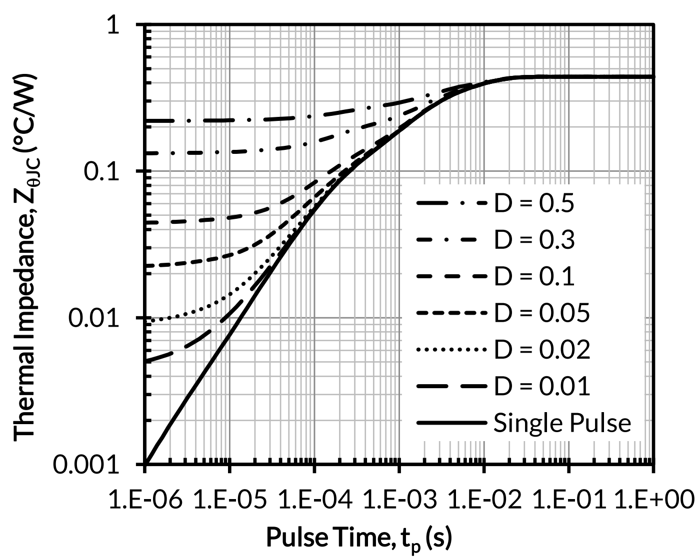


Figure 16. Maximum transient thermal impedance

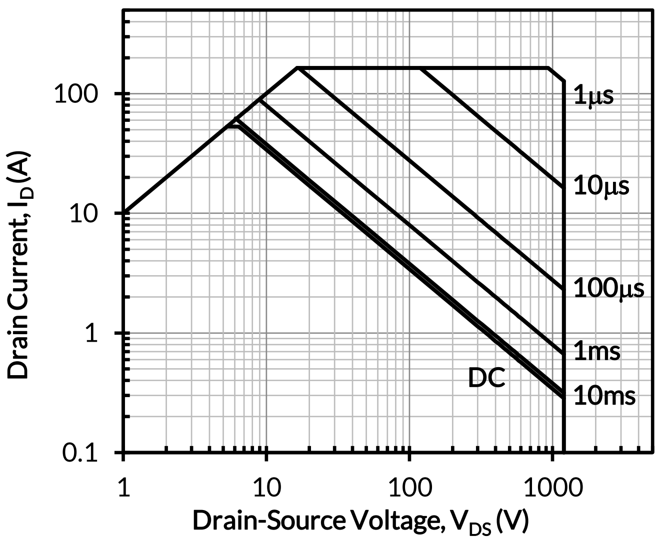


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

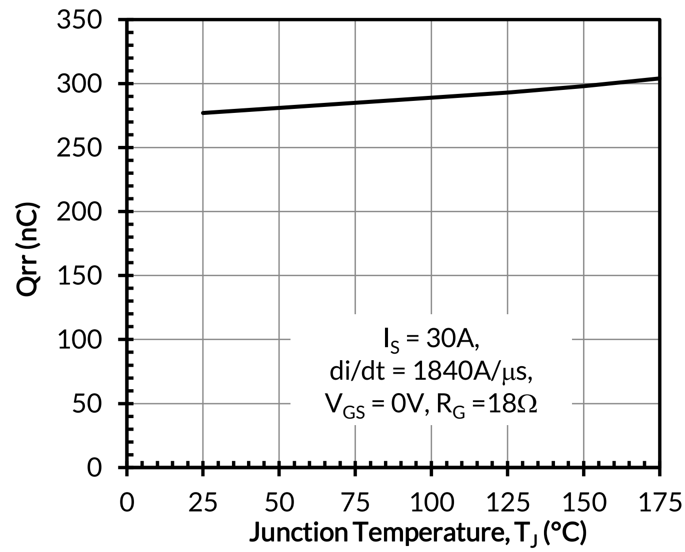


Figure 18. Reverse recovery charge Qrr vs. junction temperature at V_{DS} = 800V

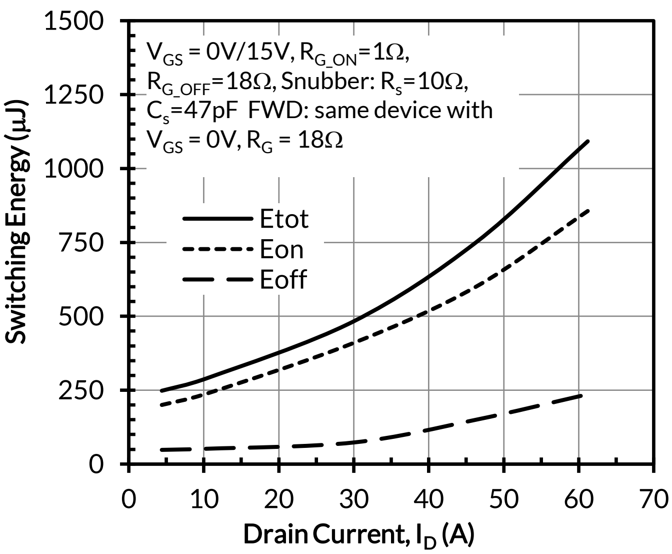


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} = 800V and T_J = 25°C

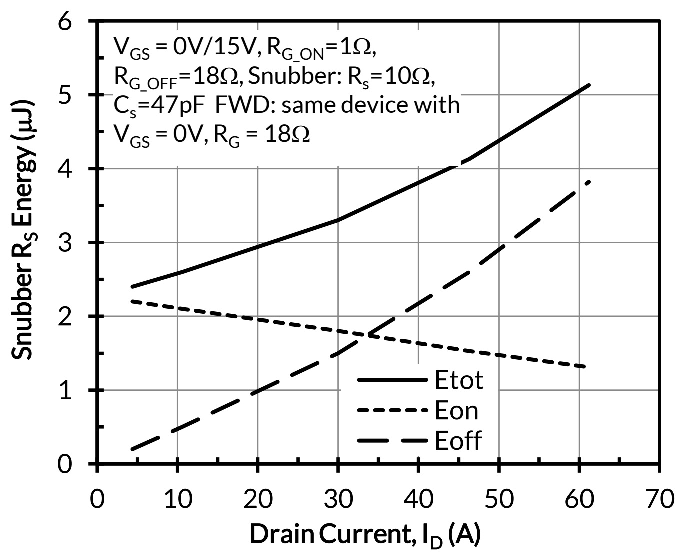


Figure 20. RC snubber energy losses vs. drain current at V_{DS} = 800V, I_D = 30A, and T_J = 25°C

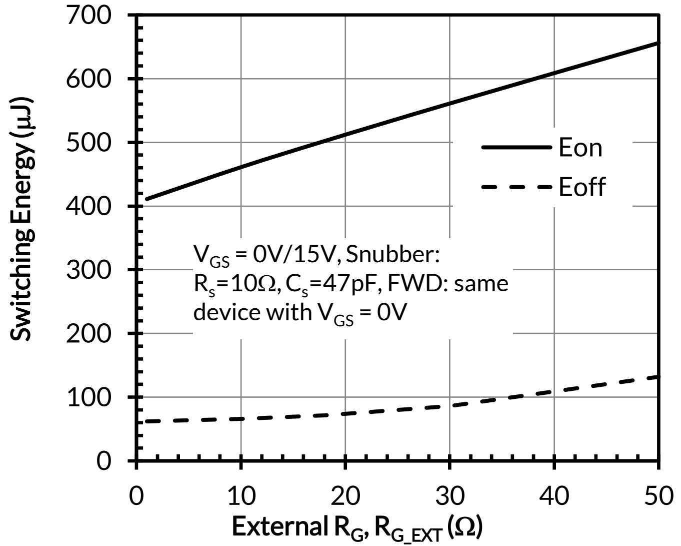


Figure 21. Clamped inductive switching energies vs. $R_{G,EXT}$ at V_{DS} = 800V, I_D =30A, and T_J = 25°C

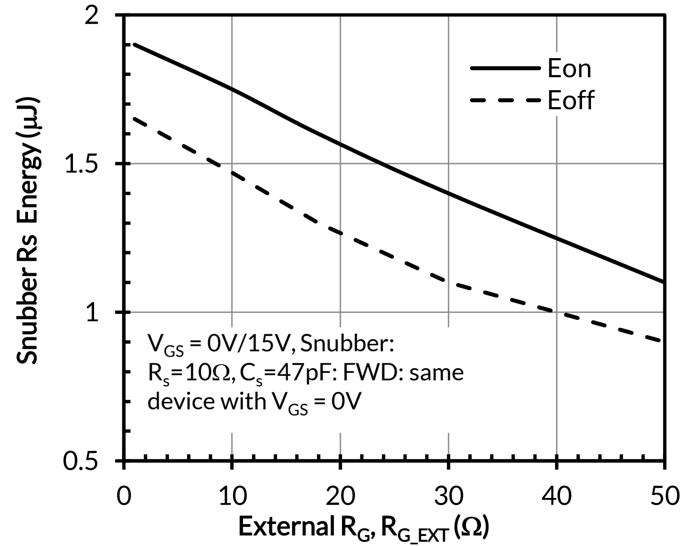


Figure 22. RC snubber energy losses vs. $R_{G,EXT}$ at V_{DS} = 800V, I_D = 30A, and T_J = 25°C

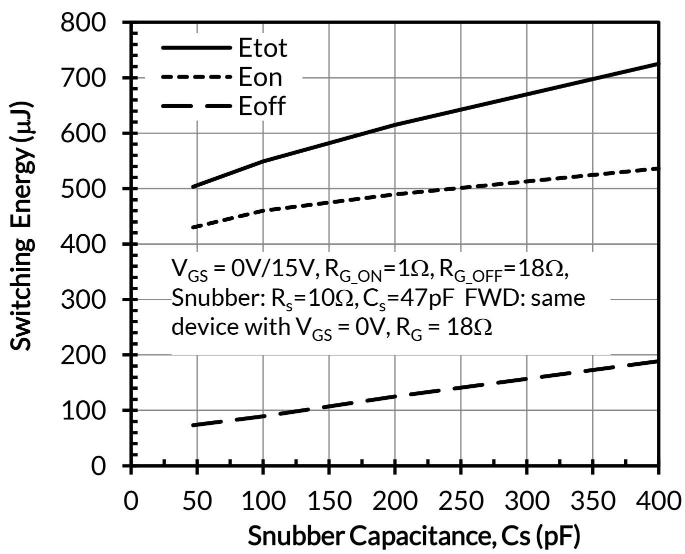


Figure 23. Clamped inductive switching energies vs. snubber capacitance C_S at V_{DS} = 800V, I_D = 30A, and

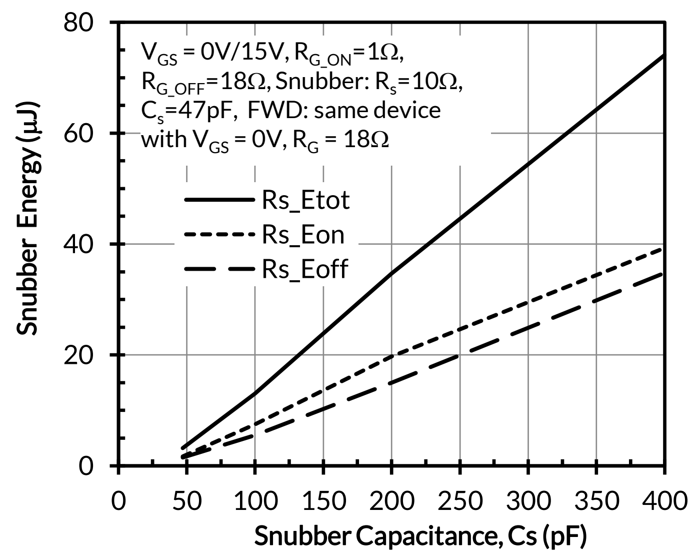


Figure 24. RC snubber energy losses vs. snubber capacitance C_S at V_{DS} = 800V, I_D =30A, and T_J = 25°C

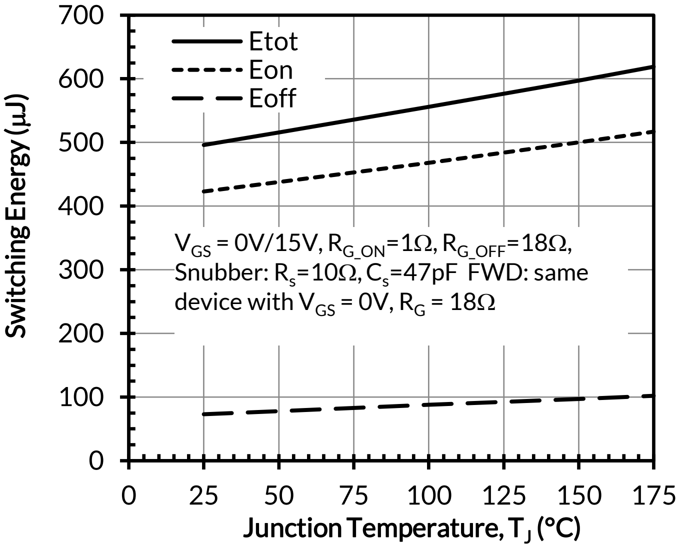


Figure 25. Clamped inductive switching energy vs. junction temperature at V_{DS} =800V and I_D =30A

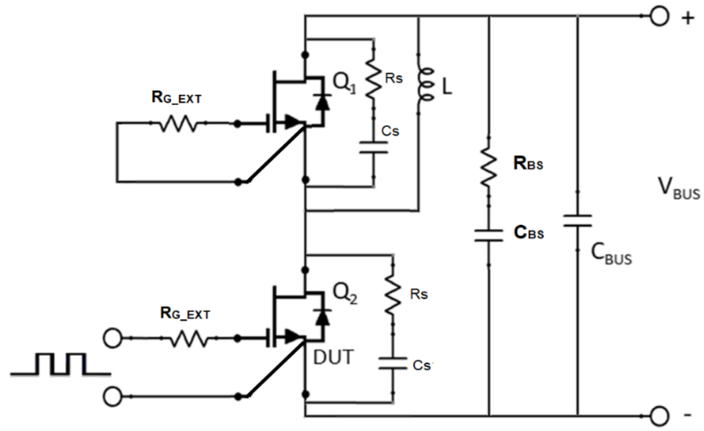


Figure 26. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_{BS} = 2.5Ω, C_{BS}=100nF) is used to reduce the power loop high frequency oscillations.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

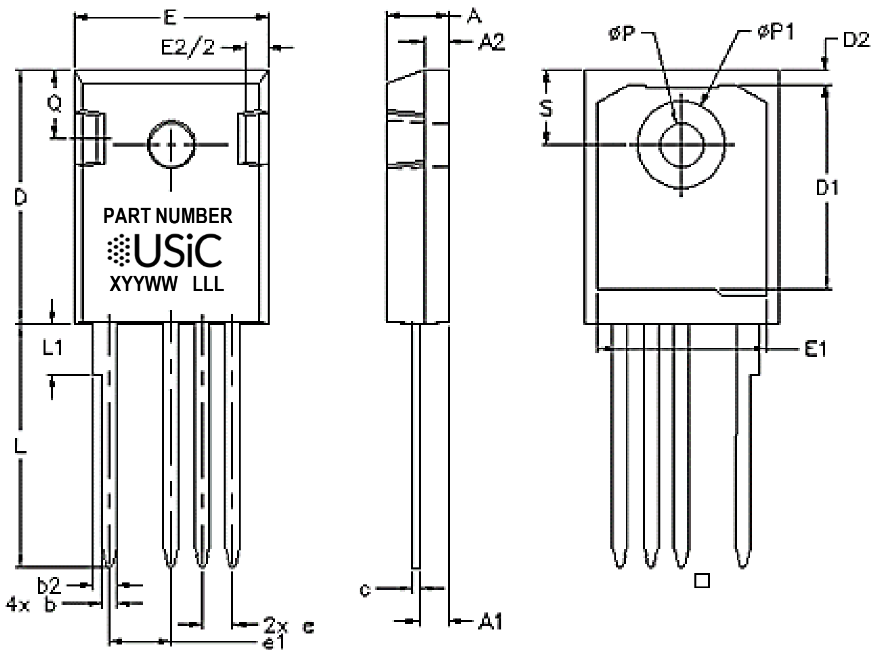
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

Important notice

TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

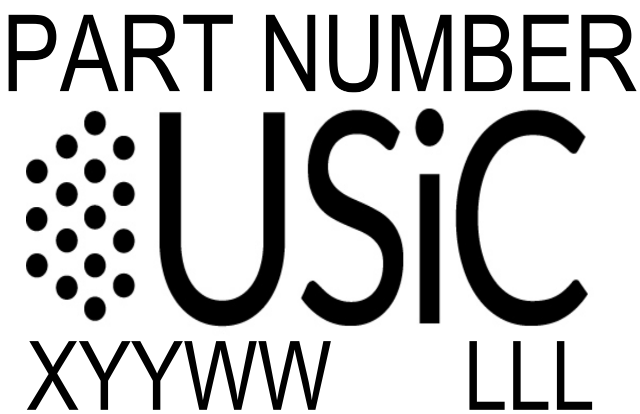
PACKAGE OUTLINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.209	4.7	5.31
A1	0.087	0.102	2.21	2.59
A2	0.059	0.098	1.5	2.49
b	0.039	0.055	0.99	1.4
b2	0.065	0.094	1.65	2.39
c	0.015	0.035	0.38	0.89
D	0.819	0.845	20.8	21.46
D1	0.515	-	13.08	-
D2	0.02	0.053	0.51	1.35
E	0.61	0.64	15.49	16.26
e	0.100 BSC		2.54 BSC	
e1	0.19	0.21	4.83	5.33
E1	0.53	-	13.46	-
E2	0.14	0.16	3.56	4.06
L	0.78	0.8	19.81	20.32
L1	-	0.177	-	4.5
ΦP	0.14	0.144	3.56	3.66
ΦP1	0.278	0.291	7.06	7.39
Q	0.212	0.244	5.38	6.2
S	0.243 BSC		6.17 BSC	

TO-247-4L PACKAGE OUTLINE, PART MARKING AND TUBE SPECIFICATIONS

PART MARKING



PART NUMBER = REFER TO DS_PN DECODER FOR DETAILS

X = ASSEMBLY SITE
YY = YEAR
WW = WORK WEEK
LLL = LOT ID

PACKING TYPE

ANTI-STATIC TUBE

QUANTITY /TUBE : 30 UNITS

DISCLAIMER

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales