DATASHEET

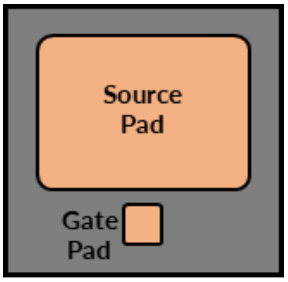
UF3N065300Z

650V-265mΩ SiC Normally-on JFET

Rev. B, January 2020

Description

UnitedSiC offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at V_{GS} = 0 V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.



Features

- Typical on-resistance $R_{DS(on),typ}$ of 265mΩ
- Voltage controlled
- Maximum operating temperature of 175°C
- Extremely fast switching not dependent on temperature
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical applications

- Over Current Protection Circuits
- DC-AC Inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Part Number	Package
UF3N065300Z	Die on tape
UF3N065300	Undiced wafer

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC [1]	-20 to +20	V
Continuous drain current [2,3]	I_D	T_C = 25°C	10	A
		T_C = 100°C	7.8	A
Pulsed drain current [3,4]	I_{DM}	T_C = 25°C	18	A
Maximum junction temperature [5]	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C

1. +20V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by $T_{J,max}$
3. Assumes a maximum junction-to-case thermal resistance of 1.8°C/W
4. Pulse width t_p limited by $T_{J,max}$
5. Package limited

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=-20V, I_D=1mA	650			V
Total drain leakage current	I_{DSS}	V_{DS}=650V, V_{GS}=-20V, T_J=25°C		0.8	5	µA
		V_{DS}=650V, V_{GS}=-20V, T_J=175°C		4		
Total gate leakage current	I_{GSS}	V_{GS}=-20V, T_J=25°C		0.1	1	µA
		V_{GS}=-20V, T_J=175°C		0.5		µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=2V, I_D=2A, T_J=25°C		210		mΩ
		V_{GS}=0V, I_D=2A, T_J=25°C		265	340	
		V_{GS}=2V, I_D=2A, T_J=175°C		345		
		V_{GS}=0V, I_D=2A, T_J=175°C		420		
Gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, I_D=5.3mA	-11.3	-8.8	-6.7	V
Gate resistance	R_G	f=1MHz, open drain		5.7		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS}=100V, V_{GS}=-20V f=100kHz		187		pF
Output capacitance	C_{oss}			27		
Reverse transfer capacitance	C_{rss}			24		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=-20V		22		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=-20V		1.7		µJ
Total gate charge	Q_G	V_{DS}=400V, I_D=5A, V_{GS} = -18V to 0V		22		nC
Gate-drain charge	Q_{GD}			12		
Gate-source charge	Q_{GS}			5		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=5A, Gate Driver =-18V to 0V, R_G=1Ω, Inductive Load, FWD: UJ3D06504TS T_J=25°C		5		ns
Rise time	t_r			15		
Turn-off delay time	$t_{d(off)}$			7		
Fall time	t_f			7		
Turn-on energy	E_{ON}			23		µJ
Turn-off energy	E_{OFF}			5		
Total switching energy	E_{TOTAL}			28		
Turn-on delay time	$t_{d(on)}$	V_{DS}=400V, I_D=5A, Gate Driver =-18V to 0V, R_G=1Ω, Inductive Load, FWD: UJ3D06504TS T_J=150°C		5		ns
Rise time	t_r			13		
Turn-off delay time	$t_{d(off)}$			6		
Fall time	t_f			7		
Turn-on energy	E_{ON}			19		µJ
Turn-off energy	E_{OFF}			4		
Total switching energy	E_{TOTAL}			23		

Typical Performance Diagrams

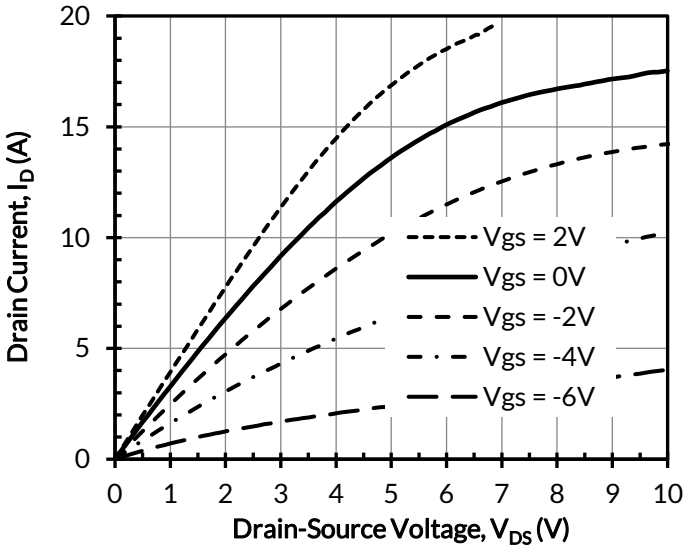


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

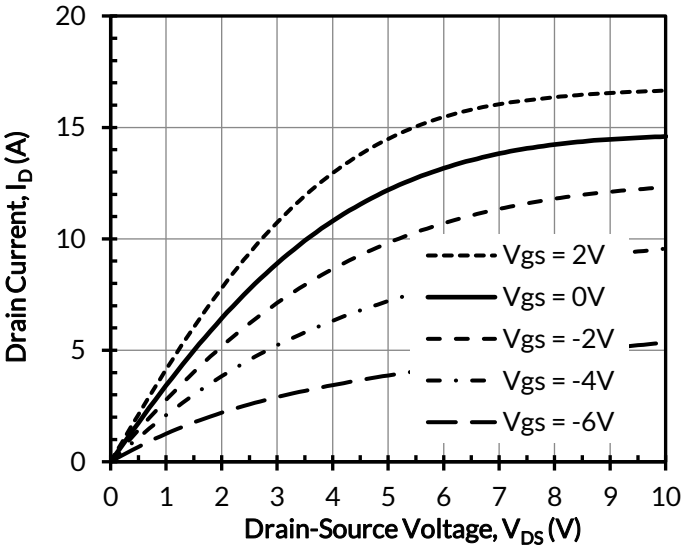


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

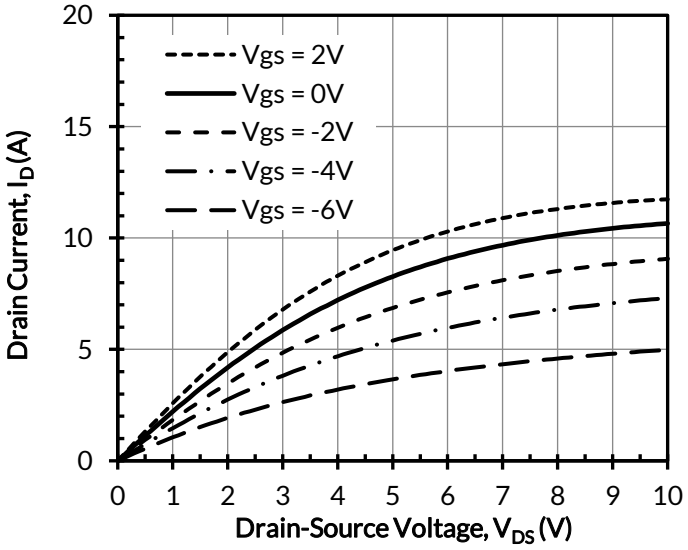


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250µs

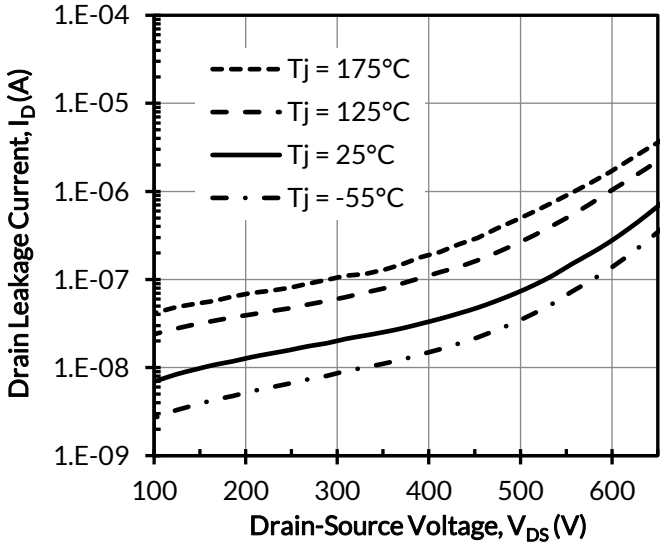


Figure 4. Typical drain-source leakage at V_{GS} = -20V

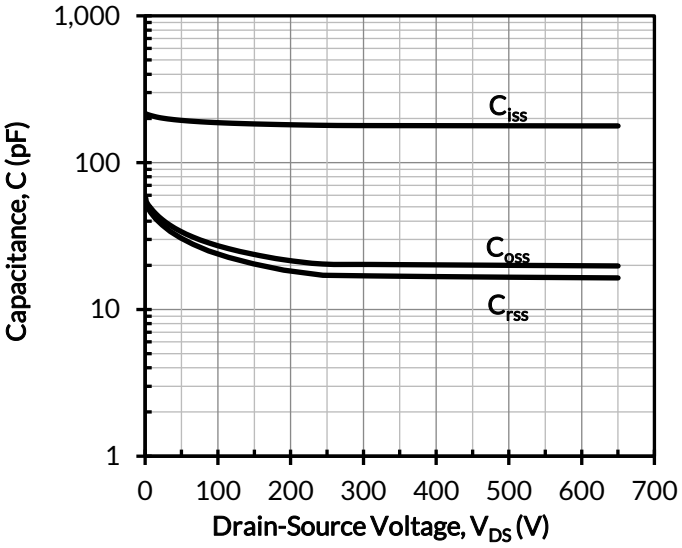


Figure 5. Typical capacitances at f = 100kHz and V_{GS} = -20V

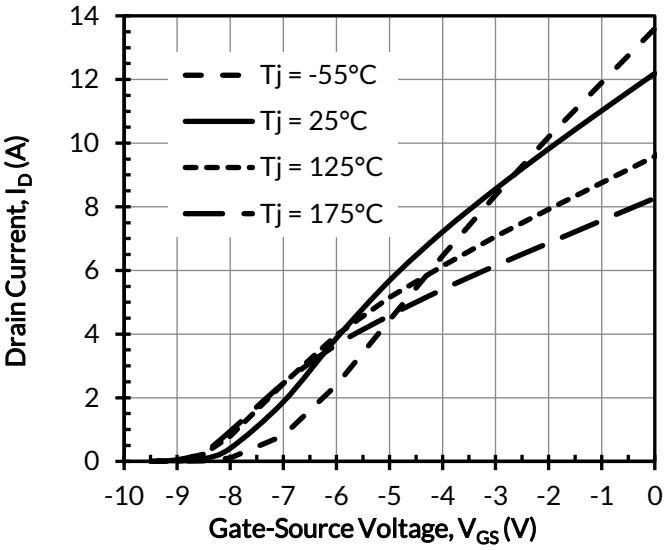


Figure 6. Typical transfer characteristics at V_{DS} = 5V

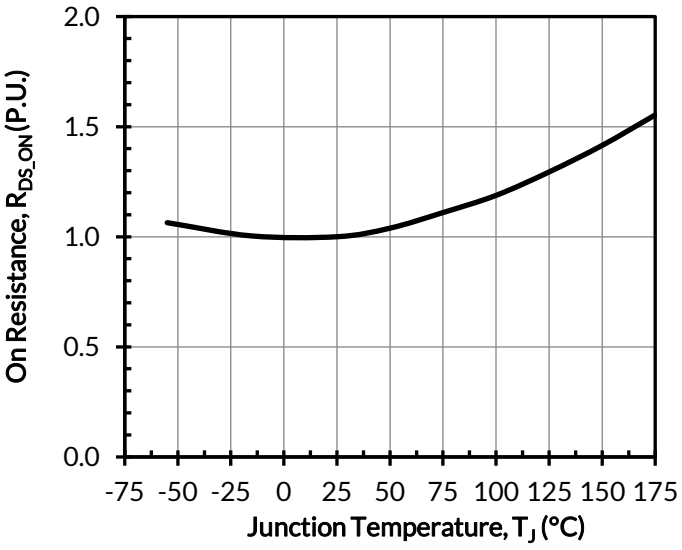


Figure 7. Normalized on-resistance vs. temperature at V_{GS} = 0V and I_D = 2A

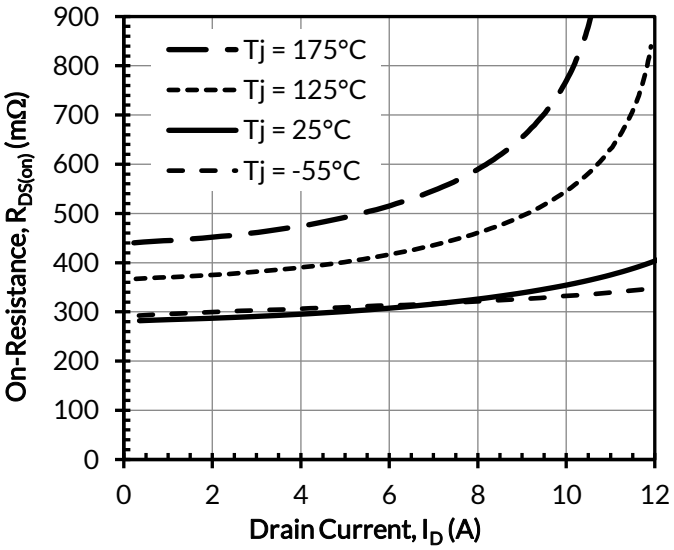


Figure 8. Typical drain-source on-resistances at V_{GS} = 0V

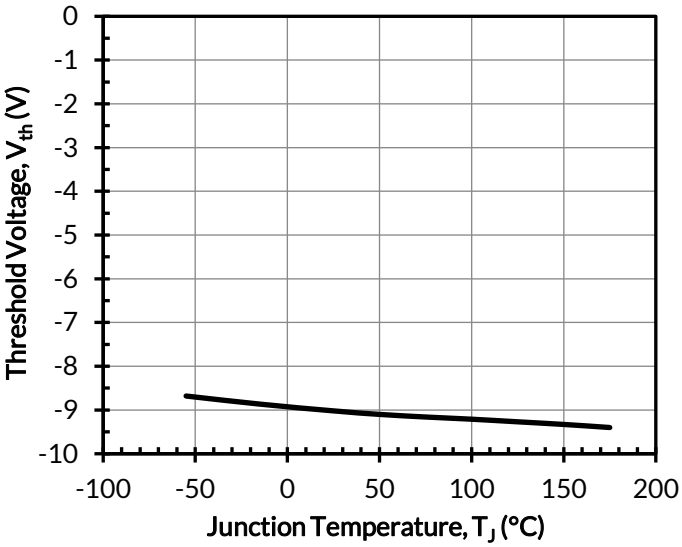


Figure 9. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 5.3mA

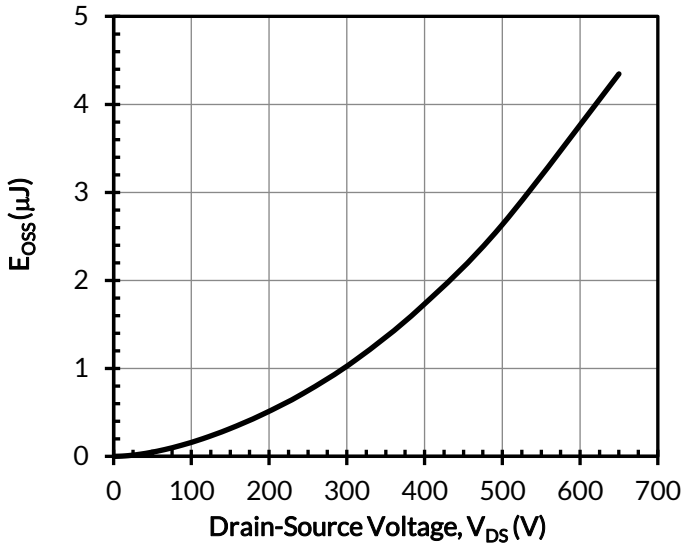


Figure 10. Typical stored energy in C_{OSS} at V_{GS} = -20V

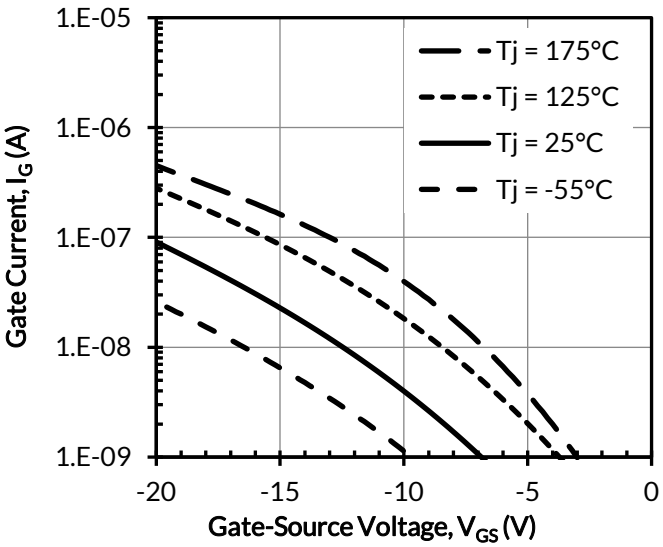


Figure 11. Typical gate leakage at V_{DS} = 0V

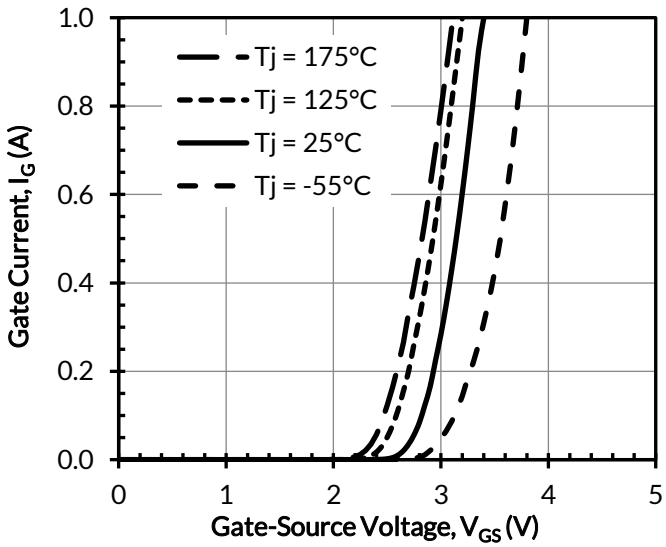


Figure 12. Typical gate forward current at V_{DS} = 0V

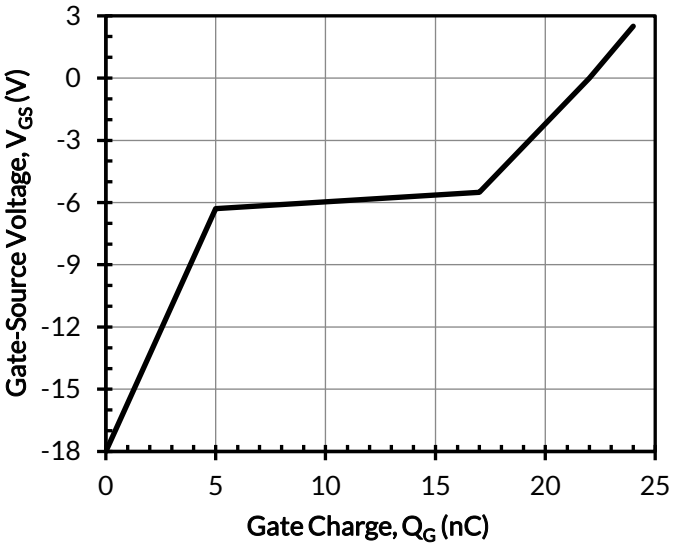


Figure 13. Typical gate charge at V_{DS} = 400V and I_D = 5A

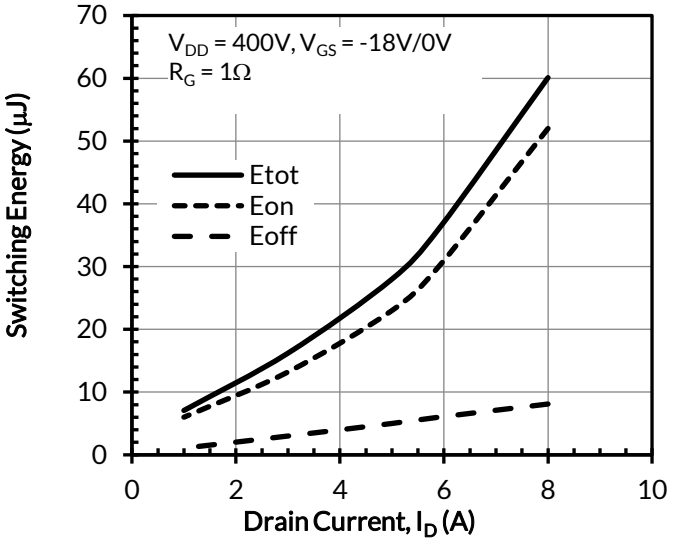


Figure 14. Clamped inductive switching energy vs. drain current at T_J = 25°C

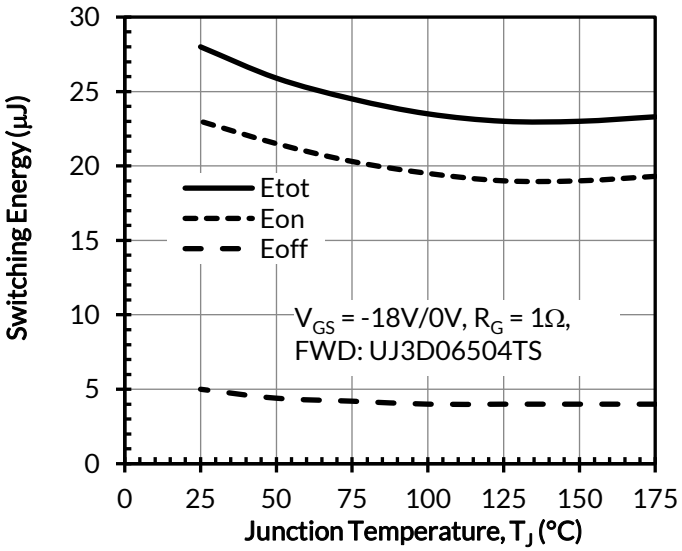


Figure 15. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 5A

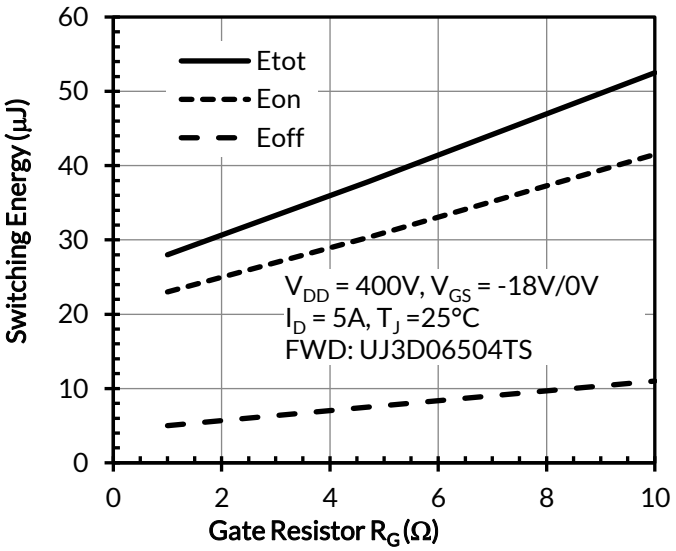
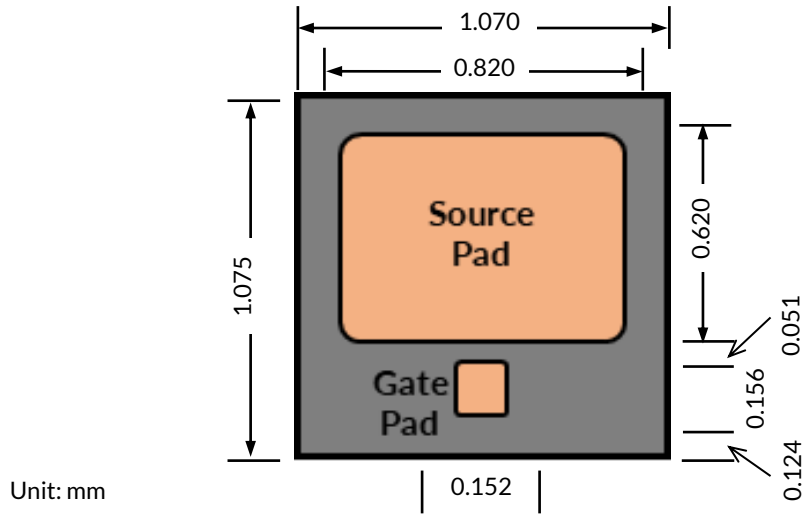


Figure 16. Clamped inductive switching energy vs. gate resistor R_G

Mechanical Characteristics

Parameter	Typical Value	Units
Die dimensions with scribe line (L x W)	1.070 x 1.075	mm
Scribe line width	80	µm
Source pad metal dimensions (L x W)	0.820 x 0.620	mm
Gate pad metal dimensions (L x W)	0.152 x 0.156	mm
Source metallization (AlCu)	5	µm
Gate metallization (AlCu)	5	µm
Backside drain metallization (Ti/Ni/Ag)	0.1/0.2/1	µm
Frontside passivation	Polyimide	
Die thickness	150	µm
Wafer size	150	mm
Gross die per wafer	12620	

Chip Dimensions



Unit: mm

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