UD052012 Advance

LINEAR INTEGRATED CIRCUIT

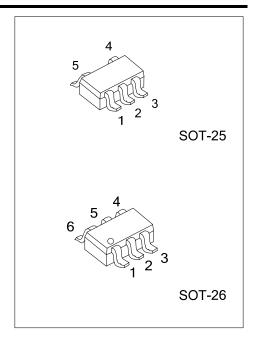
HIGH EFFICIENCY 1MHz 2A SYNCHRONOUS STEP DOWN CONVERTER

■ DESCRIPTION

The UTC **UD052012** is a high efficiency, high frequency synchronous DC-DC step-down converter. The 100% duty cycle feature provides low dropout operation, extending battery life in portable systems.

The internal synchronous switch increases efficiency and eliminates the need for external Schottky diode. At shutdown mode, the input supply current is less than $1\mu A$.

The UTC **UD052012** fault protection includes over current protection, short circuit protection, UVLO and thermal shutdown. The Internal soft-start function prevents inrush current at turn-on.

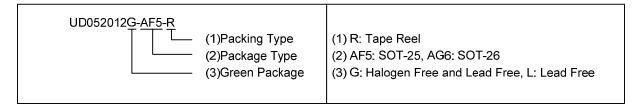


■ FEATURES

- * 2.5V~6V Input Voltage Range
- * 0.6V Reference Voltage
- * 2A Output Current
- * Low R_{DS(ON)} for Internal Switch: 140/90 mΩ (Top/Bottom)
- * 1MHz Switching Frequency
- * Internal Soft-Start Limits the Inrush Current
- * Internal Compensation Function
- * 100% Dropout Operation
- * Input Over Voltage Protection
- * Over Current Protection
- * Short Circuit Protection
- * Over Temperature Protection with Auto Recovery

■ ORDERING INFORMATION

Ordering	Daakana	Dooking	
Lead Free	Halogen Free	Package	Packing
UD052012L-AF5-R	UD052012L-AF5-R UD052012G-AF5-R		Tape Reel
UD052012L-AG6-R UD052012G-AG6-R		SOT-26	Tape Reel



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■ MARKING

PACKAGE	MARKING
SOT-25	Year and Month Code TV9WDZ Date Code Lot Code 1 2 3
SOT-26	Year and Month Code TV9WDZ Date Code Lot Code 1 2 3

■ MARKING INFORMATION

W: Year and Month Code

YEAR & MONTH	Jan-20	Feb-20	Mar-20	Apr-20	May-20	Jun-20	Jul-20	Aug-20	Sep-20	Oct-20	Nov-20	Dec-20
CODE	D	Е	F	G	Η	-	J	K	L	М	Ν	0
YEAR & MONTH	Jan-21	Feb-21	Mar-21	Apr-21	May-21	Jun-21	Jul-21	Aug-21	Sep-21	Oct-21	Nov-21	Dec-21
CODE	Р	а	R	S	Т	U	V	W	Х	Υ	Z	D
YEAR & MONTH	Jan-22	Feb-22	Mar-22	Apr-22	May-22	Jun-22	Jul-22	Aug-22	Sep-22	Oct-22	Nov-22	Dec-22
CODE	е	f	g	h	j	k	m	n	q	r	t	Υ
YEAR & MONTH	Jan-23	Feb-23	Mar-23	Apr-23	May-23	Jun-23	Jul-23	Aug-23	Sep-23	Oct-23	Nov-23	Dec-23
CODE	1	2	3	4	5	6	7	8	9	Α	В	С

D: date Code

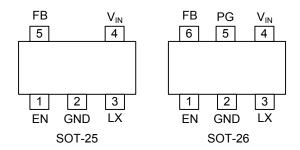
DATE	1	2	3	4	5	6	7	8	9	10	11	12
CODE	1	2	3	4	5	6	7	8	9	Α	В	С
DATE	13	14	15	16	17	18	19	20	21	22	23	24
CODE	D	Е	F	G	Н	I	J	K	L	М	N	Р
DATE	25	26	27	28	29	30	31					
CODE	Q	R	S	Т	U	V	W					

Z: Series Number (Note 1)

1	•	2		3	••	4	- •
5	- • - •	6	- • •-	7	- • • •	8	•
9	● ●	Α	• - • -	В	• - • •	С	••
D	•• - •	E	•••-	F	• • • •	G	

Note: 1. Series No., the last digit of assembly lot No. (Follow binary system)

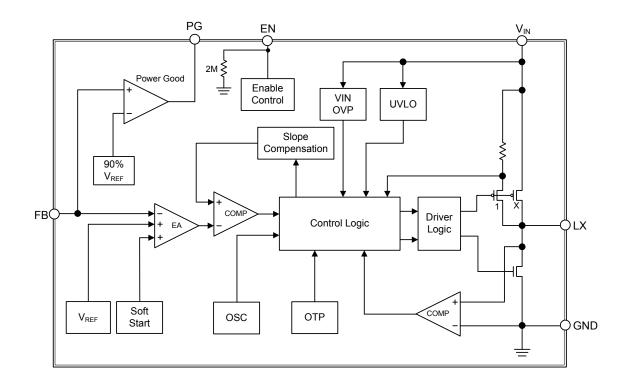
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN	NO.	PIN NAME	DESCRIPTION
SOT-25	SOT-26	PIN NAIVIE	DESCRIPTION
1	1	EN	Enable control pin. Pull high to turn the IC on, and pull low to disable the IC. Don't leave this pin floating.
2	2	GND	Ground pin.
3	3	LX	Power switching node. Connect an external inductor to this switching node.
4	4	V _{IN}	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
5	6	FB	Voltage feedback input pin. Connect FB and V _{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.6V.
-	5	PG	Open drain power good output pin

■ BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V _{IN} to GND		-0.3 ~ +6.5	V
LX to GND		-0.3 ~ V _{IN} +0.3	V
EN, FB, PG to GND		-0.3 ~ V _{IN}	V
Maximum Junction Temperature	TJ	+150	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

Advance

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{IN}	+2.5 ~ +6	V
Junction Temperature Range		-40 ~ +125	°C
Operation Temperature Range	T _{OPR}	-40 ~ +85	°C

Note: The device is not guaranteed to function outside its operating conditions.

■ THERMAL DATA

PARAMET	ER	SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	250	°C/W
lunation to Coop	SOT-25	0	130	°C/W
Junction to Case	SOT-26	$\theta_{ m JC}$	110	°C/W

■ ELECTRICAL CHARACTERISTICS V_{IN}=5V, T_A=25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Voltage	V _{IN}		2.5		6.0	V
Input Over Voltage Protection	V _{IN OVP}			6.5		V
Shutdown Current	I _{SHDN}	EN=GND		0.1	1	μΑ
Quiescent Current	Iq	V _{FB} =0.65V, I _{OUT} =0A		40		μΑ
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Leakage Current	I _{FB}	$V_{FB}=V_{IN}$		0.01	1	μΑ
On Bosistanos (Noto)	Ь	P-Channel MOSFET		140		mΩ
On-Resistance (Note)	R _{DS(ON)}	N-Channel MOSFET		90		mΩ
P-Channel Current Limit (Note)	I _{LIM}		2.2	2.7		Α
EN High-Level Input Voltage	V _{EN(H)}		1.5			V
EN Low-Level Input Voltage	$V_{\text{EN(L)}}$				0.4	V
Under Voltage Lockout Voltage	UVLO			2.4		V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillation Frequency	Fosc	I _{OUT} =300mA	8.0	1.0	1.2	MHz
Minimum On Time				50		ns
Maximum Duty Cycle			100			%
PG Rising Threshold	V _{PG (H)}	V _{FB} Rising		90		%
PG Low Threshold	V _{PG (L)}	V _{FB} falling		85		%
PG Sink Current	I_{PG}	V _{PG} =0.1V		1		mA
Internal Soft-Start Time	T _{SS}			1		ms
V _{OUT} Discharge Resistance				100		Ω
Thermal Shutdown Temperature (Note)				150		°C

Note: Guarantee by design.

■ FUNCTION DESCRIPTION

The **UD052012** is a high efficiency, internal compensation and constant frequency current mode step-down synchronous DC/DC regulator. It has integrated high-side ($140m\Omega$, typ) and low-side ($90m\Omega$, typ) power switches, and provides 2A continuous load current. It regulates input voltage from 2.5V to 6V, and down to an output voltage as low as 0.6V.

Control Loop

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load, line response, protection of the internal main switch and synchronous rectifier. The **UD052012** switches at a constant frequency (1MHz) and regulates the output voltage. During each cycle, the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until next cycle starts.

Enable

The **UD052012** EN pin provides digital control to turn on/off the regulator. When the voltage of EN exceeds the threshold voltage, the regulator will start the soft start function. If the EN pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μ A. For auto start-up operation, connect EN to VIN.

Soft Start

The **UD052012** employs internal soft start function to reduce input inrush current during start up. The internal soft start time will be 1ms.

Under Voltage Lockout

When the **UD052012** is power on, the internal circuits will be held inactive until V_{IN} voltage exceeds the UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the UVLO threshold voltage. The hysteretic of the UVLO comparator is 200mV (typ).

Short Circuit Protection

The **UD052012** provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 40% of the regulation level, the oscillator frequency will be reduced and hiccup mode will be triggered to prevent the **UD052012** from overheating during the extended short condition. Once the short condition is removed, the frequency and current limit will return to normal.

Over Current Protection

The **UD052012** over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

Over Temperature Protection

The **UD052012** incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 30°C (typ).

PG Signal Output

PG pin is an open-drain output and requires a pull up resistor. PG is actively held low in soft-start, standby and shutdown. It is released when the output voltage rises above 90% of nominal regulation point.

Input Over Voltage Protection

The **UD052012** supports input over voltage protection. When input voltage exceeds the input over Voltage threshold, the regulator will be shutdown unless the input over voltage is removed. The hysteretic of the input OVP comparator is 300mV (typ).



APPLICATION INFORMATION

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.6V. Thus the output voltage is:

$$V_{OUT} = 0.6V \times \left(1 + \frac{R1}{R2}\right)$$

Table 1 lists recommended values of R1 and R2 for most used output voltage.

Table 1. Recommended Resistance Values

V_{OUT}	R1	R2
3.3V	453kΩ	100kΩ
2.5V	316kΩ	100kΩ
1.8V	200kΩ	100kΩ
1.5V	150kΩ	100kΩ
1.2V	100kΩ	100kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$\begin{split} I_{CIN(RMS)} &= I_{OUT} \times \sqrt{D \times (1-D)} \\ D &= \frac{V_{OUT}}{V_{IN}} \end{split}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to I_{OUT}/2.

A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

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$$V_{\mathit{RIPPLE}}(t) = V_{\mathit{RIPPLE}(C)}(t) + V_{\mathit{RIPPLE}(ESR)}(t) + V_{\mathit{RIPPLE}(ESL)}(t) + V_{\mathsf{NOISE}}(t)$$

The following figures show the form of the ripple contributions.

$$V_{RIPPLE(ESR)} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{ESL}{L} \times V_{IN}$$

$$V_{RIPPLE(C)} = \frac{V_{OUT}}{8 \times {F_{OSC}}^2 \times L \times_{COUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

■ APPLICATION INFORMATION (Cont.)

Where FOSC is the switching frequency, L is the inductance value, VIN is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the COUT is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple.

Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_{L} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_{L} equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_{L} between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L = 0.3 \times I_{OUT(MAX)}$$

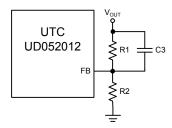
$$L = \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN} \times F_{OSC} \times \Delta I_{L}}$$

To guarantee sufficient output current, peak inductor current must be lower than the **UD052012** high-side MOSFET current limit.

$$I_{PEAK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C3 in the feedback network is recommended to improve transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C3 can be calculated with the following equation:

$$C3 = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 330pF.

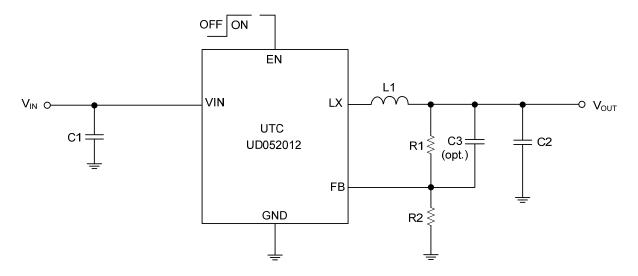
APPLICATION INFORMATION (Cont.)

PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

- 1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
- 2.Place feedback resistors close to the FB pin.
- 3. Keep the sensitive signal (FB) away from the switching signal (LX).
- 4. Multi-layer PCB design is recommended.

TYPICAL APPLICATION CIRCUIT



Note: V_{IN}=5V, the recommended BOM list is as below.

Table 2. Recommended Component Values

V _{OUT}	C1	R1	R2	L1	C2
3.3V	10μF MLCC	453kΩ	100kΩ	2.2µH	10μF MLCC
2.5V	10μF MLCC	316kΩ	100kΩ	2.2µH	10μF MLCC
1.8V	10μF MLCC	200kΩ	100kΩ	1.8µH	10µF MLCC
1.5V	10μF MLCC	150kΩ	100kΩ	1.5µH	10μF MLCC
1.2V	10μF MLCC	100kΩ	100kΩ	1.5µH	10μF MLCC
1.05V	10µF MLCC	75kΩ	100kΩ	1.2µH	10µF MLCC

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