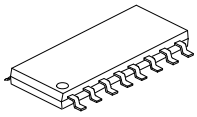
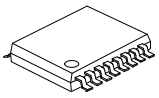
UCD4049B **Preliminary** ***CMOS IC***

CMOS HEX BUFFER/CONVERTERS



SOP-16



TSSOP-16

■ DESCRIPTION

The **UCD4049B** devices are inverting hex buffers, and feature logic-level conversion using only one supply voltage(V_{CC}).The input-signal high level(V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads.

■ FEATURES

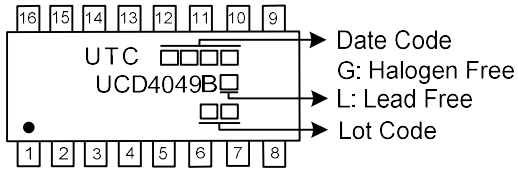
* High Sink Current for Driving 2 TTL Loads
* High-To-Low Level Logic Conversion
* Maximum Input Current of 1uA at 18V Over Full Package Temperature Rage
* 5V, 10V and 15V Parametric Ratings

■ ORDERING INFORMATION

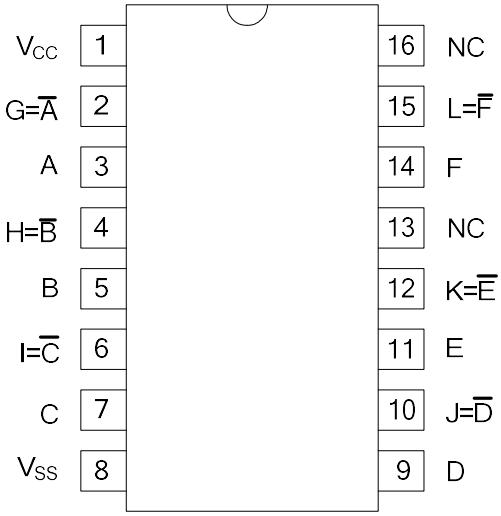
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4049BL-S16-R	UCD4049BG-S16-R	SOP-16	Tape Reel
UCD4049BL-P16-R	UCD4049BG-P16-R	TSSOP-16	Tape Reel

UCD4049BG-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16, TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



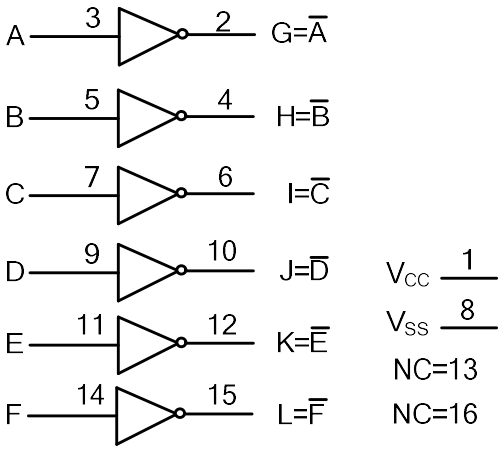
■ PIN CONFIGURATION



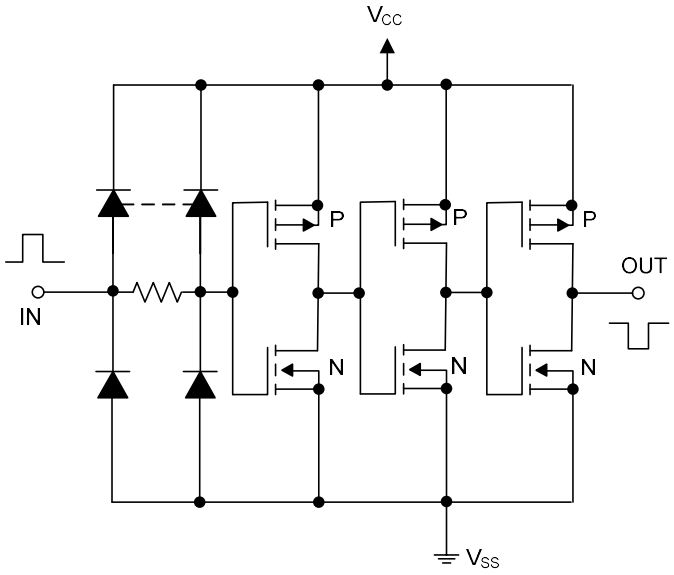
■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(G)
H	L
L	H

■ LOGIC DIAGRAM (positive logic)



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 18	V
Input Voltage	V_{IN}	-0.5 ~ V_{CC} +0.5	V
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5	V
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	3 ~ 15	V
Operating Temperature	T_{OPR}	-40 ~ +125	°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	θ_{JA}	73	°C/W
	TSSOP-16		108	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=5V, V_O=0.5V	3.5			V
		V_{CC}=10V, V_O=1.0V	7			V
		V_{CC}=15V, V_O=1.5V	11			V
Low-Level Input Voltage	V_{IL}	V_{CC}=5V, V_O=4.5V			1.5	V
		V_{CC}=10V, V_O=9.0V			3.0	V
		V_{CC}=15V, V_O=13.5V			4.0	V
High-Level Output Voltage	V_{OH}	V_{CC}=5V, V_I=0V,No Load	4.95	5		V
		V_{CC}=10V, V_I=0V,No Load	9.95	10		V
		V_{CC}=15V, V_I=0V,No Load	14.95	15		V
Low-Level Output Voltage	V_{OL}	V_{CC}=5V, V_I=5V,No Load		0	0.05	V
		V_{CC}=10V, V_I=10V,No Load		0	0.05	V
		V_{CC}=15V, V_I=15V,No Load		0	0.05	V
High-Level Output Current (Note)	I_{OH}	V_{CC}=5V, V_O=4.6V	-0.65	-1.2		mA
		V_{CC}=5V, V_O=2.5V	-2.1	-7.2		mA
		V_{CC}=10V, V_O=9.5V	-1.65	-3.5		mA
		V_{CC}=15V, V_O=13.5V	-4.3	-13		mA
Low-Level Output Current (Note)	I_{OL}	V_{CC}=4.5V, V_O=0.4V	2.6	6.5		mA
		V_{CC}=5V, V_O=0.4V	3.2	7.5		mA
		V_{CC}=10V, V_O=0.5V	8.0	16		mA
		V_{CC}=15V, V_O=1.5V	24.0	65		mA
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=15V ,V_{IN} = V_{CC} or GND			0.1	μA
Quiescent Supply Current	I_{DD}	V_{CC}=5V, V_{IN} = V_{CC} or V_{SS}, I_{OUT} = 0		0.02	1	μA
		V_{CC}=10V, V_{IN} = V_{CC} or V_{SS}, I_{OUT} = 0		0.02	2	μA
		V_{CC}=15V, V_{IN} = V_{CC} or V_{SS}, I_{OUT} = 0		0.02	4	μA

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS

(T_A=25°C, Input: t_R=t_F=20ns, C_L=50pF, R_L=200KΩ, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	V_{CC}=5V		80	120	ns
		V_{CC}=10V		40	65	ns
		V_{CC}=15V		30	50	ns
	t_{PHL}	V_{CC}=5V		40	65	ns
		V_{CC}=10V		25	40	ns
		V_{CC}=15V		20	30	ns
Transition Time	t_{TLH}	V_{CC}=5V		60	160	ns
		V_{CC}=10V		40	80	ns
		V_{CC}=15V		30	60	ns
	t_{THL}	V_{CC}=5V		30	60	ns
		V_{CC}=10V		20	40	ns
		V_{CC}=15V		15	30	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		15	22.5	pF

■ TEST CIRCUIT AND WAVEFORMS

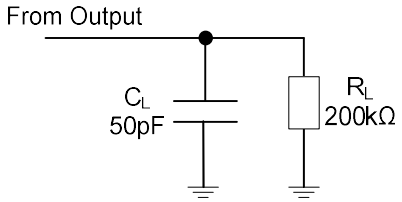


Fig 1. Definitions for test circuit

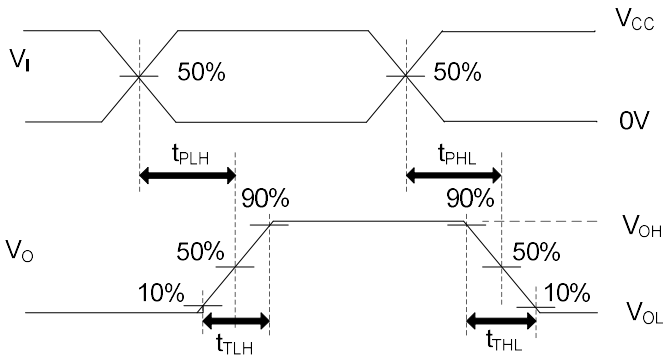


Fig 2. Propagation Delay Times

Note: C_L includes probe and jig capacitance.