HIGH-VOLTAGE MIXED-SIGNAL IC

UC8251

All-in-one driver IC w/ Timing Controller for
White/Black/Red Dot-Matrix Micro-Cup ESL

Preliminary Specifications **IC Version: d_A**
Datasheet Revision: 0.1 for_TFT_Module_Use_only **November 22, 2019**

ULTRACHIP

The Coolest EPD Driver, Ever!

Table of Content

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INTRODUCTION

The UC8251 is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VSH/VSL (±2.4V~±15.0V) and VDHR (2.4V~15.0V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

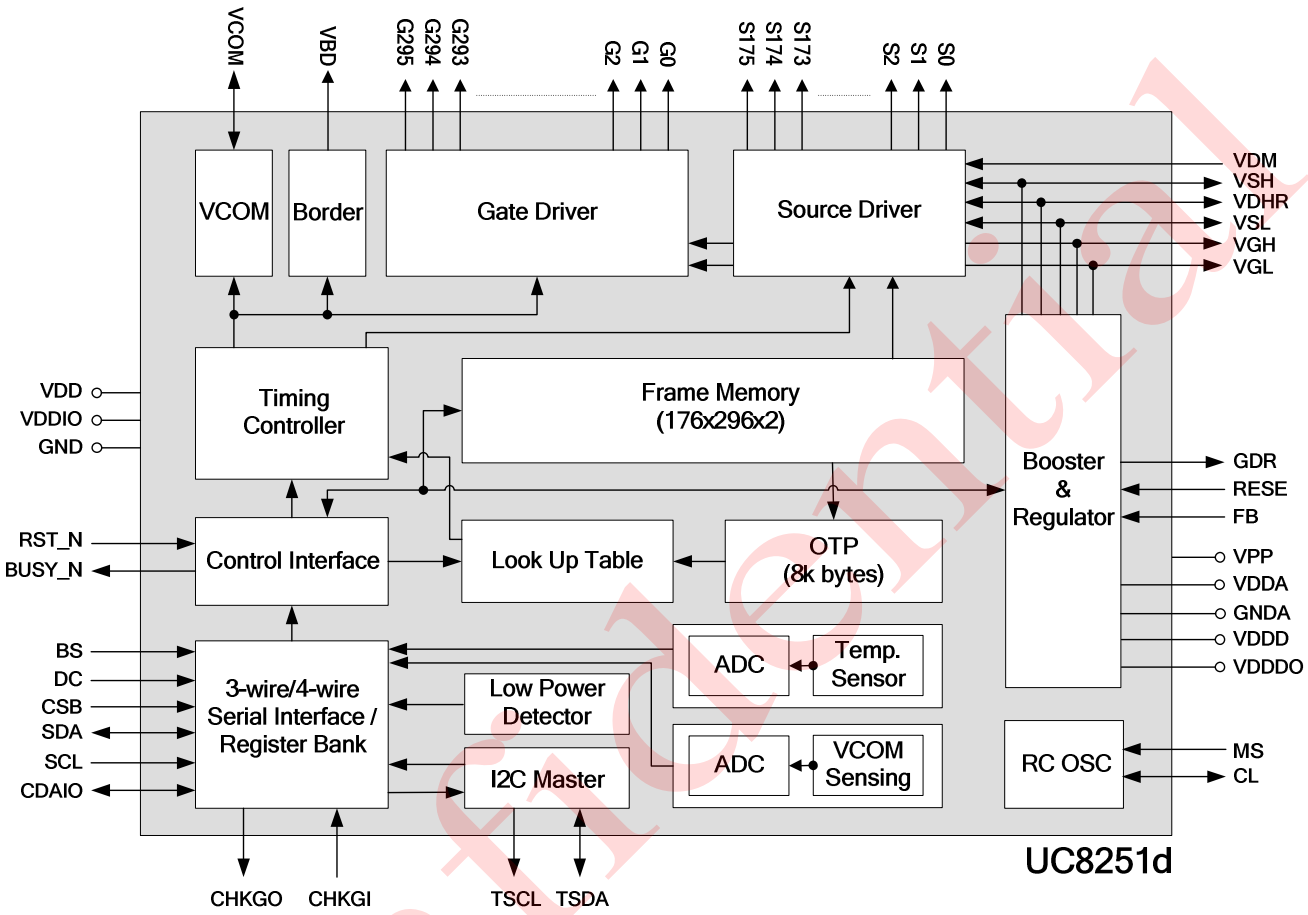
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several resolutions
  - Up to 176 source x 296 gate resolution + 1 border + 1 VCOM
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: 2 or more chips cascade mode
- Memory (Max.): 176 x 296 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 °C ± 2.0°C / 8-bit status
  - Off-Chip: -55~125°C ± 2.0°C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection (V_{DD}<2.5V)
- OSC / PLL: On-chip RC oscillator
- VCOM:
  - AC-VCOM / DC-VCOM (by LUT)
  - Support VCOM sensing (6-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +10V~+20V
  - VGL: -10V ~-20V
  - VSH: +2.4 ~ +15.0V (programmable, black/white)
  - VSL: -2.4 ~ -15.0V (programmable, black/white)
  - VDHR: +2.4 ~ +15.0V (programmable, red)
- Supply voltage VDD/VDDA/VDDIO: 2.3~ 3.6V
- OTP: 8K-byte OTP for LUTs and Settings
- Package: COG
- Source/Gate bump information
  - Bump pitch: 13 μM ± 2 μM
  - Bump space: 1 μM ± 3 μM
  - Bump surface: 1200 μM^2

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UC8251dGAA-L0X3-3	3-inch tray, wafer thickness 300uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	7	PWR	Digital power
VDDA	10	PWR	Analog power
VDDIO	10	PWR	IO power
VDDDO	4	PWR	Digital power output (1.32V)
VDDD (VDDDI)	4	PWR	Digital power input (1.32V)
VPP	6	PWR	OTP program power (8.25V)
VDM	4	PWR	Analog Ground.
GND	18	PWR	Digital Ground.
GNDA	17	PWR	Analog Ground
LDO PINS			
VSH	10	I/O	Positive source driver Voltage (+2.4V ~ +15.0V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +15.0V)
VSL	10	I/O	Negative source driver voltage (-2.4V ~ -15.0V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. H: 3-wire interface.
RST_N	1	I (Pull-up)	Global reset pin. Low: active. When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 100us.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDAIO	1	I/O	Cascade data pin. Leave it open if not used.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data Connect to GND if BS=High.

Pin (Pad) Name	Pin Count	Type	Description
I²C INTERFACE			
TSCL	2	O (open-drain)	I²C clock (External pull-up resistor is necessary.) Leave them open if not used.
TSDA	2	I/O (open-drain)	I²C data (External pull-up resistor is necessary.) Leave them open if not used.
OUTPUT PINS			
S0~S175 (S<0>~S<175>)	176	O	Source driver output signals.
G0~G295 (G<0>~G<295>)	296	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD (VBD<1>~VBD<4>)	1x4	O	Border output pins.
BOOSTER PINS			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	12	I/O	Positive Gate voltage.
VGL	16	I/O	Negative Gate voltage.
CHECK PANEL PINS			
CHKGI	1	I (Pull-down)	Check panel break input. Leave open if it is not used.
CHKGO	1	O	Check panel break output. Leave open if it is not used.
RESERVED PINS			
VSYNC	1	O	Reserved pins. Leave it floating.
TEST1~TEST3	1x3	I	Reserved pins. Leave it floating or connected to VSS.
TEST6, TEST7	1x2	O	Reserved pins. Leave it floating.
DUMMY (DUMMY<0> ~ DUMMY<14>)	15	-	Reserved pins. Leave it floating.
NC (NC<0> ~ NC<21>)	22	-	Not Connected.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	#	#	#	#	#	#	#	#	RES[1:0], REG, KW/R, UD, SHL, SHD_N, RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	--	--	--	#	#	VS_EN, VG_EN	03H
		0	1	--	--	--	--	#	#	#	#	VGHL_LV[3:0]	00H
		0	1	--	--	#	#	#	#	#	#	VSH[5:0]	3FH
		0	1	--	--	#	#	#	#	#	#	VSL[5:0]	3FH
		0	1	--	--	#	#	#	#	#	#	VDHR[5:0]	0DH
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (176x296):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00H
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (176x296):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00H
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00H
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		1	1	1	0	1	0	0	1	0	1	Check code	A5H
14	VCOM LUT (LUTC) (81-byte command, structure of bytes 2~9 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-2 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	STATE 1 REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-2[7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (57-byte command, structure of bytes 2~9 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-2 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	STATE 1 REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-2[7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
16	B2W LUT (LUTKW / LUTR) (81-byte command, structure of bytes 2~9 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-2 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	STATE 1 REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-2[7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
17	W2B LUT (LUTWK / LUTW) (81-byte command, structure of bytes 2~9 repeated 10 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-2 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	STATE 1 REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-2[7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
18	B2B LUT (LUTKK / LUTK) (81-byte command, structure of bytes 2~9 repeated 10 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 1-2 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	STATE 1 REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-1 [7:0]	-
		0	1	:	:	:	:	:	:	:	:	FRAME NUMBER 2-2[7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
19	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[15:8]	00H
		0	1	#	#	--	--	#	#	#	#	EOPT, ESO, XON[19:16]	00H
		0	1	#	#	#	#	#	#	#	#	GROUP_KWE[7:0]	FFH
		0	1	#	#	--	--	--	--	#	#	ATRED, NORED, GROUP_KWE[9:8]	3FH
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	--	#	#	#	#	#	FRS[4:0]	09H
21	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
22	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE, TO[3:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
23	Temperature Sensor Write (TSW)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**		**42H**
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
24	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43H**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
25	Panel Break Check (PBC)	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**		**44H**
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
26	VCOM and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50H**
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
27	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	--	--	--	--	--	--	--	#	LPD	01H
28	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
29	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
30	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
31	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		1	1	--	--	--	--	--	--	--	--	Reserved	N/A
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	0AH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[15:8]	FFH
		1	1	#	#	#	#	#	#	#	#	LUT_REV[23:16]	FFH
32	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG, I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
33	Cyclic Redundancy Check (CRC)	0	0	0	1	1	0	0	0	1	0		72H
		1	1	#	#	#	#	#	#	#	#	CRC_MSB[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	CRC_LSB[7:0]	FFH
34	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
35	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
36	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H
37	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07H
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
38	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
39	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
40	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
41	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
42	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	--	--	--	--	--	--	--	--	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 0000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
43	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
44	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
45	LVD Voltage Select (LVSEL)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**		**E4H**
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
46	Force Temperature (TSSET)	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**		**E5H**
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

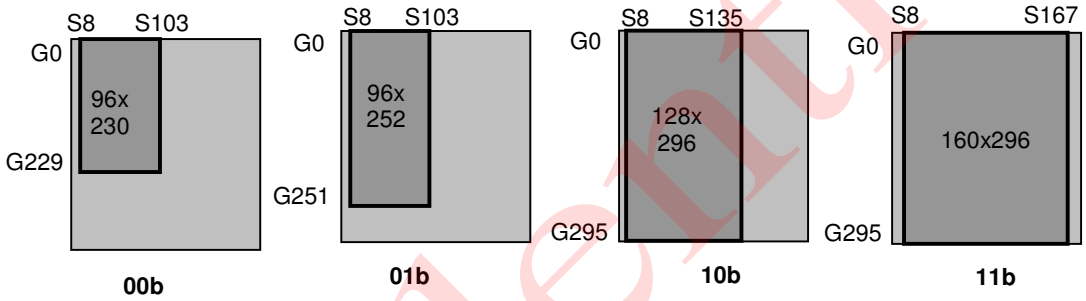
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	0	0	0	0	0	0	0	0	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

RES[1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S8 ~ S103. Active gate channels: G0 ~ G229.
01b: 96x252 Active source channels: S8 ~ S103. Active gate channels: G0 ~ G251.
10b: 128x296 Active source channels: S8 ~ S135. Active gate channels: G0 ~ G295.
11b: 160x296 Active source channels: S8 ~ S167. Active gate channels: G0 ~ G295.



(1) Minimum active GD is always G0 regardless of <UD>(R00H).
(2) Minimum active SD is always S0 regardless of <SHL>(R00H).

maximum resolution
active resolution

REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect (Default).

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	-	-	-	VS_EN	VG_EN	03H
	0	1	-	-	-	-	VGHL_LV[3:0]				00H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	-	-	VDHR[5:0]						0DH

VS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V
0001	VGH=19V, VGL= -19V
0010	VGH=18V, VGL= -18V
0011	VGH=17V, VGL= -17V
0100	VGH=16V, VGL= -16V
0101	VGH=15V, VGL= -15V
0110	VGH=14V, VGL= -14V
0111	VGH=13V, VGL= -13V
1000	VGH=12V, VGL= -12V
1001	VGH=11V, VGL= -11V
1010	VGH=10V, VGL= -10V

VSH[5:0]: Internal VSH power selection for B/W pixel.(**Default value: 11 1111b**)

VSH	**Voltage**	VSH	**Voltage**	VSH	**Voltage**	VSH	**Voltage**
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	**11 1111**	**15.0 V**

VSL[5:0]: Internal VSL power selection for B/W pixel. (**Default value: 11 1111b**)

VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
00 0000	-2.4 V	01 0000	-5.6 V	10 0000	-8.8 V	11 0000	-12.0 V
00 0001	-2.6 V	01 0001	-5.8 V	10 0001	-9.0 V	11 0001	-12.2 V
00 0010	-2.8 V	01 0010	-6.0 V	10 0010	-9.2 V	11 0010	-12.4 V
00 0011	-3.0 V	01 0011	-6.2 V	10 0011	-9.4 V	11 0011	-12.6 V
00 0100	-3.2 V	01 0100	-6.4 V	10 0100	-9.6 V	11 0100	-12.8 V
00 0101	-3.4 V	01 0101	-6.6 V	10 0101	-9.8 V	11 0101	-13.0 V
00 0110	-3.6 V	01 0110	-6.8 V	10 0110	-10.0V	11 0110	-13.2 V
00 0111	-3.8 V	01 0111	-7.0 V	10 0111	-10.2 V	11 0111	-13.4 V
00 1000	-4.0 V	01 1000	-7.2 V	10 1000	-10.4 V	11 1000	-13.6 V
00 1001	-4.2 V	01 1001	-7.4 V	10 1001	-10.6 V	11 1001	-13.8 V
00 1010	-4.4 V	01 1010	-7.6 V	10 1010	-10.8 V	11 1010	-14.0 V
00 1011	-4.6 V	01 1011	-7.8 V	10 1011	-11.0 V	11 1011	-14.2 V
00 1100	-4.8 V	01 1100	-8.0 V	10 1100	-11.2 V	11 1100	-14.4 V
00 1101	-5.0 V	01 1101	-8.2V	10 1101	-11.4 V	11 1101	-14.6 V
00 1110	-5.2 V	01 1110	-8.4 V	10 1110	-11.6 V	11 1110	-14.8 V
00 1111	-5.4 V	01 1111	-8.6 V	10 1111	-11.8 V	**11 1111**	**-15.0 V**

VDHR[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 00 1101b**)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	**5.0 V**	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	11 1111	15.0 V

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	03H
	0	1	**-**	**-**	T_VDS_OFF[1:0]		**-**	**-**	**-**	**-**	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	00H
	0	1	:	:	:	:	:	:	:	:	00H
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	00H

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “NEW” data to SRAM.

In KWR mode, this command writes “RED” data to SRAM.

(13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host’s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (81-byte command, structure of bytes 2~9 repeated 10 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	GROUP REPEAT TIMES [7:0]								-
	0	1	LEVEL SELECT1-1		LEVEL SELECT1-2		LEVEL SELECT2-1		LEVEL SELECT2-2		-
	0	1	FRAME NUMBER 1-1 [7:0]								-
	0	1	FRAME NUMBER 1-2 [7:0]								-
	0	1	STATE 1 REPEAT TIMES [7:0]								-
	0	1	FRAME NUMBER 2-1 [7:0]								-
	0	1	FRAME NUMBER 2-2[7:0]								-
	0	1	STATE 2 REPEAT TIMES [7:0]								-

This command stores VCOM Look-Up Table with 10 groups of data. This LUT includes 10 kinds of groups; each group is of 8 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 10, 18, 26 , 34,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3, 11, 19, 27, 35……:

Level selection

00b: VCOM_DC

01b: VSH+VCOM_DC (VCOMH)

10b: VSL+VCOM_DC (VCOML)

11b: Floating

Bytes 4~5, 12~13, 20~21, 28~29, 36~37,..:

Number of Frames (state1)

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Bytes 6, 14, 22, 30, 38,..:

State1 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 7~8, 14~15, 23~24, 30~31, 39~40,..:

Number of Frames (state2)

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Bytes 9, 17, 25, 33, 41,..:

State2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

(15) W2W LUT (LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (57-byte command, structure of bytes 2~9 repeated 7 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	GROUP REPEAT TIMES [7:0]								-
	0	1	LEVEL SELECT1-1		LEVEL SELECT1-2		LEVEL SELECT2-1		LEVEL SELECT2-2		-
	0	1	FRAME NUMBER 1-1 [7:0]								-
	0	1	FRAME NUMBER 1-2 [7:0]								-
	0	1	STATE 1 REPEAT TIMES [7:0]								-
	0	1	FRAME NUMBER 2-1 [7:0]								-
	0	1	FRAME NUMBER 2-2[7:0]								-
	0	1	STATE 2 REPEAT TIMES [7:0]								-

This command stores LUTW2W Look-Up Table with 7 groups of data. This LUT includes 7 kinds of groups; each group is of 8 bytes. Each group is divied to 2 states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 10, 18, 26 , 34,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3, 11, 19, 27, 35……:

Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

Bytes 4~5, 12~13, 20~21, 28~29, 36~37,..:

Number of Frames (state1)

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Bytes 6, 14, 22, 30, 38,..:

State1 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 7~8, 14~15, 23~24, 30~31, 39~40,..:

Number of Frames (state2)

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Bytes 9, 17, 25, 33, 41,..:

State2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

(16) B2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for B2W or Red (81-byte command, structure of bytes 2~9 repeated 10 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	GROUP REPEAT TIMES [7:0]								-
	0	1	LEVEL SELECT1-1		LEVEL SELECT1-2		LEVEL SELECT2-1		LEVEL SELECT2-2		-
	0	1	FRAME NUMBER 1-1 [7:0]								-
	0	1	FRAME NUMBER 1-2 [7:0]								-
	0	1	STATE 1 REPEAT TIMES [7:0]								-
	0	1	FRAME NUMBER 2-1 [7:0]								-
	0	1	FRAME NUMBER 2-2[7:0]								-
	0	1	STATE 2 REPEAT TIMES [7:0]								-

This command stores B2W Look-Up Table with 10 groups of data. This LUT includes 10 kinds of groups; each group is of 8 bytes. Each group is divied to 2 states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 10, 18, 26 , 34,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3, 11, 19, 27, 35……:

Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

Bytes 4~5, 12~13, 20~21, 28~29, 36~37,..:

Number of Frames (state1)

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Bytes 6, 14, 22, 30, 38,..:

State1 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 7~8, 14~15, 23~24, 30~31, 39~40,..:

Number of Frames (state2)

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Bytes 9, 17, 25, 33, 41,..:

State2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

(17) W2B LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to B2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

(18) B2B LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to B2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

(19) LUT OPTION (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	2AH
	0	1	STATE_XON[7:0]								00H
	0	1	STATE_XON[15:8]								00H
	0	1	EOPT	ESO	-	-	STATE_XON[19:16]				00H
	0	1	GROUP_KWE[7:0]								FFH
			ATRED	NORED	-	-	-	-	GROUP_KWE[9:8]		03H

This command sets XON and the several options of KWR mode's LUT.

STATE_XON[19:0]:

All Gate ON control (Each bit controls one states, STATE_XON [0] for Group-1/State-1, STATE_XON [1] for Group-1/State-2 .....)

0000 0000 0000 0000 0000b: no All-Gate-ON

0000 0000 0000 0000 0001b: Group-1/State-1 All-Gate-ON

0000 0000 0000 0000 0011b: Group-1/State-1 and Group-1/State-2 All-Gate-ON

0000 0000 0000 0000 0111b: Group-1/State-1, Group-1/State-2 and Group-2/State-1 All-Gate-ON

: :

EOPT: LUT Sequence option 1.

ESO: LUT Sequence option 2.

ATRED: Automatic mode. The option is only available when KW/R=0.

NORED: No Red data. The option is only available when KW/R=0.

GROUP_KWE[9:0]:

The options are only available when KW/R=0 and (ATRED | NORED) = 1.

There are only 10 groups in the K/W LUT. Each bit controls one group.

11 1111 1111b: all groups are executed sequentially.

11 1111 1110b: only Group-1 is bypassed.

11 1111 1100b: Group-1 and Group-2 are bypassed.

: :

(20) PLL CONTROL (PLL) (R30H)

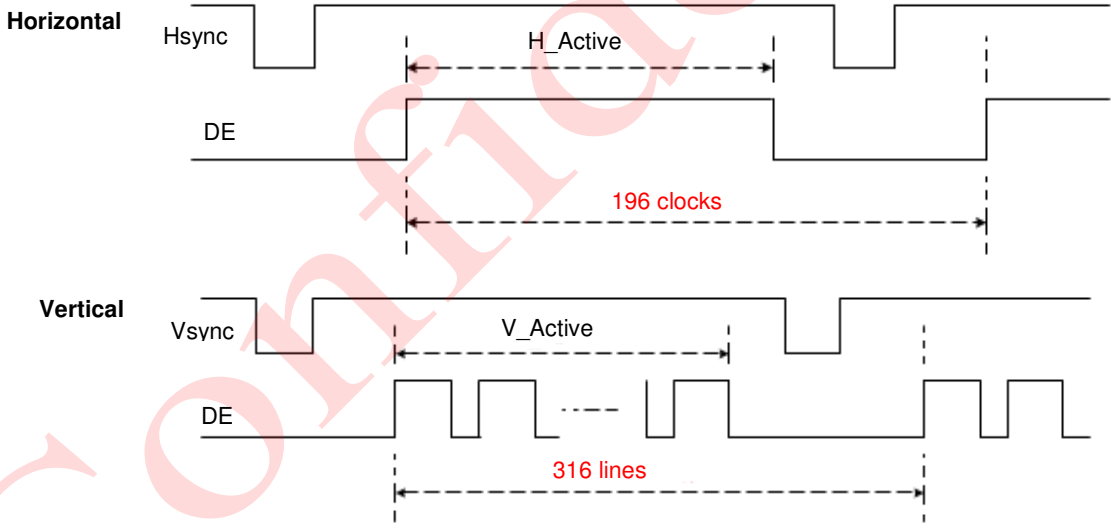
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	FRS[4:0]					09H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[4:0]: Frame rate setting

FRS	Frame rate
00000	5Hz
00001	10Hz
00010	15Hz
00011	20Hz
00100	25Hz
00101	30Hz
00110	35Hz
00111	40Hz
01000	45Hz
01001	**50Hz**
01010	55Hz
01011	60Hz
01100	65Hz
01101	70Hz
01110	75Hz
01111	80Hz

FRS	Frame rate
10000	85Hz
10001	90Hz
10010	95Hz
10011	100Hz
10100	105Hz
10101	110Hz
10110	115Hz
10111	120Hz
11000	130Hz
11001	140Hz
11010	150Hz
11011	160Hz
11100	170Hz
11101	180Hz
11110	190Hz
11111	200Hz



(21) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(22) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(23) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(24) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(25) PANEL GLASS CHECK (PBC)

Action	R/W	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	44H
	R	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(26) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				31h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

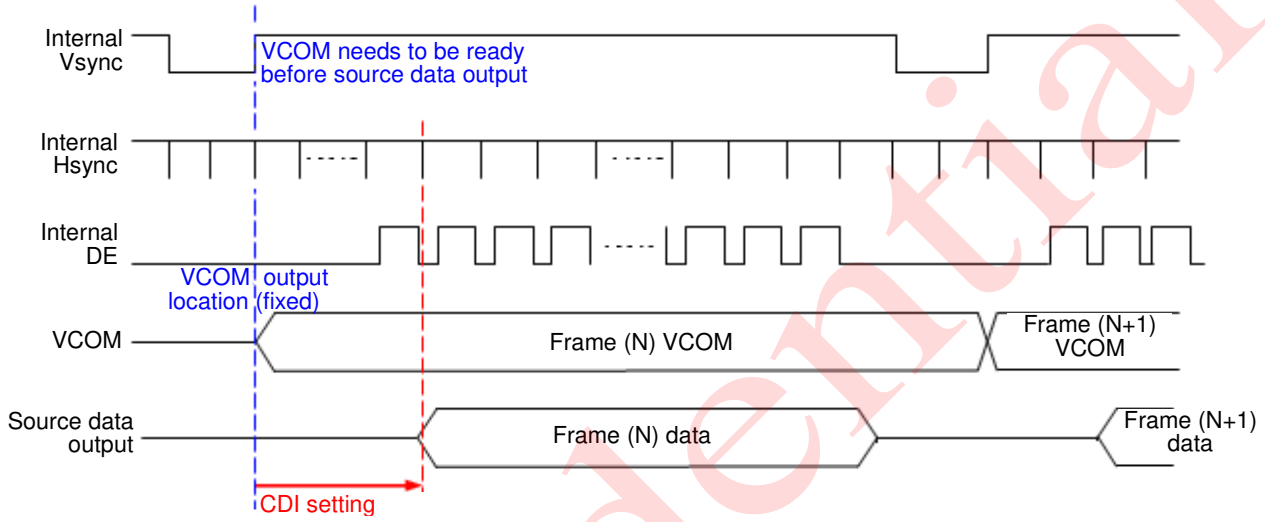
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



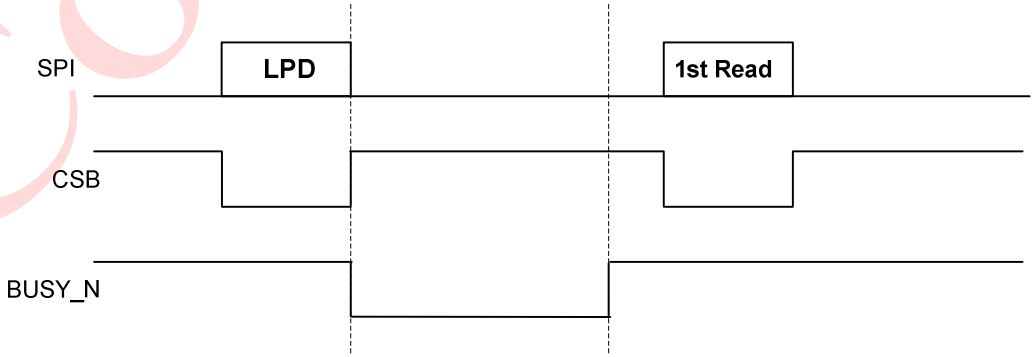
(27) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	0	1	0	1	0	0	0	1	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(28) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

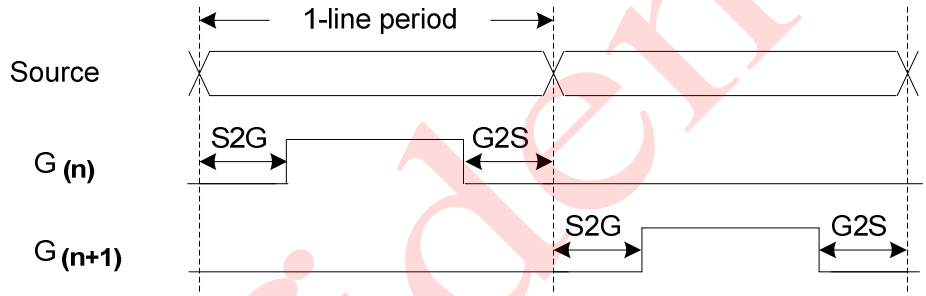
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 660 nS.



(29) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation, assuming HST[7:3]=0, VST[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[8:0] – 1

Source: First active source = X (If HRES[7:0]>160, X=0; otherwise, X=8)
Last active source = HRES[7:0] - 1 + X (If HRES[7:0]>160, X=0; otherwise, X=8)

Example: For 128 (source) x 272 (gate), assuming HST[7:3]=0, VST[8:0]=0

Gate: First active gate = G0,
Last active gate = G271 (VRES[8:0] = 272; 272 - 1= 271)

Source: First active source = S8, (HRES[7:0][160 therefore X=8)
Last active source = S135; (128 - 1 + 8 = 135)

(30) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[8:0]: Vertical Display Start Position (Gate)

Example : For 128(Source) x 240(Gate)
HST[7:0] = 32
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (240-1+32=271)

Source: First active source = S40 (HST[7:0] = 32, X=8, 32+8 = 40), (Note)
Last active source = S167 (128-1+32+8=167)

Note: If HRES[7:0] > 160, X=8; otherwise X=8.

(31) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	Reserved								00h
	1	1	CHIP_REV[7:0]								0Ah
	1	1	LUT_REV[7:0]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[23:16]								FFh

The LUT_REV is read from OTP address = 0x0017~0X0019 / 0x1017~0X1019.

CHIP_REV[7:0]: Chip Revision, it is fixed by "0x0Ah".

(32) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ flag	I²C_ERR	I²C_ BUSYN	data_ flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(33) CYCLIC REDUNDANCY CHECK (CRC) (R72H)

Action	R/W	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Cyclic redundancy check	R	0	0	1	1	1	0	0	1	0	72H
	R	1	CRC_MSB[7:0]								FFH
	R	1	CRC_LSB[7:0]								FFH

This command reads Cyclic redundancy check(CRC) result.

The calculation only includes 0x0000~0x1FEF OTP data..

Polynomial = $x^{16} + x^{12} + x^5 + 1$, initial vaulte: 16'hFFFF

The result will be reset after this command.

CRC_MSB[7:0]: Most significant bits of CRC result

CRC_LSB[7:0]: Lease significant bits of CRC result

(34) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(35) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(36) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(37) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~13h)

HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~127h)

VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(38) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(39) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(40) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(41) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

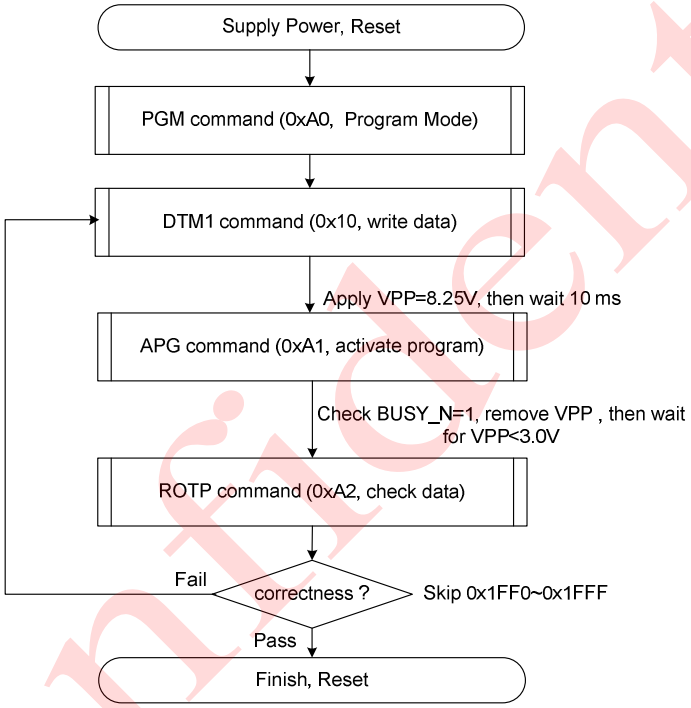
The BUSY_N flag would fall to 0 until the programming is completed.

(42) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



The sequence of programming OTP.

(43) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

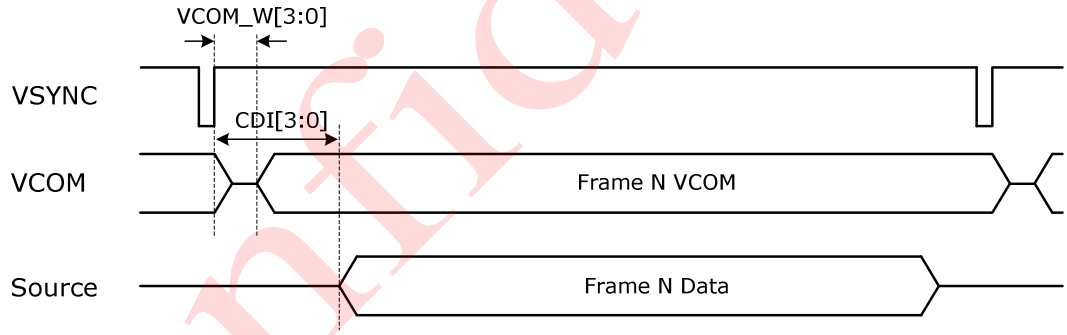
1: Temperature value is defined by TS_SET[7:0] registers.

(44) POWER SAVING (PWS) (RE3H)

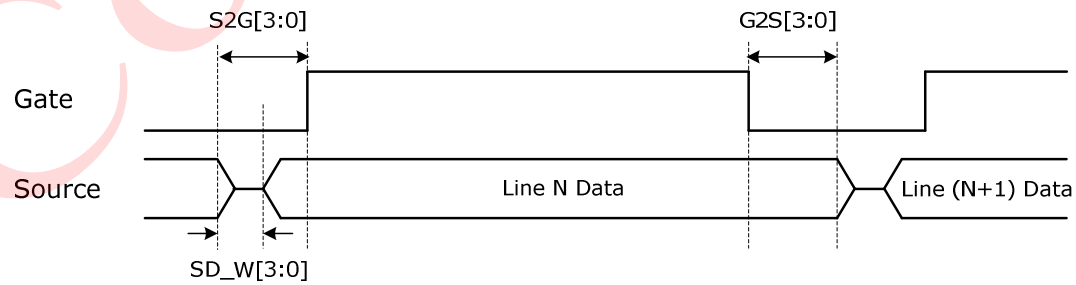
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



(45) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(46) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

HOST INTERFACES

UC8251 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

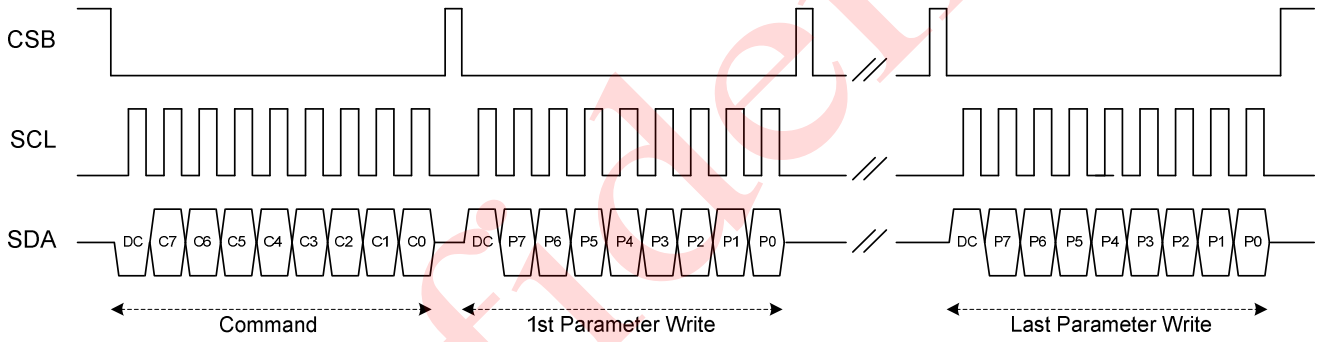


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

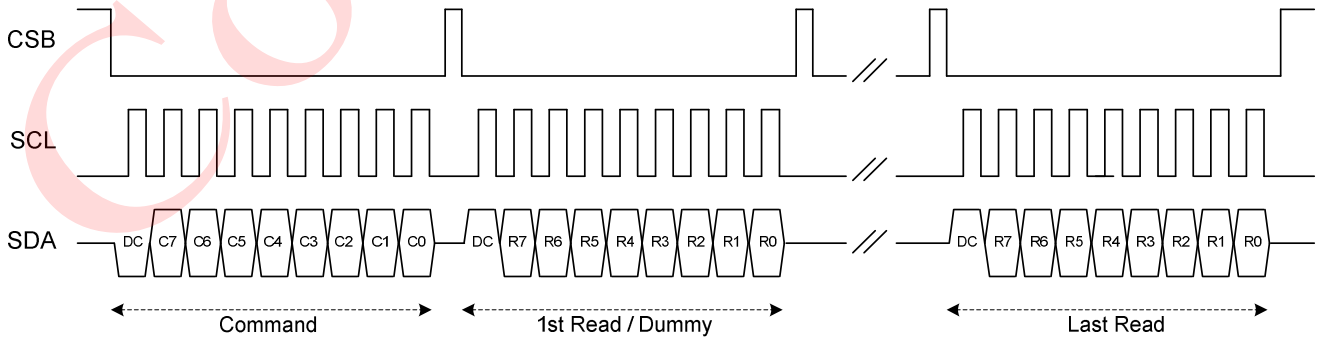


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

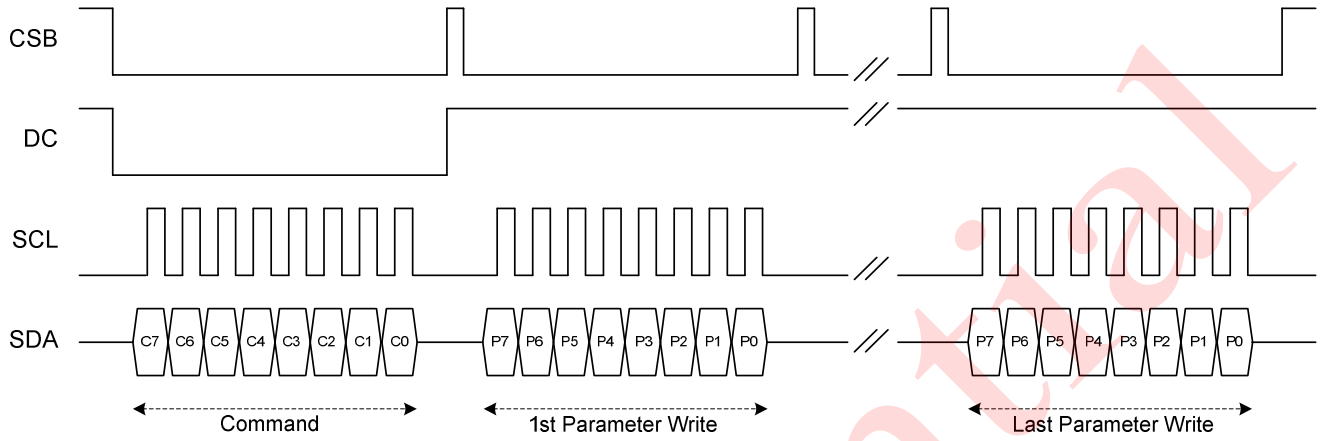


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

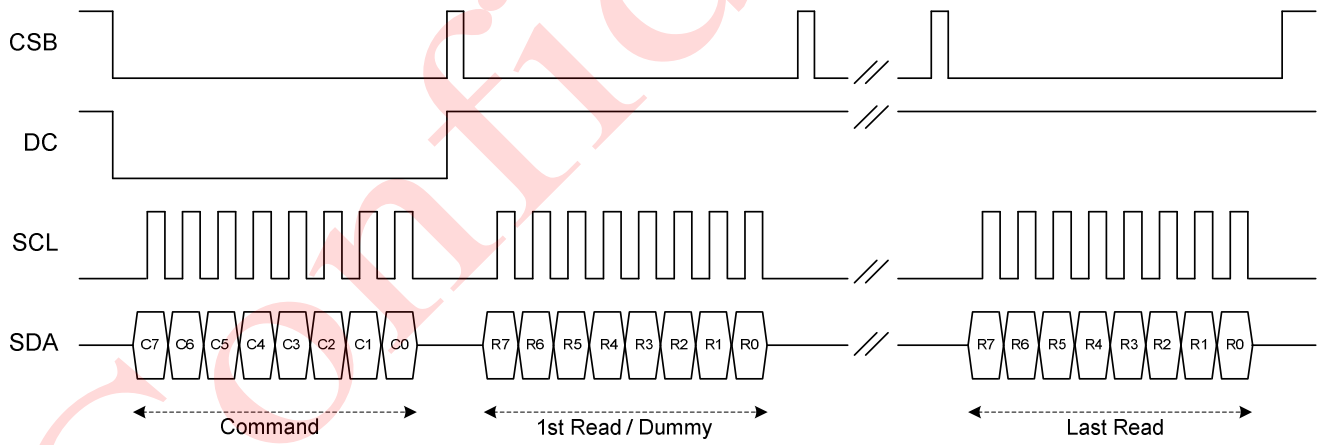
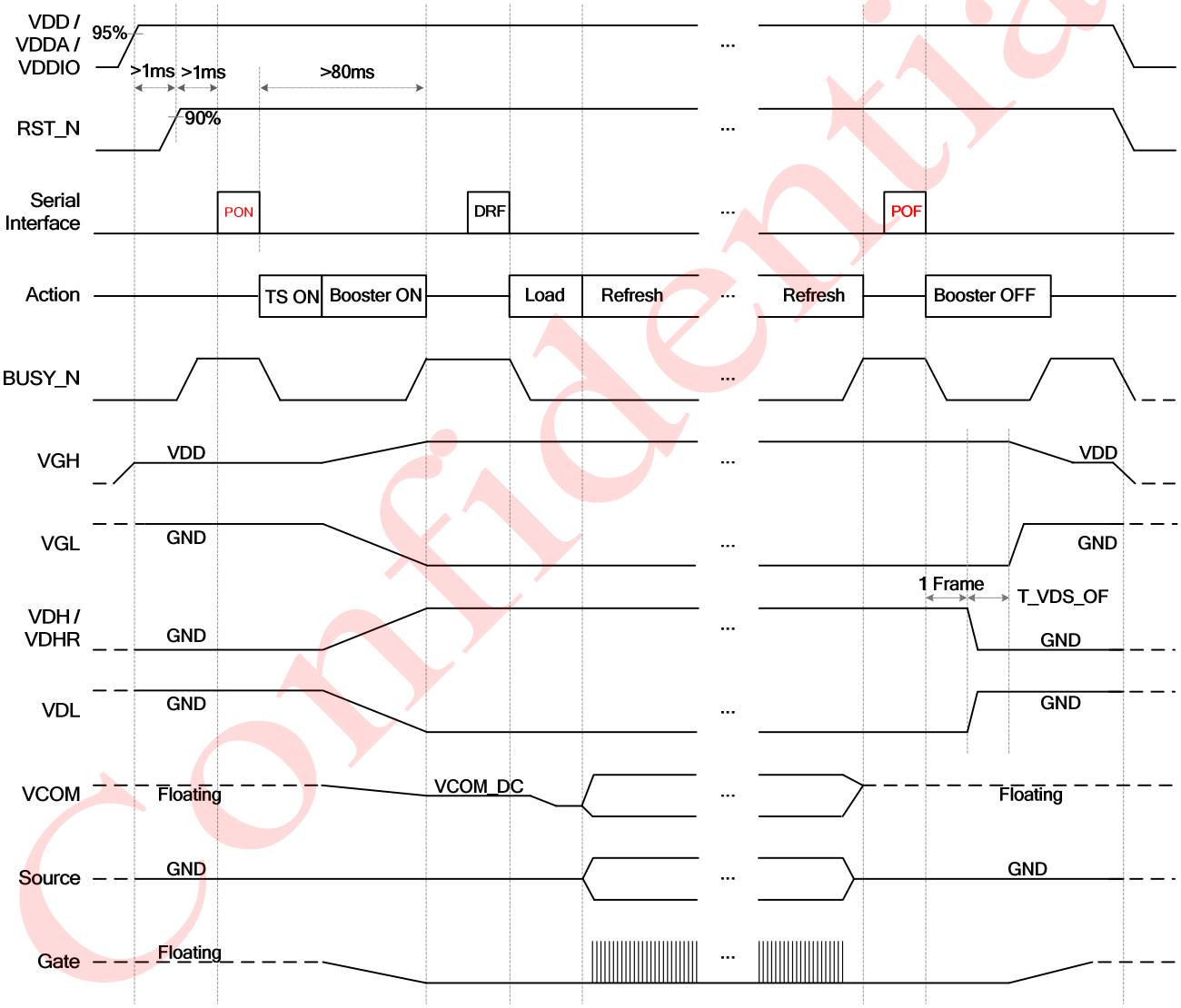


Figure: 4-wire SPI read operation

POWER MANAGEMENT

Power ON/OFF Sequence

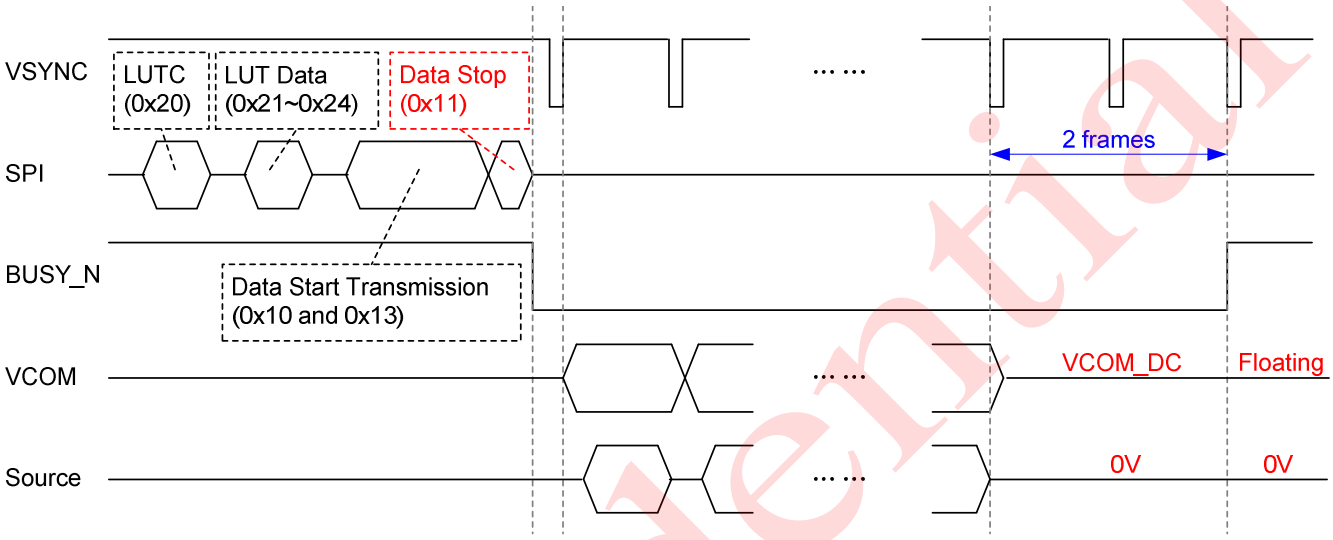
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In OTP mode (REG=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.
4. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



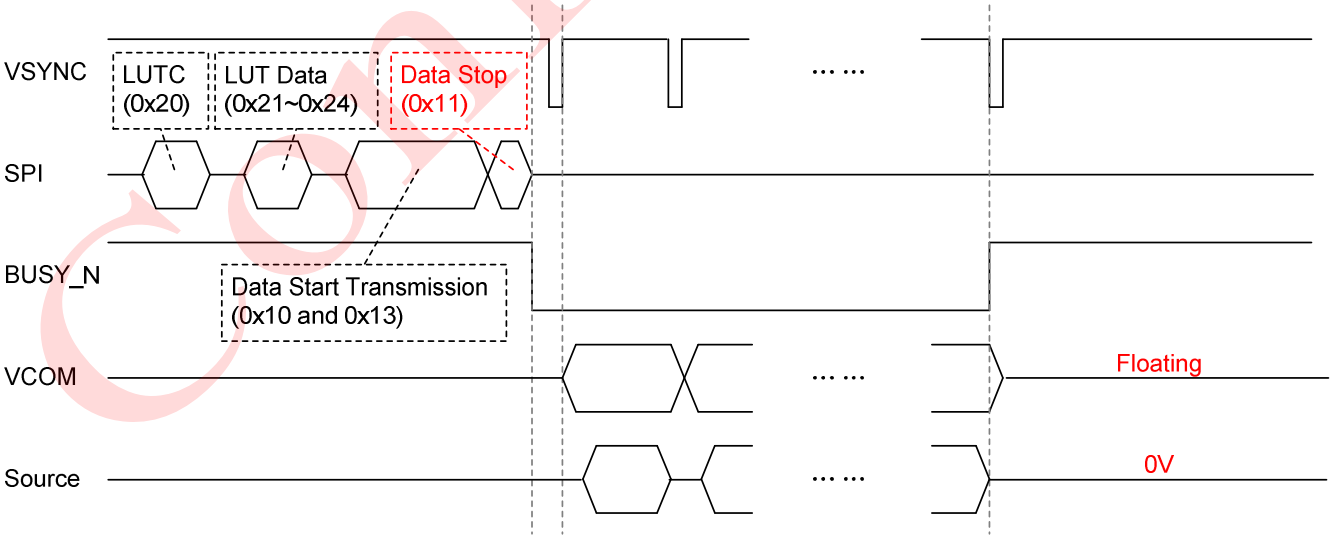
Data Transmission Waveform

Example 1: After 3 cases, the driver will send 2 frame VCOM and data to 0 V.

1. All 7 LUT groups (KW mode) or 10 LUT groups (KWR mode) complete.
2. Meet the group whose Times to Repeat =0
3. Meet the group whose all Number of Frames =0



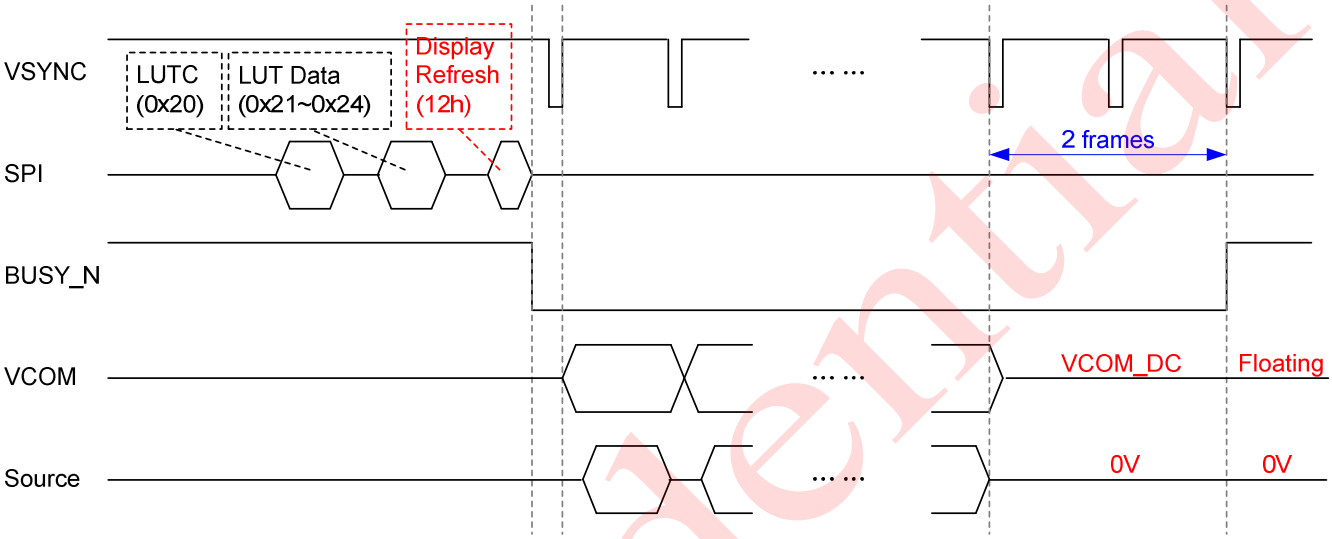
Example2: While level selection in LUT (LUTC only) is "1111_1111b", the driver will float VCOM.



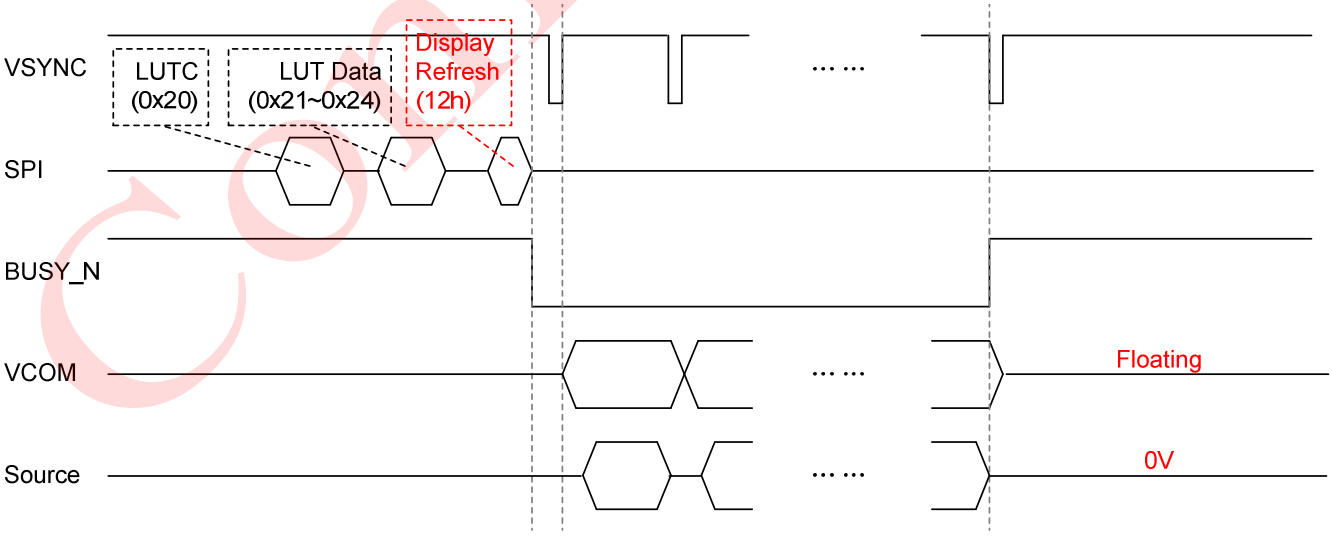
Display Refresh Waveform

Example 1: After three cases, the driver will send 2 frames VCOM and data to 0 V.

1. All 7 LUT groups (KW mode) or 10 LUT groups (KWR mode) complete.
2. Meet the group whose Times to Repeat = 0
3. Meet the group whose all Number of Frames = 0



Example2: While level selection in LUT (LUTC only) is “1111_1111b”, the driver will float VCOM.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
LUTC	X	No action
LUTWW	X	No action
LUTKW/LUTR	X	No action
LUTWK/LUTW	X	No action
LUTKK/LUTK	X	No action
LUTOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
TSW	X	No action
TSR	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
CRC	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action

V: Accepted, X: Ignored

OTP ADDRESS MAPPING

The size of the internal One Time Programmable (OTP) memory is 8K bytes, and the address is from 0x0000 to 0x1FFF. The unprogrammed bit is logic 1. Only the bit at logic 1 can be programmed to logic 0, but the bit at logic 0 cannot be converted to logic 1.

There are 2 areas (0x0FA9~0x0FEF, 0x1FA9~0x1FEF) are reserved for user defined. Write all 0xFF of data to skip the 2 areas. The recommended voltage of VPP during programming is 8.25V. In the other condition except for programming, let VPP floating or be connected to GND. The maximum current of VPP during programming is 5mA.

There are 2 banks in the internal OTP, and each bank has 4K bytes storage memory. The formats of each bank are the same, and the selection of bank is controlled by Check Code (0x0000 and 0x1000). Bank1 has higher priority than Bank0. The 2 banks are used for two times programming.

Table 1: OTP Address Map

Bank0		Bank1	
Address	Content	Address	Content
0x0000	Check Code (0xA5)	0x1000	Check Code (0xA5)
0x0001~0x0013	Command Default Setting *(1)	0x1001~0x1013	Command Default Setting *(1)
0x0014~0x0016	LUT Version [23:0]	0x1014~0x1016	LUT Version [23:0]
0x0017~0x0019	Chip ID [23:0]	0x1017~0x1019	Chip ID [23:0]
0x001A~0x0024	Temperature Boundary 0~10 (TB0~TB10)	0x101A~0x1024	Temperature Boundary 0~10 (TB0~TB10)
0x0025~0x016F	Temperature Range 0 *(2)	0x1025~0x116F	Temperature Range 0 *(2)
0x0170~0x02BA	Temperature Range 1 *(2)	0x1170~0x12BA	Temperature Range 1 *(2)
0x02BB~0x0405	Temperature Range 2 *(2)	0x12BB~0x1405	Temperature Range 2 *(2)
0x0406~0x0550	Temperature Range 3 *(2)	0x1406~0x1550	Temperature Range 3 *(2)
0x0551~0x069B	Temperature Range 4 *(2)	0x1551~0x169B	Temperature Range 4 *(2)
0x069C~0x07E6	Temperature Range 5 *(2)	0x169C~0x17E6	Temperature Range 5 *(2)
0x07E7~0x0931	Temperature Range 6 *(2)	0x17E7~0x1931	Temperature Range 6 *(2)
0x0932~0x0A7C	Temperature Range 7 *(2)	0x1932~0x1A7C	Temperature Range 7 *(2)
0x0A7D~0x0BC7	Temperature Range 8 *(2)	0x1A7D~0x1BC7	Temperature Range 8 *(2)
0x0BC8~0x0D12	Temperature Range 9 *(2)	0x1BC8~0x1D12	Temperature Range 9 *(2)
0x0D13~0x0E5D	Temperature Range 10 *(2)	0x1D13~0x1E5D	Temperature Range 10 *(2)
0x0E5E~0x0FA8	Temperature Range 11 *(2)	0x1E5E~0x1FA8	Temperature Range 11 *(2)
0x0FA9~0x0FEF	Reserved for user-defined	0x1FA9~0x1FEF	Reserved for user-defined
0x0FF0~0x0FFF	Reserved for UltraChip	0x1FF0~0x1FFF	Reserved for UltraChip

Note:

(1) See section "COMMAND DEFAULT SETTING" for more detail.

(2) See section "LUT FORMAT IN OTP" for more detail.

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 11 temperature boundary settings (TBx) to determine 12 temperature ranges. The sequence of mechanism is from TB0 to TB10, as shown below. If less than 12 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x0000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1, Read 0x1000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x001A / 0x101A	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x001B / 0x101B	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x001C / 0x101C	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x001D / 0x101D	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x001E / 0x101E	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x001F / 0x101F	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x0020 / 0x1020	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x0021 / 0x1021	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x0022 / 0x1022	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Read 0x0023 / 0x1023	Real Temperature ≦ TB9	Use TR9's table & setting, exit
12. Read 0x0024 / 0x1024	Real Temperature ≦ TB10	Use TR10's table & setting, exit
13. Other	Real Temperature > TB10	Use TR11's table & setting, finish

***Note:**

(1) TRx's content is defined in "LUT FORMAT IN OTP" section.

Example:

If temperature = -20 ºC, TR0 is selected.

If temperature = -10 ºC, TR1 is selected.

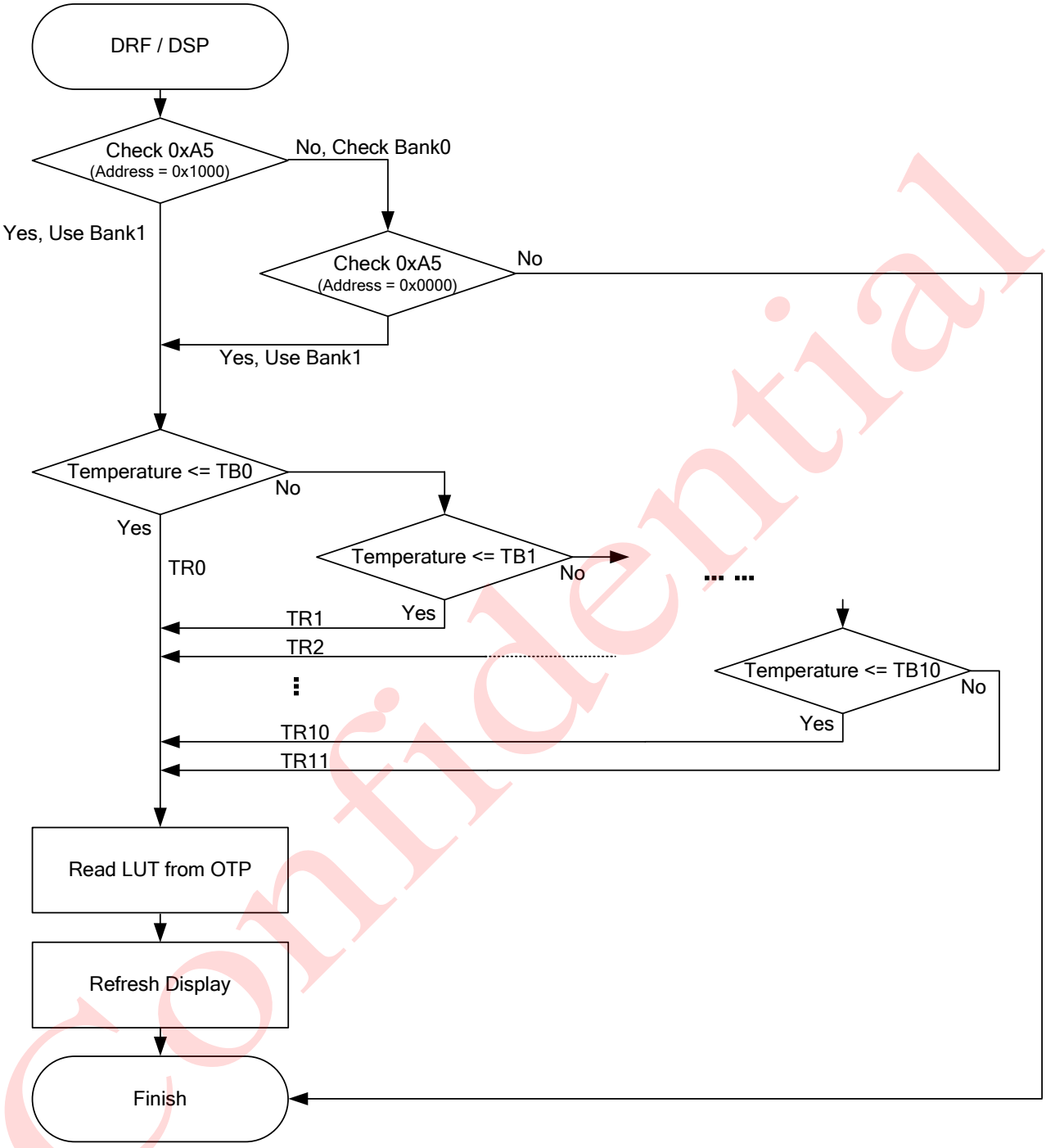
If temperature = 0 ºC, TR2 is selected.

If temperature = 20 ºC, TR4 is selected.

If temperature = 40 ºC, TR5 is selected.

If temperature > 40 ºC, TR5 is selected.

OTP Address	Content	
0002h	0xF1	(-15 ºC)
0003h	0xFB	(-5 ºC)
0004h	0x00	(0 ºC)
0005h	0x0A	(10 ºC)
0006h	0x1E	(30 ºC)
0007h	0x7F	-



Temperature Selection Mechanism

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x0001~0x0013 (or 0x1001~0x1013). The data of address 0x0001 (or 0x1001) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x0001 / 0x1001	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x0002 / 0x1002	#	#	#	#	#	#	--	--	PSR	RES[1:0], REG, KW/R, UD, SHL	0x0F
0x0003 / 0x1003	--	--	#	#	--	--	--	--	PFS	T_VDS_OF[1:0]	0x00
0x0004 / 0x1004	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x0005 / 0x1005	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x0006 / 0x1006	--	--	#	#	#	#	#	#		BT_PHC[5:0]	0x17
0x0007 / 0x1007	#	--	--	--	#	#	#	#	TSE	TSE, TO[3:0]	0x00
0x0008 / 0x1008	#	#	#	#	#	#	#	#	CDI	VBD[1:0], DDX[1:0], CDI[3:0]	0xD7
0x0009 / 0x1009	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x000A / 0x100A	#	#	#	#	#	0	0	0	TRES	HRES[7:3]	0x00
0x000B / 0x100B	--	--	--	--	--	--	--	#		VRES[8:0]	0x00
0x000C / 0x100C	#	#	#	#	#	#	#	#			0x00
0x000D / 0x100D	#	#	#	#	#	0	0	0	GSST	HST[7:3]	0x00
0x000E / 0x100E	--	--	--	--	--	--	--	#		VST[8:0]	0x00
0x000F / 0x100F	#	#	#	#	#	#	#	#			0x00
0x0010 / 0x1010	--	--	--	--	--	--	#	#	CCSET	TSFIX, CCEN	0x00
0x0011 / 0x1011	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x0012 / 0x1012	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03
0x0013 / 0x1013	#	#	#	#	#	#	#	#	TSSET	TS_SET[7:0]	0x00

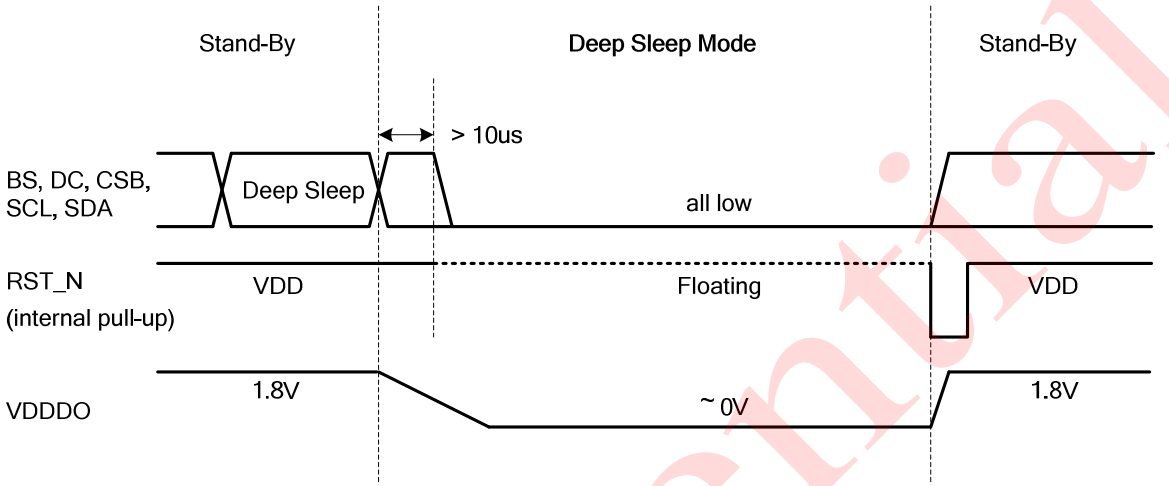
LUT FORMAT IN OTP

There are 12 TRs (temperature range) in a bank. Each TR has independant frame rate, voltage, XON settings and LUTs. The fomat of LUT is different in different mode. In KWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTK in TRs. LUTC & LUTR have 10 states. However LUTW & LUTK has only 7 states. In KW mode, there are 5 LUTs including LUT, LUTWW, LUTKW, LUTWK and LUTKK in TRs. All LUTs have same number of state.

<table>
<tr><td rowspan="2"></td><td colspan="2">KWR Mode (KW/R=0)</td><td colspan="2">KW Mode (KW/R=1)</td></tr>
<tr><td>Address</td><td>Content</td><td>Address</td><td>Content</td></tr>
<tr><td rowspan="19">TR0</td><td>0x0025</td><td>Frame rate[4:0] ,</td><td>0x0025</td><td>Frame rate[4:0] ,</td></tr>
<tr><td>0x0026</td><td>VG Voltgae[3:0]</td><td>0x0026</td><td>VG Voltgae[3:0]</td></tr>
<tr><td>0x0027</td><td>VSH Voltage[5:0]</td><td>0x0027</td><td>VSH Voltage[5:0]</td></tr>
<tr><td>0x0028</td><td>VSL Voltage[5:0]</td><td>0x0028</td><td>VSL Voltage[5:0]</td></tr>
<tr><td>0x0029</td><td>VDHR Voltage[5:0]</td><td>0x0029</td><td>VDHR Voltage[5:0]</td></tr>
<tr><td>0x002A</td><td>VCOM_DC Voltage[6:0]</td><td>0x002A</td><td>VCOM_DC Voltage[6:0]</td></tr>
<tr><td>0x002B</td><td>STATE_XON[7:0]</td><td>0x002B</td><td>STATE_XON[7:0]</td></tr>
<tr><td>0x002C</td><td>STATE_XON[15:8]</td><td>0x002C</td><td>STATE_XON[15:8]</td></tr>
<tr><td>0x002D</td><td>EOPT , ESO ,
STATE_XON[19:16]</td><td>0x002D</td><td>EOPT , ESO ,
STATE_XON[19:16]</td></tr>
<tr><td>0x002E</td><td>KWE[7:0]</td><td rowspan="2">0x002E
~0x002F</td><td rowspan="2">Blank</td></tr>
<tr><td>0x002F</td><td>ATRED , NORED,KWE[9:8]</td></tr>
<tr><td>0x0030
~0x007F</td><td>LUTC
(10 groups)</td><td>0x0030
~0x0067</td><td>LUTC
(7 groups)</td></tr>
<tr><td>0x0080
~0x00CF</td><td>LUTR
(10 groups)</td><td>0x0068
~0x009F</td><td>LUTWW
(7 groups)</td></tr>
<tr><td rowspan="2">0x00D0
~0x0011F</td><td rowspan="2">LUTW
(10 groups)</td><td>0x00A0
~0x0D7</td><td>LUTKW
(7 groups)</td></tr>
<tr><td>0x00D8
~0x010F</td><td>LUTWK
(7 groups)</td></tr>
<tr><td rowspan="2">0x00120
~0x016F</td><td rowspan="2">LUTK
(10 groups)</td><td>0x0110
~0x0147</td><td>LUTKK
(7 groups)</td></tr>
<tr><td>0x0148
~0x016F</td><td>Reserved</td></tr>
</table>

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, UC8251 enter “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

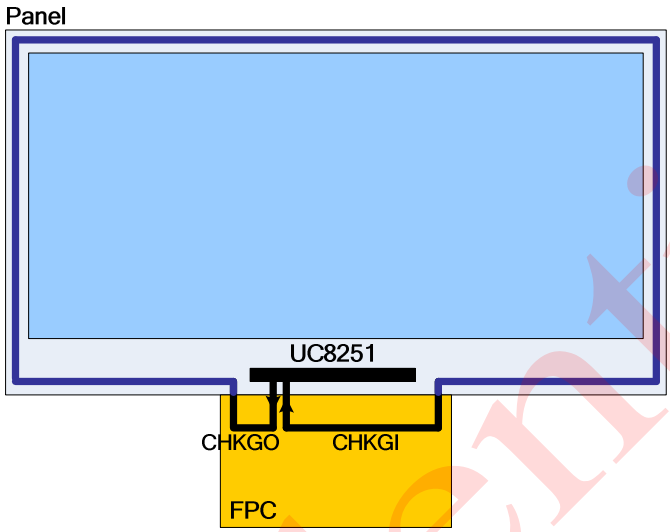


Figure: Panel break check layout example

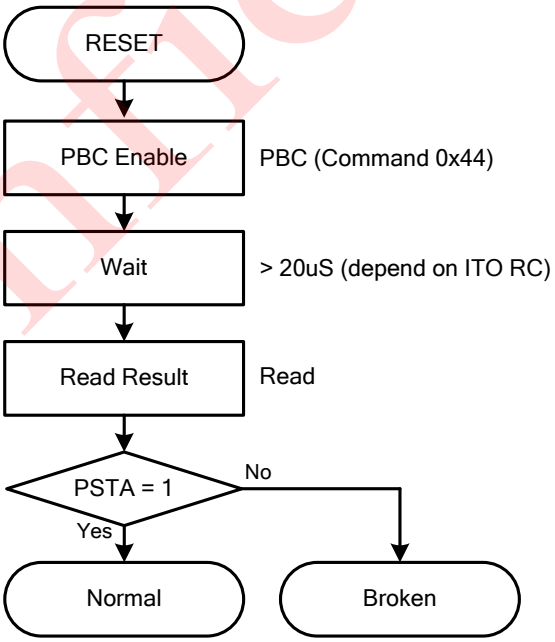
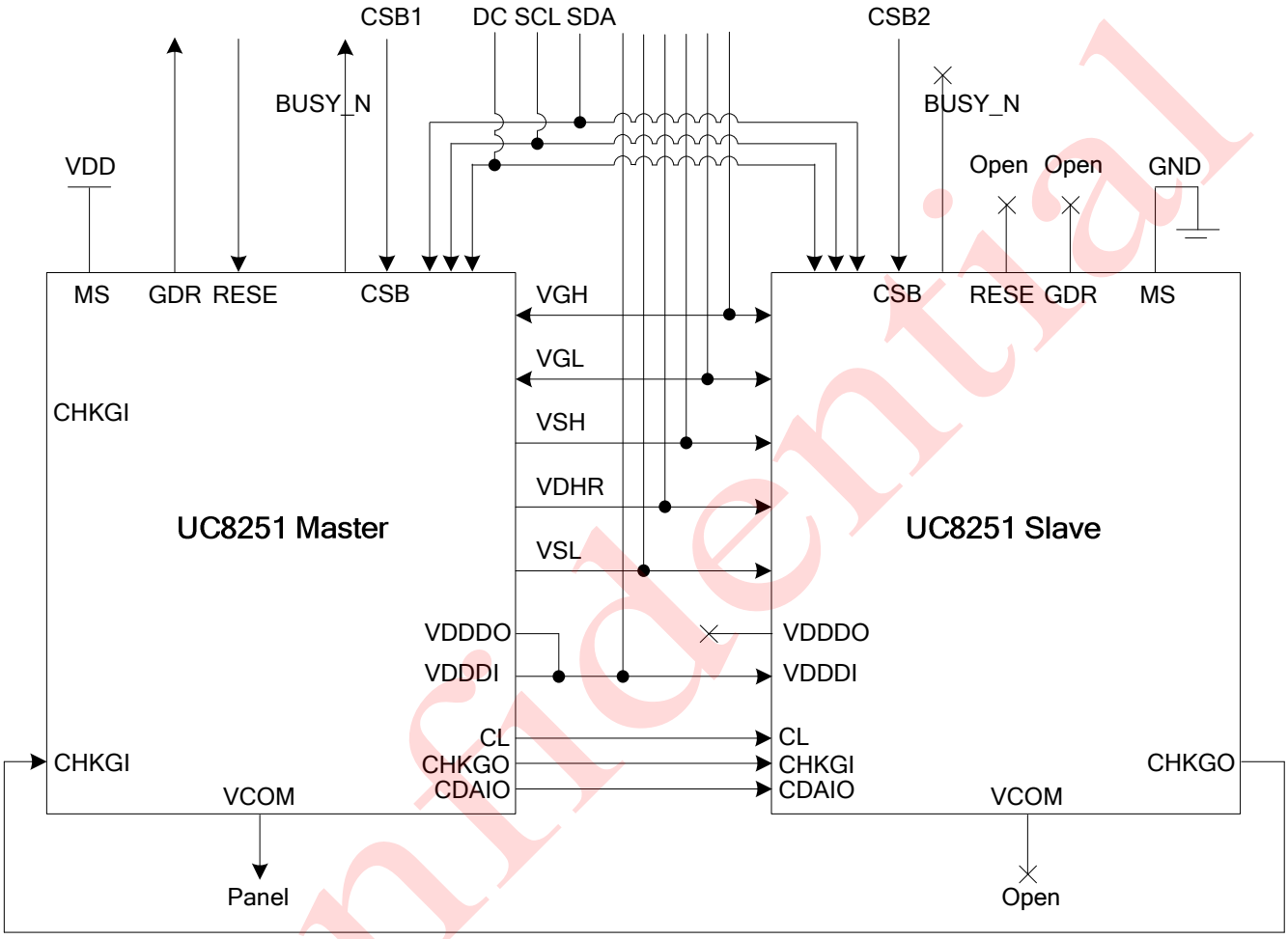


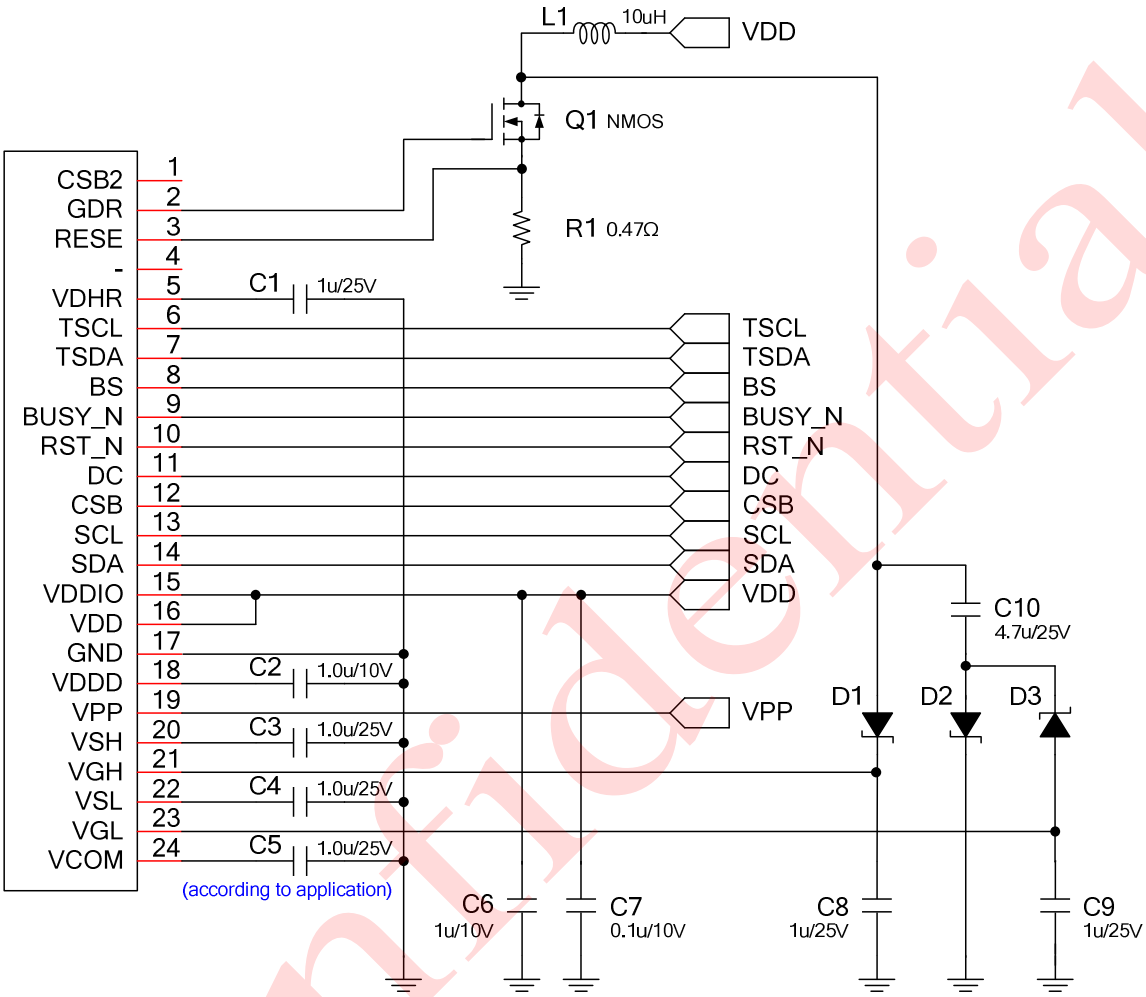
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT



All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.

BOOSTER APPLICATION CIRCUIT



Note:

1. The capacitor value of VGH/VGL must be equal or more than the one of VSH/VSL/VDHR.

Recommended Device

1. Switch MOS NMOS: Vishay Si1308EDL (V_{DS} > 25V, I_D > 500mA, V_{GS}(th) < 1.5V, C_{iss} < 200pF, R_{DS}(on) < 400mΩ)
2. Schottky Diode: OnSemi MBR0530 (V_R > 25V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_a=100°C)

Recommended Resistor

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 10 Ω
Boosters	VGL, VGH, GDR, RESE	< 10 Ω
Regulators	VSH, VSL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, GDR, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
VDD, VDDIO, VDDA	Logic Supply voltage	-0.3	+6.0	V
VPP	OTP programming voltage	-0.3	+8.5	V
VI	Digital input range	-0.3	VDDIO+0.3	V
VGH-VGL	Supply range	-	+42.0	V
Source				
VSH	Analog supply voltage – positive	+16		V
VSL	Analog supply voltage -- negative	-16		V
VDHR	Analog supply voltage – positive	+16		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+22	V
VGL	Analog supply voltage -- negative	-22	0.3	V
TSTG	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VPP	OTP program voltage		8.0	8.25	8.5	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400UA	VDDIO-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400UA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		40	V
dVSH	Supply voltage dev		-200	0	+200	mV
dVSL	Supply voltage dev		-200	0	+200	mV
dVDHR	Supply voltage dev		-200	0	+200	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
RON	Driver Output Resistance	For source driver, TOP=25°C, VOUT = ±15V		16.0	38.4	KΩ
		For gate driver, TOP=25°C, VOUT = ±20V		4.0	8	

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
IVDD	Digital deep sleep current	VDDD OFF	--	0.3	0.5	uA
	Digital stand-by current	All stopped	--	8.2	10.0	uA
	Digital operating current		--	--	0.1	mA
IVDDIO	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
IVDDA	DCDC deep sleep current	VDDD OFF	--	0.1	0.3	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VSH/VSL, Duty=0.5, Period =126us VCOM DC No load	--	--	4.0	mA
		Source output VSH/VSL, Duty=0.5, Period =126us, VCOM DC External cap: 415pF, NMOS=340pF	--	--	20.0	

AC CHARACTERISTICS

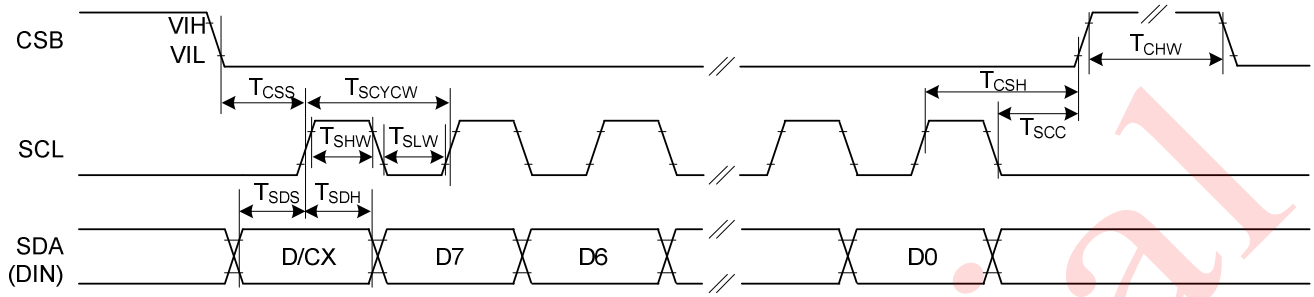


Figure: 3-wire Serial Interface Characteristics (Write mode)

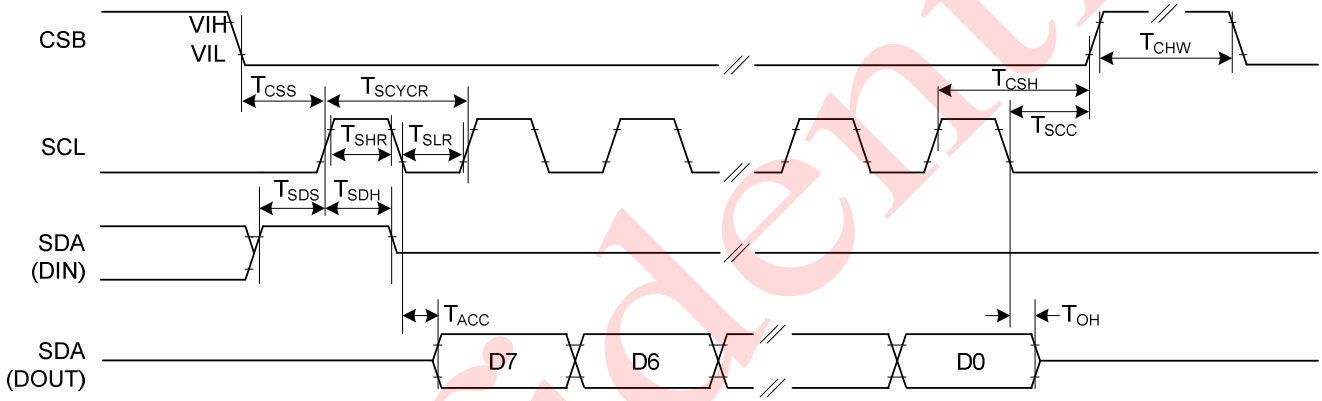


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

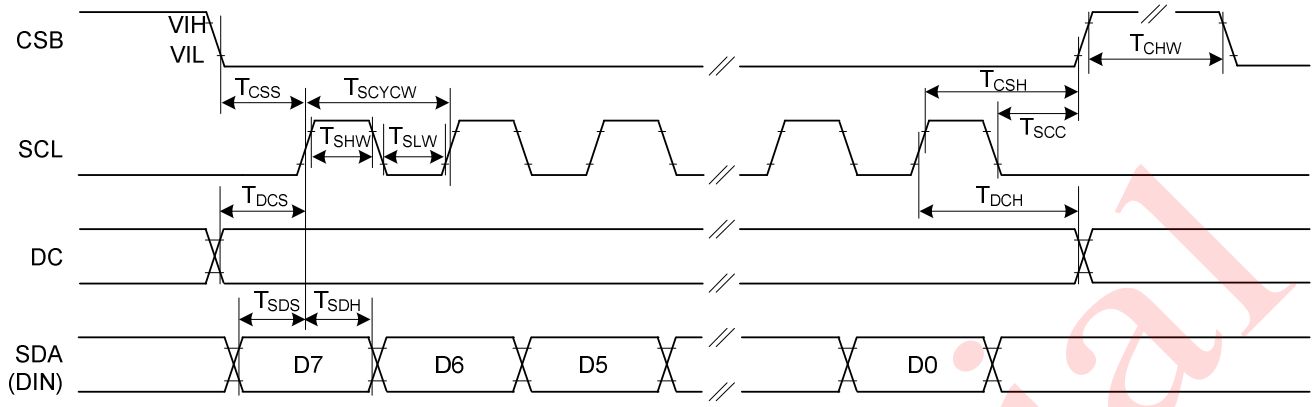


Figure: 4-wire Serial Interface Characteristics (Write mode)

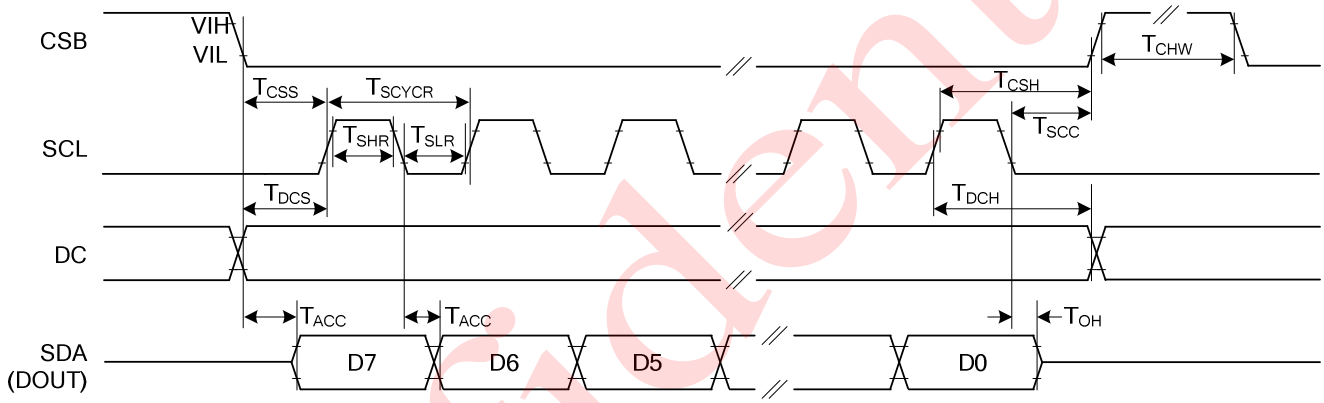
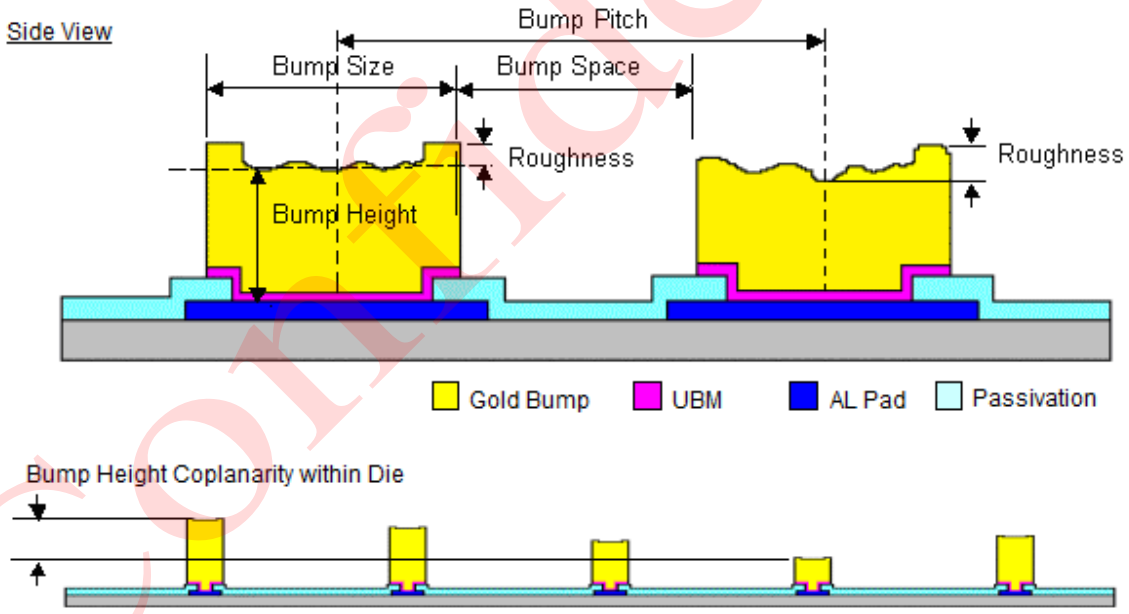


Figure: 4-wire Serial Interface Characteristics (Read mode)

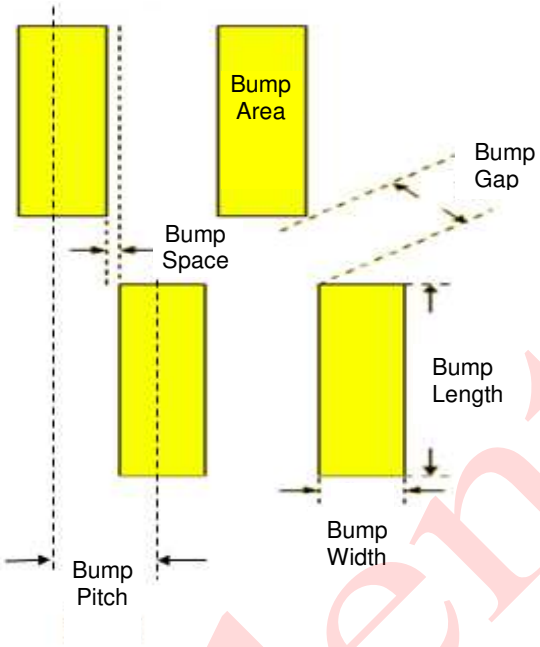
Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

PHYSICAL DIMENSIONS

Die Size:	(9522μM ± 40μM) x (772μM ± 40μM)
Die Thickness:	300 μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ≤ 2μM
Bump Size:	12 μM x 100 μM ± 2μM
Bump Area:	1200 μM^2
Bump Pitch:	13 μM ± 2μM
Bump Space:	1 μM ± 3μM
Hardness:	65 Hv ± 15Hv
Shear:	/ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center

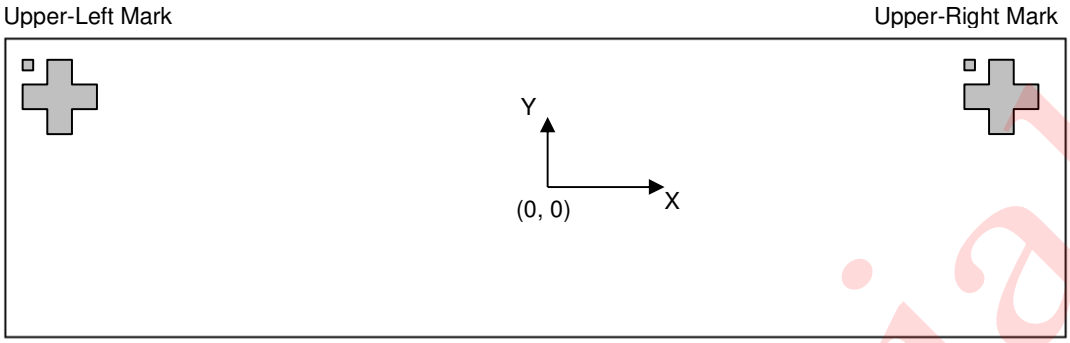


For Stagger Layout

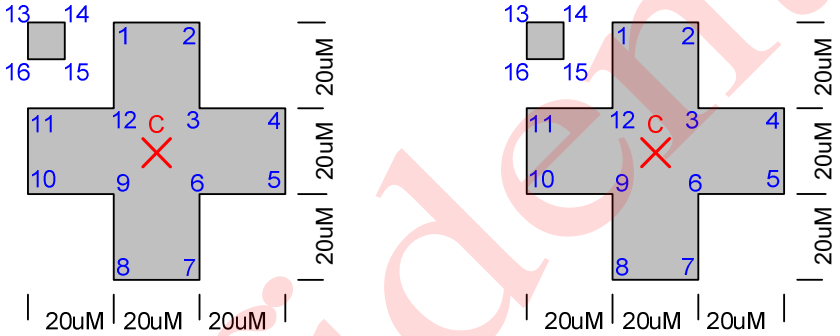


ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
C	-4665	290	4665	290
1	-4675	320	4655	320
2	-4655	320	4675	320
3	-4655	300	4675	300
4	-4635	300	4695	300
5	-4635	280	4695	280
6	-4655	280	4675	280
7	-4655	260	4675	260
8	-4675	260	4655	260
9	-4675	280	4655	280
10	-4695	280	4635	280
11	-4695	300	4635	300
12	-4675	300	4655	300
13	-4695	320	4635	320
14	-4685	320	4645	320
15	-4685	310	4645	310
16	-4695	310	4635	310

PAD COORDINATES

No.	Pad	X	Y	W	H
1	NC<0>	-4646	-298	28	70
2	VCOM	-4600	-298	28	70
3	VCOM	-4554	-298	28	70
4	VCOM	-4508	-298	28	70
5	VCOM	-4462	-298	28	70
6	VCOM	-4416	-298	28	70
7	VCOM	-4370	-298	28	70
8	VCOM	-4324	-298	28	70
9	VCOM	-4278	-298	28	70
10	VDM	-4232	-298	28	70
11	VGL	-4186	-298	28	70
12	VGL	-4140	-298	28	70
13	VGL	-4094	-298	28	70
14	VGL	-4048	-298	28	70
15	VGL	-4002	-298	28	70
16	VGL	-3956	-298	28	70
17	VGL	-3910	-298	28	70
18	VGL	-3864	-298	28	70
19	VGL	-3818	-298	28	70
20	VGL	-3772	-298	28	70
21	VGL	-3726	-298	28	70
22	VGL	-3680	-298	28	70
23	VGL	-3634	-298	28	70
24	VGL	-3588	-298	28	70
25	VGL	-3542	-298	28	70
26	VGL	-3496	-298	28	70
27	GNDA	-3450	-298	28	70
28	VSL	-3404	-298	28	70
29	VSL	-3358	-298	28	70
30	VSL	-3312	-298	28	70
31	VSL	-3266	-298	28	70
32	VSL	-3220	-298	28	70
33	VSL	-3174	-298	28	70
34	VSL	-3128	-298	28	70
35	VSL	-3082	-298	28	70
36	VSL	-3036	-298	28	70
37	VSL	-2990	-298	28	70
38	GNDA	-2944	-298	28	70
39	VGH	-2898	-298	28	70
40	VGH	-2852	-298	28	70
41	VGH	-2806	-298	28	70
42	VGH	-2760	-298	28	70
43	VGH	-2714	-298	28	70
44	VGH	-2668	-298	28	70
45	VGH	-2622	-298	28	70
46	VGH	-2576	-298	28	70
47	VGH	-2530	-298	28	70
48	VGH	-2484	-298	28	70
49	VGH	-2438	-298	28	70
50	VGH	-2392	-298	28	70
51	GNDA	-2346	-298	28	70
52	VSH	-2300	-298	28	70
53	VSH	-2254	-298	28	70
54	VSH	-2208	-298	28	70
55	VSH	-2162	-298	28	70
56	VSH	-2116	-298	28	70

No.	Pad	X	Y	W	H
57	VSH	-2070	-298	28	70
58	VSH	-2024	-298	28	70
59	VSH	-1978	-298	28	70
60	VSH	-1932	-298	28	70
61	VSH	-1886	-298	28	70
62	GNDA	-1840	-298	28	70
63	VPP	-1794	-298	28	70
64	VPP	-1748	-298	28	70
65	VPP	-1702	-298	28	70
66	VPP	-1656	-298	28	70
67	VPP	-1610	-298	28	70
68	VPP	-1564	-298	28	70
69	VDDDI	-1518	-298	28	70
70	VDDDI	-1472	-298	28	70
71	VDDDI	-1426	-298	28	70
72	VDDDI	-1380	-298	28	70
73	VDDDO	-1334	-298	28	70
74	VDDDO	-1288	-298	28	70
75	VDDDO	-1242	-298	28	70
76	VDDDO	-1196	-298	28	70
77	VDM	-1150	-298	28	70
78	VDM	-1104	-298	28	70
79	GNDA	-1058	-298	28	70
80	GNDA	-1012	-298	28	70
81	GNDA	-966	-298	28	70
82	GNDA	-920	-298	28	70
83	GNDA	-874	-298	28	70
84	GNDA	-828	-298	28	70
85	GNDA	-782	-298	28	70
86	GNDA	-736	-298	28	70
87	GNDA	-690	-298	28	70
88	GNDA	-644	-298	28	70
89	GND	-598	-298	28	70
90	GND	-552	-298	28	70
91	GND	-506	-298	28	70
92	GND	-460	-298	28	70
93	GND	-414	-298	28	70
94	GND	-368	-298	28	70
95	GND	-322	-298	28	70
96	GND	-276	-298	28	70
97	GND	-230	-298	28	70
98	GND	-184	-298	28	70
99	GND	-138	-298	28	70
100	GND	-92	-298	28	70
101	VDDA	-46	-298	28	70
102	VDDA	0	-298	28	70
103	VDDA	46	-298	28	70
104	VDDA	92	-298	28	70
105	VDDA	138	-298	28	70
106	VDDA	184	-298	28	70
107	VDDA	230	-298	28	70
108	VDDA	276	-298	28	70
109	VDDA	322	-298	28	70
110	VDDA	368	-298	28	70
111	VDD	414	-298	28	70
112	VDD	460	-298	28	70

No.	Pad	X	Y	W	H
113	VDD	506	-298	28	70
114	VDD	552	-298	28	70
115	VDD	598	-298	28	70
116	VDD	644	-298	28	70
117	VDD	690	-298	28	70
118	TEST1	736	-298	28	70
119	TEST2	782	-298	28	70
120	VDDIO	828	-298	28	70
121	VDDIO	874	-298	28	70
122	VDDIO	920	-298	28	70
123	VDDIO	966	-298	28	70
124	TEST3	1012	-298	28	70
125	DUMMY<0>	1058	-298	28	70
126	DUMMY<1>	1104	-298	28	70
127	DUMMY<2>	1150	-298	28	70
128	DUMMY<3>	1196	-298	28	70
129	DUMMY<4>	1242	-298	28	70
130	SDA	1288	-298	28	70
131	SCL	1334	-298	28	70
132	GND	1380	-298	28	70
133	CSB	1426	-298	28	70
134	VDDIO	1472	-298	28	70
135	DUMMY<5>	1518	-298	28	70
136	GND	1564	-298	28	70
137	DC	1610	-298	28	70
138	VDDIO	1656	-298	28	70
139	DUMMY<6>	1702	-298	28	70
140	GND	1748	-298	28	70
141	RST_N	1794	-298	28	70
142	BUSY_N	1840	-298	28	70
143	CL	1886	-298	28	70
144	VDDIO	1932	-298	28	70
145	VSYNC	1978	-298	28	70
146	GND	2024	-298	28	70
147	DUMMY<7>	2070	-298	28	70
148	VDDIO	2116	-298	28	70
149	BS	2162	-298	28	70
150	GND	2208	-298	28	70
151	DUMMY<8>	2254	-298	28	70
152	VDDIO	2300	-298	28	70
153	CHKGI	2346	-298	28	70
154	GND	2392	-298	28	70
155	MS	2438	-298	28	70
156	VDDIO	2484	-298	28	70
157	TSDA	2530	-298	28	70
158	TSDA	2576	-298	28	70
159	TSCL	2622	-298	28	70
160	TSCL	2668	-298	28	70
161	CHKGO	2714	-298	28	70
162	CDAIO	2760	-298	28	70
163	TEST6	2806	-298	28	70
164	TEST7	2852	-298	28	70
165	VDHR	2898	-298	28	70
166	VDHR	2944	-298	28	70
167	VDHR	2990	-298	28	70
168	VDHR	3036	-298	28	70
169	VDHR	3082	-298	28	70
170	VDHR	3128	-298	28	70
171	VDHR	3174	-298	28	70

No.	Pad	X	Y	W	H
172	VDHR	3220	-298	28	70
173	DUMMY<9>	3266	-298	28	70
174	DUMMY<10>	3312	-298	28	70
175	DUMMY<11>	3358	-298	28	70
176	DUMMY<12>	3404	-298	28	70
177	DUMMY<13>	3450	-298	28	70
178	DUMMY<14>	3496	-298	28	70
179	GNDA	3542	-298	28	70
180	FB	3588	-298	28	70
181	FB	3634	-298	28	70
182	GNDA	3680	-298	28	70
183	RESE	3726	-298	28	70
184	RESE	3772	-298	28	70
185	GNDA	3818	-298	28	70
186	GDR	3864	-298	28	70
187	GDR	3910	-298	28	70
188	GDR	3956	-298	28	70
189	GDR	4002	-298	28	70
190	GDR	4048	-298	28	70
191	GDR	4094	-298	28	70
192	GDR	4140	-298	28	70
193	GDR	4186	-298	28	70
194	VDM	4232	-298	28	70
195	VCOM	4278	-298	28	70
196	VCOM	4324	-298	28	70
197	VCOM	4370	-298	28	70
198	VCOM	4416	-298	28	70
199	VCOM	4462	-298	28	70
200	VCOM	4508	-298	28	70
201	VCOM	4554	-298	28	70
202	VCOM	4600	-298	28	70
203	NC<1>	4646	-298	28	70
204	NC<2>	4643	137	75	18
205	NC<3>	4643	179	75	18
206	NC<4>	4540	213.5	18	75
207	NC<5>	4519	313.5	18	75
208	NC<6>	4498	213.5	18	75
209	NC<7>	4477	313.5	18	75
210	NC<8>	4456	213.5	18	75
211	NC<9>	4435	313.5	18	75
212	G<0>	4414	213.5	18	75
213	G<2>	4393	313.5	18	75
214	G<4>	4372	213.5	18	75
215	G<6>	4351	313.5	18	75
216	G<8>	4330	213.5	18	75
217	G<10>	4309	313.5	18	75
218	G<12>	4288	213.5	18	75
219	G<14>	4267	313.5	18	75
220	G<16>	4246	213.5	18	75
221	G<18>	4225	313.5	18	75
222	G<20>	4204	213.5	18	75
223	G<22>	4183	313.5	18	75
224	G<24>	4162	213.5	18	75
225	G<26>	4141	313.5	18	75
226	G<28>	4120	213.5	18	75
227	G<30>	4099	313.5	18	75
228	G<32>	4078	213.5	18	75
229	G<34>	4057	313.5	18	75
230	G<36>	4036	213.5	18	75

No.	Pad	X	Y	W	H
231	G<38>	4015	313.5	18	75
232	G<40>	3994	213.5	18	75
233	G<42>	3973	313.5	18	75
234	G<44>	3952	213.5	18	75
235	G<46>	3931	313.5	18	75
236	G<48>	3910	213.5	18	75
237	G<50>	3889	313.5	18	75
238	G<52>	3868	213.5	18	75
239	G<54>	3847	313.5	18	75
240	G<56>	3826	213.5	18	75
241	G<58>	3805	313.5	18	75
242	G<60>	3784	213.5	18	75
243	G<62>	3763	313.5	18	75
244	G<64>	3742	213.5	18	75
245	G<66>	3721	313.5	18	75
246	G<68>	3700	213.5	18	75
247	G<70>	3679	313.5	18	75
248	G<72>	3658	213.5	18	75
249	G<74>	3637	313.5	18	75
250	G<76>	3616	213.5	18	75
251	G<78>	3595	313.5	18	75
252	G<80>	3574	213.5	18	75
253	G<82>	3553	313.5	18	75
254	G<84>	3532	213.5	18	75
255	G<86>	3511	313.5	18	75
256	G<88>	3490	213.5	18	75
257	G<90>	3469	313.5	18	75
258	G<92>	3448	213.5	18	75
259	G<94>	3427	313.5	18	75
260	G<96>	3406	213.5	18	75
261	G<98>	3385	313.5	18	75
262	G<100>	3364	213.5	18	75
263	G<102>	3343	313.5	18	75
264	G<104>	3322	213.5	18	75
265	G<106>	3301	313.5	18	75
266	G<108>	3280	213.5	18	75
267	G<110>	3259	313.5	18	75
268	G<112>	3238	213.5	18	75
269	G<114>	3217	313.5	18	75
270	G<116>	3196	213.5	18	75
271	G<118>	3175	313.5	18	75
272	G<120>	3154	213.5	18	75
273	G<122>	3133	313.5	18	75
274	G<124>	3112	213.5	18	75
275	G<126>	3091	313.5	18	75
276	G<128>	3070	213.5	18	75
277	G<130>	3049	313.5	18	75
278	G<132>	3028	213.5	18	75
279	G<134>	3007	313.5	18	75
280	G<136>	2986	213.5	18	75
281	G<138>	2965	313.5	18	75
282	G<140>	2944	213.5	18	75
283	G<142>	2923	313.5	18	75
284	G<144>	2902	213.5	18	75
285	G<146>	2881	313.5	18	75
286	G<148>	2860	213.5	18	75
287	G<150>	2839	313.5	18	75
288	G<152>	2818	213.5	18	75
289	G<154>	2797	313.5	18	75

No.	Pad	X	Y	W	H
290	G<156>	2776	213.5	18	75
291	G<158>	2755	313.5	18	75
292	G<160>	2734	213.5	18	75
293	G<162>	2713	313.5	18	75
294	G<164>	2692	213.5	18	75
295	G<166>	2671	313.5	18	75
296	G<168>	2650	213.5	18	75
297	G<170>	2629	313.5	18	75
298	G<172>	2608	213.5	18	75
299	G<174>	2587	313.5	18	75
300	G<176>	2566	213.5	18	75
301	G<178>	2545	313.5	18	75
302	G<180>	2524	213.5	18	75
303	G<182>	2503	313.5	18	75
304	G<184>	2482	213.5	18	75
305	G<186>	2461	313.5	18	75
306	G<188>	2440	213.5	18	75
307	G<190>	2419	313.5	18	75
308	G<192>	2398	213.5	18	75
309	G<194>	2377	313.5	18	75
310	G<196>	2356	213.5	18	75
311	G<198>	2335	313.5	18	75
312	G<200>	2314	213.5	18	75
313	G<202>	2293	313.5	18	75
314	G<204>	2272	213.5	18	75
315	G<206>	2251	313.5	18	75
316	G<208>	2230	213.5	18	75
317	G<210>	2209	313.5	18	75
318	G<212>	2188	213.5	18	75
319	G<214>	2167	313.5	18	75
320	G<216>	2146	213.5	18	75
321	G<218>	2125	313.5	18	75
322	G<220>	2104	213.5	18	75
323	G<222>	2083	313.5	18	75
324	G<224>	2062	213.5	18	75
325	G<226>	2041	313.5	18	75
326	G<228>	2020	213.5	18	75
327	G<230>	1999	313.5	18	75
328	G<232>	1978	213.5	18	75
329	G<234>	1957	313.5	18	75
330	G<236>	1936	213.5	18	75
331	G<238>	1915	313.5	18	75
332	G<240>	1894	213.5	18	75
333	G<242>	1873	313.5	18	75
334	G<244>	1852	213.5	18	75
335	G<246>	1831	313.5	18	75
336	G<248>	1810	213.5	18	75
337	G<250>	1789	313.5	18	75
338	G<252>	1768	213.5	18	75
339	G<254>	1747	313.5	18	75
340	G<256>	1726	213.5	18	75
341	G<258>	1705	313.5	18	75
342	G<260>	1684	213.5	18	75
343	G<262>	1663	313.5	18	75
344	G<264>	1642	213.5	18	75
345	G<266>	1621	313.5	18	75
346	G<268>	1600	213.5	18	75
347	G<270>	1579	313.5	18	75
348	G<272>	1558	213.5	18	75

No.	Pad	X	Y	W	H
349	G<274>	1537	313.5	18	75
350	G<276>	1516	213.5	18	75
351	G<278>	1495	313.5	18	75
352	G<280>	1474	213.5	18	75
353	G<282>	1453	313.5	18	75
354	G<284>	1432	213.5	18	75
355	G<286>	1411	313.5	18	75
356	G<288>	1390	213.5	18	75
357	G<290>	1369	313.5	18	75
358	G<292>	1348	213.5	18	75
359	G<294>	1327	313.5	18	75
360	NC<10>	1306	213.5	18	75
361	NC<11>	1285	313.5	18	75
362	VBD<3>	1176.5	320	12	100
363	S<0>	1150.5	320	12	100
364	S<1>	1137.5	201	12	100
365	S<2>	1124.5	320	12	100
366	S<3>	1111.5	201	12	100
367	S<4>	1098.5	320	12	100
368	S<5>	1085.5	201	12	100
369	S<6>	1072.5	320	12	100
370	S<7>	1059.5	201	12	100
371	VBD<1>	1046.5	320	12	100
372	S<8>	1033.5	201	12	100
373	S<9>	1020.5	320	12	100
374	S<10>	1007.5	201	12	100
375	S<11>	994.5	320	12	100
376	S<12>	981.5	201	12	100
377	S<13>	968.5	320	12	100
378	S<14>	955.5	201	12	100
379	S<15>	942.5	320	12	100
380	S<16>	929.5	201	12	100
381	S<17>	916.5	320	12	100
382	S<18>	903.5	201	12	100
383	S<19>	890.5	320	12	100
384	S<20>	877.5	201	12	100
385	S<21>	864.5	320	12	100
386	S<22>	851.5	201	12	100
387	S<23>	838.5	320	12	100
388	S<24>	825.5	201	12	100
389	S<25>	812.5	320	12	100
390	S<26>	799.5	201	12	100
391	S<27>	786.5	320	12	100
392	S<28>	773.5	201	12	100
393	S<29>	760.5	320	12	100
394	S<30>	747.5	201	12	100
395	S<31>	734.5	320	12	100
396	S<32>	721.5	201	12	100
397	S<33>	708.5	320	12	100
398	S<34>	695.5	201	12	100
399	S<35>	682.5	320	12	100
400	S<36>	669.5	201	12	100
401	S<37>	656.5	320	12	100
402	S<38>	643.5	201	12	100
403	S<39>	630.5	320	12	100
404	S<40>	617.5	201	12	100
405	S<41>	604.5	320	12	100
406	S<42>	591.5	201	12	100
407	S<43>	578.5	320	12	100

No.	Pad	X	Y	W	H
408	S<44>	565.5	201	12	100
409	S<45>	552.5	320	12	100
410	S<46>	539.5	201	12	100
411	S<47>	526.5	320	12	100
412	S<48>	513.5	201	12	100
413	S<49>	500.5	320	12	100
414	S<50>	487.5	201	12	100
415	S<51>	474.5	320	12	100
416	S<52>	461.5	201	12	100
417	S<53>	448.5	320	12	100
418	S<54>	435.5	201	12	100
419	S<55>	422.5	320	12	100
420	S<56>	409.5	201	12	100
421	S<57>	396.5	320	12	100
422	S<58>	383.5	201	12	100
423	S<59>	370.5	320	12	100
424	S<60>	357.5	201	12	100
425	S<61>	344.5	320	12	100
426	S<62>	331.5	201	12	100
427	S<63>	318.5	320	12	100
428	S<64>	305.5	201	12	100
429	S<65>	292.5	320	12	100
430	S<66>	279.5	201	12	100
431	S<67>	266.5	320	12	100
432	S<68>	253.5	201	12	100
433	S<69>	240.5	320	12	100
434	S<70>	227.5	201	12	100
435	S<71>	214.5	320	12	100
436	S<72>	201.5	201	12	100
437	S<73>	188.5	320	12	100
438	S<74>	175.5	201	12	100
439	S<75>	162.5	320	12	100
440	S<76>	149.5	201	12	100
441	S<77>	136.5	320	12	100
442	S<78>	123.5	201	12	100
443	S<79>	110.5	320	12	100
444	S<80>	97.5	201	12	100
445	S<81>	84.5	320	12	100
446	S<82>	71.5	201	12	100
447	S<83>	58.5	320	12	100
448	S<84>	45.5	201	12	100
449	S<85>	32.5	320	12	100
450	S<86>	19.5	201	12	100
451	S<87>	6.5	320	12	100
452	S<88>	-6.5	201	12	100
453	S<89>	-19.5	320	12	100
454	S<90>	-32.5	201	12	100
455	S<91>	-45.5	320	12	100
456	S<92>	-58.5	201	12	100
457	S<93>	-71.5	320	12	100
458	S<94>	-84.5	201	12	100
459	S<95>	-97.5	320	12	100
460	S<96>	-110.5	201	12	100
461	S<97>	-123.5	320	12	100
462	S<98>	-136.5	201	12	100
463	S<99>	-149.5	320	12	100
464	S<100>	-162.5	201	12	100
465	S<101>	-175.5	320	12	100
466	S<102>	-188.5	201	12	100

No.	Pad	X	Y	W	H
467	S<103>	-201.5	320	12	100
468	S<104>	-214.5	201	12	100
469	S<105>	-227.5	320	12	100
470	S<106>	-240.5	201	12	100
471	S<107>	-253.5	320	12	100
472	S<108>	-266.5	201	12	100
473	S<109>	-279.5	320	12	100
474	S<110>	-292.5	201	12	100
475	S<111>	-305.5	320	12	100
476	S<112>	-318.5	201	12	100
477	S<113>	-331.5	320	12	100
478	S<114>	-344.5	201	12	100
479	S<115>	-357.5	320	12	100
480	S<116>	-370.5	201	12	100
481	S<117>	-383.5	320	12	100
482	S<118>	-396.5	201	12	100
483	S<119>	-409.5	320	12	100
484	S<120>	-422.5	201	12	100
485	S<121>	-435.5	320	12	100
486	S<122>	-448.5	201	12	100
487	S<123>	-461.5	320	12	100
488	S<124>	-474.5	201	12	100
489	S<125>	-487.5	320	12	100
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No.	Pad	X	Y	W	H
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538	S<173>	-1124.5	201	12	100
539	S<174>	-1137.5	320	12	100
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574	G<235>	-1957	213.5	18	75
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576	G<231>	-1999	213.5	18	75
577	G<229>	-2020	313.5	18	75
578	G<227>	-2041	213.5	18	75
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No.	Pad	X	Y	W	H
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605	G<173>	-2608	313.5	18	75
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607	G<169>	-2650	313.5	18	75
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614	G<155>	-2797	213.5	18	75
615	G<153>	-2818	313.5	18	75
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617	G<149>	-2860	313.5	18	75
618	G<147>	-2881	213.5	18	75
619	G<145>	-2902	313.5	18	75
620	G<143>	-2923	213.5	18	75
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622	G<139>	-2965	213.5	18	75
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624	G<135>	-3007	213.5	18	75
625	G<133>	-3028	313.5	18	75
626	G<131>	-3049	213.5	18	75
627	G<129>	-3070	313.5	18	75
628	G<127>	-3091	213.5	18	75
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634	G<115>	-3217	213.5	18	75
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No.	Pad	X	Y	W	H
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646	G<91>	-3469	213.5	18	75
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670	G<43>	-3973	213.5	18	75
671	G<41>	-3994	313.5	18	75
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676	G<31>	-4099	213.5	18	75
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679	G<25>	-4162	313.5	18	75
680	G<23>	-4183	213.5	18	75
681	G<21>	-4204	313.5	18	75
682	G<19>	-4225	213.5	18	75
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693	NC<15>	-4456	313.5	18	75
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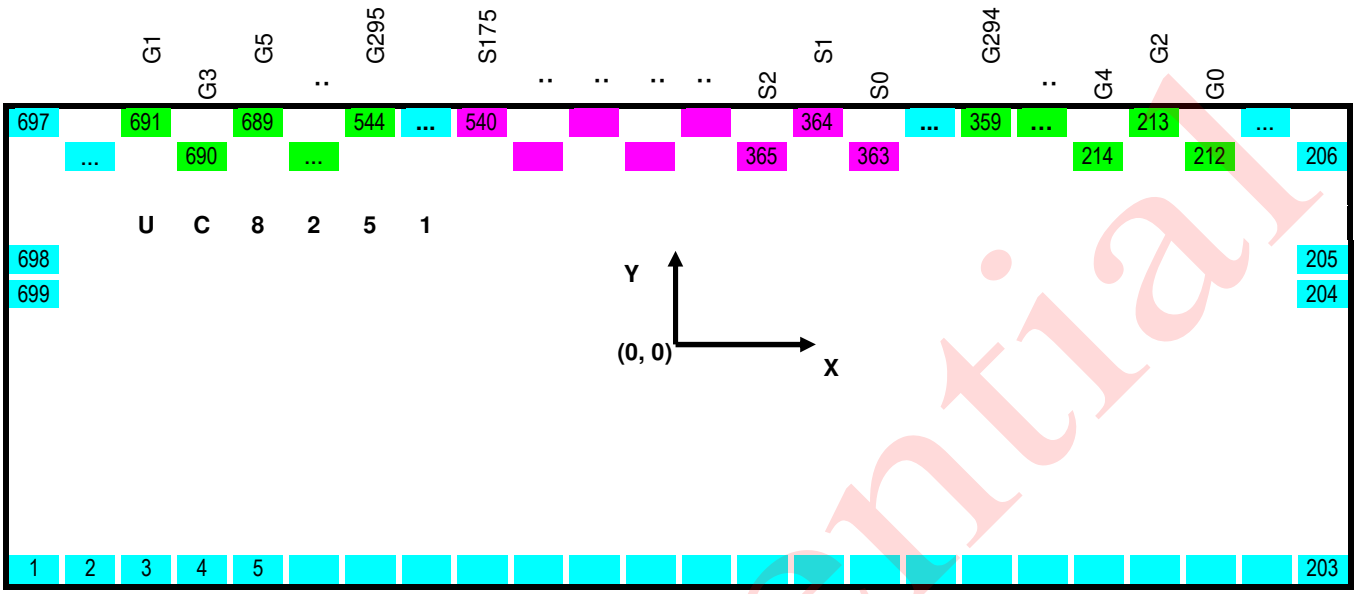
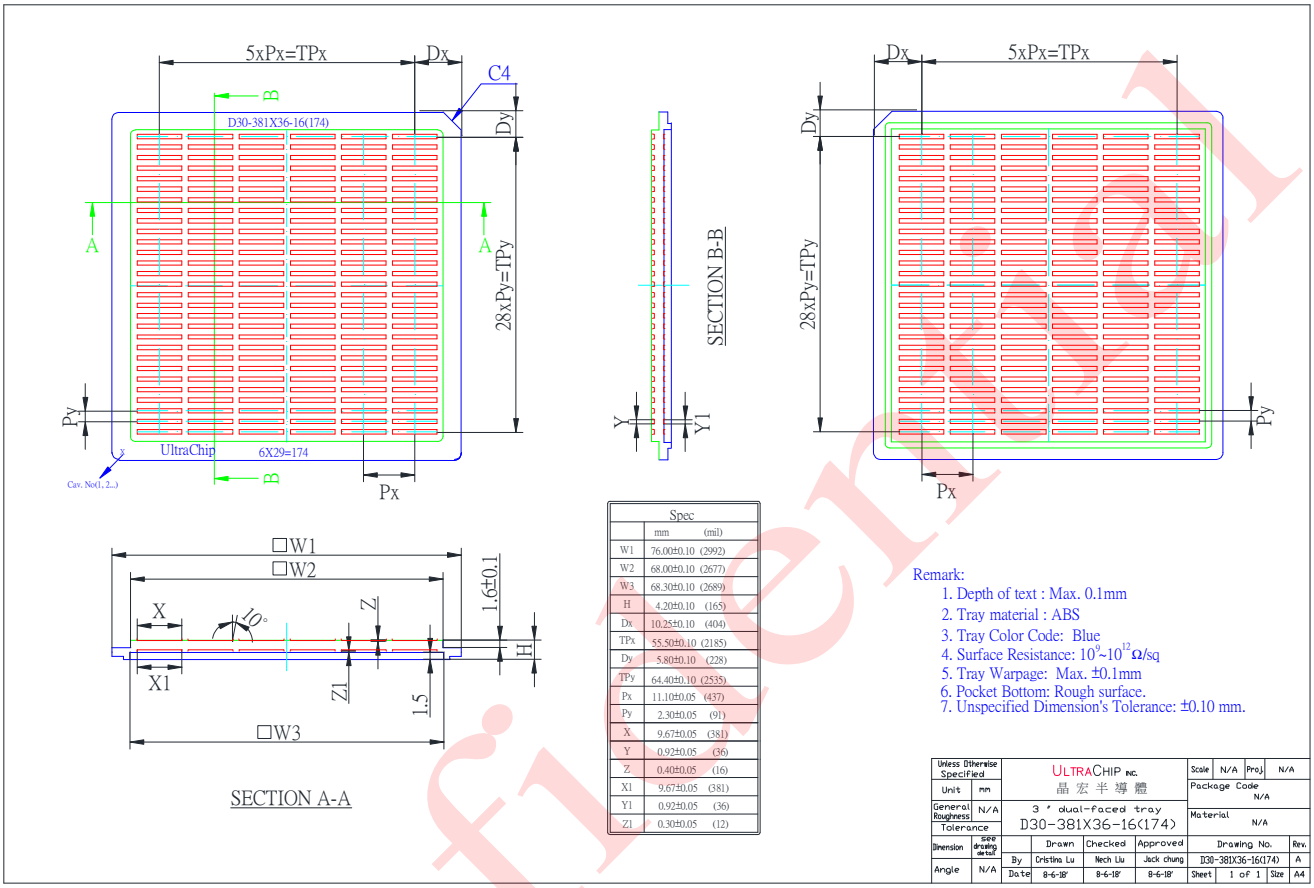
Output Pad Location



TRAY INFORMATION

3-inch Tray



Spec	mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
H	4.20±0.10	(165)
Dx	10.25±0.10	(404)
TPx	55.50±0.10	(2185)
Dy	5.80±0.10	(228)
TPy	64.40±0.10	(2535)
Px	11.10±0.05	(437)
Py	2.30±0.05	(91)
X	9.67±0.05	(381)
Y	0.92±0.05	(36)
Z	0.40±0.05	(16)
X1	9.67±0.05	(381)
Y1	0.92±0.05	(36)
Z1	0.30±0.05	(12)

Unless Otherwise Specified			Drawn	Checked	Approved	Drawing No.	Rev.
Unit	mm	By	Cristina Lu	Nech Lu	Jack chung	D30-381X36-16(174)	A
General Roughness Tolerance	N/A	Date	8-6-18'	8-6-18'	8-6-18'	Sheet 1 of 1	Size A4
Dimension	See drawing detail						
Angle	N/A						

Scale	N/A
Proj.	N/A
Package Code	N/A
Material	N/A

REVISION HISTORY

Revision	Contents	Date
0.1	First release	Nov.22 , 2019