HIGH-VOLTAGE MIXED-SIGNAL IC

UC8159

All-in-one driver IC w/ Timing Controller for
Color Application

Preliminary Specifications
Datasheet Revision: 0.5 (for EIH only)

IC Version: c_B
July 7, 2016

ULTRACHIP

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UC8159

All-in-one driver IC with Timing Controller for Color Application

INTRODUCTION

The UC8159 is an all-in-one gate source driver with an integrated timing controller for ESL application. The source is capable of 3-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and gate drivers.

The integrated DC-DC converter generates all the necessary source and gate output voltages for VSH_LV/VSL_LV (+/-3V ~ +/-15V), VSH/VSL(+/-15V) and VGH/VGL (+/-17V ~ +/-20V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

MAIN APPLICATIONS

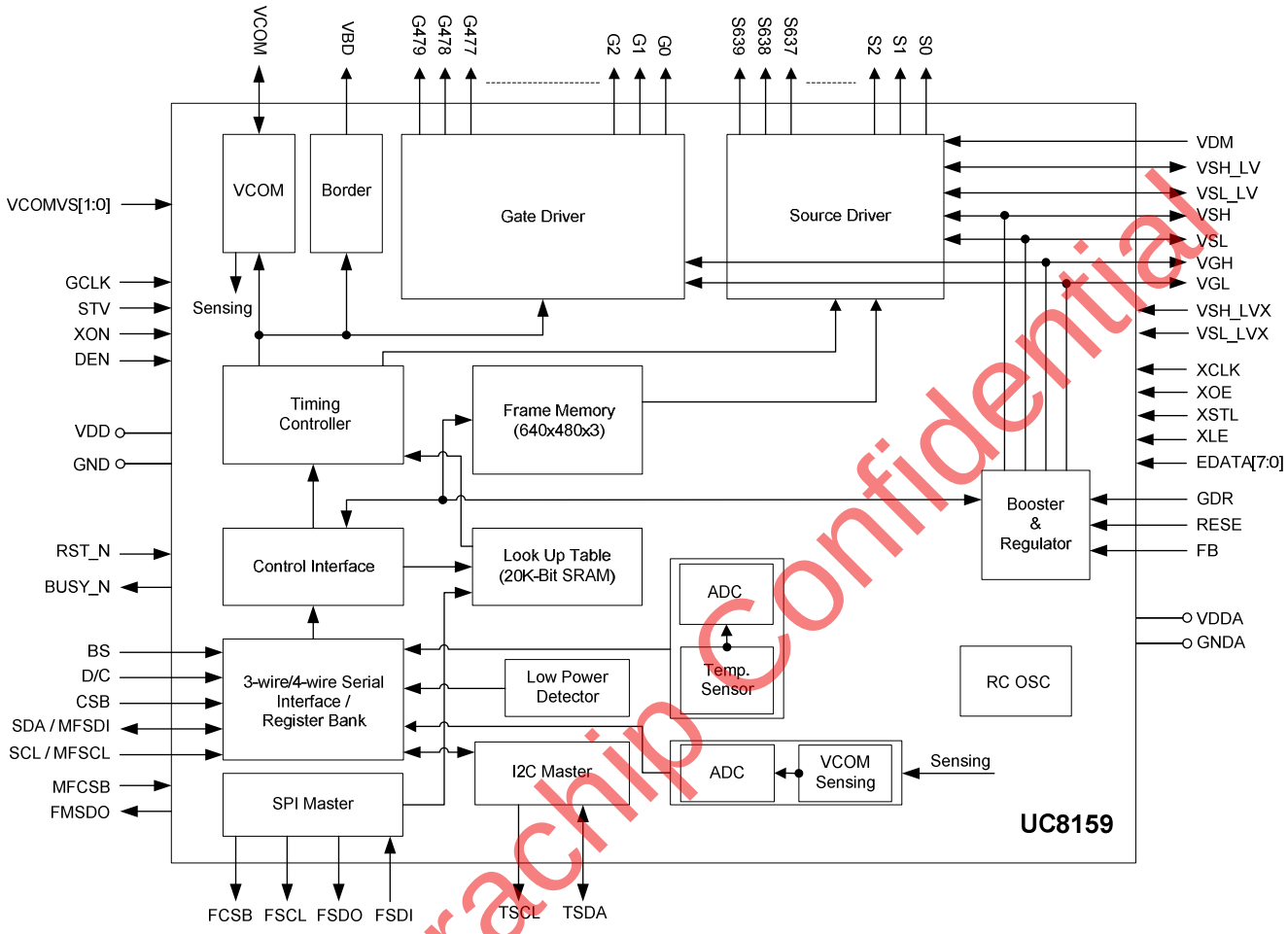
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL, including:
- Timing controller support of several resolutions
- Preselect res (640x480, 600x450, 640x448, 600x448)
- Built in Frame memory maximum (640x480x3bit)
- Support LUT (VCOM, LUT0~LUT7, XON)
- 640 outputs source driver with 3-bit white/black/red resolution
  - Output dynamic voltage : VSH, VSH_LV, VSH_LVX, 0, VSL_LVX, VSL_LV, VSL
  - Output deviation: 0.2V
  - 640 channels outputs
  - Left and Right shift capability
- 480 outputs gate driver:
  - 480 channels outputs
  - Up and Down shift capability
  - Output voltage VDNG+40
- 3-wire/4-wire (SPI) serial interface for system configuration
- DC-DC controller for generating the analog power supply
- Common electrode (VCOM AC or VCOM DC) level
- External SPI flash/EEPROM for WF
- Built-in temperature sensor
- Support I^2C interface for external temperature sensor
- Support low power detection
- Digital supply voltage: 2.3~ 3.6V
- Support frame rate: 200 Hz (max)
- Support pure source & gate driver function
- COG Package

Remark: Contact UltraChip for a visual inspection document (03-DOC-093).

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	I²C	Description
UC8159cGAB-M0P1-4	No	with 4” Tray, Wafer Thickness: 180uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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PIN DESCRIPTION

Type: C: Capacitor pin, I: Input, I/O: Input/Output, M: Mark, O: Output,
PWR: Power, PI: Power Input, PO: Power Output, PS: Power Setting, S: Shorted line

Pin (Pad) Name	Pin Count	Type	Description
SERIAL INTERFACE			
CSB	1	I, Type2	Serial communication chip select.
SDA / MFSDI*	1	I/O, Type5	Serial communication data input. It would bypass to MFSDI by R65H command.
SCL / MFSCL*	1	I, Type2	Serial communication clock input. It would bypass to MFSCL by R65H command.
D/C (DC)	1	I, Type2	Serial communication command/parameter input. L: command H: parameter
FMSDO*	1	O, Type1	Serial communication data output. It would bypass to FMSDO by R65H command.
MFCSB*	1	I, Type2	Serial communication chip select. It would bypass to MFCSB by R65H command.
FCSB	1	O, Type1	Serial communication chip select for External Flash/EEPROM.
FSCL	1	O, Type1	Serial communication clock output for External Flash/EEPROM.
FSDI	1	I, Type4 (Pull-down)	Serial communication data input for External Flash/EEPROM.
FSDO	1	O, Type1	Serial communication data output for External Flash/EEPROM.
CONTROL INTERFACE			
BS	1	I, Type2	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H: 3-wire IF
RST_N	1	I, Type3 (Pull-up), Type3	Global reset pin. Low reset. When RST_N become low, driver will reset. All register will reset to default value. All driver functions will be disabled. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.
BUSY_N	1	O, Type1	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
TSCL	2	O	I^2C clock for external temperature sensor. (A pull-up resistor is necessary).
TSDA	2	I/O	I^2C data for external temperature sensor. (A pull-up resistor is necessary).
SOURCE / GATE DRIVER			
S[0..639]	640	O	Source driver output signals.
G[0..479]	480	O	Gate driver output signals.
VBD (VBD<0>~<1>)	2	O	Border output pin.

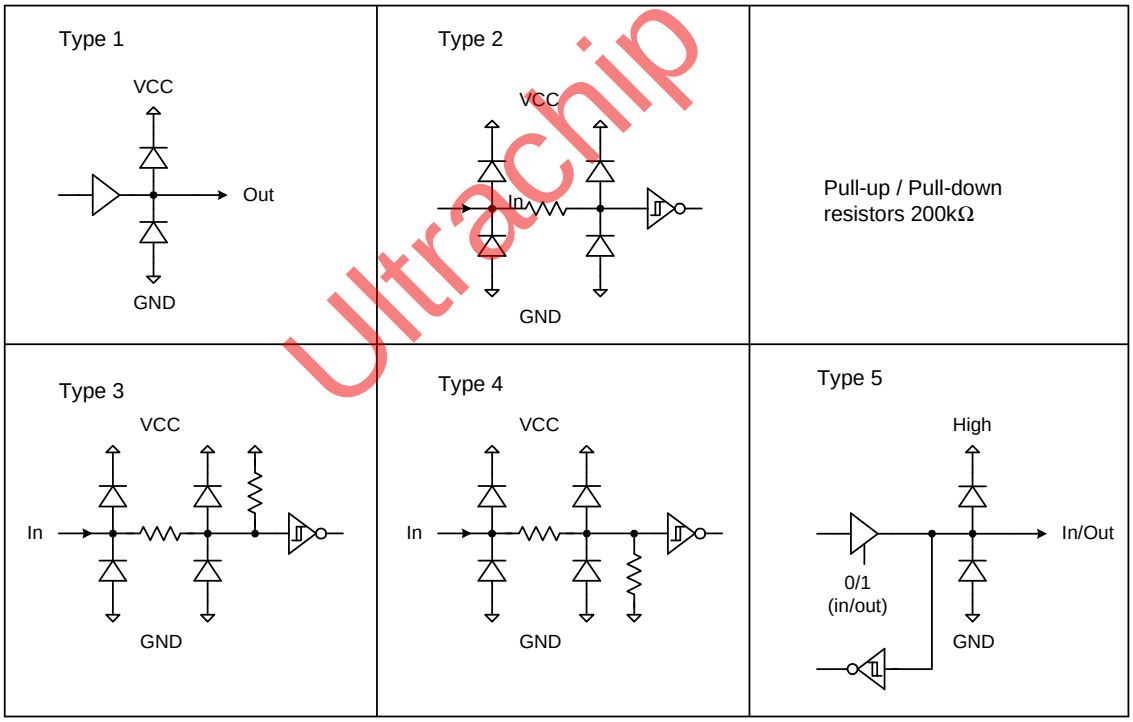
Pin (Pad) Name	Pin Count	Type	Description
VCOM	16	O	VCOM output. VCOM has four voltage states: 1. (VSH+VCM_DC) V 2. (VCM_DC) V 3. (VSL+VCM_DC) V 4. Floating
POWER CIRCUIT			
GDR	6	O	This pin is N-MOS gate control.
RESE	2	PWR	Current sense input for control loop.
FB	2	PWR	Keep open
VGH	20	C	Positive gate voltage
VGL	23	C	Negative gate voltage
VSH	10	C	Positive source voltage (+15V)
VSL	10	C	Negative source voltage (-15V)
VSH_LV	10	C	Positive source voltage (+3.0V ~ +15.0V).
VSL_LV	10	C	Negative source voltage (-3.0V ~ -15.0V).
VSH_LVX	8	C	Positive source voltage (external mode only) (+3.0V ~ +15.0V).
VSL_LVX	8	C	Negative source voltage (external mode only) (-3.0V ~ -15.0V).
PURE DRIVER INTERFACE			
DEN	1	I, Type2	Pure driver mode pin. L: Disable pure driver mode. H: Enable pure driver mode.
XCLK	1	I, Type2	Source driver clock input. Data inputs are captured on the rising edge of clock signal.
XOE	1	I, Type2	Source driver outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”. It is asynchronous to clock CLK.
XSTL	1	I, Type2	Source driver data shift start pulse
XLE	1	I, Type2	Source driver parallel latch enable, transparent when high. It is asynchronous to clock CLK
EDATA[7:0]	8	I, Type2	Source driver 8-bit data
GCLK	1	I, Type2	Gate driver shift clock pin. The shift register data are shifted synchronously with each rising edge of GCLK.
STV	1	I, Type2	Gate driver start pulse
XON	1	I, Type2	Driver XON pin. 0: Force all gate ON (VGH) 1: Normal gate function
VCOMVS[1:0] VCOMVS<0>~<1>	2	I, Type2	VCOM voltage selection 00b: VCM_DC 01b: VDPS+VCM_DC 10b: VDNS+VCM_DC 11b: floating

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY			
VDD	12	PWR	Digital voltage supply (2.3V ~ 3.6V)
VDDA	12	PWR	Analog voltage supply (2.3V ~ 3.6V)
VDDD	6	PWR	Voltage input (1.8V)
VDDDO	6	PWR	Voltage output (1.8V)
VDDIO	8	PWR	I/O voltage supply (2.3V ~ 3.6V)
VDM	6	PWR	Driver ground
VPPM	6		Connect to GND.
TEST1~15	15		Test pins for Ultrachip only, Leave it Float.
TESTVDD	1		Test pin for Ultrachip only, Connect to VSS.
DUMMY	13		Dummy pins
FSOURCE	3	PWR	Leave it float.
GND	25	PWR	Digital ground.
GNDA	22	PWR	Analog ground.
PATH1	2	S	Internally linked together.

Remark:

(1) Pull-up / Pull-down resistors 200KΩ

(2) I/O Pin Structure:



COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	--	--	#	#	#	#	RES[1:0], UD, SHL, SHD_N, RST_N	07h
		0	1	--	--	--	--	--	--	--	--		00h
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	#	#	#	#	#	#	EDATA_SEL, EDATA_SET, VCM_HZ, VS_EN, VSC_EN, VG_EN	08h
		0	1	--	--	--	--	--	--	#	#	VGHL_LV[1:0]	01h
		0	1	--	--	#	#	#	#	#	#	VSHC_LVL[5:0]	05h
		0	1	--	--	#	#	#	#	#	#	VSLC_LVL[5:0]	05h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17h
7	Deep Sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		1	1	1	0	1	0	0	1	0	1	Check code	A5h
8	Data Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	--	#	#	#	--	#	#	#	KPixel1[2:0], KPixel2[2:0]	00h
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	--	#	#	#	--	#	#	#	Kpixel[2M-1][2:0], Kpixel[2M][2:0]	00h
9	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--	Data_flag	--
10	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
11	Image Process Command (IPC)	0	0	0	0	0	1	0	0	1	1		13h
		0	1	--	--	--	#	--	#	#	#	IP_EN, IP_SEL[2:0]	00h
12	VCOM LUT (LUTC) (221-byte command, bytes 2~12 repeated 20 times)	0	0	0	0	1	0	0	0	0	0		20h
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	#	#	#	#	#	#	#	#	1stLVL[1:0], 2nd, 3rd, 4th	00h
		0	1	#	#	#	#	#	#	#	#	5th, 6th, 7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
13	LUT Blue (LUTB) (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**		**21h**
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
14	LUT White (LUTW) (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**0**		**22h**
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
15	LUTGray1 (LUTG1) (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**		**23h**
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
16	LUTGray2 (LUTG2) (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**		**24h**
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
17	LUT Red0 (LUTR0) (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**		**25h**
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
18	LUT Red1 (LUTR1) (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**		**26h**
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
19	LUT Red2 (LUTR2) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	1	1		27h
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
20	LUT Red3 (LUTR3) (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	1	0	0	0		28h
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	--	#	#	#	--	#	#	#	1stLVL[2:0], 2nd,	00h
		0	1	--	#	#	#	--	#	#	#	3rd, 4th	00h
		0	1	--	#	#	#	--	#	#	#	5th, 6th,	00h
		0	1	--	#	#	#	--	#	#	#	7th, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
21	LUT XON (LUTXON) (201-byte command, bytes 2~11 repeated 20 times)	0	0	0	0	1	0	1	0	0	1		29h
		0	1	#	#	#	#	#	#	#	#	Phase repeat times [7:0]	00h
		0	1	#	#	#	#	#	#	#	#	1stXON[0], 2nd, …, 8th	00h
		0	1	#	#	#	#	#	#	#	#	1stFrameNumber[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	2nd	00h
		0	1	#	#	#	#	#	#	#	#	3rd	00h
		0	1	#	#	#	#	#	#	#	#	4th	00h
		0	1	#	#	#	#	#	#	#	#	5th	00h
		0	1	#	#	#	#	#	#	#	#	6th	00h
		0	1	#	#	#	#	#	#	#	#	7th	00h
		0	1	#	#	#	#	#	#	#	#	8th	00h
22	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
23	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:1]	00h
		1	1	#	#	#	--	--	--	--	--	D[2:0] / TS[0]	00h
24	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	--	#	#	#	#	TSE, TO[3:0]	00h
25	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
26	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43h**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
27	Vcom and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50h**
		0	1	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	F7h
28	Lower Power Detection (LPD)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**		**51h**
		1	1	--	--	--	--	--	--	--	#	LPD	01h
29	TCON setting (TCON)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**60h**
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h
30	TCON resolution (TRES)	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**		**61h**
		0	1	--	--	--	--	--	--	#	#	HRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
31	SPI flash control (DAM)	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**		**65h**
		0	1	--	--	--	--	--	--	--	#	DAM	00h
32	Revision (REV)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**		**70h**
		1	1	#	#	#	#	#	#	#	#	LUTVER[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	LUTVER[15:8]	00h
33	Get Status (FLG)	0	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**		**71h**
		1	1	--	--	#	#	#	#	#	#	I^2C_ERR, I^2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	02h
34	Auto Measurement Vcom (AMV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**		**80h**
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], AMVX, AMVS, AMV, AMVE	10h
35	Read Vcom Value(VV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**		**81h**
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00h
36	VCM_DC Setting (VDCS)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**		**82h**
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	02h
37	Power Saving (PWS)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**		**E3h**
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(5) All write commands are "UNAVAILABLE" when BUSY_N=0 is asserted by reset, DSP (R11h), DRF (R12h) or IPC (R13h). All read commands are always "AVAILABLE".

* AVAILABLE means that Host can send command/parameter to driver.
* UNAVAILABLE means that Host cannot send command/parameter to driver.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h
	0	1	RES1	RES0	-	-	UD	SHL	SHD_N	RST_N	07h
	0	1	-	-	-	-	-	-	-	-	00h

RES[1:0]: Display Resolution setting (source x gate)
00b: 640x480 (Default)
01b: 600x450
10b: 640x448
11b: 600x448

UD: Gate Scan Direction
0: Scan down. (Default) First line to Last line: Gn-1 → … … → G0
1: Scan up. First line to Last line: G0 → … … . → Gn-1

SHL: Source Shift Direction
0: Shift left. First data to Last data: Sn-1 → … … → S0
1: Shift right. (Default) First data to Last data: S0 → … … . → Sn-1

SHD_N: Booster Switch
0: DC-DC converter OFF.
1: DC-DC converter ON (Default)
When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.

RST_N: Soft Reset
0: The controller is reset. Reset all registers to their default value.
1: Noormal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V
When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01h
	0	1	-	-	EDATA_SEL	EDATA_SET	VCM_HZ	VS_EN	VSC_EN	VG_EN	08h
	0	1	-	-	-	-	-	-	VG_LVL[1:0]		01h
	0	1	-	-	VSHC_LVL[5:0]						05h
	0	1	-	-	VSLC_LVL[5:0]						05h

EDATA_SEL: EDATA selection for pure driver mode
0 : When EDATA_SET=1, pixel bit =2`b11 output VSH_LV level (default)
1 : When EDATA_SET=1, pixel bit =2`b11 output VSL_LV level

EDATA_SET: EDATA setting for pure driver mode
0 : 3-bit data mode for pure driver (default)
1 : 2-bit data mode for pure driver

VCM_HZ: VCOM Hi-Z function
0: VCOM normal output.
1: VCOM floating. (default)

VS_EN: Source power selection.
0 : External source power from VSH and VSL pin. (default)
1 : Internal DCDC function for generate source power.

VSC_EN: Source LV power selection.
0 : External source LV power from VSH_LV and VSL_LV pin. (default)
1 : Internal DCDC function for generate source LV power.

VG_EN: Gate power selection.
0 : External gate power from VGH and VGL pin. (default)
1 : Internal DCDC function for generate gate power.

VG_LVL[1:0]: Internal VGH / VGL Voltage Level Selection.

VG_LVL[1:0]	Gate Voltage Level
00	VGH=20V, VGL= -20V
01	**VGH=19V, VGL= -19V (Default)**
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VSHC_LVL[5:0]: Internal VSH LV Voltage Level Selection for Red LUT.

VSHC_LVL[5:0]	VSH LV Voltage Level
000000	3.0 V
000001	3.2 V
000010	3.4 V
000011	3.6 V
000100	3.8 V
000101	**4.0 V (Default)**
:	:
11 1100	15.0 V

VSLC_LVL[5:0]: Internal VSL LV Voltage Selection for Red LUT.

VSLC_LVL[5:0]	VSL LV Voltage Level
000000	-3.0 V
000001	-3.2 V
000010	-3.4 V
000011	-3.6 V
000100	-3.8 V
000101	**-4.0 V (Default)**
“	:
11 1100	-15.0 V

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02h

After power off command, driver will power off based on the Power OFF Sequence, BUSY_N signal will become “0”.

The Power OFF command will turn off DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03h
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00h

T_VDS_OFF[1:0]: Power OFF Sequence of VSH /VSL and VGH/VGL..

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04h

After the Power ON command, driver will power on based on the Power ON Sequence.

After power on command and all power sequence are ready, then BUSY_N signal will become “1”.

(6) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Booster Soft Start	0	0	0	0	0	0	0	1	1	0	06h
	0	1	BTPHA7	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0	17h
	0	1	BTPHB7	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0	17h
	0	1	-	-	BTPHC5	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0	17h

BTPHA7[7:6] BTPHB7[7:6]	BTPHA[5:3], BTPHB[5:3], BTPHC[5:3]	BTPHA[2:0] BTPHB[2:0] BTPHC[2:0]
Soft Start Phase Period (mS)	Driving Strength	Minimum OFF Time (uS)
00b: 10 mS 01b: 20 10b: 30 11b: 40	000b: (reserved) 001b: (reserved) 010b: 1 011b: 2 100b: 3 101b: 4 110b: 5 111b: 6 (strongest)	000b: 0.26 uS 001b: 0.31 010b: 0.36 011b: 0.52 100b: 0.77 101b: 1.61 110b: 3.43 111b: 6.77

(7) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	1	0	0	0	0	07h
	0	1	1	0	1	0	0	1	0	1	A5h

This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardward reset assertion.
The only one parameter is a check code, the command would be executed if check code is A5h.

(8) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10h
	0	1	-	KPixel1 [2:0]			-	KPixel2 [2:0]			00h
	0	1	:	:			:	:			00h
	0	1	-	Kpixel(2M-1) [2:0]			-	Kpixel(2M) [2:0]			00h

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a DataStop command (R11H). Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0] :

	Source Driver Output	
	DDX=1 (Default)	DDX=0
KPixel[2:0]	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Red3
101	Red1	Red2
110	Red2	Red1
111	Red3	Red0

(9) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11h
	1	1	data_flag	-	-	-	-	-	-	-	00h

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1).

After "Data Start" (10h) or "Data Stop" (11h) commands, BUSY_N signal will become "0" until display update is finished.

(10) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12h

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0" until display update is finished.

(11) IMAGE PROCESS COMMAND (IPC) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Image Process Setting	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	13h
	0	1	-	-	-	IP_EN	-	IP_SEL[2:0]			00h

After this command is issued, image process engine will find thin lines/pixels from frame SRAM and update the frame SRAM for applying new gray level waveform.

IP_EN: Image process enable.
0: No action.
1: Image process enable (automatically return to '0' after image process is finished.

IP_SEL[2:0]: Image process selection.
000 : Deal with 1-pixel width
001 : Deal with 2-pixel width
010 : Deal with 3-pixel width
011 : Deal with 1-pixel and 2-pixel width
100 : Deal with 1-pixel, 2-pixel and 3-pixel width
Others : Deal with 1-pixel width

After "Image Process Command" (13h), BUSY_N signal will become "0" until image process is finished.

(12) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for VCOM (221-byte command, bytes 2~12 repeated 20 times)	0	0	0	0	1	0	0	0	0	0	20h
	0	1	Phase repeat times [7:0]								00h
	0	1	1st level sele. [1:0]		2nd level sele. [1:0]		3rd level sele. [1:0]		4th level sele. [1:0]		00h
	0	1	5th level sele. [1:0]		6th level sele. [1:0]		7th level sele. [1:0]		8th level sele. [1:0]		00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds up VCOM Look-Up Table (LUT). This LUT includes 20 kinds of states, each state is of 11 bytes, as tabove.

Each state is made up 8 phases. And each phase is combined with “Repeat number”, “Level selection”, and “Frame Number”.

Byte 2: repeat number.

Bytes 3 ~ 4: Level selection of each phase.

Bytes 5 ~12: Frame number of each phase.

Bytes 2, 13, 24, 35, 46, … : Times to Repeat

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255 times

Bytes 3~4, 14~15, 25~26, 36~37, 47~48, … : Level Selection.

00b: VCM_DC
01b: 15V + VCM_DC (VCOMH)
10b: -15V + VCM_DC (VCOML)
11b: Floating

Bytes 5~12, 16~23, 27~34, 38~45, 49~56, … : Number of Frames

0000 0000b ~ 1111 1111b: 0 ~ 255 frames

Example:

Byte	D7~D0	Remark
2	0000 1000	Repeat 8 times
3	01 00 10 00	1st level: VCOMH, 2nd level: -VCM_DC, 3rd level: VCOML, 4th level: -VCM_DC
4	01 00 10 00	5th level: VCOMH, 6th level: -VCM_DC, 7th level: VCOML, 8th level: -VCM_DC
5	0000 0010	1st frame number: 2
6	0000 0001	2nd frame number: 1
7	0000 0011	3rd frame number: 3
8	0000 0001	4th frame number: 1
9	0000 0100	5th frame number: 4
10	0000 0001	6th frame number: 1
11	0000 0101	7th frame number: 5
12	0000 0001	8th frame number: 1

(13) BLACK LUT (LUTB) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Black (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	0	1	21h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUTB for black. This LUT includes 20 kinds of states, each state is of 13 bytes as above.

Each state is made up 8 phases. And each phase is combined with “repeat number”, “Level selection”, and “frame number”.

Byte 2: repeat number.

Bytes 3 ~ 6: Level selection of each phase.

Bytes 7 ~14: Frame number of each phase.

Bytes 2, 15, 28, 41, 54, … : Times to Repeat

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255 times

Bytes 3~6, 16~19, 29~32, 42~45, 55~58, … : Level Selection.

000b: 0V
001b: 15V (VSH)
010b: -15V (VSL)
011b: VSH_LV
100b: VSL_LV
101b: VSH_LVX (external source power from VSH_LVX pin)
110b: VSL_LVX (external source power from VSL_LVX pin)
111b: Floating

Bytes 7~14, 20~27, 33~40, 46~53, 59~66, … : Number of Frames

0000 0000b ~ 1111 1111b: 0 ~ 255 frames

Example:

Byte 2	0000 0100	repeat 4 times	
3	0001 0010	1st level: VSH,	2nd level: VSL
4	0011 0100	3rd level: VSH_LV,	4th level: VSL_LV
5	0001 0010	5th level: VSH,	6th level: VSL
6	0011 0100	7th level: VSH_LV,	8th level: VSL_LV
7	0000 0001	1st frame number: 1	
8	0000 0010	2nd frame number: 2	
9	0000 0011	3rd frame number: 3	
10	0000 0100	4th frame number: 4	
11	0000 0101	5th frame number: 5	
12	0000 0110	6th frame number: 6	
13	0000 0101	7th frame number: 5	
14	0000 0001	8th frame number: 1	

(14) LUT WHITE (LUTW) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Gray1 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	1	1	23h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for White. Please refer to command (13) LUTB for similar definition details.

(15) GRAY1 LUT (LUTG1) (R23H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Gray1 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	0	1	1	23h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for Gray 1. Please refer to command (13) LUTB for similar definition details.

(16) GRAY2 LUT (LUTG2) (R24H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Gray2 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	0	24h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for Gray 2. Please refer to command (13) LUTB for similar definition details.

(17) RED0 LUT (LUTR0) (R25H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table forRed0 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	0	1	25h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for Red 0. Please refer to command (13) LUTB for similar definition details.

(18) RED1 LUT (LUTR1) (R26H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Red1 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	1	0	26h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for Red 1. Please refer to command (13) LUTB for similar definition details.

(19) RED2 LUT (LUTR2) (R27H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Red2 (261-byte command, bytes 2~14 repeated 20 times)	0	0	0	0	1	0	0	1	1	1	27h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for Red 2. Please refer to command (13) LUTB for similar definition details.

(20) RED3 LUT (LUTR3) (R28H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for Red3 (261-byte command, bytes 2~14 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	28h
	0	1	Phase repeat times [7:0]								00h
	0	1	-	1st level sele. [2:0]			-	2nd level sele. [2:0]			00h
	0	1	-	3rd level sele. [2:0]			-	4th level sele. [2:0]			00h
	0	1	-	5th level sele. [2:0]			-	6th level sele. [2:0]			00h
	0	1	-	7th level sele. [2:0]			-	8th level sele. [2:0]			00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for Red 3. Please refer to command (13) LUTB for similar definition details.

(21) XON LUT (LUTXON) (R29H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-Up Table for XON (201-byte command, bytes 2~11 repeated 20 times)	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	29h
	0	1	Phase repeat times [7:0]								00h
	0	1	1st XON	2nd XON	3rd XON	4th XON	5th XON	6th XON	7th XON	8th XON	00h
	0	1	1st Frame Number [7:0]								00h
	0	1	2nd Frame Number [7:0]								00h
	0	1	3rd Frame Number [7:0]								00h
	0	1	4th Frame Number [7:0]								00h
	0	1	5th Frame Number [7:0]								00h
	0	1	6th Frame Number [7:0]								00h
	0	1	7th Frame Number [7:0]								00h
	0	1	8th Frame Number [7:0]								00h

This command builds LUT for XON. This LUT includes 20 kinds of states, each state is of 10 bytes as above.

Each state is made up 8 phases. And each phase is combined with “repeat number”, “XON selection”, and “frame number”.

Byte 2: Repeat number.

Bytes 3: Level selection of each phase.

Bytes 4 ~11: Frame number of each phase.

Bytes 2, 12, 22, 32, 42, … : Times to Repeat

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255 times

Bytes 3, 13, 23, 43, 53, … : XON Selection.

0: All gate ON (VGH)
1: Normal gate scan function

Bytes 4~11, 14~21, 24~31, 34~41, 44~51, … : Number of Frames

0000 0000b ~ 1111 1111b: 0 ~ 255 frames

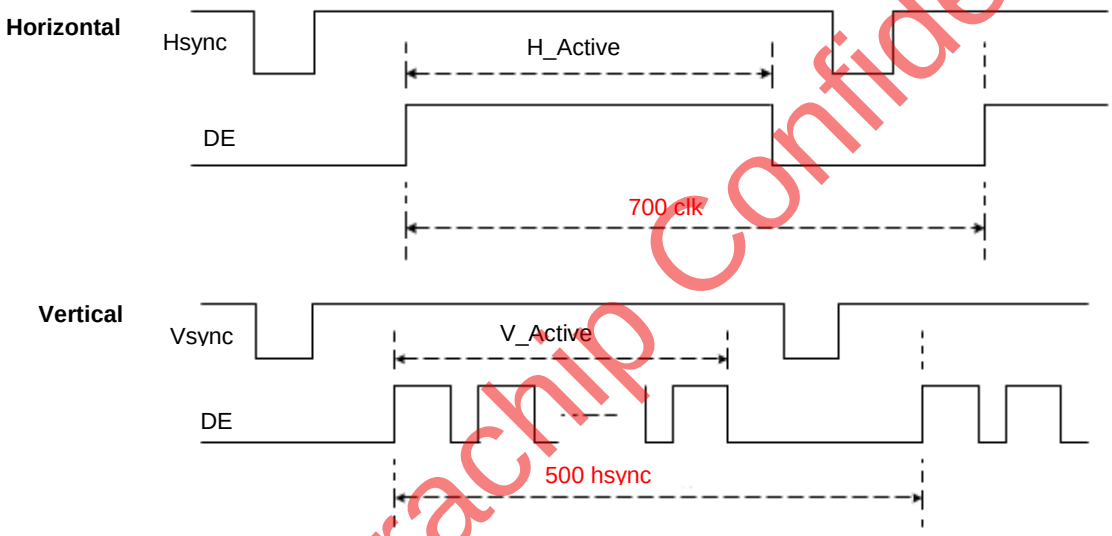
(22) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30h
	0	1	-	-	M[2:0]			N[2:0]			3Ch

The command controls the PLL clock frequency. The PLL structure supports the following frame rates:

(FR: Frame Rate, Unit: Hz)

M	N	FR	M	N	FR	M	N	FR	M	N	FR	M	N	FR	M	N	FR	M	N	FR
1	1	29	2	1	57	3	1	86	4	1	114	5	1	143	6	1	171	7	1	200
	2	14		2	29		2	43		2	59		2	71		2	86		2	100
	3	10		3	19		3	29		3	38		3	48		3	57		3	67
	4	5		4	14		4	21		4	29		4	36		4	43		**4**	**50**
	5	7		5	11		5	17		5	23		5	29		5	34		5	40
	6	6		6	10		6	14		6	19		6	24		6	29		6	33
	7	5		7	8		7	12		7	16		7	20		7	24		7	29



(23) TEMPERATURE SENSOR COMMAND (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40h
	1	1	D10	D9 / TS7	D8 / TS6	D7 / TS5	D6 / TS4	D5 / TS3	D4 / TS2	D3 / TS1	00h
	1	1	D2 / TS0	D1	D0	-	-	-	-	-	00h

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]	Temperature (^{o}C)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
0000 0011b	1.5
:	:
0111 1000b	60

BUSY_N become low after TSC command. When BUSY_N become high, Parameter can be read.

(24) TEMPERATURE SENSOR INTERNAL/EXTERNAL (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Calibrate Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41h
	0	1	TSE	-	-	-	TO[3:0]				00h

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Select internal temperature sensor (default) 1: Select external temperature sensor.

TO[3:0]: Temperature Offset

TO[3:0]	Temperature Offset
0000	+0 (Default)
0001	+0.5
0010	+1.0
0011	+1.5
0100	+2.0
0101	+2.5
0110	+3.0
0111	+3.5

TO[3:0]	Temperature Offset
1000	-4.0
1001	-3.5
1010	-3.0
1011	-2.5
1100	-2.0
1101	-1.5
1110	-1.0
1111	-0.5

(25) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Sensor Write	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	42h
	0	1	WATTR[7:0]								00h
	0	1	WMSB[7:0]								00h
	0	1	WLSB[7:0]								00h

This command could write data to the external temperature sensor.

WATTR: **D[7:6]:** I^2C Write Byte Number
00: 1 byte (head byte only)
01: 2 bytes (head byte + pointer)
10: 3 bytes (head byte + pointer + 1st parameter)
11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(26) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Sensor Read	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	42h
	0	1	RMSB[7:0]								00h
	0	1	RLSB[7:0]								00h

This command could read data from the external temperature sensor.

RMSB[7:0]: MSByte of read-data from external temperature sensor

RLSB[7:0]: LSByte of read-data from external temperature sensor

(27) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between Vcom and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	VBD[2:0]			DDX	CDI[3:0]				17h

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[2:0]: Border output selection

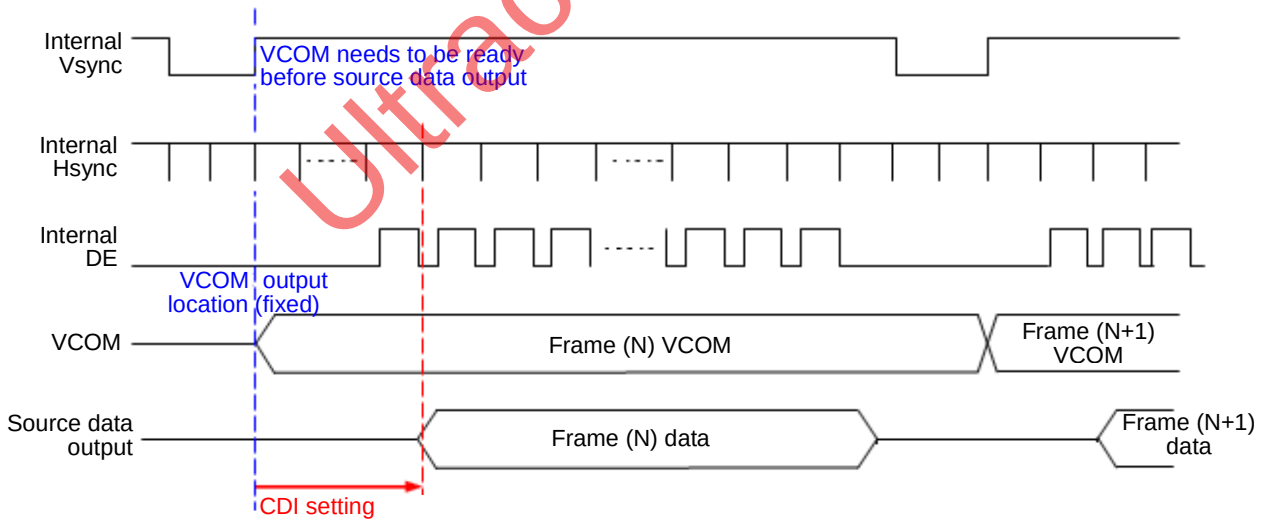
DDX: Data polality.

	Border Output	
	DDX=1 (Default)	DDX=0
VBD[2:0]	LUT	LUT
000	Black	White
001	Gray1	Gray2
010	Gray2	Gray1
011	White	Black
100	Red0	Floating
101	Red1	Red2
110	Red2	Red1
111	Floating	Red0

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	Vcom and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(28) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (V_{DD}<2.5V) **1: Normal status (default)**

(29) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period = 500 nS.

(30) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	1	-	-	-	-	-	-	HRES[9:8]		00h
	0	1	HRES[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

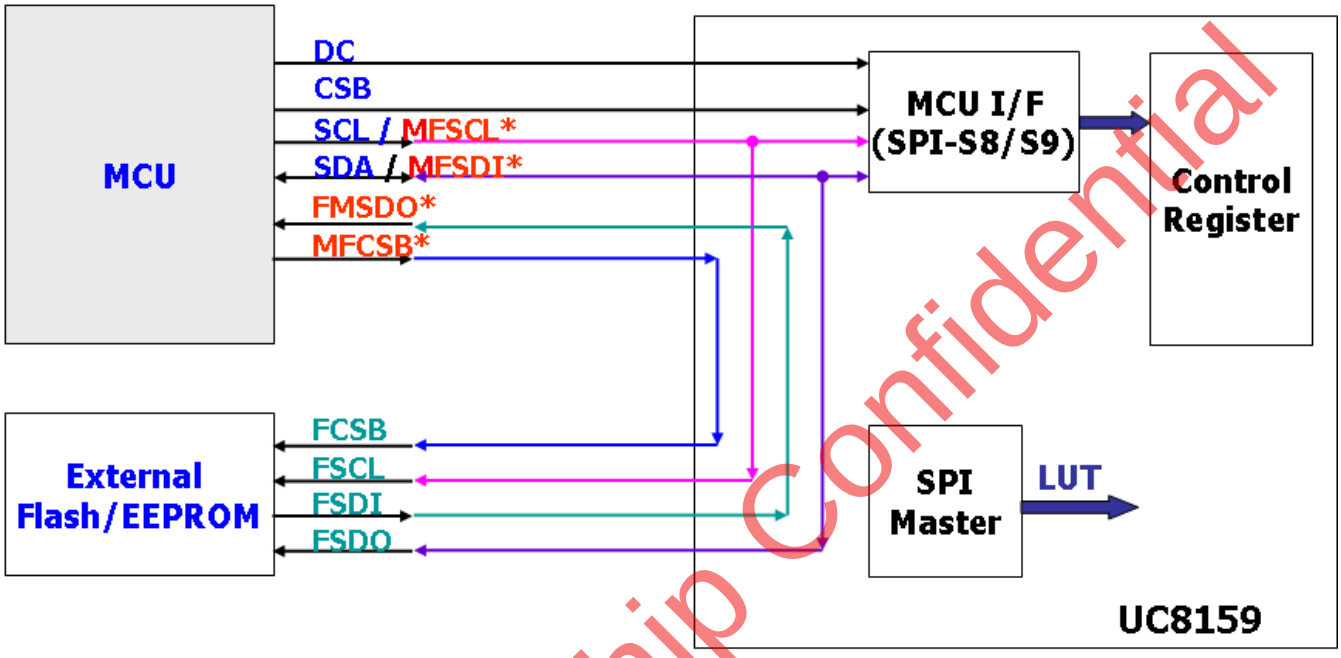
Resolution setting (R61H) has higher priority than RES[1:0] (R00H). Horizontal resolution should be even number.

(31) SPI FLASH CONTROL (DAM) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Control SPI Flash	0	0	0	1	1	0	0	1	0	1	65h
	0	1	-	-	-	-	-	-	-	DAM	00h

This command defines how MCU host directly access external flash/EEPROM mode.

DAM: 0: Disable (Default)
1: Enable. By pass MFSCL*, MFSDI*, FMSDO*, and MFCSB* to external flash.



MCU and External SPI Flash/EEPROM Connection in DAM mode

(32) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT / Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	LUTVER[7:0]								00h
	1	1	LUTVER[15:8]								

The LUTVER[15:0] is read from Flash address from 25001 to 25000.

LUTVER[15:0]: LUT version.

(33) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	-	I2C_ ERR	I2C_ BUSYN	Data_ flag	PON	POF	BUSY_N	02h

This command reads the IC status.

I2C_ERR: I^2C master error status

I2C_BUSYN: I^2C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(34) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		AMVX	AMVS	AMV	AMVE	10h

This command implements related VCOM sensing setting.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

AMVX: Auto Measure VCOM without XON function

0: Measure VCOM without XON function. (Gate scanning) (default)
1: Measure VCOM with XON function. (All Gate ON)

AMVS: Source output of AMV

0: Set Source output to 0V during Auto Measure VCOM period. (default)
1: Set Source output to VSH_LV during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)
1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0: Disabled 1: Enabled

(34) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

VV[6:0]	Vcom value
000 0000b	0 V
000 0001b	-0.05 V
000 0010b	-0.10 V
000 0011b	-0.15 V
000 0100b	-0.20 V
:	:
101 0000b	-4.0 V
(others)	-4.0 V

(36) VCM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							02h

This command sets VCOM_DC value.

VDCS[6:0]: VCOM_DC Setting

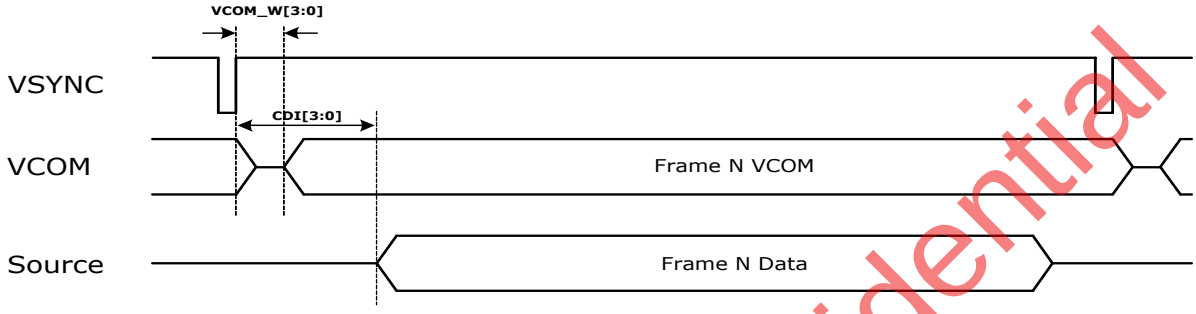
VDCS[6:0]	Vcom_DC value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.10 V
000 0011b	-0.15 V
000 0100b	-0.20 V
:	:
101 0000b	-4.0 V
(others)	-4.0 V

(37) POWER SAVING (PWS) (RE3H)

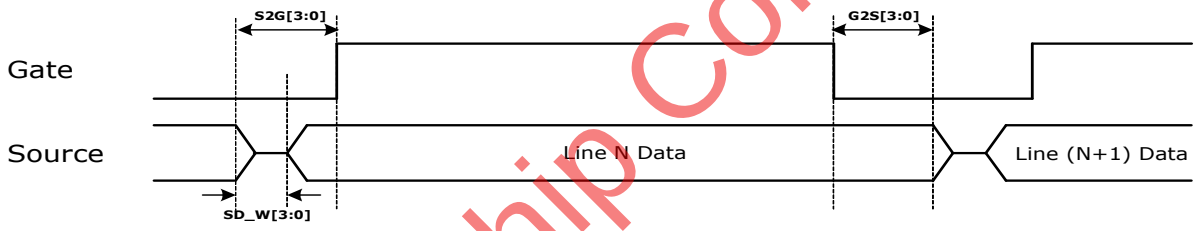
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
VCOM/Source Power Saving	0	0	1	0	0	0	0	0	1	0	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is sets for saving power VCOM/Source power saving during display refresh period. If the output voltage of VCOM/ Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM_power saving width. (unit : line period)

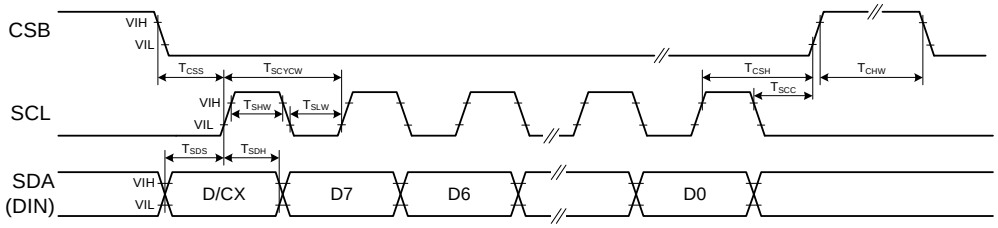


SD_W[3:0]: Source power saving width. (unit : 500ns)

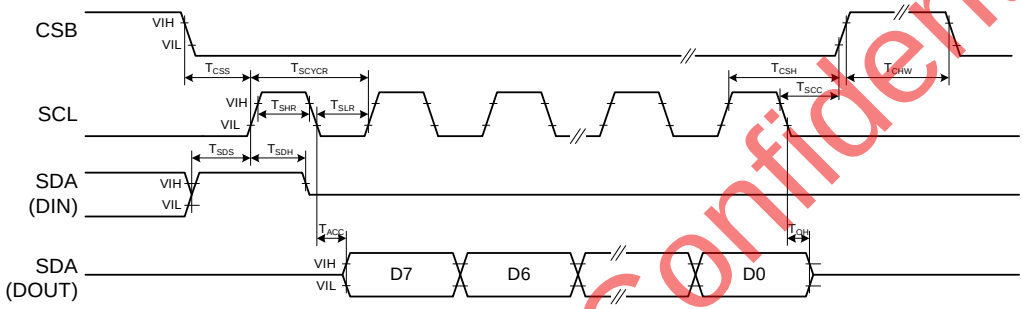


HOST INTERFACES

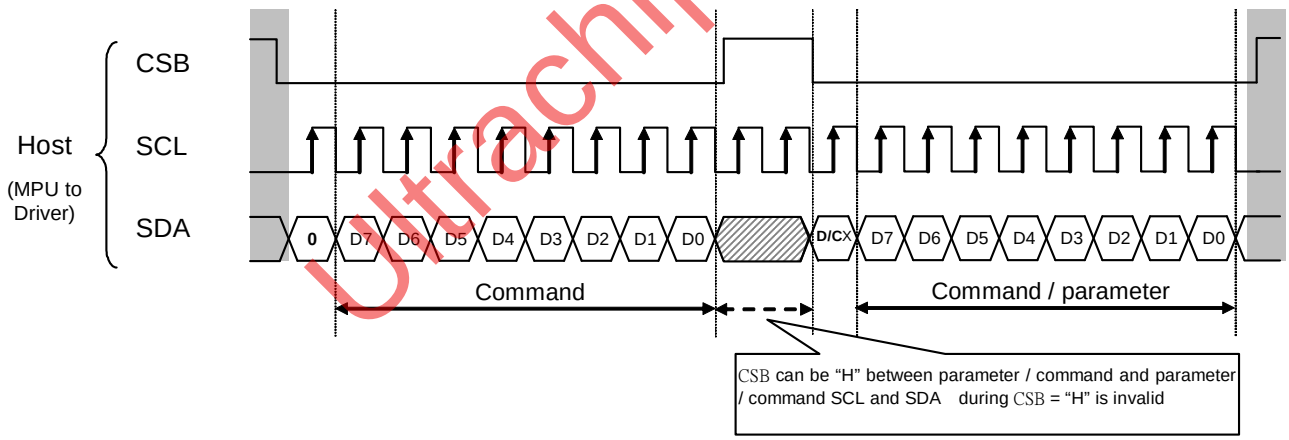
3-WIRE SPI



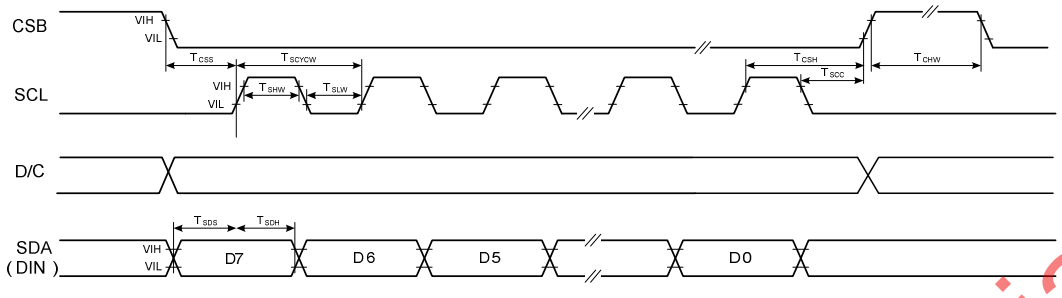
3 pin serial interface characteristics (write mode)



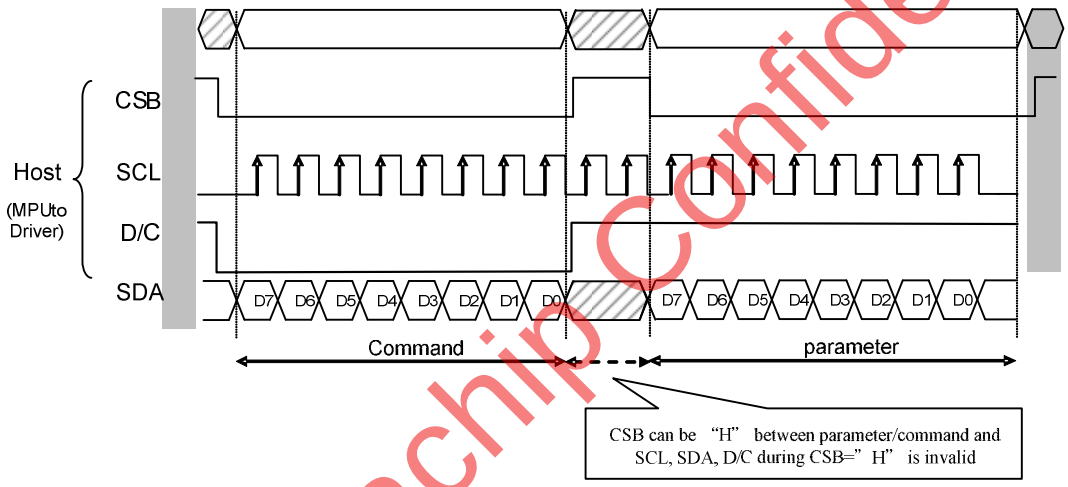
3 pin serial interface characteristics (read mode)



4-WIRE SPI

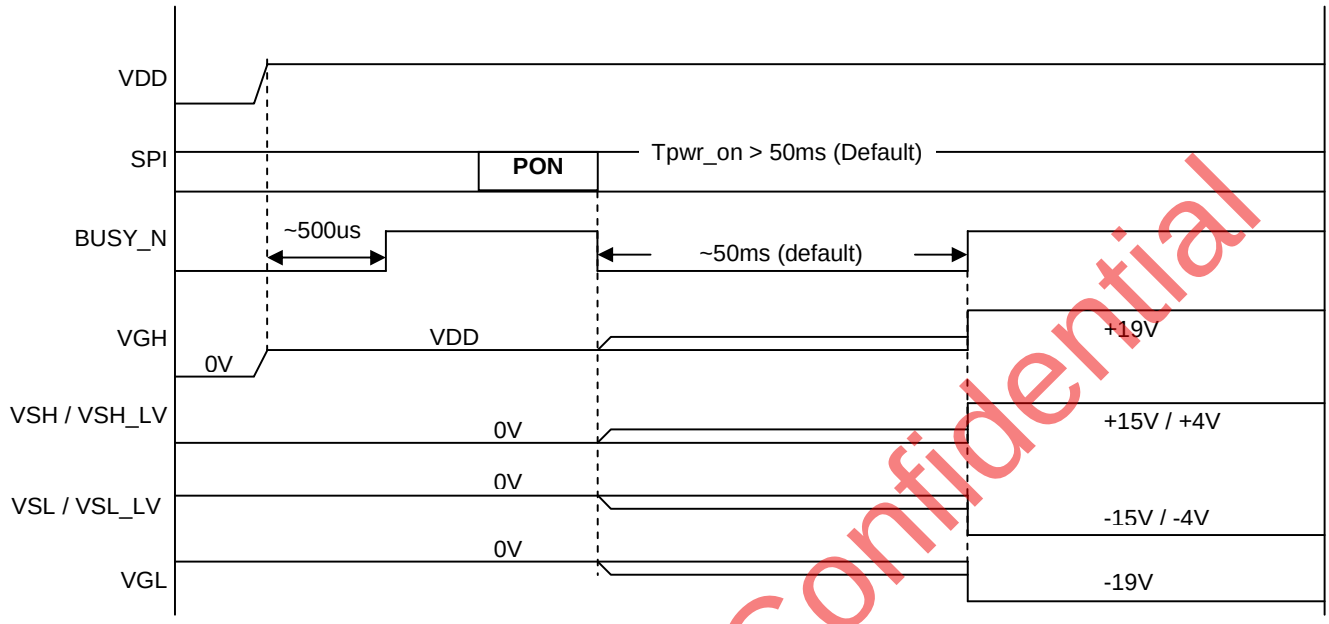


4 pin serial interface characteristics

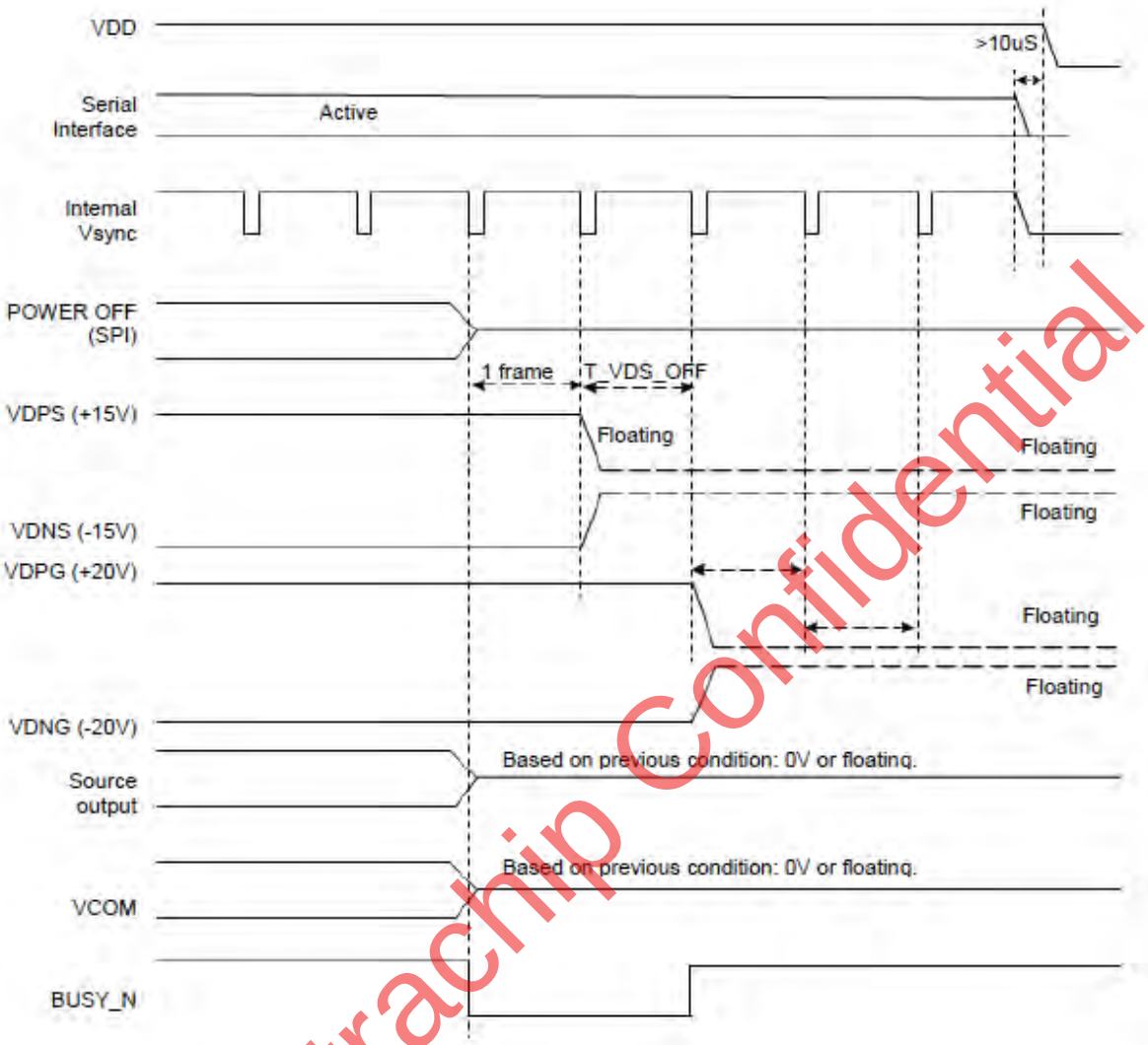


POWER MANAGEMENT

Power ON Sequence



Power OFF Sequence



LUT (Lookup Table) Definition

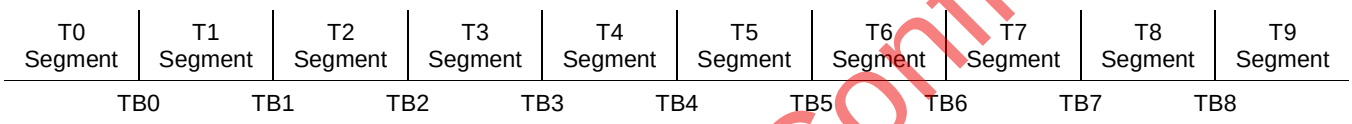
The LUT stored in external flash/EEPROM contains 10 temperature segments for application. And there are waveform, VCOM, XON, VDPS_LVSHC_LVL, VDNS_LVSLC_LVL, etc. After command DSP or DRF is asserted, the driver gets related temperature information and LUT data from the external flash/EEPROM. The corresponding VCOM/LUT/XON waveform will output. The total size of LUT is 25031 bytes.

Address	Category	Address	Temp.	Address	LUT	Remark
00000	Waveform LUT (T0~T9) (20800)	0	T0 (2080)	0~259 (260)	LUTB	See command LUTB (R21h) for details
:		:		260~519 (260)	LUTW	LUTW (R22h)
:		:		520 ~779 (260)	LUTG1	LUTG1 (R23h)
:				780~1039 (260)	LUTG2	LUTG2 (R24h)
:				1040~1299 (260)	LUTR0	LUTR0 (R25h)
:				1300~1559 (260)	LUTR1	LUTR1 (R26h)
:				1560~1819 (260)	LUTR2	LUTR2 (R27h)
:		2079		1820~2079 (260)	LUTR3	LUTR3 (R28h)
		(2080)	T1	2080~4159	8 LUT	(Same as T0)
		(2080)	T2	4160~6239	8 LUT	(Same as T0)
		(2080)	T3	6240~8319	8 LUT	(Same as T0)
		(2080)	T4	8320~10399	8 LUT	(Same as T0)
		(2080)	T5	10400~12479	8 LUT	(Same as T0)
		(2080)	T6	12480~14559	8 LUT	(Same as T0)
		(2080)	T7	14560~16639	8 LUT	(Same as T0)
		(2080)	T8	16640~18719	8 LUT	(Same as T0)
20799		(2080)	T9	18720~20799	8 LUT	(Same as T0)
20800	VCOM LUT (T0~T9) (2200)	(220)	T0	20800~21019	VCOM	See command LUTC (R20h) for details
:		(220)	T1	21020~21239		
:		(220)	T2	21240~21459		
:		(220)	T3	21460~21679		
:		(220)	T4	21680~21899		
		(220)	T5	21900~22119		
		(220)	T6	22120~22339		
		(220)	T7	22340~22559		
		(220)	T8	22560~22779		
22999		(220)	T9	22780~22999		
23000	XON LUT (T0~T9) (2000)	(200)	T0	23000~23199	XON	See command LUTXON (R29h) for details
:		(200)	T1	23200~23399		
:		(200)	T2	23400~23599		
:		(200)	T3	23600~23799		
		(200)	T4	23800~23999		
		(200)	T5	24000~24199		
		(200)	T6	24200~24399		
		(200)	T7	24400~24599		
		(200)	T8	24600~24799		
24999		(200)	T9	24800~24999		
25000 25001	Waveform version	(2)	--	25000~25001	LUTVER	If both are FFh, this flash is not programmable yet.
25002 : 25010	Temperature Boundary (TB0~TB8)	(9)	--	25002~25010	TB	9 temperature boundary for LUT
25011	T0_VSHC_LVL, T0_VSLC_LVL, T1_VSHC_LVL, T1_VSLC_LVL, : T9_VSHC_LVL, T9_VSLC_LVL	(20)	T0 | T9	25011~25030	VSHC VSLC	See VSH_LV / VSL_LV voltage setting (R01h)
:						
:						
:						
25030						

Temperature Segment Selection

There are 10 temperature segments which could be selected by specifying TB0~TB8 (address: 25002~25010). The comparison condition between real environment temperature and TB0~TB8 is illustrated as the below table.

Order	Comparison Condition	Segment
1	Real Temp. < TB0	T0 Segment
2	TB0 ≦ Real Temp. < TB1	T1 Segment
3	TB1 ≦ Real Temp. < TB2	T2 Segment
4	TB2 ≦ Real Temp. < TB3	T3 Segment
5	TB3 ≦ Real Temp. < TB4	T4 Segment
6	TB4 ≦ Real Temp. < TB5	T5 Segment
7	TB5 ≦ Real Temp. < TB6	T6 Segment
8	TB6 ≦ Real Temp. < TB7	T7 Segment
9	TB7 ≦ Real Temp. < TB8	T8 Segment
10	TB8 ≦ Real Temp.	T9 Segment

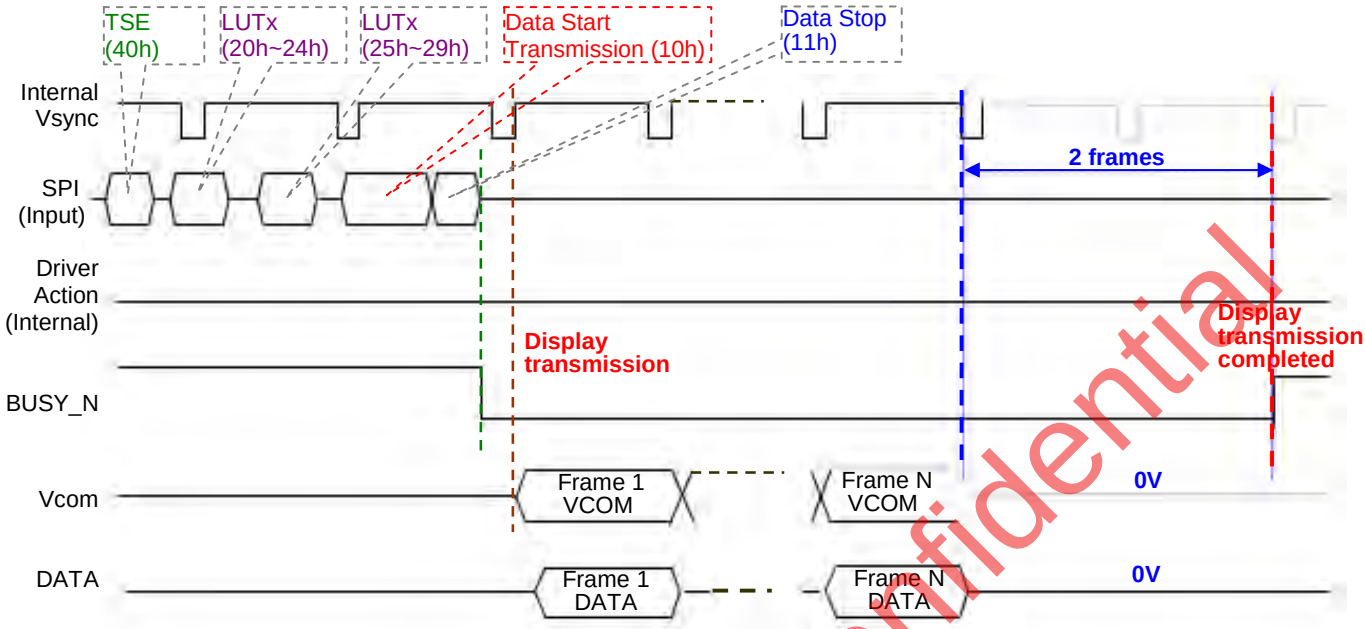


The format of TB0~TB8 is as the below.

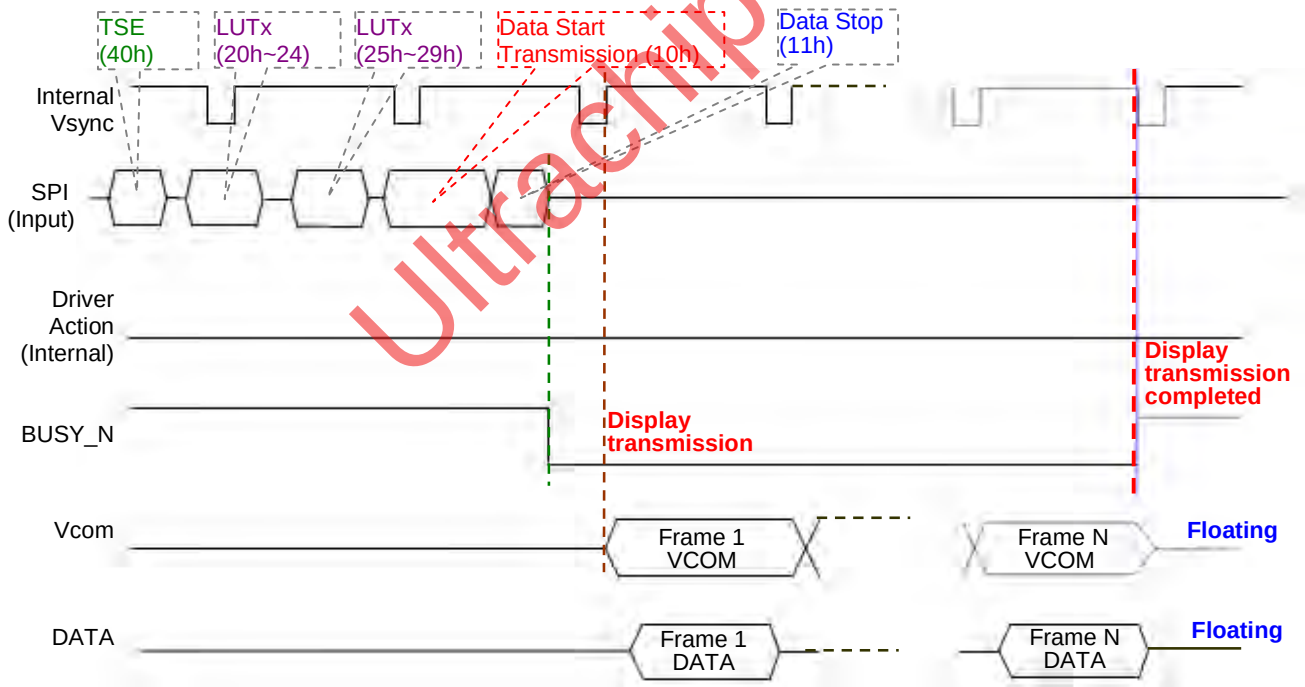
Bit7-0	Temperature (°C)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
0000 0011b	1.5
:	:
0111 1000b	60

Data Transmission Waveform

Example 1: LUT all states (20 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.

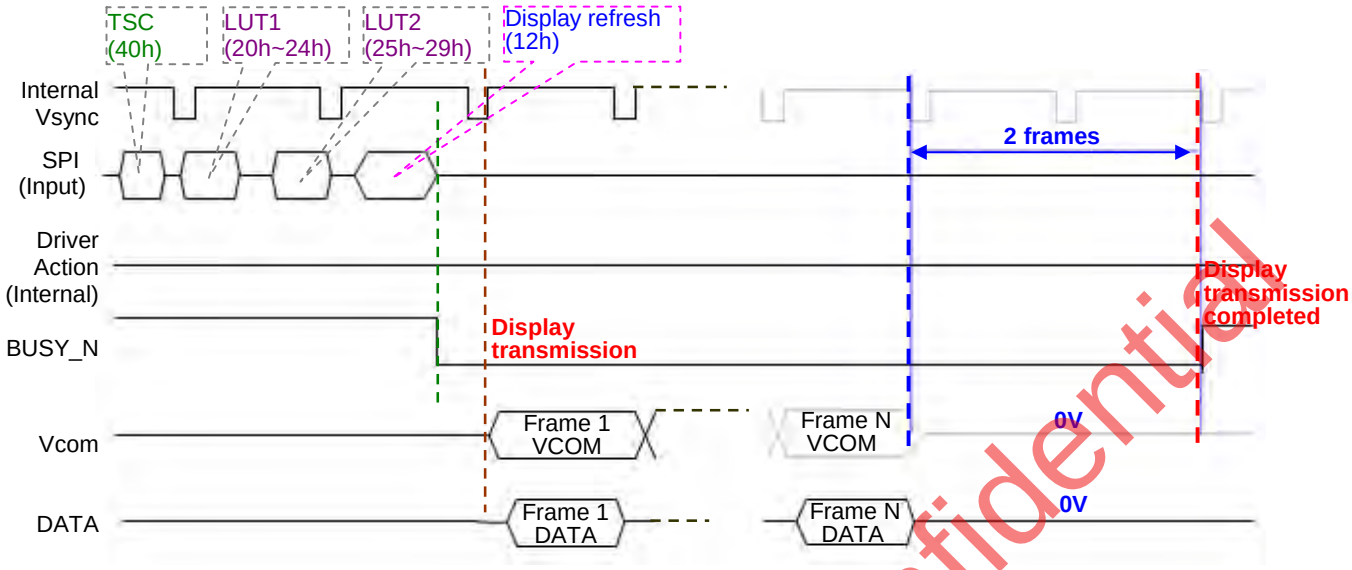


Example 2: While level selection in LUT is "11", the driver will float VCOM and data.

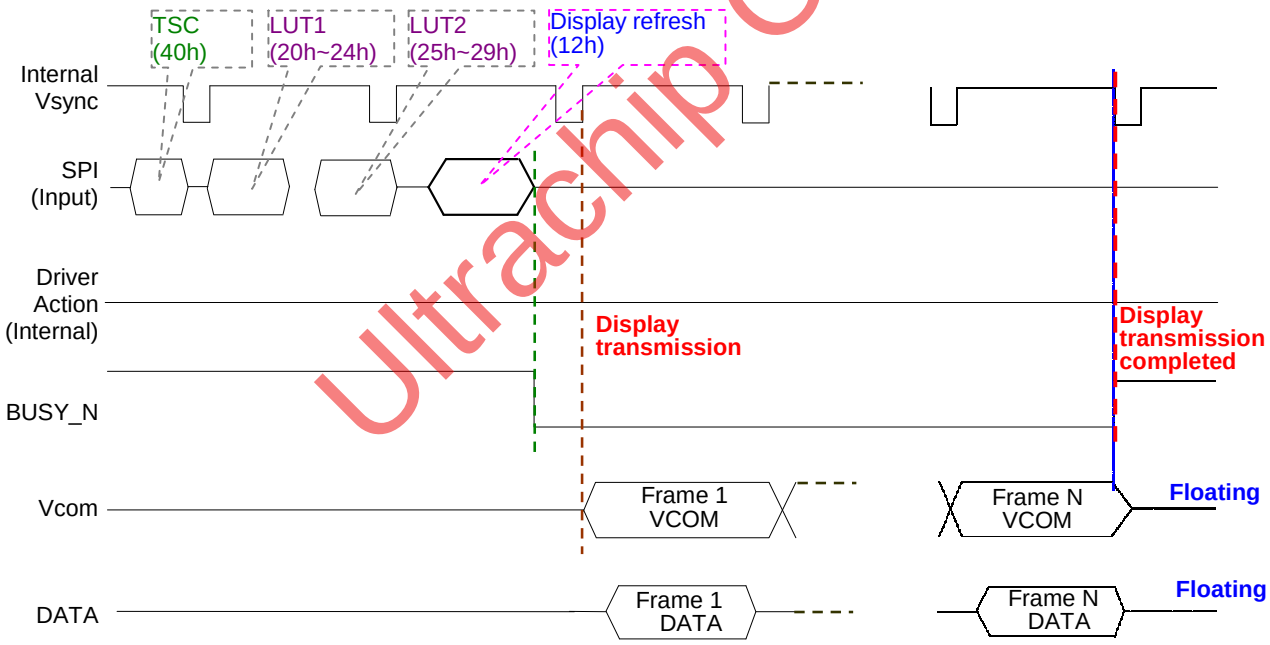


Display Refresh Waveform

Example 1: LUT all states (20 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.



Example2: While level selection in LUT is "11", the driver will float VCOM and data.



BUSY_N Signal / Command Restriction

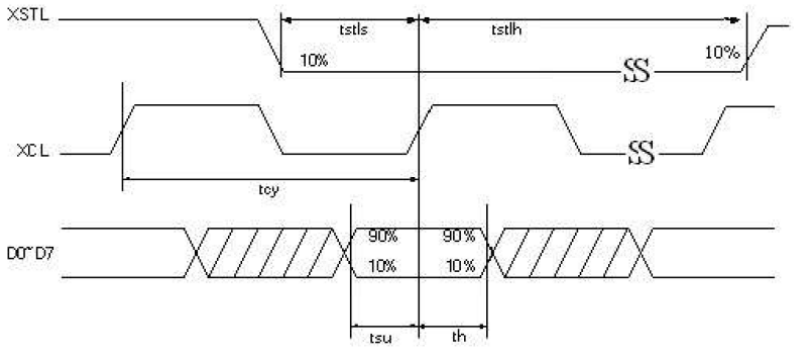
All write commands are “UNAVAILABLE” when BUSY_N=0 asserted by reset, DSP (R11h), DRF (R12h) or IPC (R13h).

All read commands are always “AVAILABLE” regardless of BUSY_N is 0 or 1.

Pure Driver Mode

Enable pure driver mode when input pin DEN=1. In pure driver mode, command R01, R02, R03, R04, R61, R82 are still useful.

Source Signal Timing (Clock & data timing)



Data arrangement: Control by command R02H, EDATA_SET bit.

3 bit mode: EDATA_SET=0,

	D0~7							
	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1st Data	-	Pixel 1			-	Pixel 2		
2nd Data	-	Pixel 3			-	Pixel 4		
…	-				-			
N-th Data	-	Pixel 2N-1			-	Pixel 2N		

If SHL=1, pixel 1 is output to S0, pixel 2 is output to S1, and so on.

If SHL=0, pixel 1 is output to Sn-1, pixel 2 is output to Sn-2, and so on.

And each pixel level selection:

Pixel bit	Level selection
000	0v.
001	15v. (VSH).
010	-15v. (VSL).
011	VSH_LV
100	VSL_LV
101	VSH_LVX
110	VSL_LVX
111	Floating.

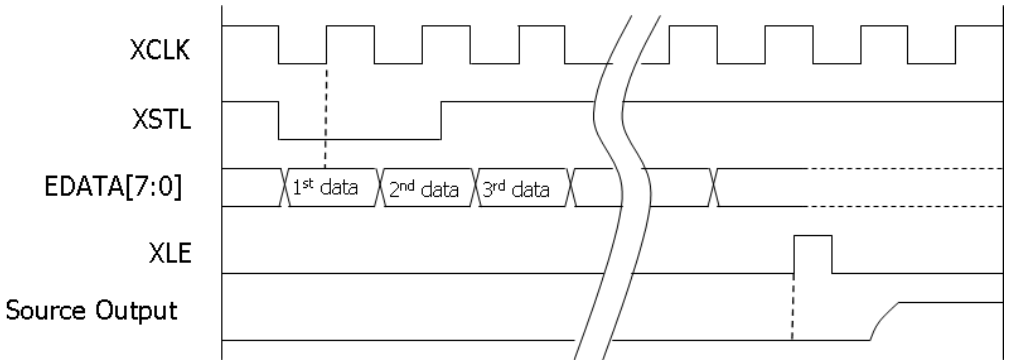
2 bit mode: EDATA_SET=1,

	D0~7							
	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1st Data	Pixel 1		Pixel 2		Pixel 3		Pixel 4	
2nd Data	Pixel 5		Pixel 6		Pixel 7		Pixel 8	
…	-				-			
N-th Data	Pixel 4N-3		Pixel 4N-2		Pixel 4N-1		Pixel 4N	

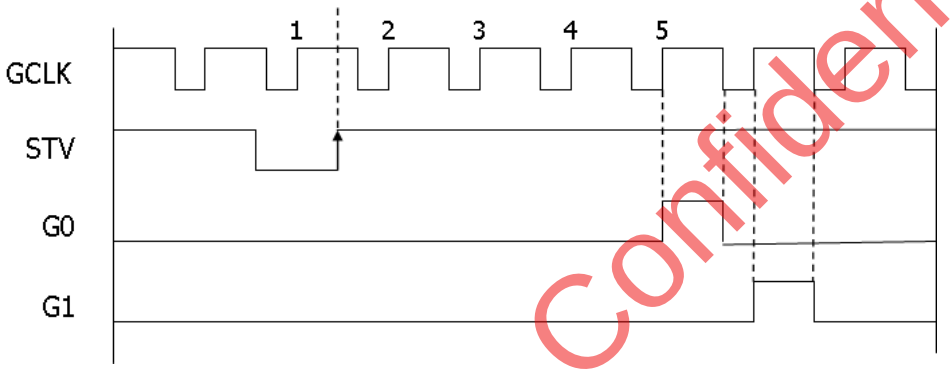
Pixel bit	Level selection
00	0v.
01	15v. (VSH).
10	-15v. (VSL).
11	VSH_LV or VSL_LV

The level selection of “pixel bit =11” is define by EDATA_SEL bit (R01 command), voltage level output VSH_LV when EDATA_SEL=0, output VSL_LV when EDATA_SEL=1.

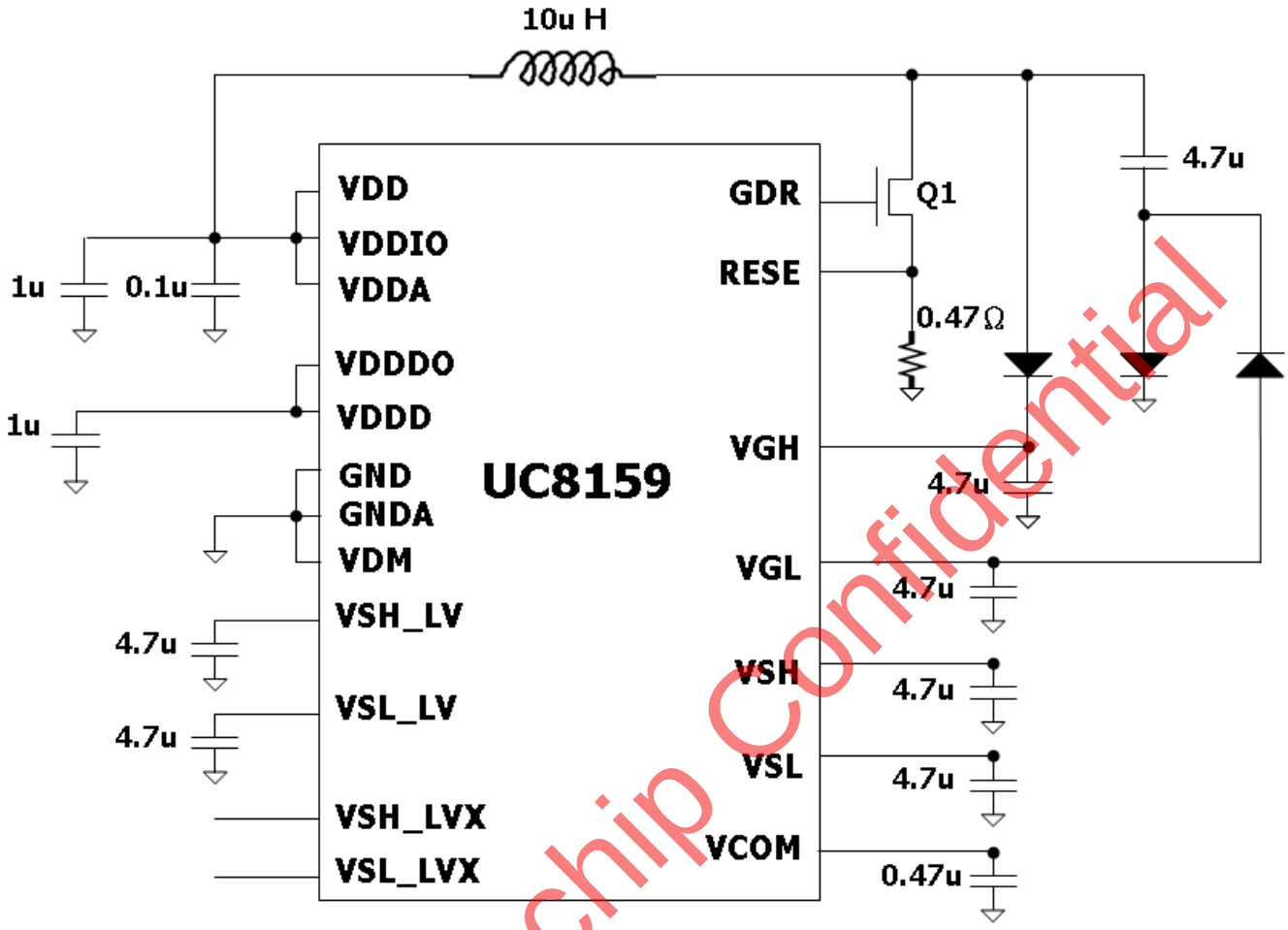
Output latch control signal



Gate Signal Timing



Booster Application Circuit



Recommended Device:

(1) NMOS Switch Q1: ROHM RUF015N02 ($V_{DS} \geq 20V$, $I_D \geq 1.2A$, $V_{GS(TH)} < 1.5V$, $R_{DS(ON)} < 350m\text{-}\Omega$)

(2) Schottky Diode: OnSemi MBR0530 ($V_R \geq 20V$, $I_F \geq 500mA$, $I_R < 1mA$)

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{DDA}, V_{DDIO}	Logic Supply voltage	+2.3	+3.6	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VGH-VGL	Supply range	VGH-0.3	VGL+0.3	V
Source				
VSH	Analog supply voltage – positive	+15		V
VSL	Analog supply voltage – negative	-15		V
VSH_LV	Analog supply voltage – positive	+3 ~ +15		V
VSL_LV	Analog supply voltage – negative	-3 ~ -15		V
Gate				
V_{GH}	Analog supply voltage – positive	-17	+20	V
V_{GL}	Analog supply voltage -- nagetive	-17	-20	V
I_{VGH}	Input rush current for VGH	(TBD)	(TBD)	mA
I_{VGL}	Input rush current for VGL	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	^{o}C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
V_{DDIO}	IO supply voltage		2.3	3.3	3.6	V
V_{DD}	Supply voltage		2.3	3.3	3.6	V
V_{DDA}	DCDC driver supply voltage		2.3	3.3	3.6	V
V_{DDD}	Supply voltage			1.8		
V_{IH}	HIGH Level input voltage	Digital input pins	0.8xV_{DDIO}	--	V_{DDIO}	V
V_{IL}	LOW Level input voltage	Digital input pins	GND	--	0.2xV_{DDIO}	V
V_{OH}	HIGH Level output voltage	Digital output pins, I_{OH}=400uA	0.8xV_{DDIO}	--	--	V
V_{OL}	LOW Level Output voltage	Digital output pins, I_{OL}=-400uA	GND	--	0.2xV_{DDIO}	V
I_{IN}	Input leakage current	Digital input pins except pull-up, pull-down pin	-1.0	--	1.0	uA
R_{IN}	Pull-up/down impedance			200		KΩ
I_{VDD}	Digital deep sleep current	VDDD OFF	--	0.1	--	uA
	Digital stand-by current	VDD=3.3V, all stopped	--	0.5	2.0	uA
	Digital operating current	VDD=3.3V				uA
I_{VDDIO}	IO deep sleep current	VDDD OFF		0.4	1.0	uA
	IO stand-by current	VDDIO=3.3V, all stopped		--	0.2	uA
	IO operating current	VDDIO=3.3V				uA
I_{VDDA}	Analog deep sleep current	all stopped (power off mode)		0.3		uA
	Analog stand-by current	VDDA=3.3V, all stopped				uA
	Analog operating current	VDDA=3.3V DC/DC ON No waveform output, fdcdc=250kHz, External cap :415pF NMOS=340pF, No load		--	2	mA
Top	Operating temperature		-30		85	^{o}C
Note: TYP. and MAX. values are to be confirmed by design.						

ANALOG DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VSH	Supply Voltage	For source driver/VCOM		15		V
dVSH	Supply voltage deviation		-300	0	+300	mV
VSL	Supply Voltage	For source driver/VCOM		-15		V
dVSL	Supply voltage deviation		-300	0	+300	mV
Idd	Analog Operating Current	No load,		TBD		mA
Vvd	Voltage Deviation of Outputs		--	±16	±35	mV
Vdr	Dynamic Range of Output		0.1	--	VSH-0.1	V
VGH-VGL	Voltage Range of VGH - VGL		12		40	V
VGL	VGL voltage Range	For gate driver	-20		-18	V
dVGL	VGL Supply voltage dev		-400	0	+400	mV
VGH	VGH voltage Range	For gate driver	20		22	V
dVGH	VGH Supply voltage dev		-400	0	+400	mV
IstVSH	Positve HV Stand-by Current (power off mode)	Include VSH power With load	-	0	0.01	µA
IVSH	Positve HV Operating Current	Include VSH power With load all SD=L VCOM external resistor divider not included	-	0.7	1.1	mA
		Include VSH power With load all SD=H VCOM external resistor divider not included	-	0.8	1.2	mA
IstVSL	Negative HV Stand-by Current (power off mode)	Include VSL power With load	-	0	0.01	µA
IVSL	Negative HV Operating Current	Include VSL power With load all SD=L	-	0.8	1.2	mA
		Include VSL power With load all SD=H	-	0.9	1.3	mA
Note: TYP. and MAX. values are to be confirmed by design.						

AC CHARACTERISTICS

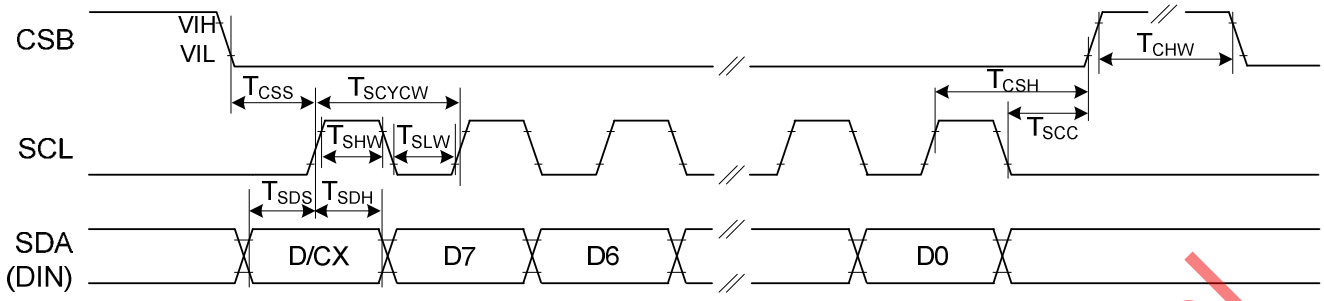


Figure: 3-wire Serial Interface Characteristics (Write mode)

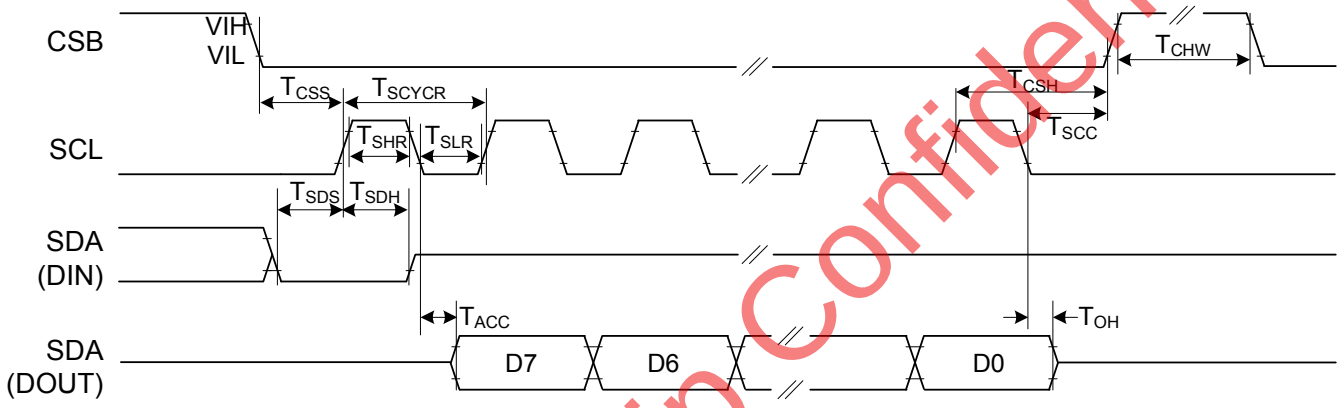


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

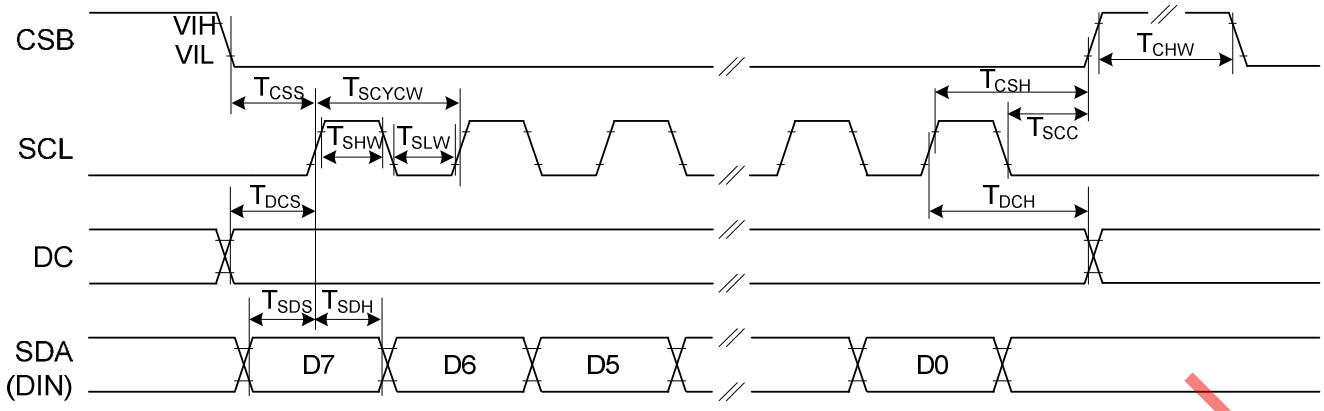


Figure: 4-wire Serial Interface Characteristics (Write mode)

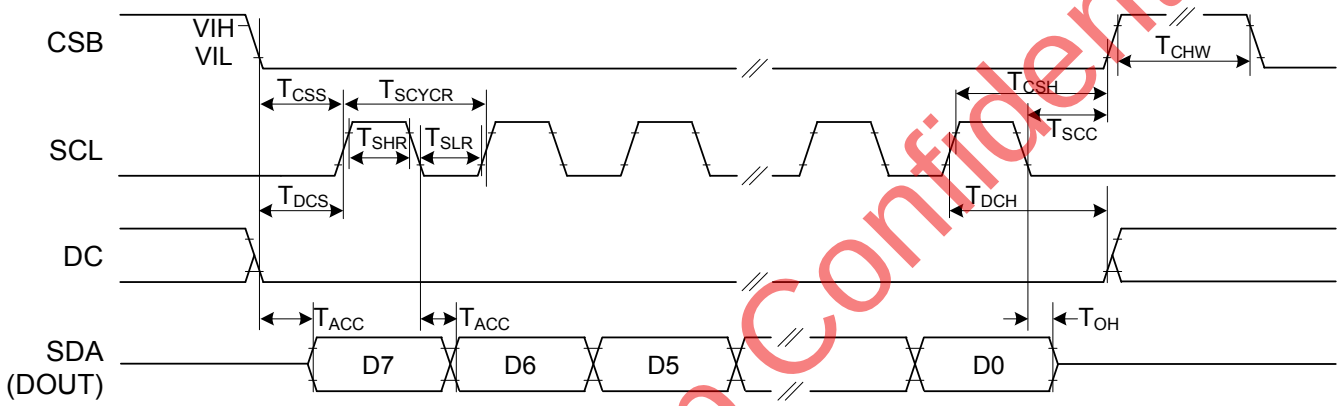
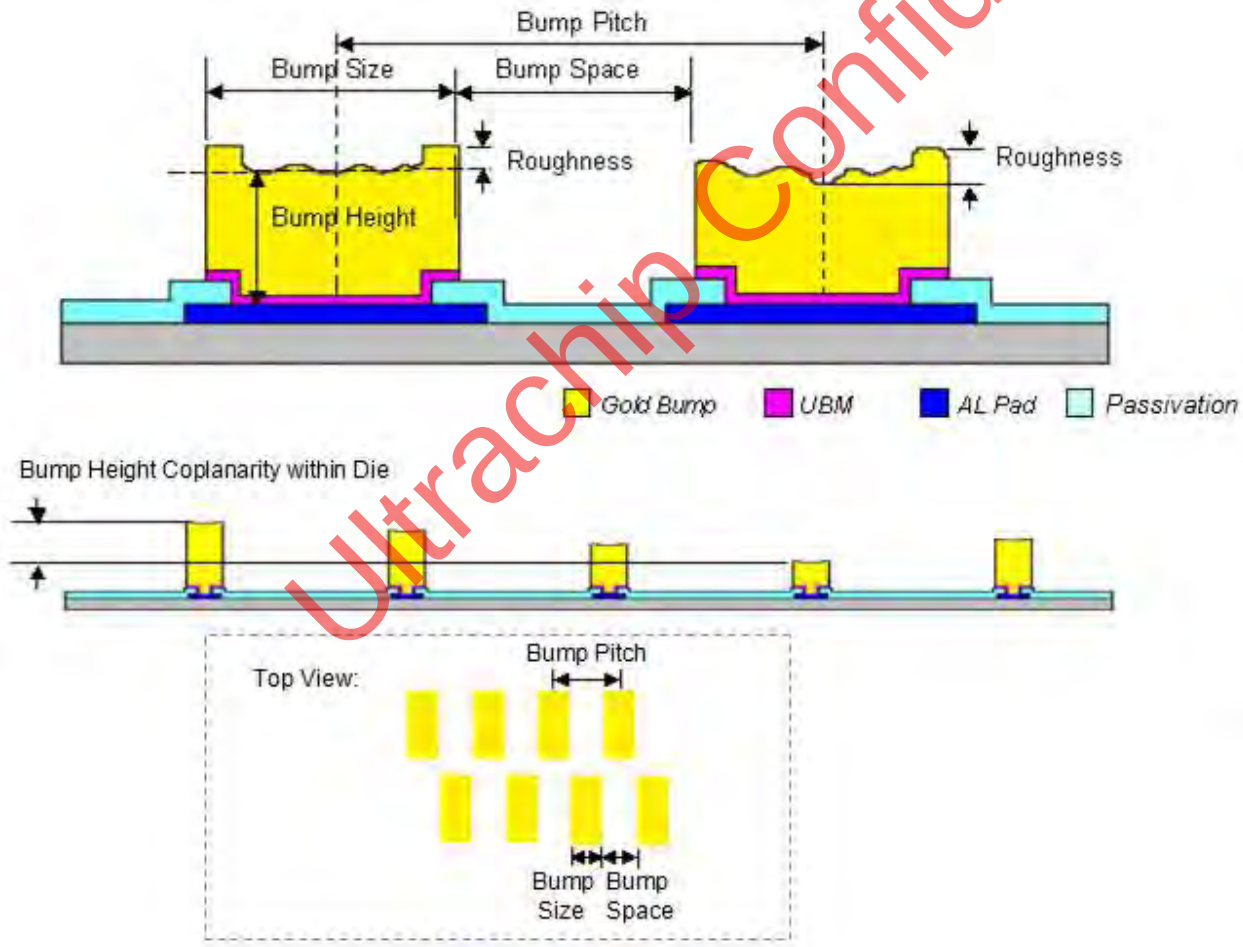


Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	150			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			50	ns
T_{OH}		Output disable time	15			ns

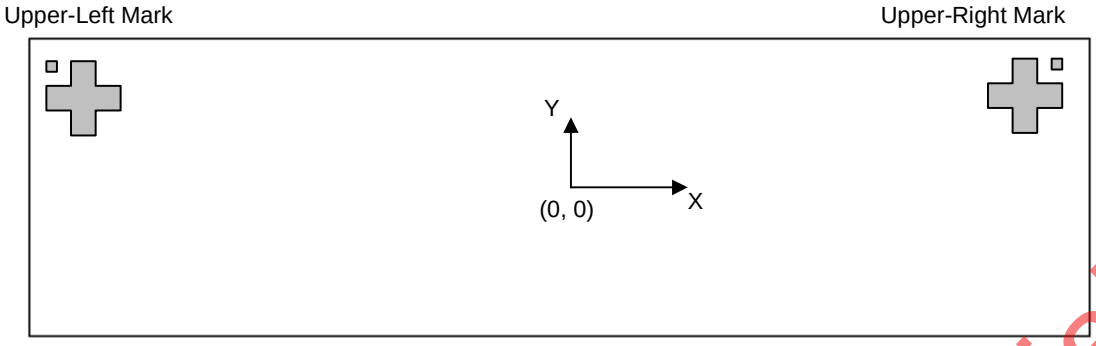
PHYSICAL DIMENSIONS

Die Size:	(17620 μM ± 40μM) x (1670 μM ± 40μM)
Die Thickness:	180 μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Hardness:	65 Hv ± 15Hv
Bump Size:	12 μM x 100 μM ± 2μM
Bump Area:	1200 μM^2
Bump Pitch:	30 μM
Bump Gap:	20.38 μM ± 3μM
Shear:	⩾ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center

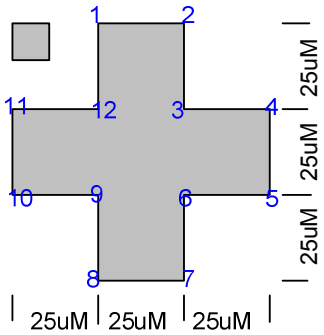


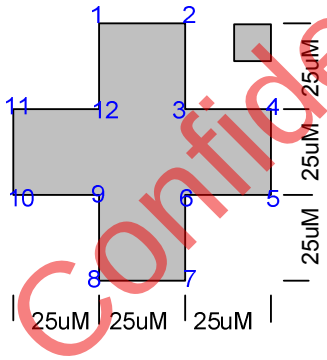
ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:





Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-8700	725	8700	725
1	-8712.5	762.5	8687.5	762.5
2	-8687.5	762.5	8712.5	762.5
3	-8687.5	737.5	8712.5	737.5
4	-8662.5	737.5	8737.5	737.5
5	-8662.5	712.5	8737.5	712.5
6	-8687.5	712.5	8712.5	712.5
7	-8687.5	687.5	8712.5	687.5
8	-8712.5	687.5	8687.5	687.5
9	-8712.5	712.5	8687.5	712.5
10	-8737.5	712.5	8662.5	712.5
11	-8737.5	737.5	8662.5	737.5
12	-8712.5	737.5	8687.5	737.5

PAD COORDINATES

No.	Name	X	Y	W	H
1	DUMMY	-8610	-755	40	50
2	VCOM	-8550	-755	40	50
3	VCOM	-8490	-755	40	50
4	VCOM	-8430	-755	40	50
5	VCOM	-8370	-755	40	50
6	VCOM	-8310	-755	40	50
7	VCOM	-8250	-755	40	50
8	VCOM	-8190	-755	40	50
9	VCOM	-8130	-755	40	50
10	PATH1	-8070	-755	40	50
11	VDM	-8010	-755	40	50
12	VDM	-7950	-755	40	50
13	VGL	-7890	-755	40	50
14	VGL	-7830	-755	40	50
15	VGL	-7770	-755	40	50
16	VGL	-7710	-755	40	50
17	VGL	-7650	-755	40	50
18	VGL	-7590	-755	40	50
19	VGL	-7530	-755	40	50
20	VGL	-7470	-755	40	50
21	VGL	-7410	-755	40	50
22	VGL	-7350	-755	40	50
23	VGL	-7290	-755	40	50
24	VGL	-7230	-755	40	50
25	VGL	-7170	-755	40	50
26	VGL	-7110	-755	40	50
27	VGL	-7050	-755	40	50
28	VGL	-6990	-755	40	50
29	GNDA	-6930	-755	40	50
30	VSL	-6870	-755	40	50
31	VSL	-6810	-755	40	50
32	VSL	-6750	-755	40	50
33	VSL	-6690	-755	40	50
34	VSL	-6630	-755	40	50
35	VSL	-6570	-755	40	50
36	VSL	-6510	-755	40	50
37	VSL	-6450	-755	40	50
38	VSL	-6390	-755	40	50
39	VSL	-6330	-755	40	50
40	GNDA	-6270	-755	40	50
42	VSL_LV	-6210	-755	40	50
41	VSL_LV	-6150	-755	40	50
43	VSL_LV	-6090	-755	40	50
44	VSL_LV	-6030	-755	40	50
45	VSL_LV	-5970	-755	40	50
46	VSL_LV	-5910	-755	40	50
47	VSL_LV	-5850	-755	40	50
48	VSL_LV	-5790	-755	40	50
49	VSL_LV	-5730	-755	40	50
50	VSL_LV	-5670	-755	40	50
51	GNDA	-5610	-755	40	50
52	VSL_LVX	-5550	-755	40	50
53	VSL_LVX	-5490	-755	40	50
54	VSL_LVX	-5430	-755	40	50
55	VSL_LVX	-5370	-755	40	50
56	VSL_LVX	-5310	-755	40	50
57	VSL_LVX	-5250	-755	40	50
58	VSL_LVX	-5190	-755	40	50

No.	Name	X	Y	W	H
59	VSL_LVX	-5130	-755	40	50
60	GNDA	-5070	-755	40	50
61	VGH	-5010	-755	40	50
62	VGH	-4950	-755	40	50
63	VGH	-4890	-755	40	50
64	VGH	-4830	-755	40	50
65	VGH	-4770	-755	40	50
66	VGH	-4710	-755	40	50
67	VGH	-4650	-755	40	50
68	VGH	-4590	-755	40	50
69	VGH	-4530	-755	40	50
70	VGH	-4470	-755	40	50
71	VGH	-4410	-755	40	50
72	VGH	-4350	-755	40	50
73	GNDA	-4290	-755	40	50
74	VSH	-4230	-755	40	50
75	VSH	-4170	-755	40	50
76	VSH	-4110	-755	40	50
77	VSH	-4050	-755	40	50
78	VSH	-3990	-755	40	50
79	VSH	-3930	-755	40	50
80	VSH	-3870	-755	40	50
81	VSH	-3810	-755	40	50
82	VSH	-3750	-755	40	50
83	VSH	-3690	-755	40	50
84	GNDA	-3630	-755	40	50
85	VSH_LV	-3570	-755	40	50
86	VSH_LV	-3510	-755	40	50
87	VSH_LV	-3450	-755	40	50
88	VSH_LV	-3390	-755	40	50
89	VSH_LV	-3330	-755	40	50
90	VSH_LV	-3270	-755	40	50
91	VSH_LV	-3210	-755	40	50
92	VSH_LV	-3150	-755	40	50
93	VSH_LV	-3090	-755	40	50
94	VSH_LV	-3030	-755	40	50
95	GNDA	-2970	-755	40	50
96	VSH_LVX	-2910	-755	40	50
97	VSH_LVX	-2850	-755	40	50
98	VSH_LVX	-2790	-755	40	50
99	VSH_LVX	-2730	-755	40	50
100	VSH_LVX	-2670	-755	40	50
101	VSH_LVX	-2610	-755	40	50
102	VSH_LVX	-2550	-755	40	50
103	VSH_LVX	-2490	-755	40	50
104	GNDA	-2430	-755	40	50
105	VDDD	-2370	-755	40	50
106	VDDD	-2310	-755	40	50
107	VDDD	-2250	-755	40	50
108	VDDD	-2190	-755	40	50
109	VDDD	-2130	-755	40	50
110	VDDD	-2070	-755	40	50
111	VDDDO	-2010	-755	40	50
112	VDDDO	-1950	-755	40	50
113	VDDDO	-1890	-755	40	50
114	VDDDO	-1830	-755	40	50
115	VDDDO	-1770	-755	40	50
116	VDDDO	-1710	-755	40	50

No.	Name	X	Y	W	H
117	GND	-1650	-755	40	50
118	VDM	-1590	-755	40	50
119	VDM	-1530	-755	40	50
120	GND	-1470	-755	40	50
121	GND	-1410	-755	40	50
122	GND	-1350	-755	40	50
123	GND	-1290	-755	40	50
124	GND	-1230	-755	40	50
125	GND	-1170	-755	40	50
126	GND	-1110	-755	40	50
127	GND	-1050	-755	40	50
128	GND	-990	-755	40	50
129	GND	-930	-755	40	50
130	GNDA	-870	-755	40	50
131	GNDA	-810	-755	40	50
132	GNDA	-750	-755	40	50
133	GNDA	-690	-755	40	50
134	GNDA	-630	-755	40	50
135	GNDA	-570	-755	40	50
136	GNDA	-510	-755	40	50
137	GNDA	-450	-755	40	50
138	GNDA	-390	-755	40	50
139	GNDA	-330	-755	40	50
140	GNDA	-270	-755	40	50
141	VDDA	-210	-755	40	50
142	VDDA	-150	-755	40	50
143	VDDA	-90	-755	40	50
144	VDDA	-30	-755	40	50
145	VDDA	30	-755	40	50
146	VDDA	90	-755	40	50
147	VDDA	150	-755	40	50
148	VDDA	210	-755	40	50
149	VDDA	270	-755	40	50
150	VDDA	330	-755	40	50
151	VDD	390	-755	40	50
152	VDD	450	-755	40	50
153	VDD	510	-755	40	50
154	VDD	570	-755	40	50
155	VDD	630	-755	40	50
156	VDD	690	-755	40	50
157	VDD	750	-755	40	50
158	VDD	810	-755	40	50
159	VDD	870	-755	40	50
160	VDD	930	-755	40	50
161	TEST1	990	-755	40	50
162	TEST2	1050	-755	40	50
163	VDDIO	1110	-755	40	50
164	VDDIO	1170	-755	40	50
165	VDDIO	1230	-755	40	50
166	VDDIO	1290	-755	40	50
167	TEST3	1350	-755	40	50
168	XCLK	1410	-755	40	50
169	XSTL	1470	-755	40	50
170	XOE	1530	-755	40	50
171	XLE	1590	-755	40	50
172	EDATA<0>	1650	-755	40	50
173	EDATA<1>	1710	-755	40	50
174	EDATA<2>	1770	-755	40	50
175	EDATA<3>	1830	-755	40	50
176	EDATA<4>	1890	-755	40	50

No.	Name	X	Y	W	H
177	EDATA<5>	1950	-755	40	50
178	EDATA<6>	2010	-755	40	50
179	EDATA<7>	2070	-755	40	50
180	GND	2130	-755	40	50
181	GCLK	2190	-755	40	50
182	STV	2250	-755	40	50
183	VDDIO	2310	-755	40	50
184	XON	2370	-755	40	50
185	DEN	2430	-755	40	50
186	GND	2490	-755	40	50
187	GND	2550	-755	40	50
188	FCSB	2610	-755	40	50
189	GND	2670	-755	40	50
190	FSCL	2730	-755	40	50
191	GND	2790	-755	40	50
192	FSDO	2850	-755	40	50
193	FSDI	2910	-755	40	50
194	SCL	2970	-755	40	50
195	SDA	3030	-755	40	50
196	GND	3090	-755	40	50
197	CSB	3150	-755	40	50
198	VDDIO	3210	-755	40	50
199	MFCSB	3270	-755	40	50
200	GND	3330	-755	40	50
201	DC	3390	-755	40	50
202	VDDIO	3450	-755	40	50
203	FMSDO	3510	-755	40	50
204	BUSY_N	3570	-755	40	50
205	GND	3630	-755	40	50
206	RST_N	3690	-755	40	50
207	TESTVDD	3750	-755	40	50
208	DUMMY	3810	-755	40	50
209	DUMMY	3870	-755	40	50
210	VDDIO	3930	-755	40	50
211	BS	3990	-755	40	50
212	GND	4050	-755	40	50
213	GND	4110	-755	40	50
214	VDD	4170	-755	40	50
215	VDD	4230	-755	40	50
216	VDDA	4290	-755	40	50
217	VDDA	4350	-755	40	50
218	TSDA	4410	-755	40	50
219	TSDA	4470	-755	40	50
220	TSCL	4530	-755	40	50
221	TSCL	4590	-755	40	50
222	GND	4650	-755	40	50
223	TEST4	4710	-755	40	50
224	GND	4770	-755	40	50
225	TEST5	4830	-755	40	50
226	GND	4890	-755	40	50
227	TEST6	4950	-755	40	50
228	GND	5010	-755	40	50
229	TEST7	5070	-755	40	50
230	TEST8	5130	-755	40	50
231	TEST9	5190	-755	40	50
232	TEST10	5250	-755	40	50
233	TEST11	5310	-755	40	50
234	TEST12	5370	-755	40	50
235	TEST13	5430	-755	40	50
236	TEST14	5490	-755	40	50

No.	Name	X	Y	W	H
237	TEST15	5550	-755	40	50
238	VCOMVS<0>	5610	-755	40	50
239	VCOMVS<1>	5670	-755	40	50
240	FSOURCE	5730	-755	40	50
241	FSOURCE	5790	-755	40	50
242	FSOURCE	5850	-755	40	50
243	VPPM	5910	-755	40	50
244	VPPM	5970	-755	40	50
245	VPPM	6030	-755	40	50
246	VPPM	6090	-755	40	50
247	VPPM	6150	-755	40	50
248	VPPM	6210	-755	40	50
249	VGH	6270	-755	40	50
250	VGH	6330	-755	40	50
251	VGH	6390	-755	40	50
252	VGH	6450	-755	40	50
253	VGH	6510	-755	40	50
254	VGH	6570	-755	40	50
255	VGH	6630	-755	40	50
256	VGH	6690	-755	40	50
257	VGL	6750	-755	40	50
258	VGL	6810	-755	40	50
259	VGL	6870	-755	40	50
260	VGL	6930	-755	40	50
261	VGL	6990	-755	40	50
262	VGL	7050	-755	40	50
263	VGL	7110	-755	40	50
264	GNDA	7170	-755	40	50
265	FB	7230	-755	40	50
266	FB	7290	-755	40	50
267	GNDA	7350	-755	40	50
268	RESE	7410	-755	40	50
269	RESE	7470	-755	40	50
270	GNDA	7530	-755	40	50
271	GDR	7590	-755	40	50
272	GDR	7650	-755	40	50
273	GDR	7710	-755	40	50
274	GDR	7770	-755	40	50
275	GDR	7830	-755	40	50
276	GDR	7890	-755	40	50
277	VDM	7950	-755	40	50
278	VDM	8010	-755	40	50
279	PATH1	8070	-755	40	50
280	VCOM	8130	-755	40	50
281	VCOM	8190	-755	40	50
282	VCOM	8250	-755	40	50
283	VCOM	8310	-755	40	50
284	VCOM	8370	-755	40	50
285	VCOM	8430	-755	40	50
286	VCOM	8490	-755	40	50
287	VCOM	8550	-755	40	50
288	DUMMY	8610	-755	40	50
289	DUMMY	8617	626	12	100
290	DUMMY	8602	751	12	100
291	G<0>	8587	626	12	100
292	G<2>	8572	751	12	100
293	G<4>	8557	626	12	100
294	G<6>	8542	751	12	100
295	G<8>	8527	626	12	100
296	G<10>	8512	751	12	100

No.	Name	X	Y	W	H
297	G<12>	8497	626	12	100
298	G<14>	8482	751	12	100
299	G<16>	8467	626	12	100
300	G<18>	8452	751	12	100
301	G<20>	8437	626	12	100
302	G<22>	8422	751	12	100
303	G<24>	8407	626	12	100
304	G<26>	8392	751	12	100
305	G<28>	8377	626	12	100
306	G<30>	8362	751	12	100
307	G<32>	8347	626	12	100
308	G<34>	8332	751	12	100
309	G<36>	8317	626	12	100
310	G<38>	8302	751	12	100
311	G<40>	8287	626	12	100
312	G<42>	8272	751	12	100
313	G<44>	8257	626	12	100
314	G<46>	8242	751	12	100
315	G<48>	8227	626	12	100
316	G<50>	8212	751	12	100
317	G<52>	8197	626	12	100
318	G<54>	8182	751	12	100
319	G<56>	8167	626	12	100
320	G<58>	8152	751	12	100
321	G<60>	8137	626	12	100
322	G<62>	8122	751	12	100
323	G<64>	8107	626	12	100
324	G<66>	8092	751	12	100
325	G<68>	8077	626	12	100
326	G<70>	8062	751	12	100
327	G<72>	8047	626	12	100
328	G<74>	8032	751	12	100
329	G<76>	8017	626	12	100
330	G<78>	8002	751	12	100
331	G<80>	7987	626	12	100
332	G<82>	7972	751	12	100
333	G<84>	7957	626	12	100
334	G<86>	7942	751	12	100
335	G<88>	7927	626	12	100
336	G<90>	7912	751	12	100
337	G<92>	7897	626	12	100
338	G<94>	7882	751	12	100
339	G<96>	7867	626	12	100
340	G<98>	7852	751	12	100
341	G<100>	7837	626	12	100
342	G<102>	7822	751	12	100
343	G<104>	7807	626	12	100
344	G<106>	7792	751	12	100
345	G<108>	7777	626	12	100
346	G<110>	7762	751	12	100
347	G<112>	7747	626	12	100
348	G<114>	7732	751	12	100
349	G<116>	7717	626	12	100
350	G<118>	7702	751	12	100
351	G<120>	7687	626	12	100
352	G<122>	7672	751	12	100
353	G<124>	7657	626	12	100
354	G<126>	7642	751	12	100
355	G<128>	7627	626	12	100
356	G<130>	7612	751	12	100

No.	Name	X	Y	W	H
357	G<132>	7597	626	12	100
358	G<134>	7582	751	12	100
359	G<136>	7567	626	12	100
360	G<138>	7552	751	12	100
361	G<140>	7537	626	12	100
362	G<142>	7522	751	12	100
363	G<144>	7507	626	12	100
364	G<146>	7492	751	12	100
365	G<148>	7477	626	12	100
366	G<150>	7462	751	12	100
367	G<152>	7447	626	12	100
368	G<154>	7432	751	12	100
369	G<156>	7417	626	12	100
370	G<158>	7402	751	12	100
371	G<160>	7387	626	12	100
372	G<162>	7372	751	12	100
373	G<164>	7357	626	12	100
374	G<166>	7342	751	12	100
375	G<168>	7327	626	12	100
376	G<170>	7312	751	12	100
377	G<172>	7297	626	12	100
378	G<174>	7282	751	12	100
379	G<176>	7267	626	12	100
380	G<178>	7252	751	12	100
381	G<180>	7237	626	12	100
382	G<182>	7222	751	12	100
383	G<184>	7207	626	12	100
384	G<186>	7192	751	12	100
385	G<188>	7177	626	12	100
386	G<190>	7162	751	12	100
387	G<192>	7147	626	12	100
388	G<194>	7132	751	12	100
389	G<196>	7117	626	12	100
390	G<198>	7102	751	12	100
391	G<200>	7087	626	12	100
392	G<202>	7072	751	12	100
393	G<204>	7057	626	12	100
394	G<206>	7042	751	12	100
395	G<208>	7027	626	12	100
396	G<210>	7012	751	12	100
397	G<212>	6997	626	12	100
398	G<214>	6982	751	12	100
399	G<216>	6967	626	12	100
400	G<218>	6952	751	12	100
401	G<220>	6937	626	12	100
402	G<222>	6922	751	12	100
403	G<224>	6907	626	12	100
404	G<226>	6892	751	12	100
405	G<228>	6877	626	12	100
406	G<230>	6862	751	12	100
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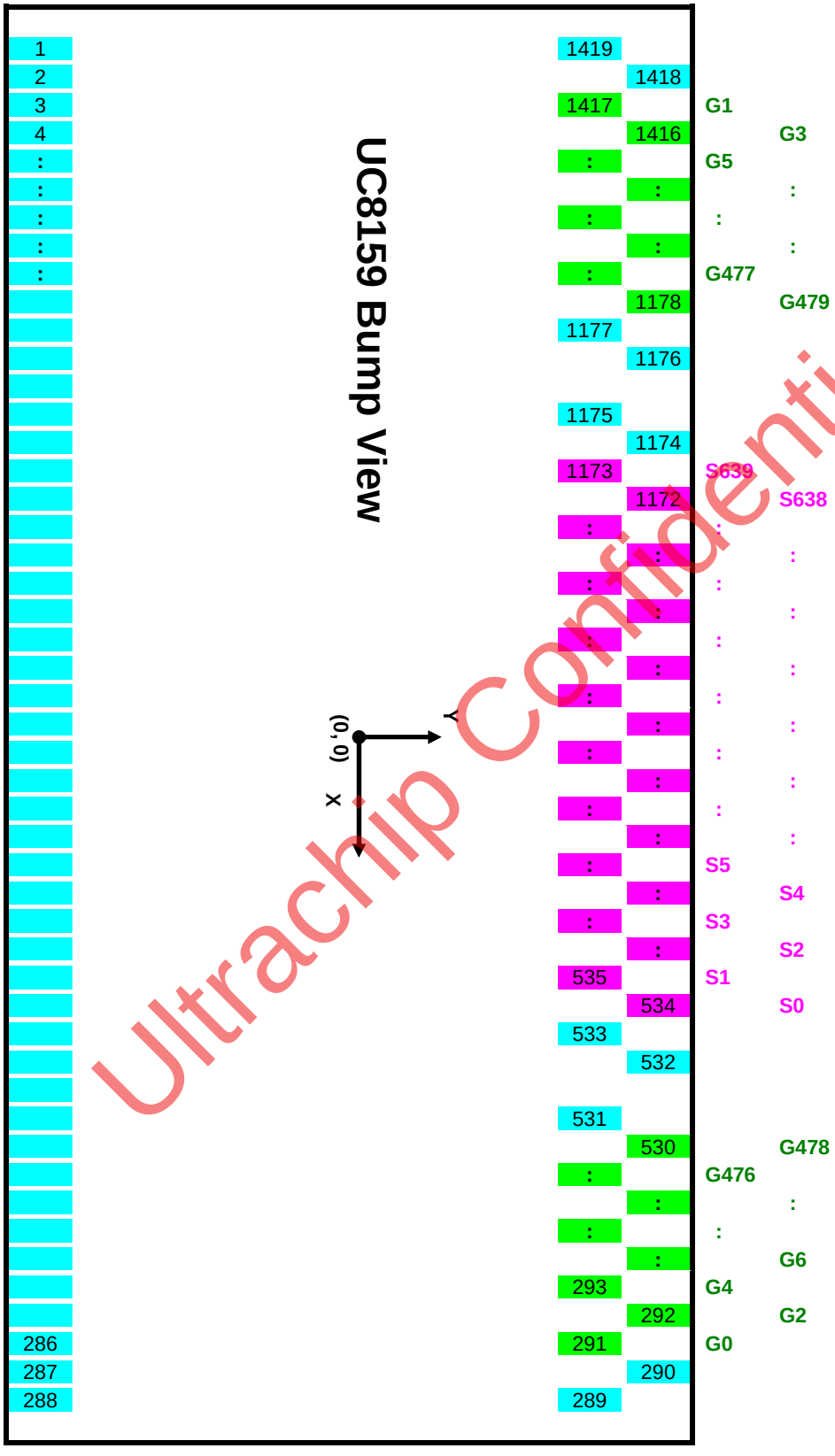
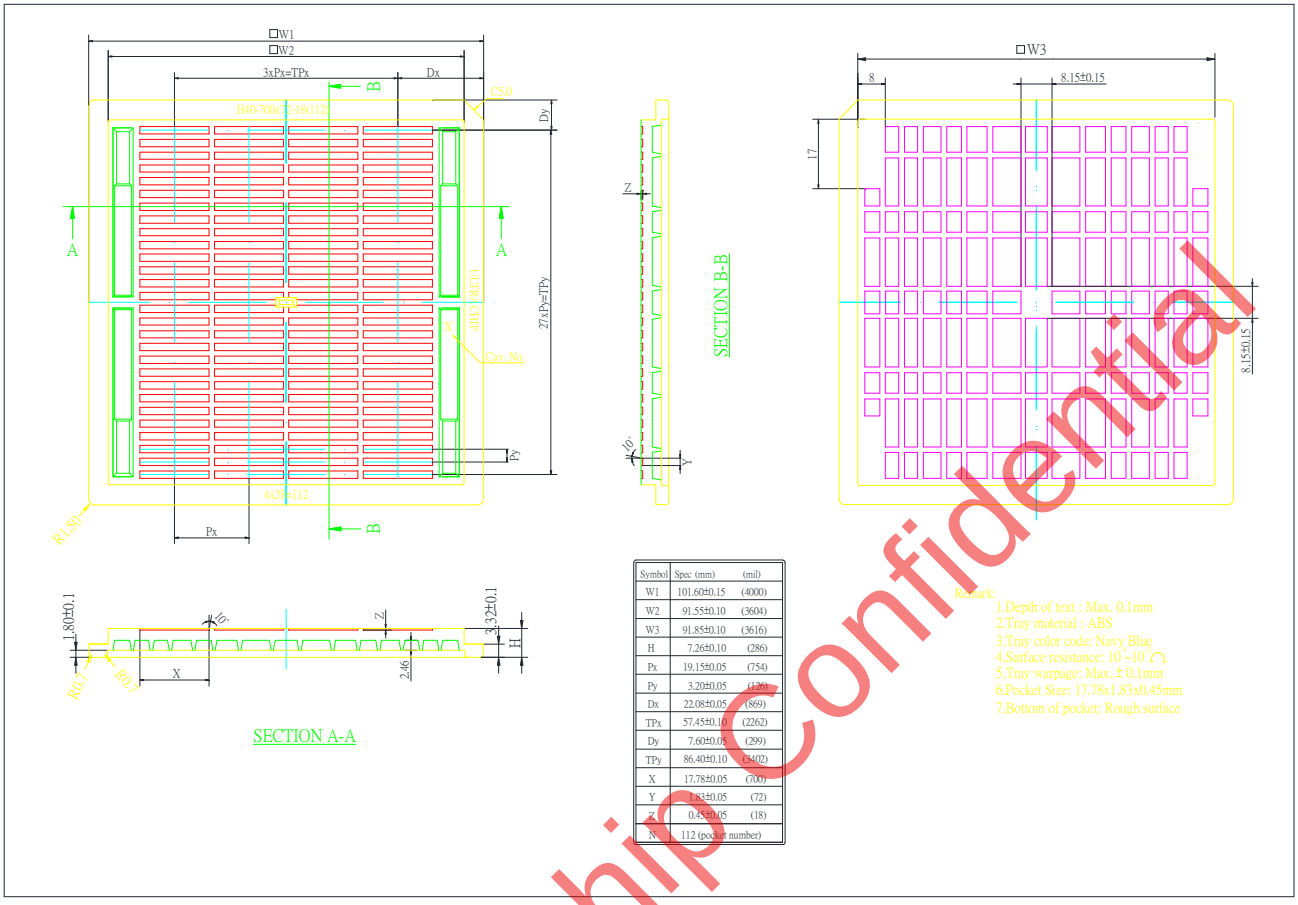
Output Pad Loacation :



TRAY INFORMATION



Symbol	Spec (mm)	(mil)
W1	101.60±0.15	(4000)
W2	91.55±0.10	(3604)
W3	91.85±0.10	(3616)
H	7.26±0.10	(286)
Px	19.15±0.05	(754)
Py	3.20±0.05	(126)
Dx	22.08±0.05	(869)
TPx	57.45±0.10	(2262)
Dy	7.60±0.05	(299)
TPy	86.40±0.10	(3402)
X	17.78±0.05	(700)
Y	1.83±0.05	(72)
Z	0.45±0.05	(18)
N	112 (pocket number)	

Remark:
1.Depth of text : Max. 0.1mm
2.Tray material : ABS
3.Tray color code: Navy Blue
4.Surface resistance: 10^{7}~$10^{11}\,\Omega$
5.Tray warpage: Max. ± 0.1mm
6.Pocket Size: 17.78x1.83x0.45mm
7.Bottom of pocket: Rough surface

REVISION HISTORY

Revision	Contents	Date
	(N/A)	