

Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Digital Selection of High Mode EIA232E/CCITT V.28 only, and Low Mode EIA232E/V.28 & EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins

DESCRIPTION

The UC5171 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is accomplished by the select pin Ms logic "low" for low output mode (EIA232E/V.28 & EIA423A/V.10) or pin Ms logic "high" for high mode (EIA232E/V.28). High mode should only be used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20)	15V
V- (Pin 11)	-15V
PLCC Power Dissipation, TA = 25°C (Note 2)	1000 mW
DIP Power Dissipation, TA = 25°C (Note 2)	1250 mW
Input Voltage	-1.5V to +7V
Output Voltage	-12V to +12V
Slew Rate Resistor	2k to 10kΩ
Storage Temperature	-65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.

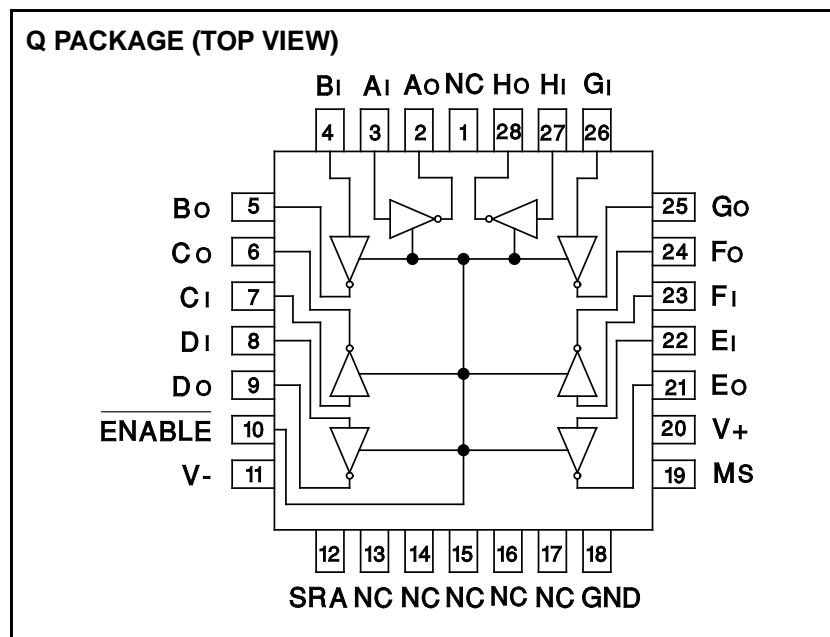
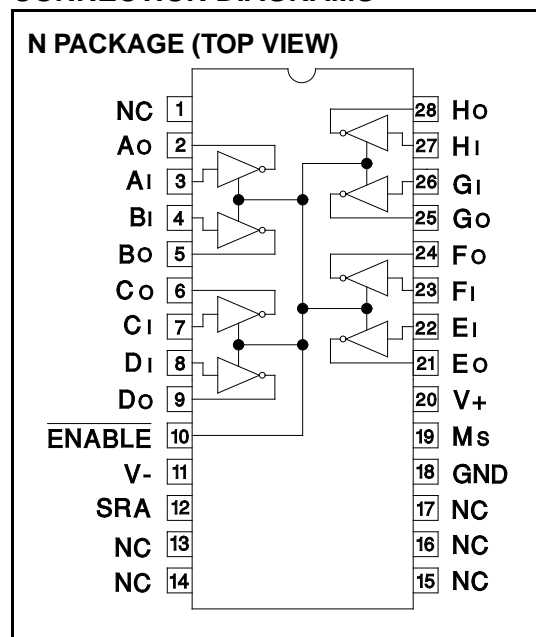
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

FUNCTIONAL TABLE

INPUTS		OUTPUTS	
EN	DATA	EIA-232E(3)	EIA-232E/EIA-423A
0	0	(V+)-3V	5V to 6V
0	1	(V-)+3V	-5V to -6V
1	X	High Z	High Z

Note 3: Minimum output swings.

CONNECTION DIAGRAMS



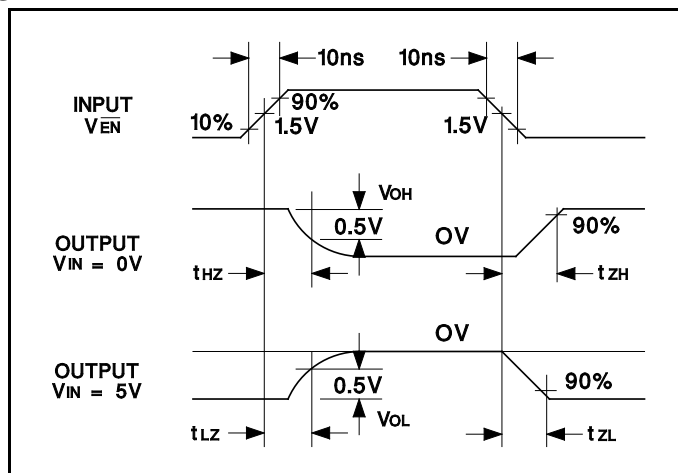
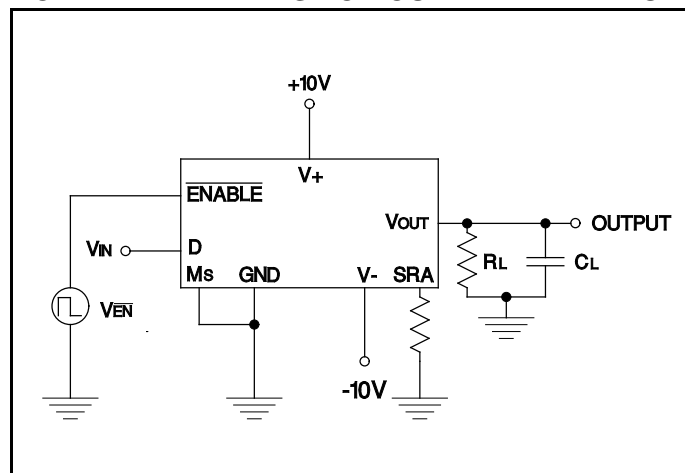
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V_+| = |V_-| = +10V$, $0 < T_A < +70^\circ C$, $M_S \leq 0.8V$, $R_{SRA} = +10k$, $T_A = T_J$.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V+ Range			9		15	V
V- Range			-15		-9	V
V+ Supply Current	I+	$R_L = \text{Infinite}$ $\overline{E_n} = 0V$		25	42	mA
V- Supply Current	I-	$R_L = \text{Infinite}$ $\overline{E_n} = 0V$	-42	-23		mA
INPUTS						
High Level Input Voltage	V _{IH}		2.0			V
Low Level Input Voltage	V _{IL}				0.8	V
Input Clamp Voltage	V _{IK}	I _I = -15 mA	-1.8	-1.1		V
High Level Input Current	I _{IH}	V _{IH} = 2.4V		0.25	40	μA
Low Level Input Current	I _{IL}	V _{IL} = 0.4V	-200	-8.0		μA
OUTPUTS						
High Level Output Voltage EIA232E (EIA423A)	V _{OH}	V _{IN} = 0.8V $\overline{E_n} = 0.8V$ R _L = Inf. R _L = 3k R _L = 450	5.0 5.0 4.5	5.3 5.3 5.2	6.0 6.0 6.0	V V V
Low Level Output Voltage EIA232E (EIA423A)	V _{OL}	V _{IN} = 2.0V $\overline{E_n} = 0.8V$ R _L = Inf. R _L = 3k R _L = 450	-6.0 -6.0 -6.0	-5.3 -5.3 -5.2	-5.0 -5.0 -4.5	V V V
Output Balance (EIA423A)	V _{BAL}	R _L = 450 V _{OH} + V _{OL} = V _{BAL}		0.2	0.4	V
High Level Output Voltage (EIA232E)	V _{OH}	V _{IN} = 0.8V, M _S = 2.0V $\overline{E_n} = 0.8V$ R _L = Inf. R _L = 3k	7.0 7.0	7.6 7.6	10 10	V V
Low Level Output Voltage (EIA232E)	V _{OL}	V _{IN} = 2.0V, M _S = 2.0V $\overline{E_n} = 0.8V$ R _L = Inf. R _L = 3k	-10 -10	-7.7 -7.7	-7.0 -7.0	V V
Off-State Output Current	I _{oz}	$\overline{E_n} = 2.0V$, V _O = ±6V, M _S = 2.0V	-100		100	μA
Short-Circuit Current	I _{os}	$\overline{E_n} = 0V$ V _{IN} = 0V V _{IN} = 5V	25 25	50 40		mA mA

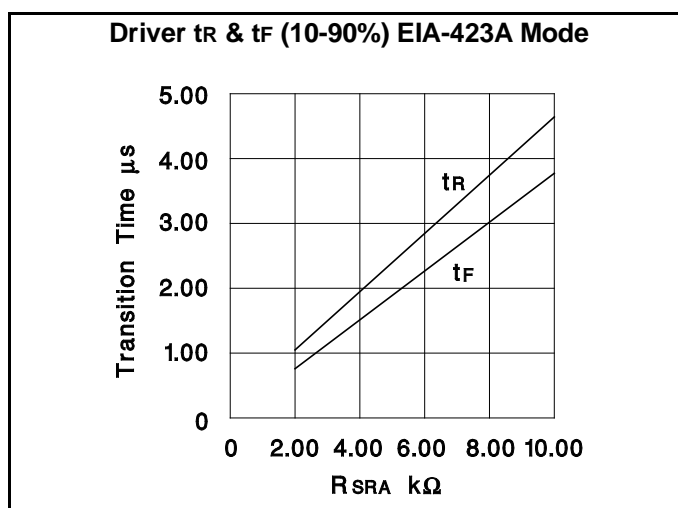
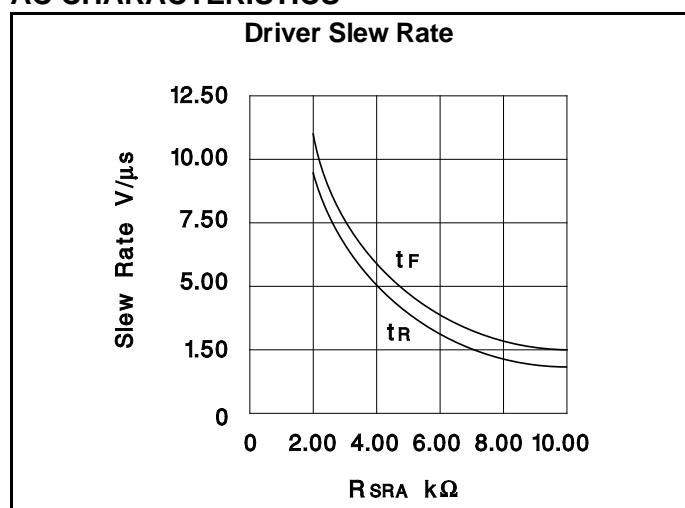
AC ELECTRICAL CHARACTERISTICS: at $|V_+| = |V_-| = +10V$, $0 < T_A < +70^\circ C$, $M_S \leq 0.8V$, $T_A = T_J$.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t _R	R _{SRA} = 2k	6.65	9.5	12.3	V/μs
	t _F	R _L = 450, C _L = 50pF	6.65	10	12.3	V/μs
Output Slew Rate	t _R	R _{SRA} = 10k	1.33	1.9	2.45	V/μs
	t _F	R _L = 450, C _L = 50pF	1.33	2.2	2.45	V/μs
Propagation Output to High Impedance	t _{HZ}	R _{SRA} = 10k		0.3	1.0	μs
	t _{LZ}	R _L = 450, C _L = 50pF		0.5	1.0	μs
Propagation High Impedance to Output	t _{ZH}	R _{SRA} = 10k		6.0	15	μs
	t _{ZL}	R _L = 450, C _L = 50pF		7.0	15	μs

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



AC CHARACTERISTICS



APPLICATIONS INFORMATION

Slew Rate Programming

Slew rate for the UC5171 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V_{\mu s} = \frac{20}{R_{SRA}} (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/μs, respectively. The relationship between slew rate and R_{SRA} is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = 100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s, t may be up to 300 microseconds.

Output Voltage Programming

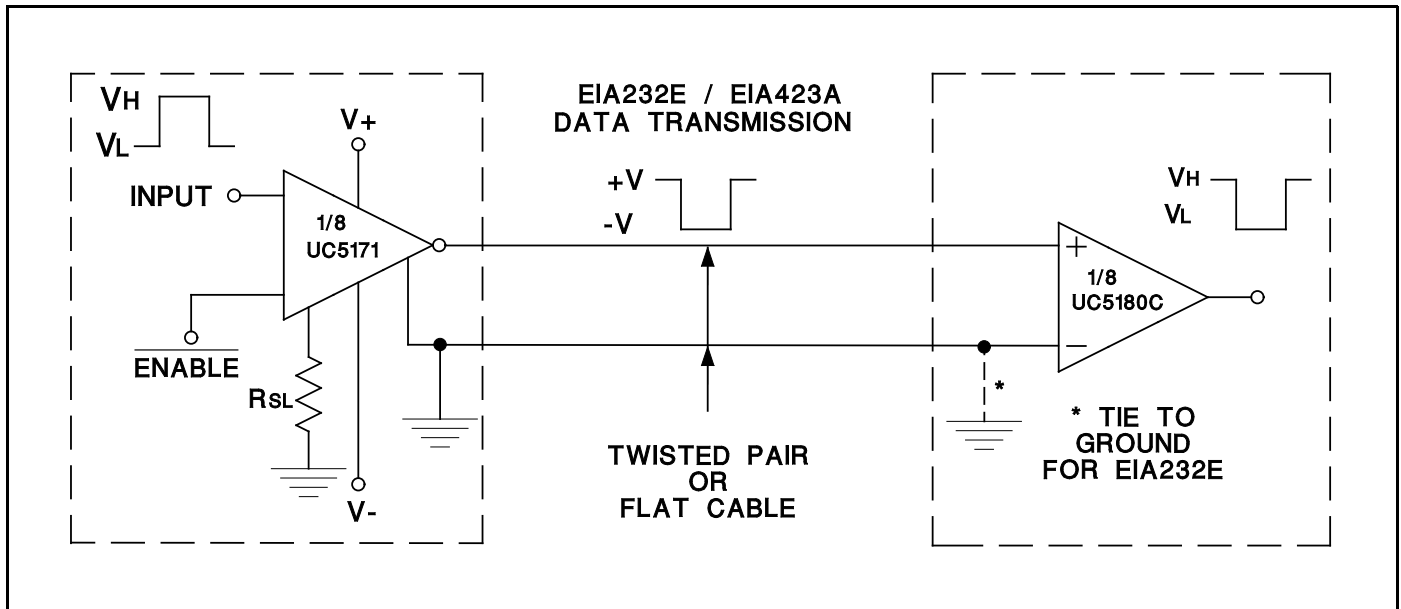
The UC5171 has two programmable output modes, either a low voltage mode which meets EIA-423A operational specifications, or the high output voltage mode which meets the EIA-232E specifications.

The high output mode provides greater output swings, minimum of 3V below the supply rails, for driving higher, attenuated lines. This mode is selected by connecting the modes select pin, (Ms), to a TTL "high" level. The low output mode provides a controlled output swing and is accomplished by connecting the mode select pin, (Ms), to a TTL "low level."

EIA Standards

The UC5171 meets or exceeds the EIA Standards for EIA-232E and EIA-423A modes of operation except under power down conditions. When powered down with the output attached to an active buss, the UC5171 has the potential to load the bus under transient conditions.

APPLICATIONS

**UC5171 Specific Layout Notes**

The UC5171 layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5171 on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5171 can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorb should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal-to-metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5171 is P6KEIOCA

*Transzorb is a trademark of General Semiconductor Industries.