

Precision Adjustable Shunt Regulator

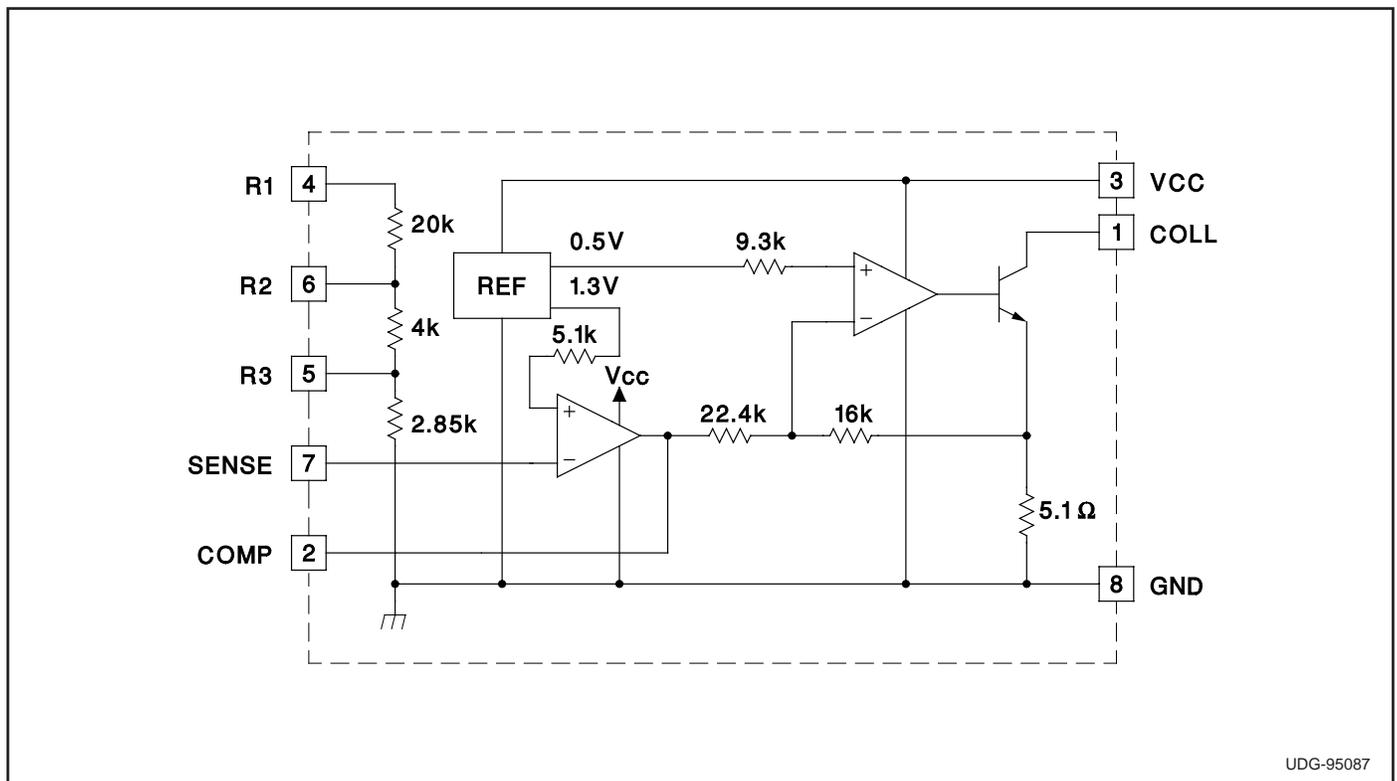
FEATURES

- Multiple On-Chip Programmable Reference Voltages
- 0.4% Initial Accuracy
- 0.7% Overall Reference Tolerance
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- 36.0V Operating Supply Voltage
- Reference Accuracy Maintained For Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Improved Architecture Provides a Known Linear Transconductance with a +5% Typical Tolerance

DESCRIPTION

The UC39431 is an adjustable shunt voltage regulator with 100mA sink capability. The architecture, comprised of an error amplifier and transconductance amplifier, gives the user separate control of the small signal error voltage frequency response along with a fixed linear transconductance. A minimum 3MHz gain bandwidth product for both the error and transconductance amplifiers assures fast response. In addition to external programming, the IC has three internal resistors that can be connected in six different configurations to provide regulated voltages of 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, and 12.24V. A sister device (UC39432) provides access to the non-inverting error amplifier input and reference, while eliminating the three internal resistors.

BLOCK DIAGRAM



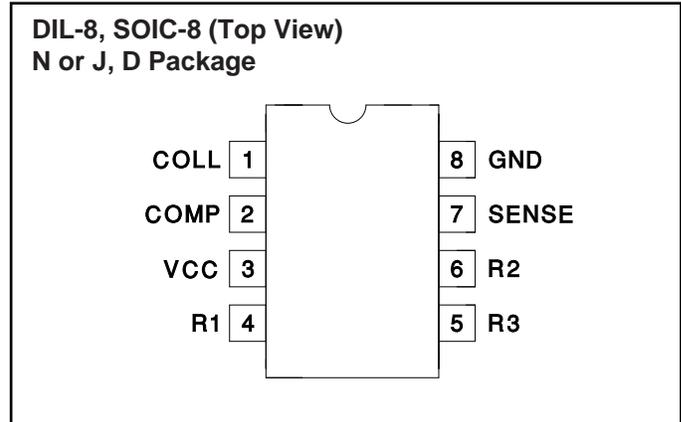
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ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V	36V
Regulated Output: V	36V
Internal Resistors: R1, R2, R3	13V
E/A Input: SENSE	6V
E/A Compensation: COMP	6V
Output Sink Current: I	140mA
Power Dissipation at $T_A \leq 25^\circ\text{C}$ (DIL-8)	1W
Derate 8mW/ $^\circ\text{C}$ for $T_A > 25^\circ\text{C}$	
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Junction Temperature	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	$+300^\circ\text{C}$

Currents are positive into negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ and COLL Output = 2.4V to 36.0V for the UC19431, $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ and COLL Output = 2.3V to 36.0V for the UC29431, and $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ and COLL Output = 2.3V to 36.0V for the UC39431/B, VCC = 15V, $I_{\text{COLL}} = 10\text{mA}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	$T_A = 25^\circ\text{C}$	19431*	1.295	1.3	1.305	V
		39431B	1.29	1.3	1.31	V
Reference Temperature Tolerance	$V_{\text{COLL}} = 5.0$	19431*	1.291	1.3	1.309	V
		39431B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.2V to 36.0V, $V_{\text{COLL}} = 5\text{V}$	19431*		10	38	mV
		39431B		10	57	mV
Reference Load Regulation	$I_{\text{COLL}} = 10\text{mA}$ to 50mA , $V_{\text{COLL}} = 5\text{V}$	19431*		10	38	mV
		39431B		10	57	mV
Sense Input Current				0.2	0.5	μA
Minimum Operating Current	VCC = 36.0V, $V_{\text{COLL}} = 5\text{V}$			0.50	0.80	mA
Collector Current Limit	$V_{\text{COLL}} = V_{\text{CC}} = 36.0\text{V}$, Ref = 1.35V			130	145	mA
Collector Saturation	$I_{\text{COLL}} = 20\text{mA}$		0.7	1.1	1.5	V
Transconductance (gm)	VCC = 2.4V to 36.0V, $V_{\text{COLL}} = 3\text{V}$, $I_{\text{COLL}} = 20\text{mA}$	19431*	-170	-140	-110	mS
		39431B	-180	-140	-100	mS
5.1V Reference	Internal Divider	19431*	5.05	5.1	5.15	V
		39431B	5	5.1	5.2	V
12.24V Reference	Internal Divider	19431*	12	12.24	12.5	V
		39431B	12	12.24	12.5	V
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

* Also applies to the UC29431 and UC39431

Note: The internal divider can be configured to give six unique references. These references are 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, 12.24V.

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is $g_m \cdot R_L$, where g_m is designed to be $-140\text{mS} \pm 30\text{mS}$ and R_L represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to

compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

R1, R2, R3: Connection points to the three internal resistors.

RESISTOR DIVIDER CONNECTION TABLE FOR SHUNT AND OPTO APPLICATIONS

To obtain the shunt regulated or optocoupler sensed voltage specified in the left column, connect the internal resistors (R1, R2, R3) as indicated.

REGULATED VOLTAGE	CONNECT R1 TO:	CONNECT R2 TO:	CONNECT R3 TO:
2.82V	SENSE (pin 7)	COLL (pin 1)	SENSE (pin 7)
3.12V	open	COLL (pin 1)	SENSE (pin 7)
5.1V	COLL (pin 1)	SENSE (pin 7)	open
7.8V	COLL (pin 1)	SENSE (pin 7)	GND (pin 8)
10.42V	COLL (pin 1)	SENSE (pin 7)	SENSE (pin 7)
12.24V	COLL (pin 1)	open	SENSE (pin 7)

FREQUENCY COMPENSATION

The UC39431 shunt regulator is designed with two independent gain stages. The error amplifier provides 90dB of gain with a typical gain bandwidth product of 5MHz. The error amplifier provides sufficient gain in order for the sense voltage to be accurately compared to the 1.3V on-chip reference. Complete control of the frequency response of the error amplifier is accomplished with the COMP pin. By putting negative feedback across the error amplifier, either a pole or a pole-zero can be added.

The second gain stage is the transconductance (g_m) amplifier. The g_m amplifier is designed with a known linear 140mS of transconductance. The voltage gain is consequently $g_m \cdot R_o$, where R_o is the output impedance at the collector pin. The frequency response

of the transconductance amplifier is controlled with the COLL pin. The gain bandwidth product of the g_m amplifier is typically 3MHz. A pole or pole-zero can be added to this stage by connecting a capacitor or a series capacitor and resistor between COLL and GND.

The compensation of a control loop containing the UC39431 is made easier due to the independent compensation capability of the error amplifier and g_m amplifier. As shown in the applications information, a pole-zero is created with a series resistor and capacitor between SENSE and COMP. The pole created is dominant, while the zero is used to increase the bandwidth and cancel the effects of the pole created by the capacitor between the COLL and GND pins.

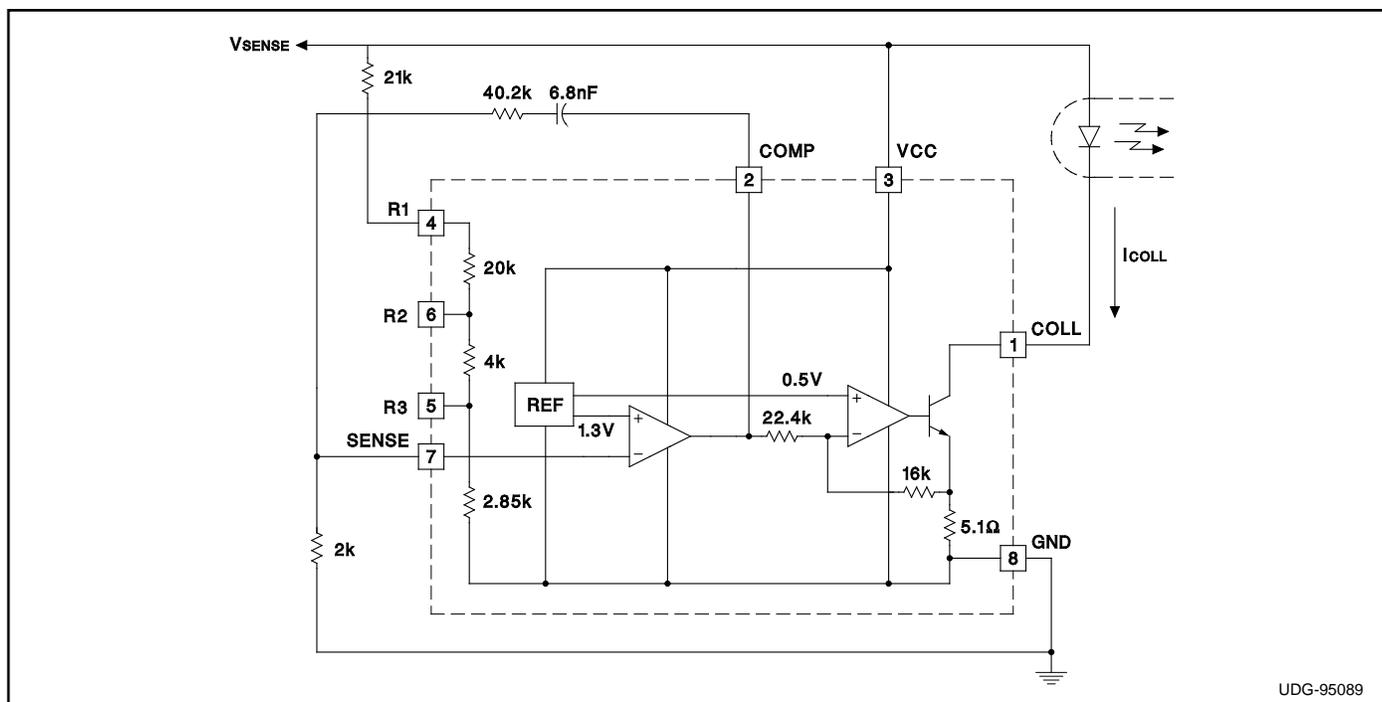


Figure 2. 15.0V Optocoupler Application

OPTOCOPLER APPLICATION

The two amplifier circuit architecture employed in the UC39431 is most advantageous for the optocoupler application. The error amplifier provides a fixed open loop gain that is available to apply flexible loop compensation of either poles or zeroes. A fixed transconductance amplifier provides a linear current source compared to the typical transistor's exponential output characteristics. It also eliminates the traditional optocoupler's CTR variations with power supply and voltage, and the need to suffer the additional voltage drop of a series resistor.

MAGNETIC AMPLIFIER CONTROLLER APPLICATION

The UC39431 makes an excellent controller for magnetic amplifier regulated outputs. Working from either a square wave drive or from a PWM signal controlled by another output, a saturable reactor provides highly efficient control, requiring only a reset current which can be generated from its own output.

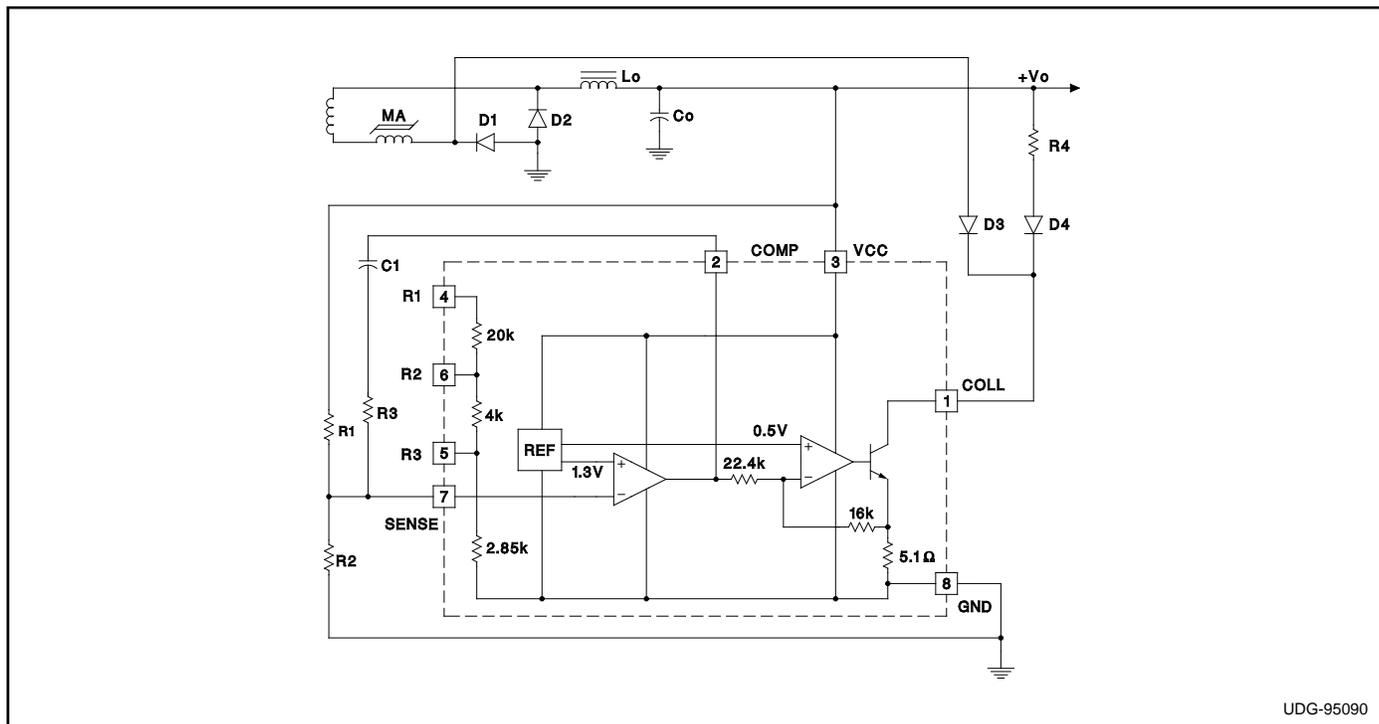


Figure 3. Magnetic Amplifier Controller Application

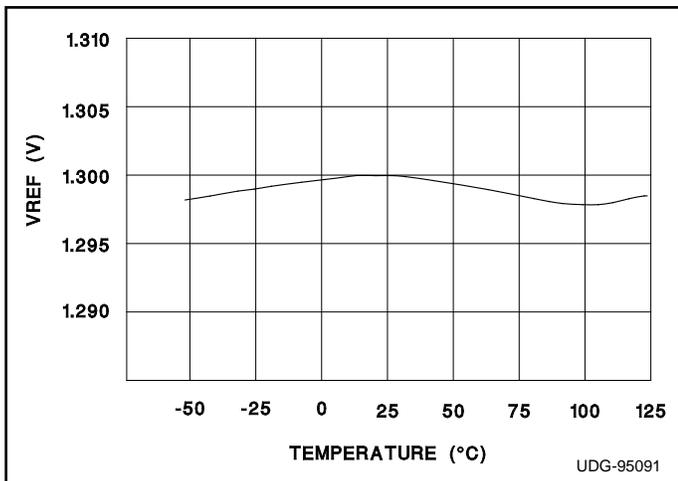


Figure 4. Internal 1.3V vs. Temperature

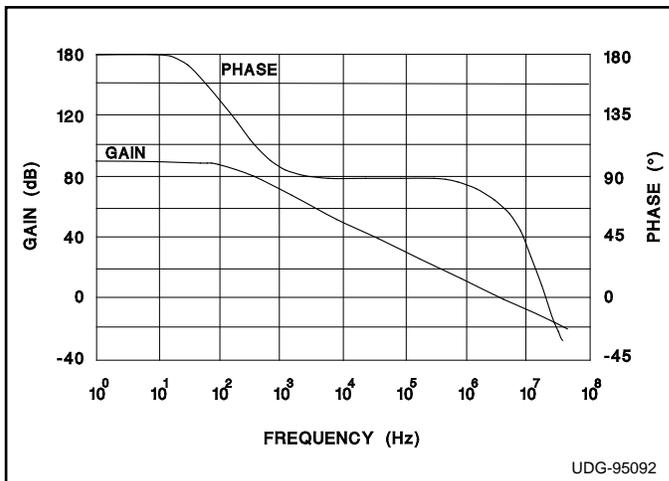


Figure 5. Error Amp Voltage Gain and Phase vs. Frequency