U430 SERIES

Siliconix incorporated

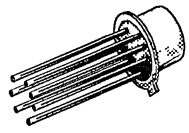
N-Channel JFET Pairs

The U430 Series are pairs of matched JFETs assembled in one TO-78 package. They feature high gain, low noise and low gate leakage and are intended for high performance, high slew rate, mixing and differential amplification. Additionally, these devices offer good power gain even as frequencies are increased beyond 250 MHz. The TO-78 package may be processed for military applications. (See Section 1.)

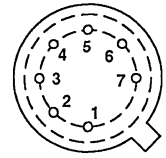
For additional design information please consult performance curves NZB which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G TYP (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ TYP (mV)
U430	-25	10	-15	25
U431	-25	10	-15	25

TO-78



BOTTOM VIEW



1 SOURCE 1
2 GATE 1
3 DRAIN 1
4 CASE
5 DRAIN 2
6 GATE 2
7 SOURCE 2

SIMILAR PRODUCTS

- Low-Noise, See U401 Series
- High-Gain, See 2N5911 Series
- Low-Leakage, See U421 Series
- Chips, Order U43XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				U430		U431		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-1	-4	-2	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-150		-150	pA
		T_A = 150°C	-10		-150		-150	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-15					pA
		T_A = 150°C	-10					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA, V_{DS} = 0 V	0.8		1		1	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	15	10		10		mS
Common-Source Output Conductance	g_{os}		100		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = -10 V, V_{DS} = 0 V, f = 1 MHz	4.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2		2.5		2.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz	6					$nV/\sqrt{Hz}$
HIGH FREQUENCY								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz	14					mS
Common-Source Output Conductance	g_{os}		0.13					mS
Power-Match Source Admittance	g_{ig}		12					mS
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 10 mA	25					mV
Saturation Drain[4] Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.95	0.9	1	0.9	1	
Transconductance[4] Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	0.95	0.9	1	0.9	1	
Gate-Source Cutoff Voltage Ratio	$\frac{V_{GS(OFF)1}}{V_{GS(OFF)2}}$	V_{DS} = 10 V, I_D = 1 nA	0.95	0.9	1	0.9	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	-2					pA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 10 mA	75					dB

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Assumes smaller value in the numerator.

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