Siliconix incorporated

U421 SERIES

N-Channel JFET Pairs

The U421 Series are monolithic pairs of n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250 fA (U421-3), high gain at low operating currents , and tight matching (10 mV for U421 and U424). Additionally, its TO-78 package is hermetically sealed and may be screened per MIL-S-19500. (See Section 1.)

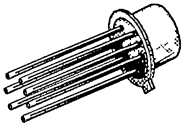
For additional design information please see performance curves NNT, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U421	-40	0.3	-0.25	10
U422	-40	0.3	-0.25	15
U423	-40	0.3	-0.25	25
U424	-40	0.3	-0.5	10
U425	-40	0.3	-0.5	15
U426	-40	0.3	-0.5	25

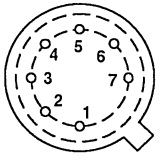
SIMILAR PRODUCTS

- Low-Noise, See U401 Series
- High-Gain, See 2N5911 Series
- Chips, Order U42XCHP

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-40	V
Gate-Source Voltage		V_{GS}	-40	
Gate-Gate Voltage		V_{GG}	± 40	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	400	mW
	Total		750	
Power Derating	Per Side		3.2	mW/°C
	Total		6	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

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ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U421		U422		U423		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-60	-40		-40		-40		V
Gate-Gate Breakdown Voltage	V_{GG}	I_G = -1 µA, I_D = 0, I_S = 0	±55	±40		±40		±40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-1.2	-0.4	-2	-0.4	-2	-0.4	-2	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400	60	1000	60	1000	60	1000	µA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.6		-1		-1		-1	pA
		T_A = 125°C	-0.3		-1		-1		-1	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 µA	-0.2		-0.25		-0.25		-0.25	pA
		T_A = 125°C	-150		-250		-250		-250	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 µA	2000							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 µA	-0.8		-1.8		-1.8		-1.8	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	0.6	0.3	1.5	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10		10	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 30 µA, f = 1 kHz	0.2	0.12	0.35	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3		3	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.4		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz	30		70		70		70	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz, R_G = 10 MΩ			1		1		1	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 30 µA			10		15		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 30 µA, T = -55 to 25°C			10		25		40	µV/°C
		T = 25 to 125°C			10		25		40	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 µA	102	90		80		80		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U424		U425		U426		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-60	-40		-40		-40		V
Gate-Gate Breakdown Voltage	V_{GG}	I_G = -1 µA, I_D = 0, I_S = 0	±55	±40		±40		±40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-2	-0.4	-3	-0.4	-3	-0.4	-3	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	800	60	1800	60	1800	60	1800	µA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.8		-3		-3		-3	pA
		T_A = 125°C	-0.4		-3		-3		-3	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 µA	-0.3		-0.5		-0.5		-0.5	pA
		T_A = 125°C	-200		-500		-500		-500	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 µA	2000							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 µA	-1.5		-2.9		-2.9		-2.9	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	0.6	0.3	1.5	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10		10	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 30 µA, f = 1 kHz	0.2	0.12	0.35	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3		3	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.4		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz	30		70		70		70	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz, R_G = 10 MΩ			1		1		1	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 30 µA			10		15		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 30 µA, T = -55 to 25°C			10		25		40	µV/°C
		T = 25 to 125°C			10		25		40	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 µA	100	90		80		80		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.