DATA SHEET

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TZA3052AHW
2.5 and 2.7 Gbits/s fibre optic receiver

Product specification
Supersedes data of 2002 Aug 15

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Philips
Semiconductors

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2.5 and 2.7 Gbits/s fibre optic receiver TZA3052AHW

FEATURES

- Single 3.3 V power supply
- Supports SDH/SONET bit rates at 2488.32 and 2666.06 Mbits/s (STM16/OC48 and STM16/OC48 + FEC) with 19.44 MHz reference frequency
- Limiting input with 12 mV sensitivity
- Received Signal Strength Indicator (RSSI)
- Loss Of Signal (LOS) indicator with threshold adjust
- Frequency lock indicator
- ITU-T compliant jitter tolerance
- 1:16 demultiplexing ratio
- Low Voltage Positive Emitter Coupled Logic (LVPECL) demultiplexer outputs
- Frame detector for SDH/SONET frames
- Parity bit generation
- Recovered data and clock loop mode outputs
- Loop mode inputs on demultiplexer
- Temperature alarm
- Pin compatible with TZA3012AHW.

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APPLICATIONS

- SDH/SONET optical transmission system with bit rates of 2.5 and 2.7 Gbits/s
- Physical interface IC in receive channels
- Transponder applications
- Dense Wavelength Division Multiplexing (DWDM) systems.

GENERAL DESCRIPTION

The TZA3052AHW is a fully integrated optical network receiver containing a limiter, Data and Clock Recovery (DCR) and 1:16 demultiplexer. The IC operates at the bit rates 2.5 and 2.7 Gbits/s with one single reference frequency. The receiver supports loop modes with serial clock and data inputs and outputs.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3052AHW	HTQFP100	plastic, heatsink thin quad flat package; 100 leads; body 14 × 14 × 1.0 mm	SOT638-1

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BLOCK DIAGRAM

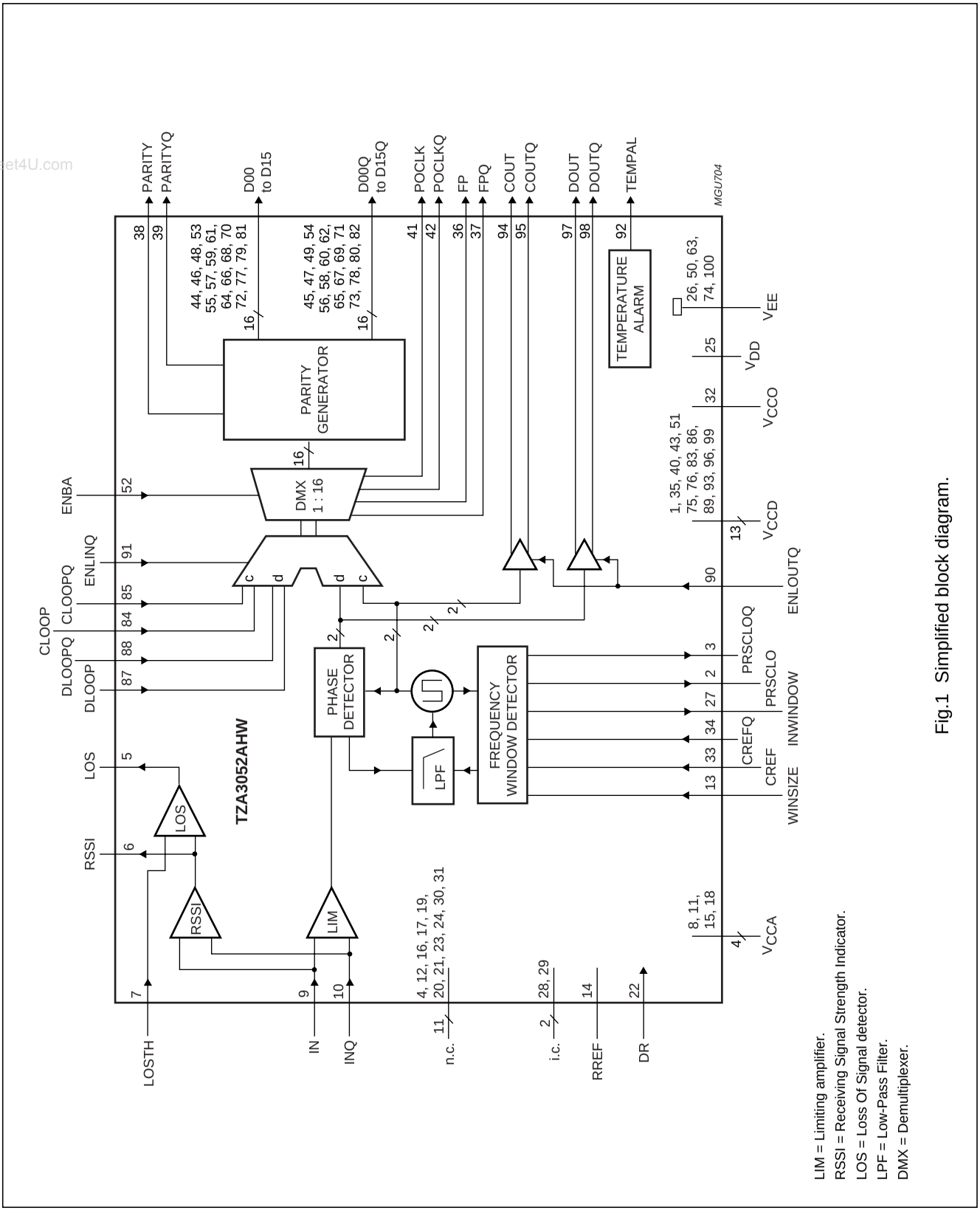

Fig.1 Simplified block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
V_{EE}	die pad	common ground plane
V_{CCD}	1	supply voltage (digital part)
PRSCLO	2	prescaler output
PRSCLOQ	3	prescaler output inverted
n.c.	4	not connected
LOS	5	LOS output of input channel
RSSI	6	received signal strength indicator output of input channel
LOSTH	7	LOS threshold input for input channel
V_{CCA}	8	supply voltage (analog part)
IN	9	channel input
INQ	10	channel input inverted
V_{CCA}	11	supply voltage (analog part)
n.c.	12	not connected
WINSIZE	13	wide and narrow frequency detect window select
RREF	14	reference resistor input
V_{CCA}	15	supply voltage (analog part)
n.c.	16	not connected
n.c.	17	not connected
V_{CCA}	18	supply voltage (analog part)
n.c.	19	not connected
n.c.	20	not connected
n.c.	21	not connected
DR	22	data rate selection input
n.c.	23	not connected
n.c.	24	not connected
V_{DD}	25	supply voltage (digital)
V_{EE}	26	ground
INWINDOW	27	frequency window detector output
i.c.	28	internally connected
i.c.	29	internally connected
n.c.	30	not connected
n.c.	31	not connected
V_{CCO}	32	supply voltage (clock generator)
CREF	33	reference clock input
CREFQ	34	reference clock input inverted
V_{CCD}	35	supply voltage (digital part)
FP	36	frame pulse output
FPQ	37	frame pulse output inverted
PARITY	38	parity output
PARITYQ	39	parity output inverted
V_{CCD}	40	supply voltage (digital part)
POCLK	41	parallel clock output
POCLKQ	42	parallel clock output inverted
V_{CCD}	43	supply voltage (digital part)
D00	44	parallel data output 00
D00Q	45	parallel data output 00 inverted
D01	46	parallel data output 01
D01Q	47	parallel data output 01 inverted
D02	48	parallel data output 02
D02Q	49	parallel data output 02 inverted
V_{EE}	50	ground
V_{CCD}	51	supply voltage (digital part)
ENBA	52	byte alignment enable input
D03	53	parallel data output 03
D03Q	54	parallel data output 03 inverted
D04	55	parallel data output 04
D04Q	56	parallel data output 04 inverted
D05	57	parallel data output 05
D05Q	58	parallel data output 05 inverted
D06	59	parallel data output 06
D06Q	60	parallel data output 06 inverted
D07	61	parallel data output 07
D07Q	62	parallel data output 07 inverted
V_{EE}	63	ground
D08	64	parallel data output 08
D08Q	65	parallel data output 08 inverted
D09	66	parallel data output 09
D09Q	67	parallel data output 09 inverted
D10	68	parallel data output 10
D10Q	69	parallel data output 10 inverted
D11	70	parallel data output 11
D11Q	71	parallel data output 11 inverted
D12	72	parallel data output 12
D12Q	73	parallel data output 12 inverted
V_{EE}	74	ground
V_{CCD}	75	supply voltage (digital part)

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SYMBOL	PIN	DESCRIPTION
V_{CCD}	76	supply voltage (digital part)
D13	77	parallel data output 13
D13Q	78	parallel data output 13 inverted
D14	79	parallel data output 14
D14Q	80	parallel data output 14 inverted
D15	81	parallel data output 15
D15Q	82	parallel data output 15 inverted
V_{CCD}	83	supply voltage (digital part)
CLOOP	84	loop mode clock input
CLOOPQ	85	loop mode clock input inverted
V_{CCD}	86	supply voltage (digital part)
DLOOP	87	loop mode data input
DLOOPQ	88	loop mode data input inverted
V_{CCD}	89	supply voltage (digital part)

SYMBOL	PIN	DESCRIPTION
ENLOUTQ	90	line loop back enable input (active LOW)
ENLINQ	91	diagnostic loop back enable input (active LOW)
TEMPAL	92	temperature alarm output
V_{CCD}	93	supply voltage (digital part)
COUT	94	recovered clock output
COUTQ	95	recovered clock output inverted
V_{CCD}	96	supply voltage (digital part)
DOUT	97	recovered data output
DOUTQ	98	recovered data output inverted
V_{CCD}	99	supply voltage (digital part)
V_{EE}	100	ground

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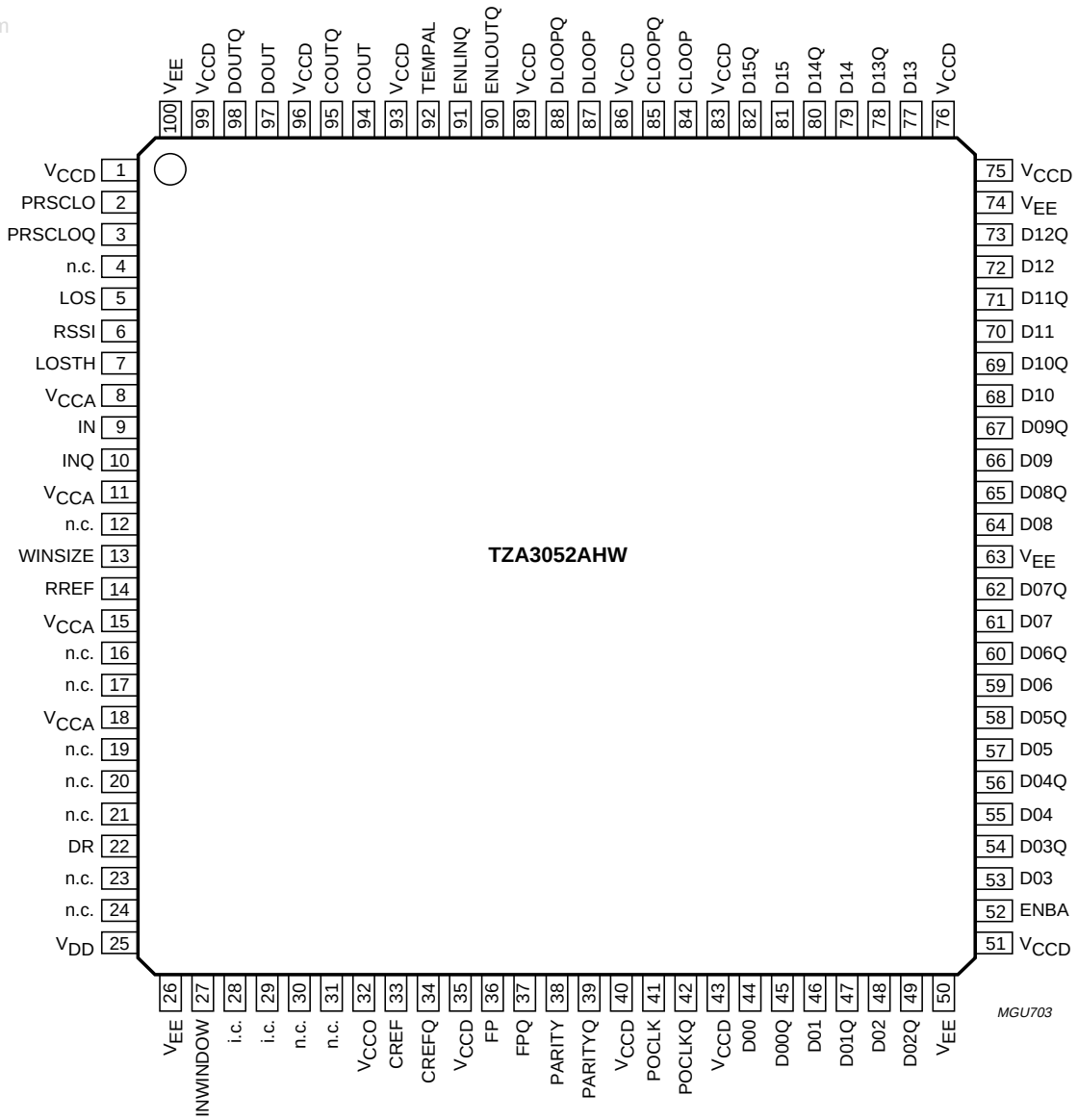

Fig.2 Pin configuration.

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FUNCTIONAL DESCRIPTION

The TZA3052AHW receives data from an incoming bit stream with a bit rate of 2.5 or 2.7 Gbits/s. A DCR section synchronizes the internal clock generator with the incoming data. The recovered serial data and clock are demultiplexed with a ratio of 1:16.

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Configuring the TZA3052AHW using pin DR

The IC features two types of bit rates with the use of a 19.44 MHz reference clock connected to pins CREF and CREFQ. Pin DR acts as a standard CMOS input that selects one of the desired bit rates as given in Table 1.

Table 1 Truth table for pin DR

PIN DR	PROTOCOL	BIT RATE (Mbits/s)
LOW	STM16/OC48	2488.32
HIGH	STM16 + FEC	2667.00

Limiting amplifier

The incoming bitstream is amplified by the limiting amplifier (see Fig.3).

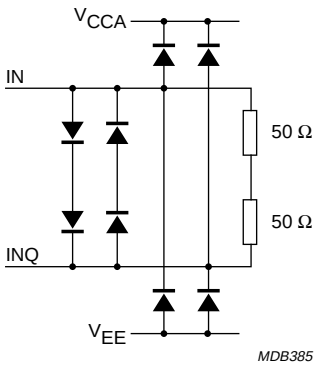

Fig.3 Limiter input termination configuration.

Received Signal Strength Indicator (RSSI)

The signal strength at the input is measured with a logarithmic detector and presented at pin RSSI. The RSSI reading has a sensitivity of typically 17 mV/dB for a $V_{i(p-p)}$ range of 5 to 500 mV (see Fig.4). V_{RSSI} can be calculated using the following formula:

$$V_{RSSI} = V_{RSSI(32mV)} + S_{RSSI} \times 20\log\frac{V_{i(p-p)}}{32\ mV}$$

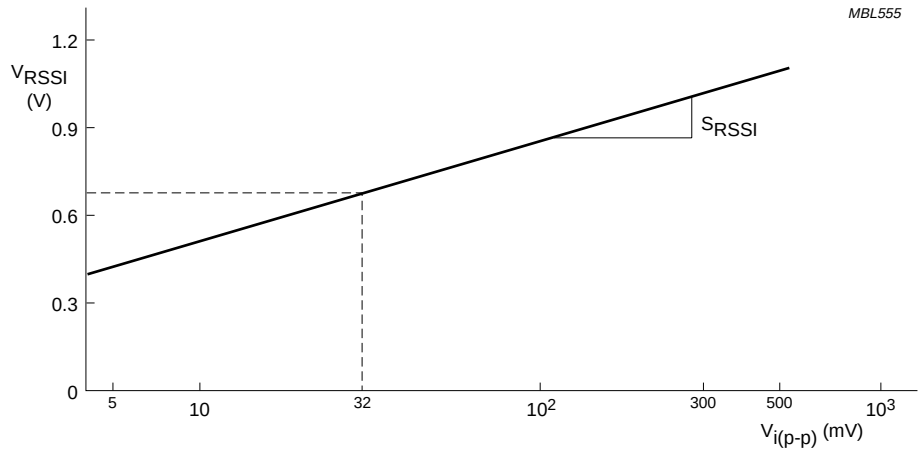

Fig.4 V_{RSSI} as a function of $V_{i(p-p)}$.

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Loss Of Signal (LOS) indicator

Besides the analog RSSI output, a digital LOS indication is present on the TZA3052AHW. The RSSI level is internally compared with a LOS threshold, which can be set by an external resistor (pin LOSTH).

If the received signal strength is **below** the threshold value, pin LOS will be HIGH. A hysteresis of 2.5 dB is applied in the comparator.

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Setting LOSTH reference level by external resistor

The reference voltage level on pin LOSTH can be set by connecting an external resistor (R2) between the relevant pin and ground (see Fig.5). The voltage on the pin is determined by the ratio of resistors R2 and R1.
For resistor R1 a value of 10 to 20 kΩ is recommended, yielding a current of 120 to 60 μA.

The LOSTH voltage equals $\frac{R2}{R1} \times V_{ref}$

Voltage V_{ref} represents a temperature stabilized, accurate reference voltage of 1.2 V. The minimum threshold level corresponds to 0 V and the maximum to 1.2 V. Hence, the value of R2 may not be higher than R1. The accuracy of the LOSTH voltage depends mainly on the matching of the two external resistors.

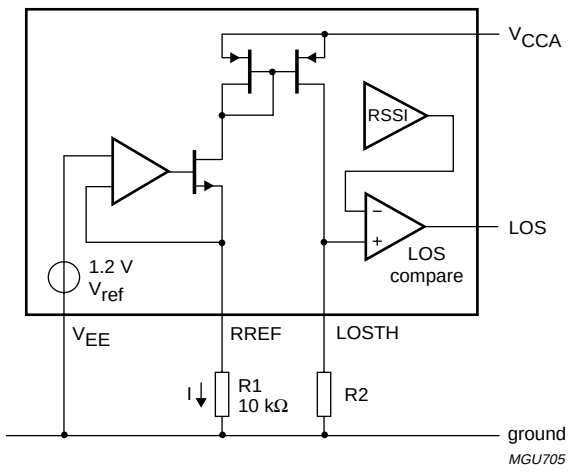

Fig.5 Setting the LOSTH reference level by external resistors.

Instead of using resistors (R1 and R2) to set the LOS threshold, an accurate external voltage source can be used.

If no resistor is connected to pin LOSTH, or an external voltage higher than $^2/_3 \times V_{CC}$ is applied to the pin, the LOS detection circuit (including the RSSI reading) is automatically switched off to reduce power dissipation.

Data and Clock Recovery (DCR)

The TZA3052AHW recovers the clock and data contents from the incoming bit stream (see Fig.6). The DCR uses a combined frequency and phase locking scheme, providing reliable and quick data acquisition.

Initially, at power-up, coarse adjustment of the free running VCO frequency is required. This is achieved by the Frequency Window Detector (FWD) circuit. The FWD is a conventional frequency locked PLL.

The FWD checks the VCO frequency, which has to be within a 1000 ppm (parts per million) window around the desired frequency. The FWD then compares the divided VCO frequency (also available on pins PRSCLO and PRSCLOQ with the reference frequency of 19.44 MHz on pins CREF and CREFQ.

If the VCO frequency is found to be outside this window, the FWD disables the Data Phase Detector (DPD) and forces the VCO to a frequency within the window. As soon as the ‘in window’ condition occurs, which is visible on pin INWINDOW, the DPD starts acquiring lock on the incoming bit stream. Since the VCO frequency is very close to the expected bit rate, the phase acquisition will be almost instantaneous, resulting in quick phase lock to the incoming data stream.

Although the VCO is now locked to the incoming bit stream, the FWD is still supervising the VCO frequency and takes over control if the VCO drifts outside the predefined frequency window. This might occur during a ‘loss of signal’ situation. Due to the FWD, the VCO frequency is always close to the required bit rate, enabling rapid phase acquisition if the lost input signal state returns.

Due to the loose coupling of 1000 ppm, the reference frequency does not need to be highly accurate or stable. Any crystal-based oscillator that generates a reasonably accurate frequency (e.g. within 100 ppm) can be used.

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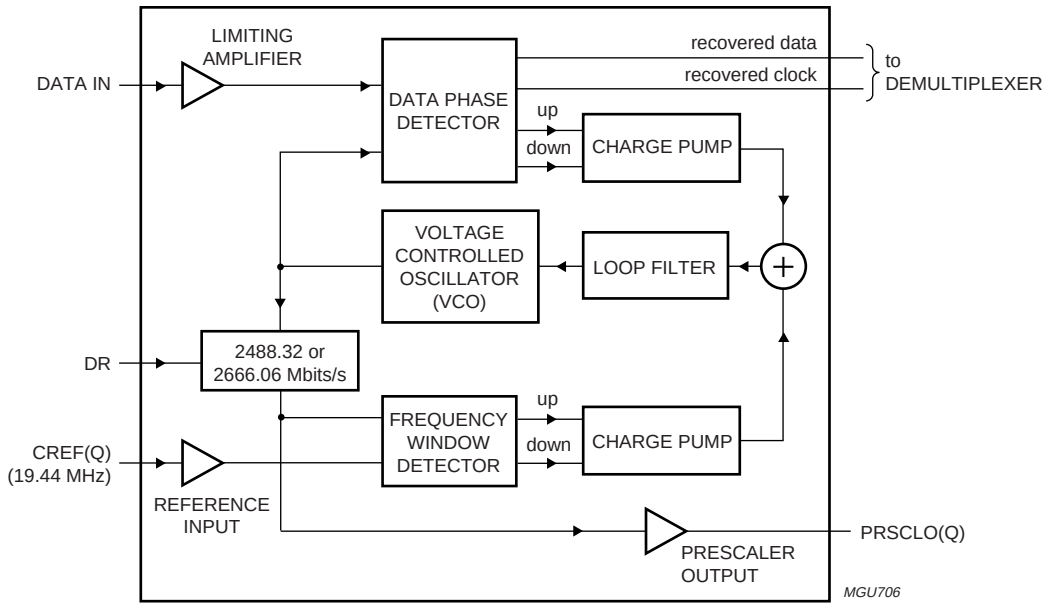

Fig.6 Block diagram of data and clock recovery.

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Prescaler outputs

Prescaler output pins PRSCLO and PRSCLOQ are always a measure of the internal frequency of the DCR. It is the VCO frequency divided by the selected division factor. It can be used as an accurate reference for another PLL, since it corresponds to the recovered data rate.

Programming the FWD

The default width of the window for frequency acquisition is 1000 ppm around the desired bit rate. A window width of 0 ppm can be set using pin WINSIZE. This effectively removes the dead zone from the FWD, rendering the FWD into a classical PLL.

The VCO will be locked directly to the reference signal instead of to the incoming bit stream.

Table 2 Truth table for pin WINSIZE

PIN WINSIZE	FREQUENCY WINDOW
LOW	0 ppm
HIGH	1000 ppm

Accurate clock generation during loss of signal

A zero window size is especially interesting in the absence of input data, since the frequency of the recovered clock will be equal to the reference frequency including its tolerance.

The accuracy of the reference frequency needs to be better than 20 ppm if the application is to comply with ITU-T recommendations.

INWINDOW signal

The status of the FWD circuit is reflected in the state of pin INWINDOW: HIGH for an ‘in window’ situation and LOW whenever the VCO is outside the defined frequency window.

Jitter performance

The TZA3052AHW has been optimized for best jitter tolerance performance. For the SDH/SONET STM16/OC48 bit rate, the jitter tolerance exceeds compliance with ITU-T standard G.958.

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Demultiplexer

The demultiplexer converts the serial input bit stream to parallel format (1:16). The output data is available on a standard LVPECL output driver type (see Fig.10). As well as the deserializing function, the demultiplexer comprises a parity calculator and a frame header detection circuit. The calculated parity (EVEN) is output at pins PARITY and PARITYQ, whereas occurrence of the frame header pattern in the data stream results in a 1 clock cycle wide pulse on pins FP and FPQ.

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Frame detection

Byte alignment is enabled if the Enable Byte Alignment (ENBA) input is HIGH. Whenever a 32-bit sequence matches the frame header pattern, the incoming data is formatted into logical bytes or words and a frame pulse is generated on differential outputs FP and FPQ.

The frame header pattern is F6F62828H, corresponding to the middle section of the standard SDH/SONET frame header (the last two A1 bytes plus the first two A2 bytes).

Figure 7 shows a typical SDH/SONET reframe sequence involving byte alignment.

Frame and byte boundary detection is enabled on the rising edge of ENBA and remains enabled while ENBA is HIGH. Boundaries are recognized on receipt of the second A2 byte and FP goes HIGH for one POCLK cycle.

The first two A2 bytes in the frame header are the first data word to be reported with the correct alignment on the outgoing data bus (D00 to D15).

When interfacing with a section terminating device, ENBA must remain HIGH for a full frame after the initial frame pulse. This is to allow the section terminating device to verify internally that frame and byte alignment are correct (see Fig.8). Byte boundary detection is disabled on the first FP pulse after ENBA has gone LOW.

Figure 9 shows frame and byte boundary detection activated on the rising edge of ENBA, and deactivated by the first FP pulse after ENBA has gone LOW.

If ENBA is LOW, no active alignment takes place. However, if the framing pattern happens to occur in the formatted data, a frame pulse will still be output on pins FP and FPQ.

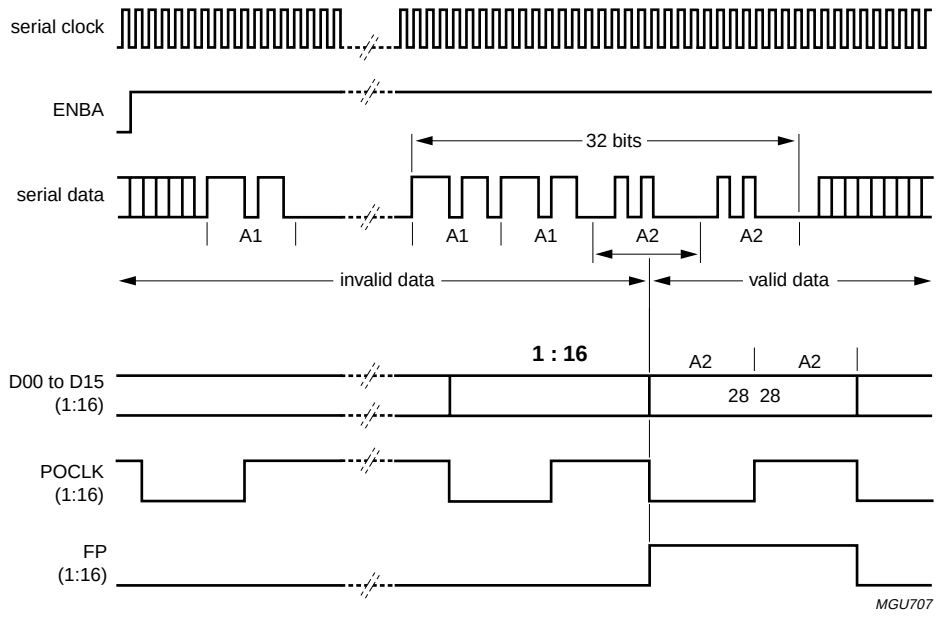

Fig.7 Frame and byte detection in SDH/SONET application.

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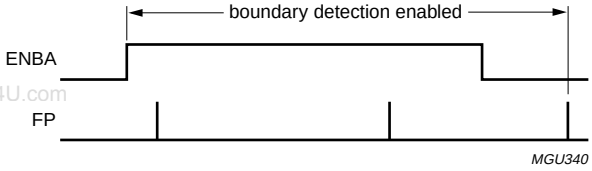

Fig.8 ENBA timing with section terminating device.

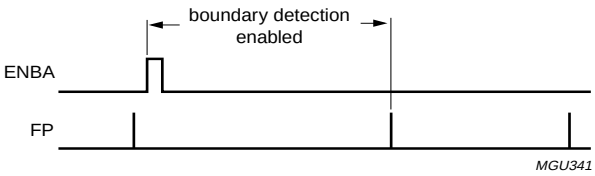

Fig.9 Alternate ENBA timing.

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Parity generation

Output pins PARITY and PARITYQ provide the EVEN parity of the byte/word that is currently available on the parallel bus.

Loop mode I/Os

The IC can be used in a ‘diagnostic loop back’ mode by setting pin ENLINQ to LOW. In this case, the demultiplexer will select inputs DLOOP and DLOOPQ, CLOOP and CLOOPQ instead of taking the input from the DCR. The ‘line loop back’ mode is activated by setting pin ENLOUTQ to LOW. Now, the recovered clock and serial data will be available at output pins DOUT and DOUTQ and COUT and COUTQ.

RF I/Os

The RF CML outputs have an amplitude of 80 mV (p-p) single-ended. The termination scheme is AC coupled (see Fig.11).

CMOS control inputs

Most CMOS control inputs have an internal pull-up resistor. If the input is required to be HIGH, it can be left open-circuit. Only the LOW state needs to be actively forced. This applies to pins WINSIZE, ENBA, ENLOUTQ, ENLINQ and DR.

Power supply connections

Four separate supply domains (V_{DD}, V_{CCD}, V_{CCO} and V_{CCA}) provide isolation between the various functional blocks. Each supply domain should be connected to a common V_{CC} via separate filters. **All supply pins, including the exposed die pad, must be connected**. The die pad should be connected with the lowest inductance possible. Since the die pad is also used as the main ground return of the chip, the connection should have a low DC impedance as well. The voltage supply levels should be in accordance with the values specified in Chapter “Characteristics”.

All external components should be surface mounted devices, preferably of size 0603 or smaller.
The components must be mounted as closely to the IC as possible.

Temperature alarm

The TZA3052AHW features a temperature alarm.
The temperature alarm switches the open-drain output of pin TEMPAL to LOW at a junction temperature above 130 °C.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}, V_{CCD}, V_{CCO}, V_{DD}	supply voltages	–0.5	+3.6	V
V_n	DC voltage on			
	pins D00 and D00Q to D15 and D15Q, POCLK and POCLKQ, FP and FPQ, PARITY and PARITYQ, PRSCLO and PRSCLOQ	V_{CC} – 2.5	V_{CC} + 0.5	V
	pins LOSTH and RREF	–0.5	V_{CC} + 0.5	V
	pin RSSI	–0.5	V_{CC} + 0.5	V
	pins WINSIZE, DR, ENBA, ENLOUTQ and ENLINQ	–0.5	V_{CC} + 0.5	V
	pins LOS and INWINDOW	–0.5	V_{CC} + 0.5	V
	pin TEMPAL	–0.5	V_{CC} + 0.5	V
I_n	input current on			
	pins IN and INQ	–30	+30	mA
	pins CREF and CREFQ, CLOOP and CLOOPQ, DLOOP and DLOOPQ	–20	+20	mA
	pin TEMPAL	–2	+2	mA
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature		+125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	notes 1 and 2	16	K/W

Notes

1. In compliance with JEDEC standards JESD51-5 and JESD51-7.
2. Four-layer Printed-Circuit Board (PCB) in still air with 36 plated vias connected with the heatsink and the second and fourth layers of the PCB.

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CHARACTERISTICS

T_{amb} = –40 to +85 °C; V_{CC} = 3.14 to 3.47 V; $R_{th(j-a)} \leq 16$ K/W; all characteristics are specified for the default setting (note 1); all voltages are referenced to ground; positive currents flow into the device; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
I_{CCA}	analog supply current		15	20	27	mA
I_{CCD}	digital supply current		270	350	450	mA
I_{CCO}	oscillator supply current		20	25	33	mA
I_{DD}	digital supply current		0	0	1	mA
$I_{CC(tot)}$	total supply current		305	395	511	mA
P_{tot}	total power dissipation		0.96	1.3	1.77	W
CMOS input; pins DR, WINSIZE, ENBA, ENLOUTQ and ENLINQ						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{CC}$	V
V_{IH}	HIGH-level input voltage		$0.8V_{CC}$	–	–	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–200	–		μA
I_{IH}	HIGH-level input current	$V_{IH} = V_{CC}$	–	–	10	μA
CMOS output; pins LOS and INWINDOW						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.5 mA	$V_{CC} - 0.2$	–	V_{CC}	V
Open-drain output; pin TEMPAL						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.2	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{CC}$	–	–	10	μA
Serial output; pins COUT, COUTQ, DOUT and DOUTQ						
$V_{o(p-p)}$	output voltage swing (peak-to-peak value)	single-ended with 50 Ω external load; ENLOUTQ = LOW; see Fig.11	50	80	110	mV
Z_o	output impedance	single-ended to V_{CC}	80	100	120	Ω
t_r	rise time	20% to 80%	–	100	–	ps
t_f	fall time	80% to 20%	–	100	–	ps
t_{D-C}	data-to-clock delay	between differential crossovers of COUT, COUTQ, DOUT and DOUTQ; see Fig.12	80	140	200	ps
δ	duty cycle signals COUT and COUTQ	between differential crossovers	40	50	60	%
Serial input; pins CLOOP, CLOOPQ, DLOOP and DLOOPQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	DC input voltage		$V_{CC} - 1$	–	$V_{CC} + 0.25$	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
t_d	clock delay	see Fig.13	260	340	400	ps

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{su}	set-up,	see Fig.13	15	30	60	ps
t_h	hold time	see Fig.13	15	30	60	ps
δ	duty cycle signals CLOOP and CLOOPQ	between differential crossovers	40	50	60	%
LVPECL mode parallel output; pins D00 and D00Q to D15 and D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ						
V_{OH}	HIGH-level output voltage	50 Ω termination to V_{CC} – 2 V; see Fig.10	V_{CC} – 1.2	V_{CC} – 1.0	V_{CC} – 0.9	V
V_{OL}	LOW-level output voltage	50 Ω termination to V_{CC} – 2 V; see Fig.10	V_{CC} – 2.0	V_{CC} – 1.9	V_{CC} – 1.7	V
t_r	rise time	20% to 80%	300	350	400	ps
t_f	fall time	80% to 20%	300	350	400	ps
Timing parallel output; pins D00 and D00Q to D15 and D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ						
t_{D-C}	data-to-clock delay between differential crossovers of D00 to D15 and POCLK	see Fig.14; note 2	100	100	250	ps
δ	duty cycle POCLK		40	50	60	%
skew	channel to channel skew between channels (D00 and Dn)	note 2	–	–	200	ps
Reference; pin RREF						
V_{ref}	reference voltage	10 to 20 kΩ resistor to V_{EE}	1.17	1.21	1.26	V
RF input; pins IN and INQ						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; note 3	12	–	500	mV
Z_i	input impedance	differential	80	100	120	Ω
α_{iso}	between channel isolation		–	60	–	dB
Received Signal Strength Indicator (RSSI)						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended	5	–	500	mV
S_{RSSI}	RSSI sensitivity	see Fig.4	15	17	20	mV/dB
V_{RSSI}	RSSI output voltage	$V_{i(p-p)}$ = 32 mV; PRBS (2^{31}–1)	580	680	780	mV
$\Delta V_{o(RSSI)}$	output voltage variation	input 2.5 and 2.7 Gbits/s; PRBS (2^{31}–1); V_{CC} = 3.14 to 3.47 V; ΔT_{amb} = 120 °C	–50	–	+50	mV
Output; pin RSSI						
Z_o	output impedance		–	1	10	Ω
$I_{O(source)}$	output source current		–	–	1	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{O(sink)}$	output sink current		–	–	0.4	mA
LOS detector						
hys	hysteresis		2	3	4	dB
t_a	assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
t_d	de-assert time	$\Delta V_{i(p-p)}$ = 3 dB	–	–	5	µs
Reference frequency input; pins CREF and CREFQ						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	single-ended	50	–	1000	mV
V_i	DC input voltage		V_{CC} − 1	–	V_{CC} + 0.25	V
Z_i	input impedance	single-ended to V_{CC}	40	50	60	Ω
Δf_{CREF}	reference clock frequency accuracy	SDH/SONET operation, f_{CREF} = 19.44 MHz	−20	–	+20	ppm
PLL characteristics						
t_{acq}	acquisition time		–	–	200	µs
$t_{acq(pc)}$	acquisition time at power cycle		–	–	10	ms
TDR	transitionless data run		–	1000	–	bits
Jitter tolerance						
$J_{tol(p-p)}$	jitter tolerance (peak-to-peak value)	STM16/OC48 mode (ITU-T G.958); PRBS (2^{23}–1); note 4				
		f = 100 kHz	3	10	–	UI
		f = 1 MHz	0.3	1	–	UI
		f = 20 MHz	0.3	0.5	–	UI

Notes

1. Default settings: DR = LOW (STM16/OC48); WINSIZE = HIGH (1000 ppm); ENBA = HIGH (automatic byte alignment); ENLOUTQ = HIGH (DOUT, COUT disabled); ENLINQ = HIGH (DLOOP, CLOOP disabled); CREF and CREFQ = 19.44 MHz; D00 and D00Q to D15 and D15Q, FP, FPQ, PARITY, PARITYQ, POCLK, POCLKQ, PRSCLO and PRSCLOQ are not connected.
2. With 50% duty cycle.
3. The RF input is protected against a differential overvoltage; the maximum input current is 30 mA. It is assumed that both inputs carry a complementary signal of the specified peak-to-peak value.
4. At T_{amb} = −40 to 0 °C the minimum value is 0.25 UI at f = 1 MHz and 20 MHz.

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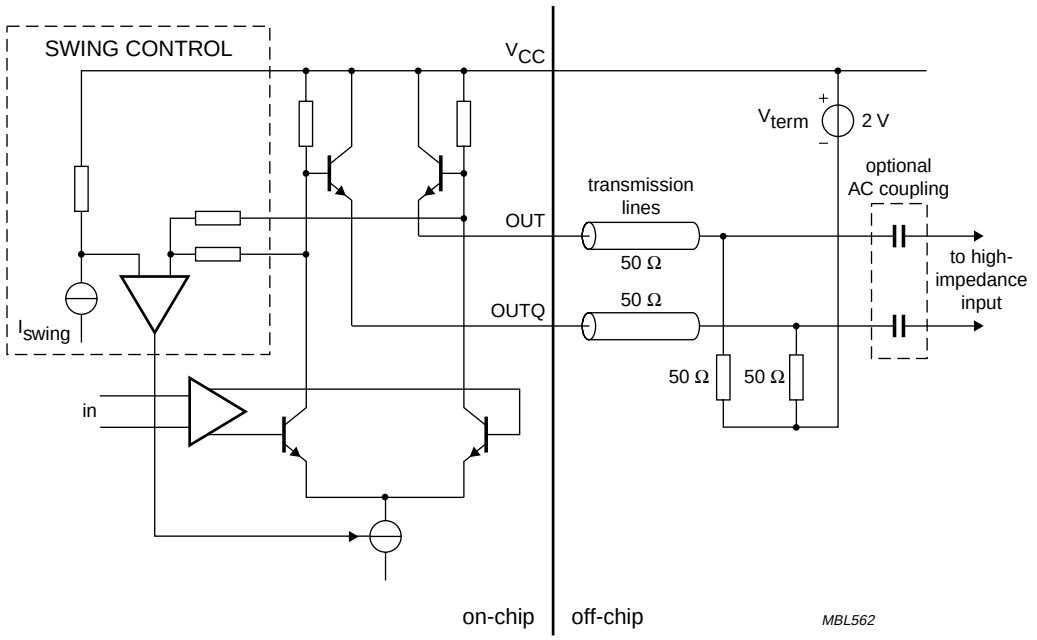

Fig.10 Standard PECL mode.

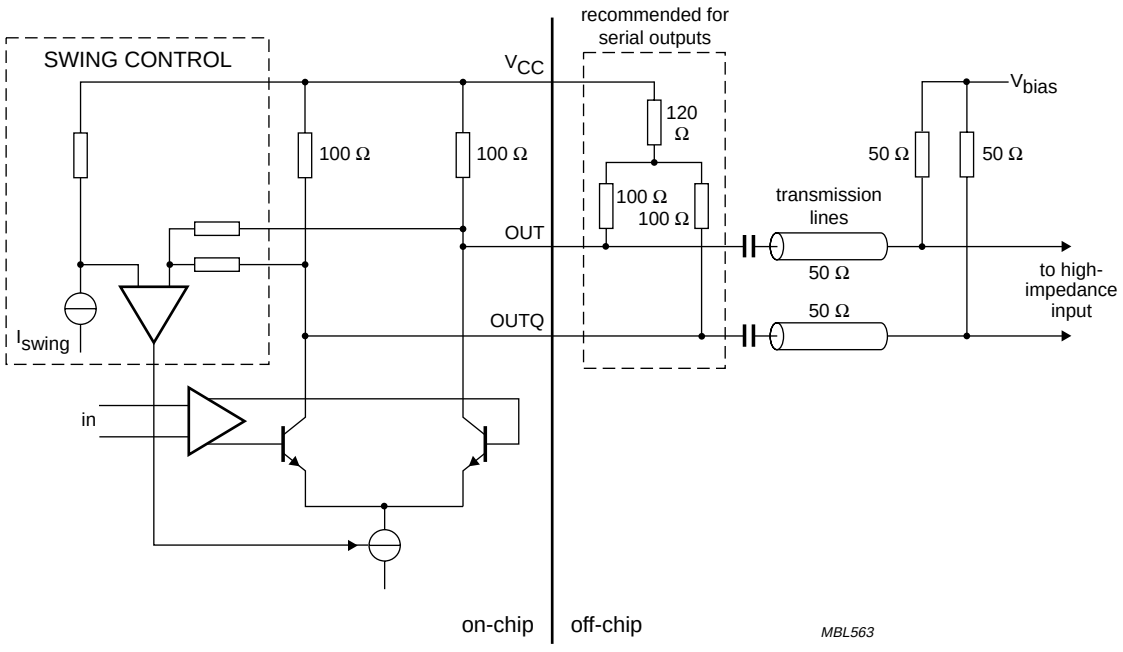

Fig.11 CML AC coupled mode.

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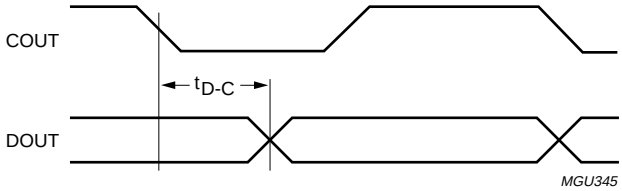
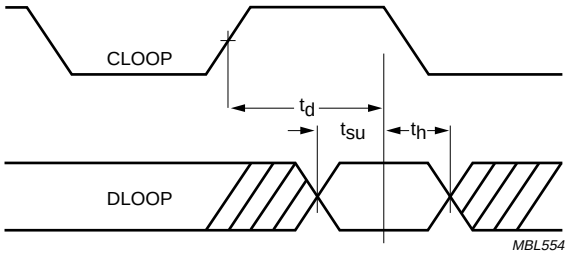


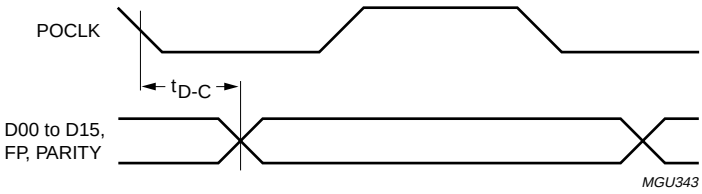
The timing is measured from the crossover point of the clock output signal to the crossover point of the data output (all signals are differential).

Fig.12 Loop mode output timing.



The timing is measured from the crossover point of the clock input signal to the crossover point of the data input.

Fig.13 Loop mode input timing.



The timing is measured from the crossover point of the clock output signal to the crossover point of the data output (all signals are differential).

Fig.14 Parallel bus output timing.

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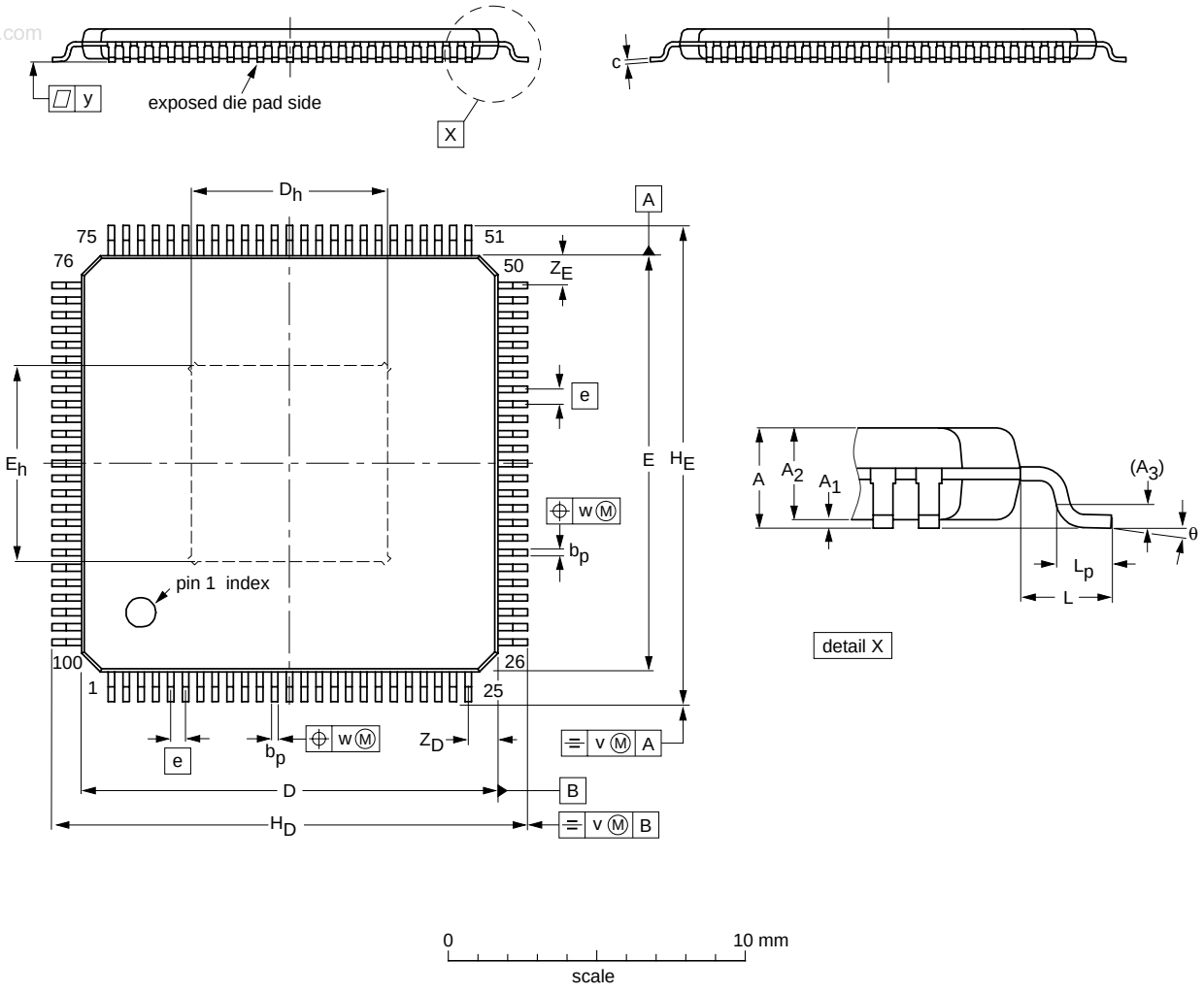
PACKAGE OUTLINE

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed die pad **SOT638-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	14.1 13.9	7.1 6.1	14.1 13.9	7.1 6.1	0.5	16.15 15.85	16.15 15.85	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-1						~~01-03-30~~ 03-04-07

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

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There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

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Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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