ASPEN-PX Device
ASPEN® Port Expander
TXC-05811

DATA SHEET

FEATURES

- Interoperable with ASPEN® (TXC-05810B) UTOPIA Level 2 interface
- Provides port expansion for up to 64 UTOPIA Level 2 ports
- Utilizes ASPEN ATM AccessEDGE firmware for design and field upgrades
- Supports unicast and spatial multicast traffic to all 64 ports
- Backpressure mechanism to prevent cell loss
- ASPEN-PX management integrated with ASPEN via the host mailbox interface
- Single +3.3 V power supply
- 256-lead Plastic Ball Grid Array (PBGA) package, 17 mm x 17 mm

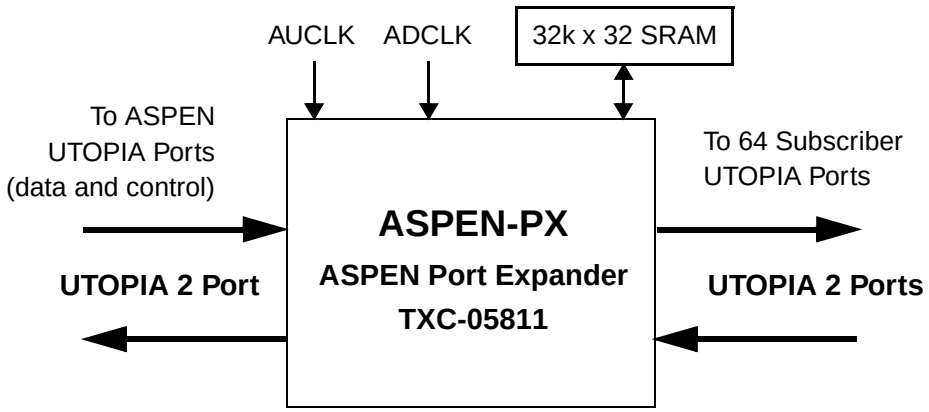
DESCRIPTION

The ASPEN-PX (TXC-05811), ASPEN Port Expander provides state of the art UTOPIA port expansion capability, increasing ASPEN's PHY support from 16 to 64 ports with unicast and multicast traffic delivery to enhance system flexibility. Its seamless interface with ASPEN (TXC-05810B) enables customers to increase the system port density of their *CellBus*-based UTOPIA Level 2 platforms, and leverage existing ASPEN hardware and software designs, reducing time-to-market.

All traffic management for the 64 ports is handled directly by ASPEN. Coupled with the ASPEN-PX, ASPEN creates a new value proposition for the industry, particularly in the broadband access market, by extending the *CellBus* architecture to form a distributed processing and switching environment that can directly implement multi-service network functionality for ATM cell-based traffic effectively and efficiently.

APPLICATIONS

- ATM Access Multiplexers
- DSLAM Applications
- Multi-Service Access Multiplexers
- ATM LAN Switch
- VoIP/VoATM Voice Gateways
- Frame Relay Switch



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LIST OF FIGURES

APPLICATION EXAMPLE

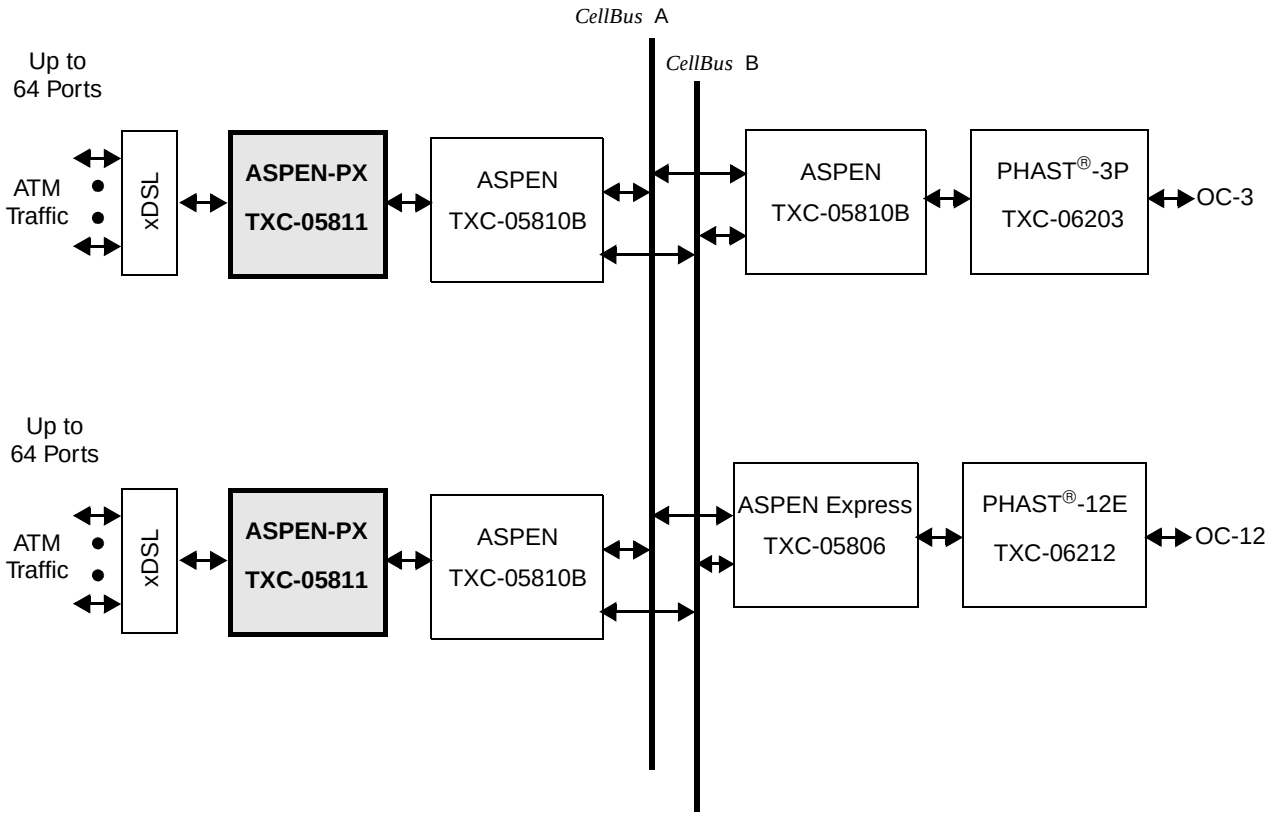


Figure 1. DSLAM Application with OC-3 and OC-12 Network Uplinks

BLOCK DIAGRAM

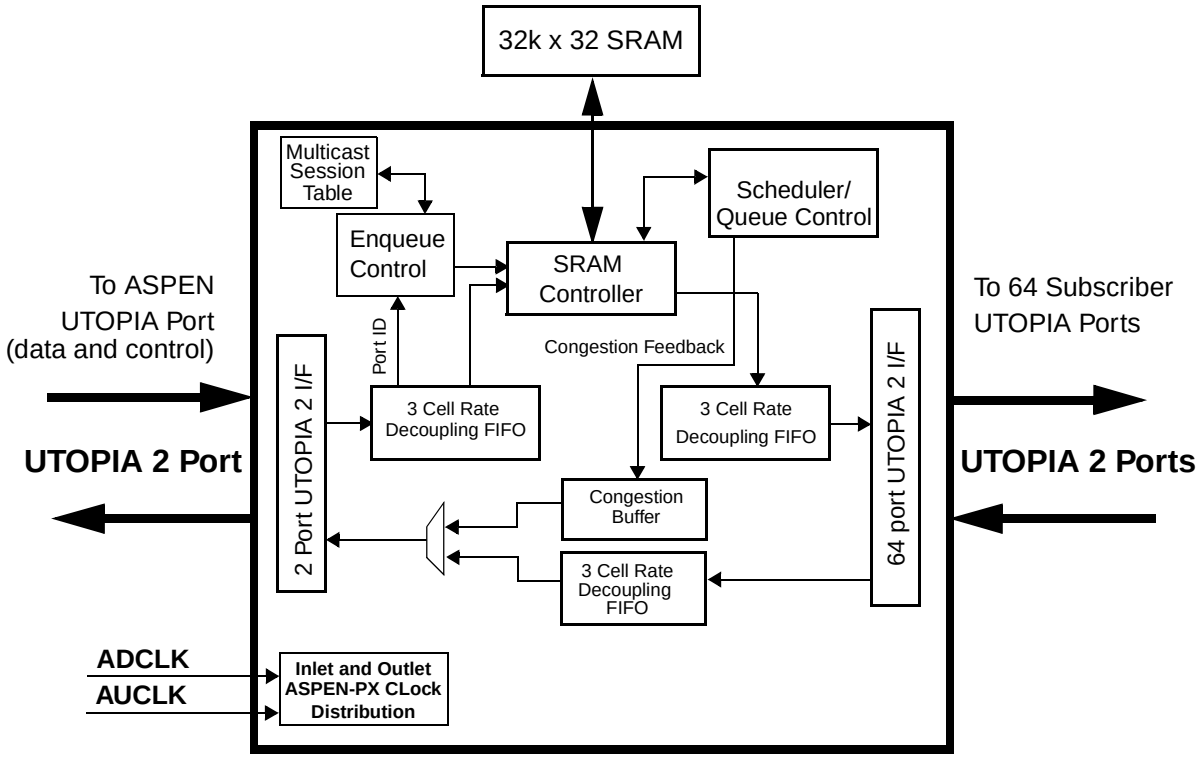


Figure 2. ASPEN-PX (TXC-05811) Block Diagram

BLOCK DIAGRAM DESCRIPTION

UTOPIA PORTS

The ASPEN-PX has a single UTOPIA master port and a single UTOPIA slave port. The slave port interfaces with the ASPEN and is UTOPIA Level 1/2 compliant. Cell size is 56 bytes in both directions to and from the ASPEN. The UTOPIA interface to ASPEN operates in 16-bit slave mode and uses a 2 port UTOPIA Level 2 interface. One port supports user data transport to and from ASPEN and the second port supports the control path to and from ASPEN. This insures that the communication path for control, configuration, and status remain open under heavy load conditions in the ASPEN or ASPEN-PX.

The Master port interfaces with the PHY device and is UTOPIA Level 1/2 compliant. Cell size is 53/54 bytes to and from the PHY. The UTOPIA interface to the PHYs operates in 8-bit or 16-bit master mode and utilizes the Multi-PHY addressing scheme outlined in the ATM Forum UTOPIA-2 standard, Appendix 1, example A1.1. This mechanism implements 64 ports by adding 3 additional CLAV/ENB signals for a total of 4 pairs. Each CLAV/ENB pair represents a 16-port group.

UTOPIA PORT MAPPING

The Multi-PHY addressing scheme outlined in the ATM Forum UTOPIA-2 standard, Appendix 1, example A1.1 is used by the ASPEN-PX. Each independent CLAV/ENB pair represents a 16-port group using the 5-bit UTOPIA address. This is illustrated in the following table:

Logical port number for ASPEN header lookup	CLAV/ENB Pair	Master UTOPIA address
0 - 15	0	Base_utopia_address + 15
16 - 31	1	Base_utopia_address + 15
32 - 47	2	Base_utopia_address + 15
48 - 63	3	Base_utopia_address + 15

INGRESS ATM HEADER LOOKUP

The ASPEN-PX appends 2 bytes to the 54 byte cell (total = 56 bytes) which encodes the source port in the lower 6 bits. The upper 10 bits are padded 0s.

Cell Format from ASPEN-PX to ASPEN

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad = 0								0	0	**PHY ID**					
1	ATM Header[31:16]															
2	ATM Header[15:0]															
3	UDF1 (HEC)								UDF2 (Unused)							
4	Payload byte 0								Payload byte 1							
5	Payload byte 2								Payload byte 3							
6	Payload byte 4								Payload byte 5							
7	Payload byte 6								Payload byte 7							
8	Payload byte 8								Payload byte 9							
9	Payload byte 10								Payload byte 11							
10	Payload byte 12								Payload byte 13							
11	Payload byte 14								Payload byte 15							
12	Payload byte 16								Payload byte 17							
13	Payload byte 18								Payload byte 19							
14	Payload byte 20								Payload byte 21							
15	Payload byte 22								Payload byte 23							
16	Payload byte 24								Payload byte 25							
17	Payload byte 26								Payload byte 27							
18	Payload byte 28								Payload byte 29							
19	Payload byte 30								Payload byte 31							

20	Payload byte 32	Payload byte 33
21	Payload byte 34	Payload byte 35
22	Payload byte 36	Payload byte 37
23	Payload byte 38	Payload byte 39
24	Payload byte 40	Payload byte 41
25	Payload byte 42	Payload byte 43
26	Payload byte 44	Payload byte 45
27	Payload byte 46	Payload byte 47

Valid ASPEN-PX ports are 0-63 in the ingress direction and are reserved for user traffic ports. ASPEN-PX is compatible with the ASPEN (TXC-05810B) and utilizes a 30-bit direct header lookup mechanism to support a 64-port UNI interface. After ASPEN receives the cell, a header lookup process is initiated to insure a valid cell flow. A 14-bit index is used for the Header Lookup table (6-bit PHY, 8-bit VPI) and a 16-bit index is retained for the Inlet Connection table (16-bit VCI).

MEMORY INTERFACE

An asynchronous 32k x 32-bit or 64k x 32-bit SRAM is used to provide cell storage for outbound traffic. The clock is derived directly from ASPEN's transmit UTOPIA interface and operates up to 25 MHz. This interface can be configured as a single 32k x 32-bit memory or two 32k x 16-bit memories.

BUFFERS

In the upstream direction (toward ASPEN), buffering is kept internal and is 3 cells deep shared by all ports.

In the downstream direction (toward PHY), besides two internal 3-cell-deep shared buffers, a cell buffer is maintained in the external RAM for each UTOPIA port. The size is 16 cells for each port.

BACKPRESSURE

A backpressure control loop is required between the ASPEN-PX and ASPEN to control the cell scheduling toward each of the ASPEN-PX PHY egress ports. The backpressure messages are sent as cells at a periodic configurable rate depending on the maximum subscriber downlink rate supported. The backpressure messages are sent on UTOPIA Port 1, which functions as the control interface between the ASPEN-PX and ASPEN.

A buffer overflow protection mechanism is provided in the event that a cell buffer overflows for one of the 64-ports, resulting in cell discard.

PORT DESIGNATION TAG

From the ASPEN to ASPEN-PX, the ASPEN appends 2 bytes to the 54 byte cell (total = 56 bytes). The second byte includes a 6-bit value in the lower 6 bits which specifies the port destination. The LSB of the first byte is the multicast bit. If this bit is set to 0, the cell is a unicast cell and the port destination field is valid. If the multicast bit is set to 1, the cell is a multicast cell and the port destination field signifies the multicast session number (8 bits).

Cell Format from ASPEN to ASPEN-PX

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad = 0							**M**	**PHY ID or Multicast Session ID**							
1	ATM Header[31:16]															
2	ATM Header[15:0]															
3	UDF1 (HEC)								UDF2 (Unused)							
4	Payload byte 0								Payload byte 1							
5	Payload byte 2								Payload byte 3							
6	Payload byte 4								Payload byte 5							
7	Payload byte 6								Payload byte 7							
8	Payload byte 8								Payload byte 9							
9	Payload byte 10								Payload byte 11							
10	Payload byte 12								Payload byte 13							
11	Payload byte 14								Payload byte 15							
12	Payload byte 16								Payload byte 17							
13	Payload byte 18								Payload byte 19							
14	Payload byte 20								Payload byte 21							
15	Payload byte 22								Payload byte 23							
16	Payload byte 24								Payload byte 25							
17	Payload byte 26								Payload byte 27							
1‘8	Payload byte 28								Payload byte 29							
19	Payload byte 30								Payload byte 31							
20	Payload byte 32								Payload byte 33							
21	Payload byte 34								Payload byte 35							
22	Payload byte 36								Payload byte 37							
23	Payload byte 38								Payload byte 39							
24	Payload byte 40								Payload byte 41							
25	Payload byte 42								Payload byte 43							
26	Payload byte 44								Payload byte 45							
27	Payload byte 46								Payload byte 47							

MULTICAST

Multicast on ASPEN-PX is implemented as a compatible version of *CellBus* multicast, but offers a reduced set of features from ASPEN-only multicast. It supports the same 256 sessions with up to 64 spatial multicast leaves for each session, but will not offer egress header translation or per-VC statistics for each leaf. *CellBus* multicast cells are held by ASPEN in one of the *CellBus* multicast queues prior to being sent to ASPEN-PX. The ASPEN scheduler will service all multicast sessions round robin.

A cell arriving from the ASPEN that is designated as a multicast cell by the multicast tag bit is buffered in a dedicated multicast queue to await scheduling on all participating ports. The depth of the ASPEN-PX multicast

queue is provided in the backpressure message to control ASPEN multicast scheduling. The multicast cell at the head of the queue is eligible for transmission on each of the participating ports. Each multicast cell is identified as being part of a multicast session by the port destination field. The 8-bit value (2^{nd} byte of the cell) represents an entry into a 256 x 64 multicast session table. Each entry into the table contains a unary encoding for all destination ports of the multicast session. The multicast cell is sent to every port designated in the multicast session table for the designated session. Multicast cells from the multicast queue destined for a given port are multiplexed with unicast cells buffered in the 64 unicast port queues. A programmable multicast timeout expiration is used to insure that inactive or inoperative ports do not create a head-of-line blocking condition, if they cannot accept the multicast cell in a maximum delay time.

The Multicast Session Table (MST) is programmed using in-band control cells. The host processor is responsible for setup and maintenance of the MST and sends the control cells to the ASPEN-PX using the Outlet Processor inbox. One control cell is required to configure a single multicast session. A unary encoding method of ports participating in this multicast session is used. The ASPEN-PX does not enqueue these control cells but decodes the MST programming code and writes the MST entry to the MST table.

Features not supported with ASPEN-PX multicast are: logical multicast, egress header translation, and per-VC statistics for each leaf.

CLOCK DOMAINS

The ASPEN-PX has two clock domains: ADCLK for the UTOPIA receive interface (from ASPEN to PHY) and the AUCLK for the UTOPIA transmit interface (from PHY to ASPEN). The ASPEN device supplies both the AUCLK and ADCLK clocks. The SRAM interface is driven by the receive clock (ADCLK).

Note: For accurate POST results:

a.) Reset should occur when no clocks are present.

b.) AUCLK should start no later than ADCLK.

ASPEN-PX CONFIGURATION/STATUS

The mechanism used to communicate with the ASPEN-PX are inband control cells coming from the ASPEN. Command messages are sent via the Outlet Processor inbox and response messages are received by the Inlet Processor outbox.

Configuration/Status Items

Configuration and Status:

1. UTOPIA base address for every group of 16 subscriber ports
2. PHY side UTOPIA width 8/16
3. Backpressure message delay time
4. Multicast session table 256 x 64
5. Multicast delay timeout
6. Reset lead

Status only:

1. Per-port FIFO depth
2. Per-port congestion discard count 16-bit

Command Message Format

ASPEN-PX management is integrated with ASPEN management procedures/protocols and supported by the ATM AccessEDGE device driver. All configuration parameters may be written and read by the host by sending write/read requests to ASPEN via the Outlet Processor inbox. Response messages will be returned via the Inlet Processor outbox. No acknowledgement is sent by ASPEN-PX after receiving a configuration command.

These new command messages are sent/received in a 64-byte message consistent with existing Host-to-ASPEN message formats.

	BIT # / BYTE #	7	6	5	4	3	2	1	0
WORD 0	**3**	OPCODE=00100					0=Write	1=GPBus	1=DRQ
	2	0	0	0	LENGTH = EH				
	1	SRC = 01100 (host)					DEST = 00101 (OP)		
	0	DEST (cont)		SR=0	IRH = 0				
WORD 1	**3**	00H							
	2	00H							
	1	00H							
	0	00H							
WORD 2	**3**	00H (not used, CBRH)							
	2	00H (not used, CBRH)							
	1	00H (not used, TRH)							
	0	00H (not used, TRH)							
WORD 3	**3**	FFH (ATM Cell Header)							
	2	FFH (ATM Cell Header)							
	1	FFH (ATM Cell Header)							
	0	F0H (ATM Cell Header)							
WORD 4	**3**	00H (future use)							
	2	00H (future use)							
	1	**Message ID=00H**							
	0	**Message Sub ID=xxH (ASPEN-PX message specific)**							
WORD 5	**3**	Payload							
	2	|							
	1	|							
	0	|							
WORD 6	**3**	V							
	2								
	1								
	0								
WORD 7	**3**								
	2								
	1								
	0								
WORD 8-15	**3**								
	2								
	1								
	0								

Figure 3. Host-to-ASPEN Message Format

SYSTEM OVERVIEW

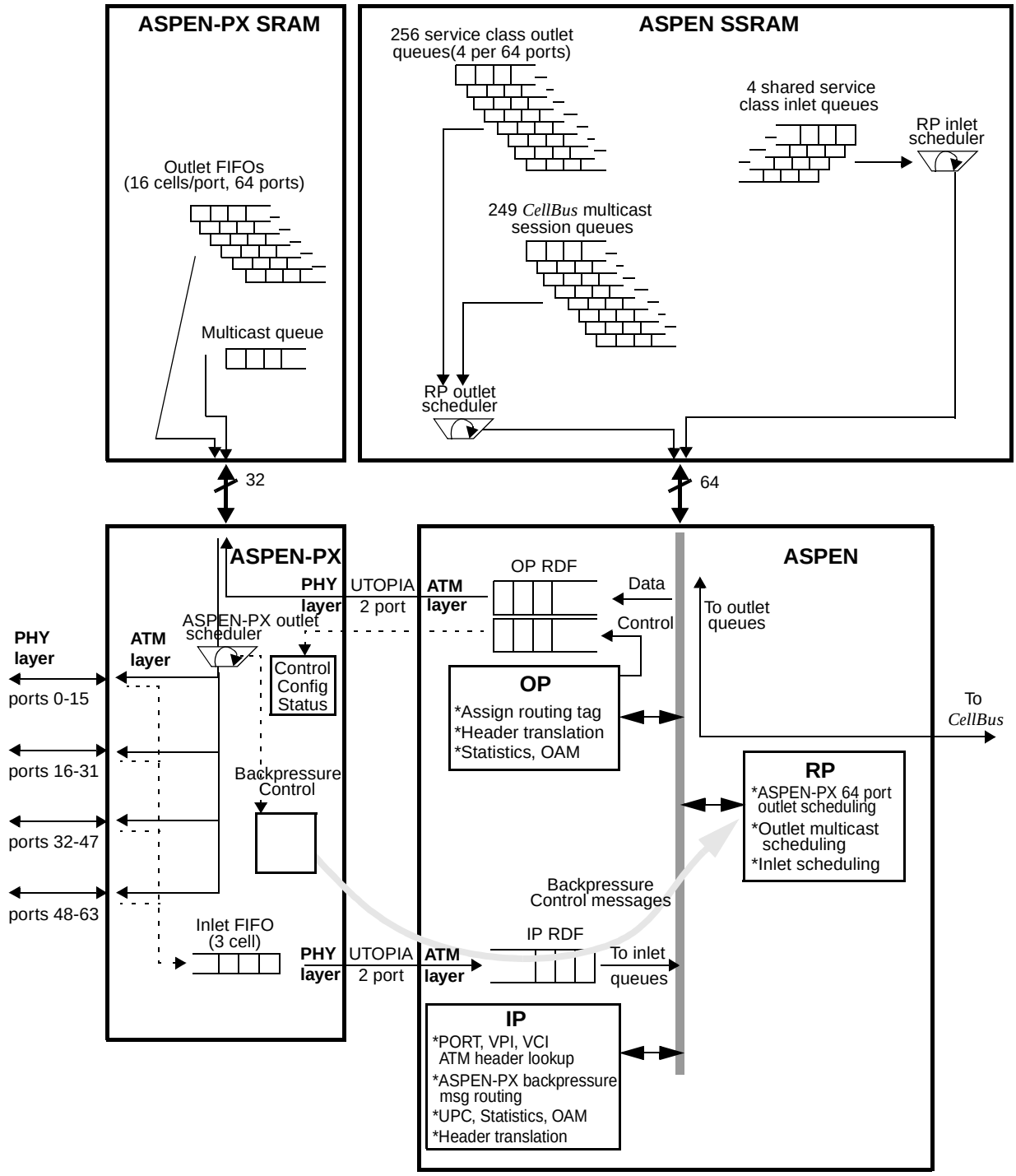


Figure 4. ASPEN-PX (TXC-05811)/ASPEN (TXC-05810B) Data Flow Diagram

Upstream Data Flow

Subscriber traffic enters the ASPEN-PX through its 64-port UTOPIA interface where it is buffered in a 3-cell Rate Decoupling FIFO (RDF). When a cell enters the RDF a 2-byte routing tag is prepended to the front of the cell identifying the source port ID. The UTOPIA slave to ASPEN is immediately notified (as soon as the entire cell has been stored) that a cell is available to be read out from the RDF. Cells written into the RDF are immediately available to be clocked out the UTOPIA interface to the ASPEN. The ASPEN-PX and ASPEN use UTOPIA address 0 for the user data port and UTOPIA address 1 for the ASPEN-PX control port. This insures control path integrity under heavy traffic load conditions. If the user data port RDF fills, the master UTOPIA interface must be notified to stop requesting cells from the subscriber PHYs until a cell slot becomes available in the RDF. The ASPEN uses the prepended routing tag applied by ASPEN-PX to initiate a header lookup.

Downstream Data Flow

The ASPEN will maintain 256 unicast service category queues (4 per port), and 249 multicast queues. It also maintains a congestion table which indicates congestion status for the multicast queue, and unicast queues. Cells enter from the *CellBus* interface and are automatically enqueued by the Tandem Routing Header. Using the outlet queue state and ASPEN-PX congestion status, the RP dequeues cells toward the ASPEN-PX. The cells pass through the Outlet Processor, where they go through connection table lookup, header translation, and statistics maintenance before having a routing tag prepended for use by the ASPEN-PX. The ASPEN-PX uses the routing tag for final port queuing before forwarding traffic to the PHY device. The maximum traffic rate recommended for a single-PHY device is 14 Mbit/s.

ASPEN-PX (TXC-05811)/ASPEN (TXC-05810B) COMMUNICATION

Control communication between ASPEN and ASPEN-PX is required for:

1. Configuration setup of messages to the ASPEN-PX
2. Status request messages to the ASPEN-PX
3. Status response messages to the ASPEN
4. Congestion backpressure messages to the ASPEN

To provide a reliable control path to the ASPEN-PX, a UTOPIA port is dedicated for control message use. A hardcoded convention is suitable for this internal interface. ASPEN's internal port 0 uses UTOPIA address 0 for the data port. ASPEN's internal port 1 uses UTOPIA address 1 for the control port. To send control, configuration, or status request messages to the ASPEN-PX, the host sends the request to the Outlet Processor inbox who forwards the request message to the port 1 interface. Similarly, status response messages and backpressure messages enter the ASPEN on port 1. Status messages are forwarded to the host using the Inlet Processor outbox while backpressure messages are forwarded to the Rate Processor for processing.

ASPEN DRIVER API FUNCTIONS (HOST)

The ASPEN driver for ATM AccessEdge control firmware includes a set of API functions which direct messages to ASPEN for control and status communication through the ASPEN host mailbox. These functions include the following commands required for a complete system design:

ASPEN-PX Diagnostic Loopback: The diagnostic loopback API is used by the host to verify connectivity to ASPEN-PX over the UTOPIA interface.

ASPEN-PX Device Information Retrieval: Host retrieves revision level, TranSwitch part number and manufacturing information of the ASPEN-PX device and results of POST.

ASPEN-PX Configure UTOPIA API: This API is provided for the host processor to write the master (subscriber-side) UTOPIA configuration parameters.

ASPEN-PX Get UTOPIA Configuration API: This API is provided for the host processor to retrieve the UTOPIA configuration parameters.

ASPEN-PX Get UTOPIA Error API: This API is provided for the host processor to retrieve the UTOPIA errors.

ASPEN-PX Reset UTOPIA Error Count API: This API is provided for the host processor to reset the UTOPIA error counts.

ASPEN-PX Configure Backpressure API: Backpressure cells must be generated by ASPEN-PX periodically to support a closed-loop scheduler between ASPEN and the subscriber TX UTOPIA ports. This API is provided for the host processor to configure backpressure delay time in terms of elapsed UTOPIA slave TX clock ticks.

ASPEN-PX Get Backpressure Configuration API: This API is provided for the host processor to determine the backpressure delay time in terms of elapsed UTOPIA slave TX clock ticks.

ASPEN-PX Reset Port Discard API: Host resets the port discard counters.

ASPEN-PX Get Port Discard Counters API: Host retrieves the port discard counters.

ASPEN-PX Set Multicast Configuration API: Host sets the multicast configuration parameters.

ASPEN-PX Read Multicast Configuration API: Host retrieves the multicast configuration parameters.

ASPEN-PX Reset Queue API: Host resets a specific queue on the ASPEN-PX. When to use: If a port is experiencing frequent cell discards due to ASPEN-PX queue congestion, this message will be sent to ASPEN-PX to begin at an initial state and realign ASPEN scheduler with ASPEN-PX. Effects: Upon reception of this message, the ASPEN-PX discards all cells in the queue and resets the "Port 'n' cells sent" counter to its initial value of zero.

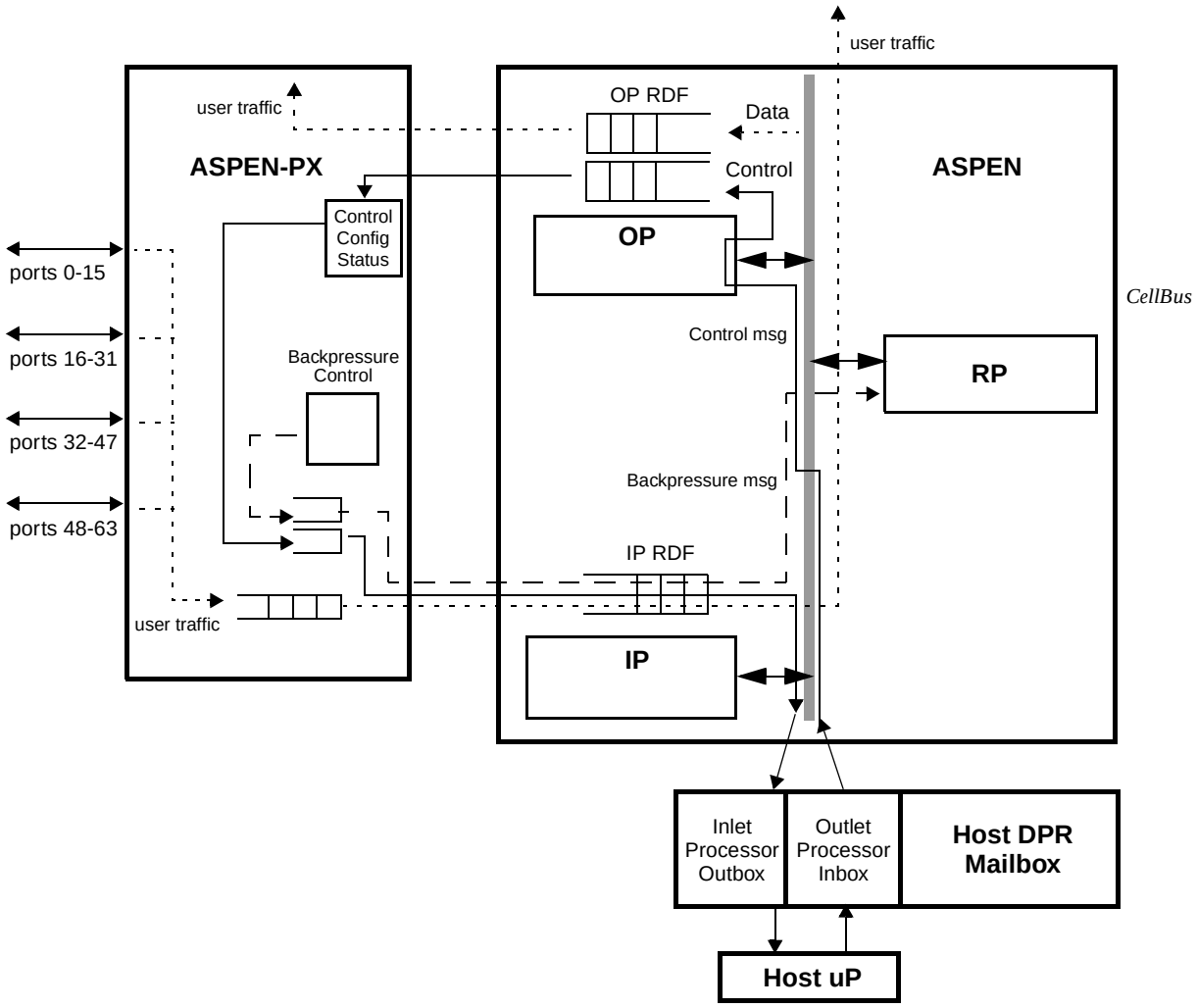


Figure 5. ASPEN-PX Control Path

ASPEN-PX MESSAGES

Backpressure

Backpressure cells are generated by the ASPEN-PX periodically to support a closed-loop scheduler between the ASPEN and the subscriber transmit UTOPIA ports. Based on ASPEN-PX UTOPIA clock of 25 MHz, a nominal value of 16384 (4000H) should be used for the Backpressure_message_delay. The backpressure cell contains congestion information for all 65 queues (64 unicast user queues and 1 multicast queue).

Table 1. Diagnostic Loopback Message Format

This message has a user defined payload which is assigned and verified by the host processor. It is used to verify connectivity and integrity of the UTOPIA interface between ASPEN and ASPEN-PX.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0		CLP=0	
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 02H (Loopback response), 03H (Loopback request)**							
6-27	Diagnostic Message Payload															

Table 2. Revision Message Format

The revision message is used by the host to read the hardware revision of ASPEN-PX.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0			CLP=0
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 04H (Revision request msg), 05H (Reserved)**							
6	ASPEN-PX Part Number=16B3H (TXC-05811)															
7	Version=1				Mask Level=1				Growth Field=0				Not Used=0			
8	Not Used=0															
9	Manufacturer ID=006BH															
10																
11	QPRF	MSTRF	BPRF	CMRF	OEGRF	OIGRF	IGRF	SRAMF								Reserved
12-27	Not Used=0															

POST Results in UTOPIA Word 11

QPRF - Queue Pointer RAM Failure
MSTRF - Multicast Session Table RAM Failure
BPRF - Backpressure RAM Failure
CMRF - Control Message RAM Failure
OEGRF - Outlet Egress FIFO RAM Failure
OIGRF - Outlet Ingress FIFO RAM Failure
IGRF - Inlet FIFO RAM Failure
SRAMF - SRAM Failure

Notes:
1. For POST results, a value of "0" indicates pass. A value of "1" in any location indicates a failure.
2. For accurate POST results:
   a.) Reset should occur when no clocks are present.
   b.) AUCLK should start no later than ADCLK.

Table 3. UTOPIA Configuration/Status Message Format

This message writes or reads the master (subscriber-side) UTOPIA configuration parameters.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0		CLP=0	
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 10H (Read UTOPIA config), 11H (Write UTOPIA config)**							
6																
7													Base_utopia_address			
8																
9																Ut16
10																
11																Ut_ parity
12																
13															Utopia_group_ enable	
14-27	Not Used															

1. Base_utopia_address: 4-bit UTOPIA address to begin polling. 16 consecutive addresses will be polled beginning at the base address. Largest value allowed is FH.
2. Ut16: 0 = Master UTOPIA bus is in 8-bit mode
   1 = Master UTOPIA bus is in 16-bit mode.
3. Ut_parity: 0 = Master UTOPIA has odd parity disabled
   1 = Master UTOPIA has odd parity enabled.
4. Utopia_group_enable: Identifies which UTOPIA CLAV/ENB pairs are active on the master (subscriber-side) UTOPIA bus.

   0: Group 0 enabled

   1: Groups 0 and 1 enabled

   2: Groups 0, 1, and 2 enabled

   3: Groups 0, 1, 2, and 3 enabled

Table 4. UTOPIA status message

This message writes (clears) or reads the UTOPIA error counters. These are rollover counters and will not clear after read. To clear the counters, the host writes a zero. All counters must be cleared together in the same write operation.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0			CLP=0
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 12H (Read UTOPIA status), 13H (Write UTOPIA status to clear it)**							
6																
7	Master_utopia_SOC_errors															
8																
9	Master_utopia_parity_errors															
10																
11	Slave_utopia_SOC_errors															
12																
13	Slave_utopia_parity_errors															
14-27	Not Used															

1. Master_utopia_SOC_errors: 16-bit rollover counter of the SOC errors detected on the UTOPIA bus which interfaces with the subscriber PHY devices. A SOC error is detected when a SOC signal is either not asserted by a subscriber PHY after being selected OR asserted during the middle of a cell transfer.
2. Master_utopia_parity_errors: 16-bit rollover counter of the odd-parity errors detected during RX cell transfers on the UTOPIA bus which interfaces with the subscriber PHY devices.
3. Slave_utopia_SOC_errors: 16-bit rollover counter of the SOC errors detected on the UTOPIA bus which interfaces with the ASPEN. A SOC error is detected when a SOC signal is either not asserted by ASPEN after being selected OR asserted during the middle of a cell transfer.
4. Slave_utopia_parity_errors: 16-bit rollover counter of the odd-parity errors detected during RX cell transfers on the UTOPIA bus which interfaces with ASPEN.
5. A SOC error is indicated for each clock cycle that the SOC is not present, while the enable is low.
6. The UTOPIA error counters may detect spurious errors during the power-up sequence. The UTOPIA error counters should be reset after the ASPEN-PX device has been initialized.

Table 5. Backpressure Configuration/Status Message Format

This message writes or reads the backpressure configuration parameter.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0		CLP=0	
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 14H (Read backpressure delay), 15H (Write backpressure delay)**							
6																
7	Backpressure_message_delay															
8-27	Not Used															

1. Backpressure_message_delay: 16-bit counter indicating number of UTOPIA slave TX clock ticks that should elapse between backpressure message updates to ASPEN.

Table 6. Port Discard Initialization/Status Message Format

This message writes or reads the Port Discard parameters.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0			CLP=0
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 16H (Read discard counts), 17H (Write discard counts to clear it)**							
6																
7													Mcast discard count			
8	Port 7 discard count				Port 6 discard count				Port 5 discard count				Port 4 discard count			
9	Port 3 discard count				Port 2 discard count				Port 1 discard count				Port 0 discard count			
10	Port 15 discard count				Port 14 discard count				Port 13 discard count				Port 12 discard count			
11	Port 11 discard count				Port 10 discard count				Port 9 discard count				Port 8 discard count			
12	Port 23 discard count				Port 22 discard count				Port 21 discard count				Port 20 discard count			
13	Port 19 discard count				Port 18 discard count				Port 17 discard count				Port 16 discard count			
14	Port 31 discard count				Port 30 discard count				Port 29 discard count				Port 28 discard count			
15	Port 27 discard count				Port 26 discard count				Port 25 discard count				Port 24 discard count			
16	Port 39 discard count				Port 38 discard count				Port 37 discard count				Port 36 discard count			
17	Port 35 discard count				Port 34 discard count				Port 33 discard count				Port 32 discard count			
18	Port 47 discard count				Port 46 discard count				Port 45 discard count				Port 44 discard count			
19	Port 43 discard count				Port 42 discard count				Port 41 discard count				Port 40 discard count			
20	Port 55 discard count				Port 54 discard count				Port 53 discard count				Port 52 discard count			
21	Port 51 discard count				Port 50 discard count				Port 49 discard count				Port 48 discard count			
22	Port 63 discard count				Port 62 discard count				Port 61 discard count				Port 60 discard count			
23	Port 59 discard count				Port 58 discard count				Port 57 discard count				Port 56 discard count			
24	DP63	DP62	DP61	DP60	DP59	DP58	DP57	DP56	DP55	DP54	DP53	DP52	DP51	DP50	DP49	DP48
25	DP47	DP46	DP45	DP44	DP43	DP42	DP41	DP40	DP39	DP38	DP37	DP36	DP35	DP34	DP33	DP32
26	DP31	DP30	DP29	DP28	DP27	DP26	DP25	DP24	DP23	DP22	DP21	DP20	DP19	DP18	DP17	DP16
27	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0

1. Port xx discard count: 4-bit rollover counter indicating the number of cells that have been discarded due to downstream queue overflow for a given port.
2. DP63 - DP0 (Dead PHY): This field is read-only; write operations have no effect. Status bit indicating which subscriber ports are experiencing multicast timeouts. This status is used by the host processor to locate all ports with multicast timeouts in effect. Status bit is reset by ASPEN-PX after a single CLAV is asserted by the PHY device.

Table 7. Multicast Session Table Message Format

This message writes or reads a single Multicast Session Table entry. There are 256 session entries. Each multicast session corresponds directly with a *CellBus* multicast session. All multicast parameters must be specified for any write operations.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0		CLP=0	
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 18H (Read MST entry), 19H (Write MST entry)**							
6																
7									Multicast Session ID							
8	P63	P62	P61	P60	P59	P58	P57	P56	P55	P54	P53	P52	P51	P50	P49	P48
9	P47	P46	P45	P44	P43	P42	P41	P40	P39	P38	P37	P36	P35	P34	P33	P32
10	P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
11	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
12																
13	Multicast_timeout															
14-27	Not Used															

1. Multicast session ID: 8-bit field identifying the multicast session table entry to be read or written.
2. P63 - P0: Port bit indicating which ports are participating in a given multicast session.
   0 = Not participating
   1 = Participating
3. Multicast_timeout: The multicast timeout is used to control head-of-line blocking on the multicast queue. The multicast cell that is at the head of the queue is the "active" cell and is replicated to all participating ports based on the multicast session table entry. A multicast cell destined for a given port has priority over a unicast cell destined for the same port. The multicast timeout limits the amount of time a cell is allowed to sit at the head of the queue without being sent to all participating ports. The multicast timeout is in terms of ASPEN-PX ADCLK ticks. For reference, a timeout value of three cell times on the slowest link is suggested, but the timeout can be adjusted above or below this reference value. With a 25 MHz ADCLK and 2.3 Mbit/s SHDSL traffic, a multicast timeout of 3000H is suggested. For 8 Mbit/s ADSL traffic, a multicast timeout of 1000H is suggested.

Table 8. Reset Queue Message Format

This message is write-only and specifies which queue should be reset. The multicast queue will also be reset using this message. If a port is experiencing frequent cell discards due to ASPEN-PX queue congestion, this message will be sent to ASPEN-PX to begin at an initial state and realign the ASPEN scheduler with the ASPEN-PX. Upon reception of this message, the ASPEN-PX will discard all cells in the queue and reset the **"Port 'n' cells sent"** counter to its initial value of zero. The **"Queue_number"** is 0 - 3FH for the unicast queues and 40H for the multicast queue.

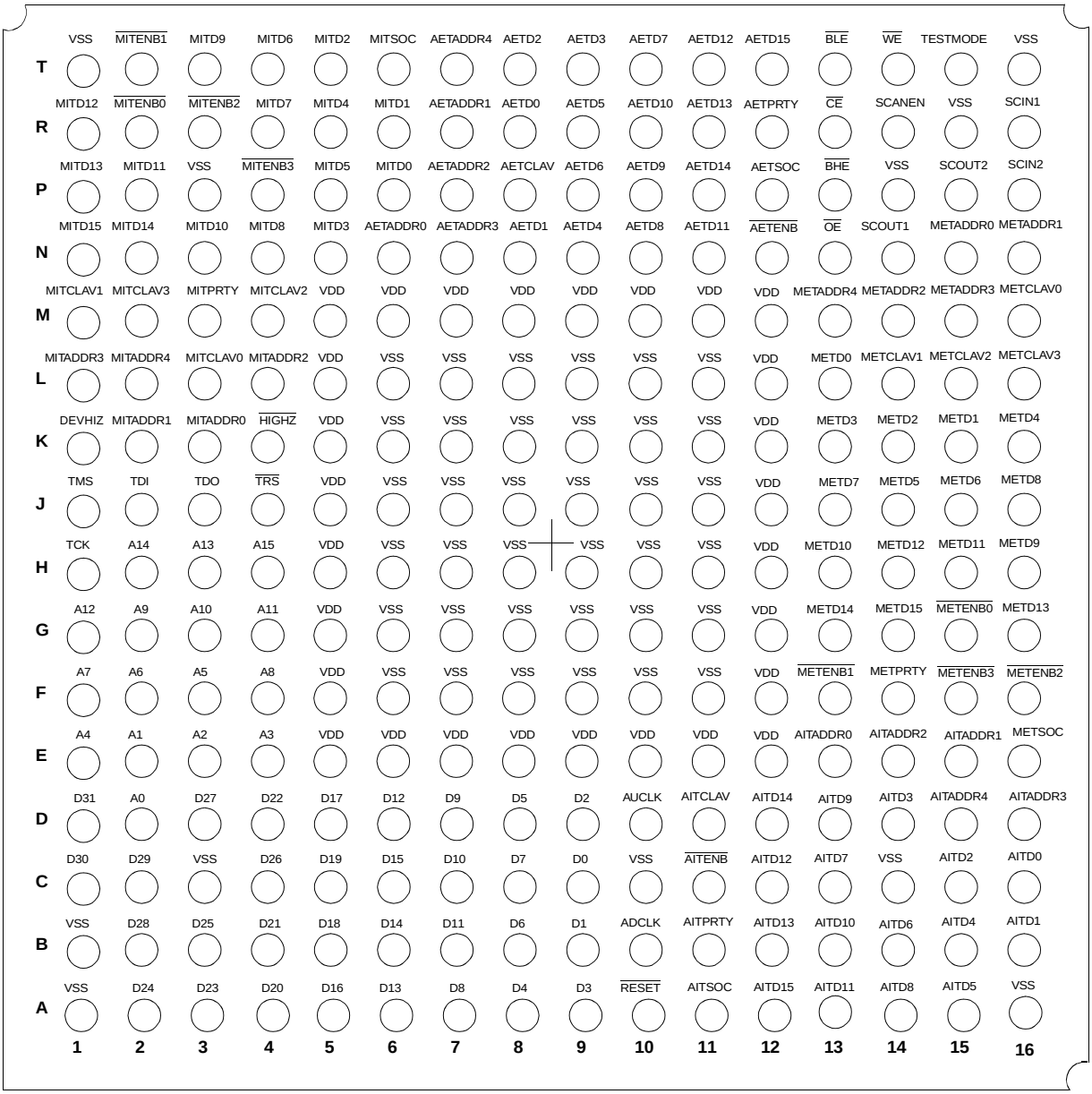
The sequence to perform a scheduler reset from the host is as follows:

1. Determine repeated queue congestion errors are occurring.
2. Set "port discard" state in the Rate Processor to halt scheduling toward ASPEN-PX for a port.
3. Send "Reset Queue" control message to ASPEN-PX for specific queue.
4. Use Maskable Data RAM write to initialize the appropriate 4-bit port scheduler counter in the RP with ASPEN-PX.
5. Release "port discard" state in the Rate Processor to resume scheduling toward ASPEN-PX.

UTOPIA Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Pad=0							M=0	**PHY ID = 00H**							
1	GFC=0				VPI=0								VCI (15:12)=0			
2	VCI (11:0)=0												PTI=0		CLP=0	
3	HEC								Pad							
4																
5	**Message ID=00H**								**Message Sub ID= 1AH (Not Used), 1BH (Reset queue#)**							
6																
7										Queue_number						
8-27	Not Used															

LEAD DIAGRAM

Bottom view of package



SOLDER BALL
A1 CORNER

Note: The dimensions of the package are shown in Figure 16, the bottom view of which is rotated 90°.

Figure 6. ASPEN-PX TXC-05811 Lead Diagram

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT LEADS

Symbol	Lead No.	I/O/P*	Type	Name/Function
VDD	E5, E6, E7, E8, E9, E10, E11, E12, F5, F12, G5, G12, H5, H12, J5,J12, K5, K12, L5, L12, M5, M6, M7, M8, M9, M10, M11, M12	P		V_{DD}: +3.3 volt supply voltage, ±5%
VSS	A1, A16, B1, C3, C10 C14, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, L11, P3, P14, R15, T1, T16	P		V_{SS}: Ground, 0 volt reference.

* Note: I=Input; O=Output; P=Power; T=Tristate

TERMINAL EGRESS INTERFACE (ASPEN)

Symbol	Lead No.	I/O/P	Type *	Name/Function
$\overline{\text{AETENB}}$	N12	I	LVTTL	**ASPEN Egress Terminal Enable:** Active low read enable signal for cell transfer from ASPEN-PX to ASPEN.
AETCLAV	P8	O (T)	TTL 8mA	**ASPEN Egress Terminal Cell Available:** Egress terminal output in PHY mode. Active high signal indicating a cell space is available to be sent to the ATM device.
AETD(15-0)	T12, P11, R11, T11, N11, R10, P10, N10, T10, P9, R9, N9, T9, T8, N8, R8	O (T)	TTL 8mA	**ASPEN Egress Terminal Data:** 16-bit output data bus for cell transfers from ASPEN-PX to ASPEN.
AETSOC	P12	O (T)	TTL 8mA	**ASPEN Egress Terminal Start of Cell:** Start of Cell indicator from ASPEN-PX to ASPEN.
AETADDR(4-0)	T7, N7, P7, R7, N6	I	LVTTL	**ASPEN Egress Terminal Multi-PHY Address:** Used for polling the ASPEN-PX to determine the availability of a cell.
AETPRTY	R12	O (T)	TTL 8mA	**ASPEN Egress Terminal Parity:** Odd parity over AETD(15-0).

* See Input, Output and Input/Output Parameters section for Type descriptions.

TERMINAL EGRESS INTERFACE (Multi-PHY)

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{METENB(3-0)}}$	F15, F16, F13, G15	O (T)	TTL 8mA	**Multi-PHY Egress Terminal Enable:** Active low read enable signal for cell transfer from ASPEN-PX to PHY.
METCLAV(3-0)	L16, L15, L14, M16	I	LVTTL	**Multi-PHY Egress Terminal Cell Available:** Active high signal indicating a cell is available for transfer from ASPEN-PX to a PHY group.
METD(15-0)	G14, G13, G16, H14, H15, H13, H16, J16, J13, J15, J14, K16, K13, K14, K15, L13	O (T)	TTL 8mA	**Multi-PHY Egress Terminal Data:** 8/16-bit output data bus for cell transfers from ASPEN-PX to PHY.
METSOC	E16	O (T)	TTL 8mA	**Multi-PHY Egress Terminal Start of Cell:** Start of Cell indicator for transfer from ASPEN-PX to PHY.
METADDR(4-0)	M13, M15, M14, N16, N15	O (T)	TTL 8mA	**Multi-PHY Egress Terminal Multi-PHY Address:** Used for polling each PHY group to determine the availability of a cell.
METPRTY	F14	O (T)	TTL 8mA	**Multi-PHY Egress Terminal Parity:** Odd parity over METD(15-0) or METD(7-0).

TERMINAL INGRESS INTERFACE (ASPEN)

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{AITENB}}$	C11	I	LVTTL	**ASPEN Ingress Terminal Enable:** Active low read enable signal for cell transfer from ASPEN to ASPEN-PX.
AITCLAV	D11	O (T)	TTL 8mA	**ASPEN Ingress Terminal Cell Available:** Active high signal indicating that a cell is available for transfer from ASPEN to ASPEN-PX.
AITD(15-0)	A12, D12, B12, C12, A13, B13, D13, A14, C13, B14, A15, B15, D14, C15, B16, C16,	I	LVTTL	**ASPEN Ingress Terminal Data:** 16-bit input data bus for cell transfers from ASPEN to ASPEN-PX.
AITSOC	A11	I	LVTTL	**ASPEN Ingress Terminal Start of Cell:** Start of Cell indicator from ASPEN to ASPEN-PX.
AITADDR(4-0)	D15, D16, E14, E15, E13	I	LVTTL	**ASPEN Ingress Terminal Multi-PHY Address:** Used for polling the ASPEN-PX to determine the availability of a cell space.
AITPRTY	B11	I	LVTTL	**ASPEN Ingress Terminal Parity:** Odd parity over AITD (15-0).

TERMINAL INGRESS INTERFACE (Multi-PHY)

Symbol	Lead No.	I/O/P	Type	Name/Function
$\overline{\text{MITENB(3-0)}}$	P4, R3, T2, R2	O (T)	TTL 8mA	**Multi-PHY Ingress Terminal Enable:** Active low read enable signal for cell transfer from PHY to ASPEN-PX.
MITCLAV(3-0)	M2, M4, M1, L3	I	LVTTL	**Multi-PHY Ingress Terminal Cell Available:** Active high signal indicating that a cell is available for transfer from a PHY group to ASPEN-PX.
MITD(15-0)	N1, N2, P1, R1, P2, N3, T3, N4, R4, T4, P5, R5, N5, T5, R6, P6	I	LVTTL	**Multi-PHY Ingress Terminal Data:** 8/16-bit input data bus for cell transfers from PHY to ASPEN-PX.
MITSOC	T6	I	LVTTL	**Multi-PHY Ingress Terminal Start of Cell:** Start of Cell indicator from PHY to ASPEN-PX.
MITADDR(4-0)	L2, L1, L4, K2, K3	O (T)	TTL 8mA	**Multi-PHY Ingress Terminal Multi-PHY Address:** Used for polling each PHY group to determine the availability of cell space.
MITPRTY	M3	I	LVTTL	**Multi-PHY Ingress Terminal Parity:** Odd parity over MITD(15-0) or MITD(7-0).

MISCELLANEOUS LEADS

Symbol	Lead No.	I/O/P	Type	Name/Function
ADCLK	B10	I	LVTTL	**ASPEN Downstream UTOPIA Clock:** 25 MHz maximum UTOPIA interface clock for the downstream direction (from ASPEN to ASPEN-PX).
AUCLK	D10	I	LVTTL	**ASPEN Upstream UTOPIA Clock:** 25 MHz maximum UTOPIA interface clock for the upstream direction (from ASPEN-PX to ASPEN).
$\overline{\text{RESET}}$	A10	I	LVTTL	**Hardware Reset:** An active low pulse with minimum width of 200 ns which must be asserted to reset all registers, counters, and FIFOs.
$\overline{\text{HIGHZ}}$	K4	O (T)	TTL 8 mA	**High Impedance Status:** TranSwitch internal use only. Leave unconnected.
DEVHIZ	K1	I	LVTTL	**Device High Impedance:** Active high signal to set all outputs (except TDO) to high-impedance (Hi-Z) state.

BOUNDARY SCAN AND OTHER TEST LEADS

Symbol	Lead No.	I/O/P	Type	Name/Function
TDO	J3	O (T)	TTL 8 mA	**Test Data Output:** Boundary scan output for data and test instructions from internal test registers.
$\overline{\text{TRS}}$	J4	I	LVTTLp	**Test Mode Reset:** A 1 microsecond (minimum) low on this lead resets the boundary scan; recommended for use after power-up initialization as well.
TMS	J1	I	LVTTLp	**Test Mode Select:** Boundary scan test mode select.
TDI	J2	I	LVTTLp	**Test Data Input:** Boundary scan input for data and test instructions.
TCK	H1	I	LVTTL	**Test Clock:** Boundary scan clock. Input signals are clocked in on its rising edge.
TESTMODE	T15	I	LVTTL	**Test Mode:** TranSwitch internal use only. Tie to VSS.
SCANEN	R14	I	LVTTL	**Scan Enable:** TranSwitch internal use only. Tie to VSS.
SCIN1	R16	I	LVTTL	**Scan In 1:** TranSwitch internal use only. Tie to VSS.
SCIN2	P16	I	LVTTL	**Scan In 2:** TranSwitch internal use only. Tie to VSS.
SCOUT1	N14	O (T)	TTL 8 mA	**Scan Out 1:** TranSwitch internal use only. Leave unconnected.
SCOUT2	P15	O (T)	TTL 8 mA	**Scan Out 2:** TranSwitch internal use only. Leave unconnected.

SRAM INTERFACE PORT

Symbol	Lead No.	I/O/P	Type	Name/Function
D(31-0)	D1, C1, C2, B2, D3, C4, B3, A2, A3, D4, B4, A4, C5, B5, D5, A5, C6, B6, A6, D6, B7, C7, D7, A7, C8, B8, D8, A8, A9, D9, B9, C9	I/O (T)	LVTTL/ TTL 8 mA	**SRAM Data:** Bidirectional 32-bit data bus used for reading input and writing output data to/from the external asynchronous SRAM.
A(15-0)	H4, H2, H3, G1, G4, G3, G2, F4, F1, F2, F3, E1, E4, E3, E2, D2	O (T)	TTL 8 mA	**SRAM Address:** 16-bit address output bus used to select external asynchronous SRAM address for read or write access.
$\overline{OE}$	N13	O (T)	TTL 8 mA	**SRAM Output (Read) Enable:** This output signal is asserted low to initiate an asynchronous SRAM read cycle.
$\overline{WE}$	T14	O (T)	TTL 8 mA	**SRAM Write Enable:** This output signal is asserted low to initiate an asynchronous SRAM write cycle.
$\overline{BHE}$	P13	O (T)	TTL 8 mA	**Bank High Enable:**
$\overline{BLE}$	T13	O (T)	TTL 8 mA	**Bank Low Enable:**
$\overline{CE}$	R13	O (T)	TTL 8 mA	**SRAM Chip Select:** Active low output signal enables the interface to the asynchronus SRAM and allows the transfer of information between the ASPEN-PX and the selected asynchronous SRAM.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply Voltage, 3.3 V nominal	V_{DD}	-0.3	4.6	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} +0.3	V	Note 1
Storage temperature range	T_S	-55	150	°C	Note 1
Ambient operating temperature	T_A	-40	85	°C	0 ft/min. linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative humidity, during assembly	RH	30	60	%	Note 2
Relative humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883E, Method 3015.7.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		22		^{o}C/W	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	3.15	3.30	3.45	V	
I_{DD}		227		mA	See Notes 1 and 2
P_{DD}		750		mW	See Notes 1 and 2

Notes:

1. Typical values are based on measurements made with nominal voltages, 25 ^{o}C ambient, and 25 MHz UTOPIA.
2. All I_{DD} and P_{DD} values are dependent upon V_{DD} and the bus operation.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS FOR LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current			10	µA	V_{DD}=3.45, V_{IN}=0 to 3.45
Input capacitance		5		pF	

INPUT PARAMETERS FOR LVTTLp (TTL WITH INTERNAL PULL-UP)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input current	-35	-115	-214	µA	$V_{IN}=V_{SS}$
Input leakage current			10	µA	$V_{IN}=V_{DD}$
Input capacitance		5		pF	

OUTPUT PARAMETERS FOR TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -8.0 mA
V_{OL}		0.2	0.4	V	I_{OL} = 8.0 mA
Tristate leakage current	-10		10	µA	
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

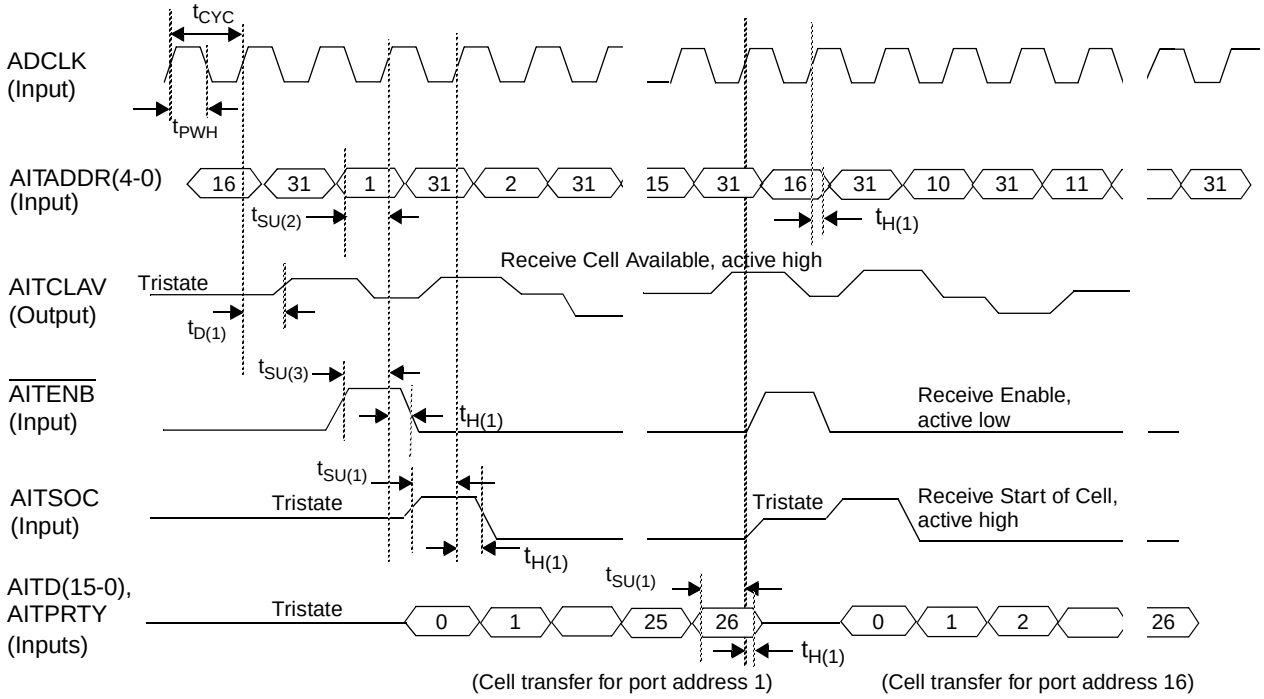
INPUT/OUTPUT PARAMETERS FOR LVTTL/TTL 8 mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.15 \leq V_{DD} \leq 3.45$
V_{IL}			0.8	V	$3.15 \leq V_{DD} \leq 3.45$
Input leakage current			10	µA	V_{DD} = 3.45
Input capacitance		7		pF	
V_{OH}	2.4			V	V_{DD} = 3.15; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 3.15; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

TIMING CHARACTERISTICS

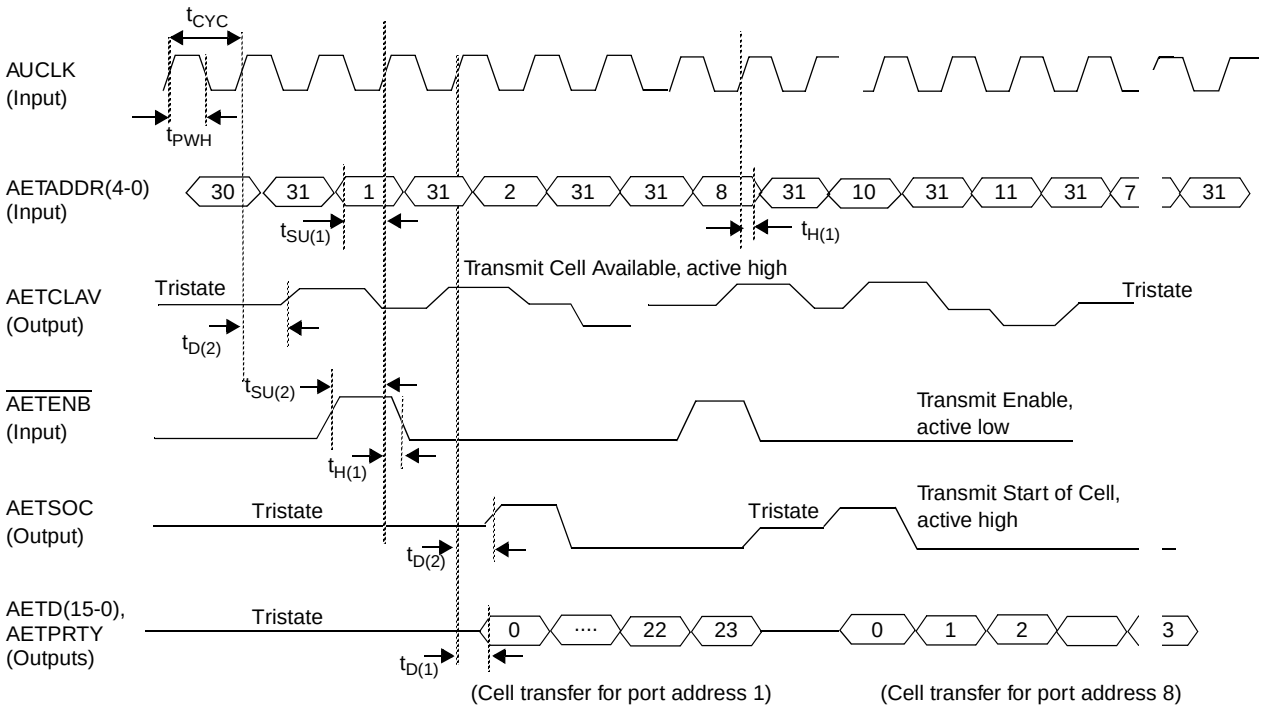
Detailed timing diagrams for the ASPEN-PX device are provided in Figures 7 through 15, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum 25 pF load capacitance, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ and $(V_{OH}+V_{OL})/2$, for input and output signals, respectively.

Figure 7. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 16-bit)



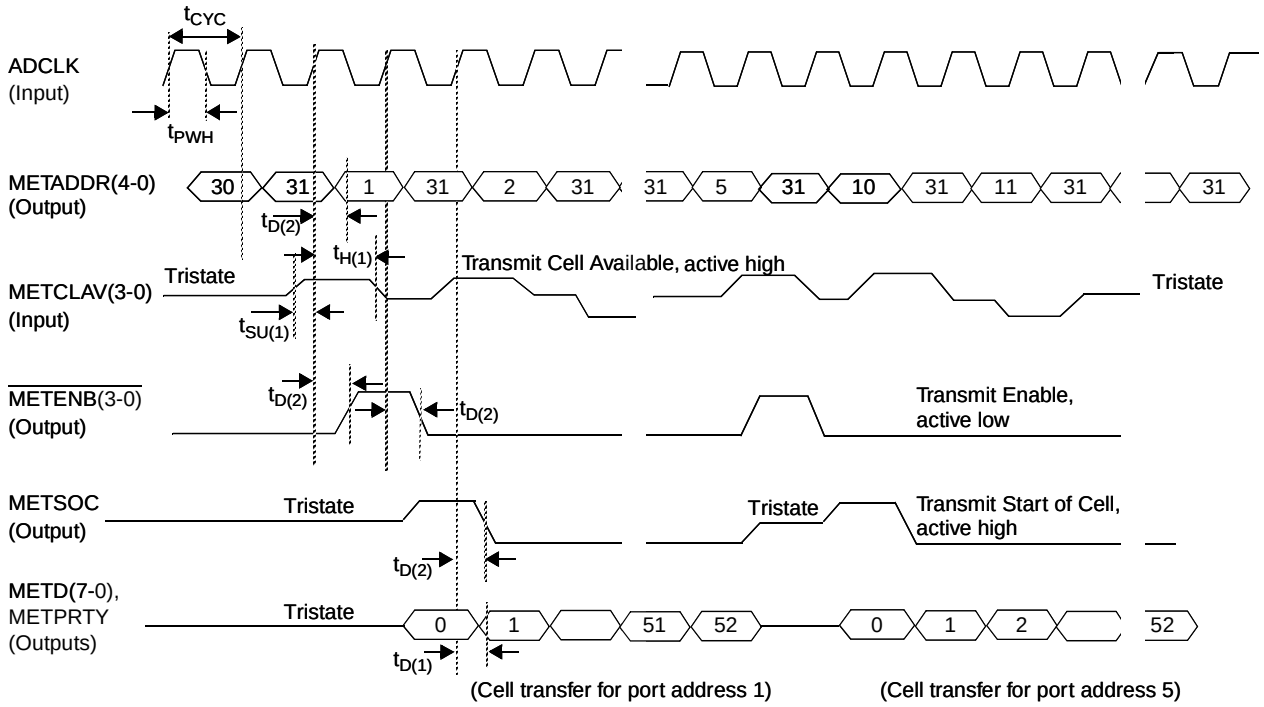
Parameter	Symbol	Min	Typ	Max	Unit
ADCLK clock cycle time	t_{CYC}	40			ns
ADCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
AITD(15-0), AITPRTY, AITSOC setup time to ADCLK↑	$t_{SU(1)}$	7.5			ns
AITADDR(4-0) setup time to ADCLK↑	$t_{SU(2)}$	7.5			ns
$\overline{\text{AITENB}}$ setup time to ADCLK↑	$t_{SU(3)}$	8.0			ns
AITD(15-0), AITPRTY, AITSOC, AITADDR(4-0), $\overline{\text{AITENB}}$ hold time after ADCLK↑	$t_{H(1)}$	0.0			ns
AITCLAV delay from ADCLK↑	$t_{D(1)}$	2.0		14	ns

Figure 8. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 16-bit)



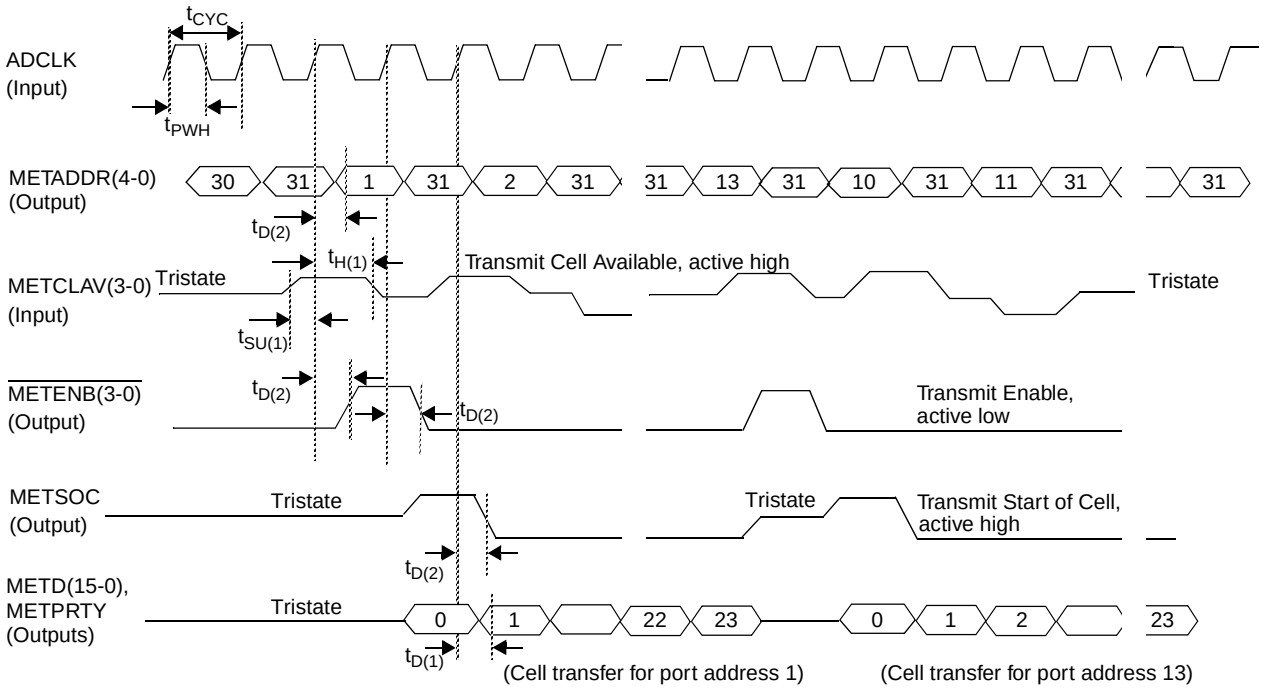
Parameter	Symbol	Min	Typ	Max	Unit
AUCLK clock cycle time	t_{CYC}	40			ns
AUCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
AETADDR(4-0) setup time to AUCLK↑	$t_{SU(1)}$	7.5			ns
$\overline{\text{AETENB}}$ setup time to AUCLK↑	$t_{SU(2)}$	13.0			ns
$\overline{\text{AETENB}}$, AETADDR(4-0) hold time after AUCLK↑	$t_{H(1)}$	0.0			ns
AETD(15-0), AETPRTY delay from AUCLK↑	$t_{D(1)}$	2.0		14	ns
AETSOC, AETCLAV delay from AUCLK↑	$t_{D(2)}$	2.0		14	ns

Figure 9. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 8-bit)



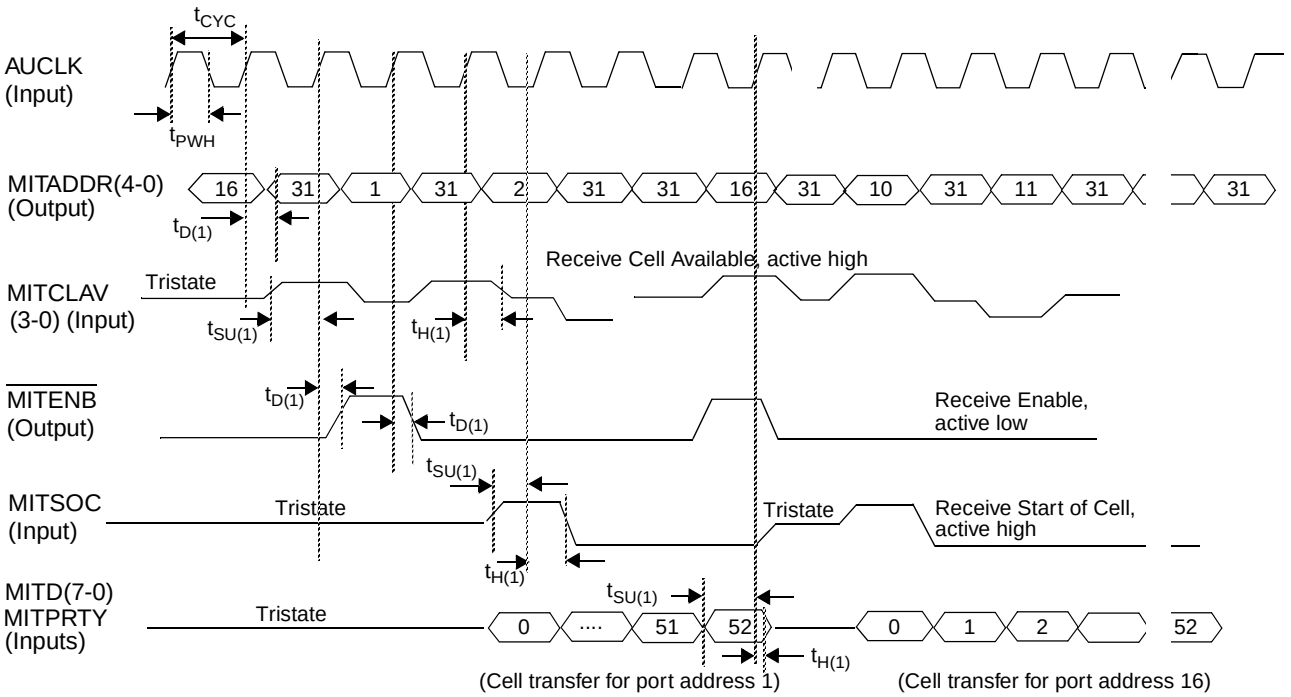
Parameter	Symbol	Min	Typ	Max	Unit
ADCLK clock cycle time	t_{CYC}	40			ns
ADCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
METCLAV setup time to ADCLK↑	$t_{SU(1)}$	7.5			ns
METCLAV hold time after ADCLK↑	$t_{H(1)}$	1.0			ns
METD(7-0), METPRTY delay from ADCLK↑	$t_{D(1)}$	2.0		14	ns
METSOC, METADDR(4-0), $\overline{\text{METENB}}$(3-0) delay from ADCLK↑	$t_{D(2)}$	2.0		14	ns

Figure 10. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 16-bit)



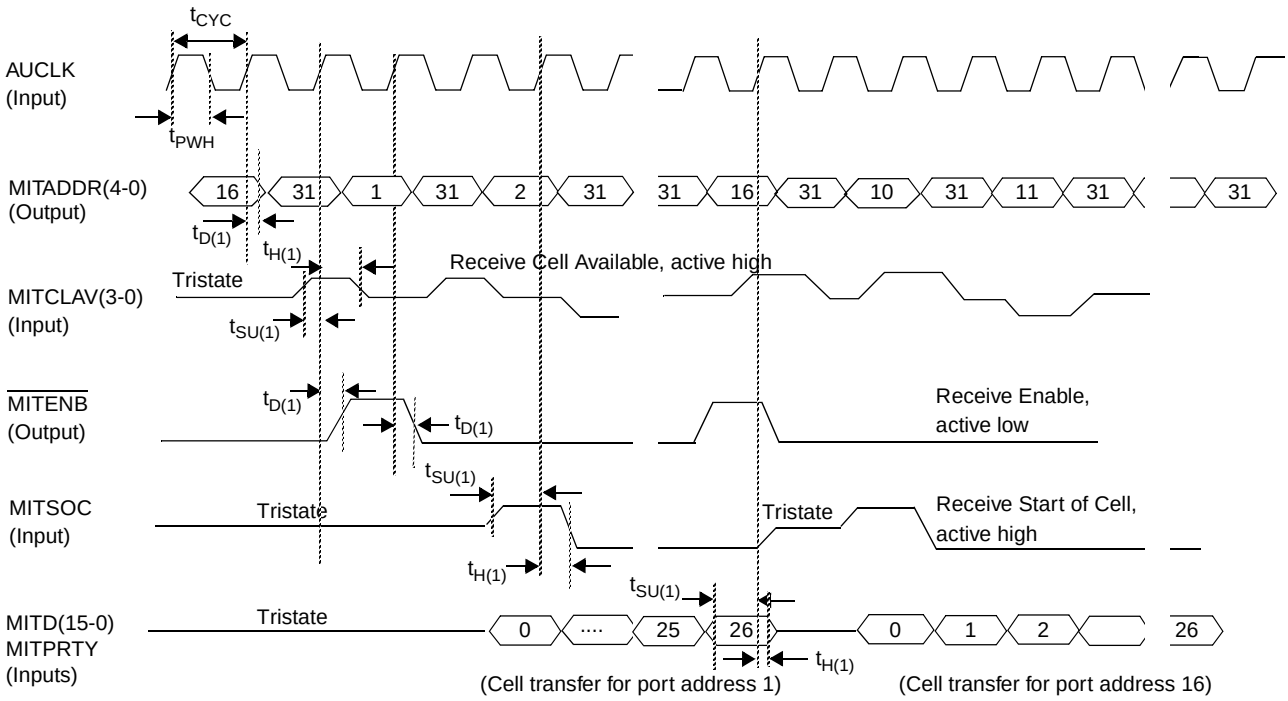
Parameter	Symbol	Min	Typ	Max	Unit
ADCLK clock cycle time	t_{CYC}	40			ns
ADCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
METCLAV setup time to ADCLK↑	$t_{SU(1)}$	7.5			ns
METCLAV hold time after ADCLK↑	$t_{H(1)}$	1.0			ns
METD(15-0), METPRTY delay from ADCLK↑	$t_{D(1)}$	2.0		14	ns
METSOC, METADDR(4-0), $\overline{\text{METENB}}$(3-0) delay from ADCLK↑	$t_{D(2)}$	2.0		14	ns

Figure 11. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 8-bit)



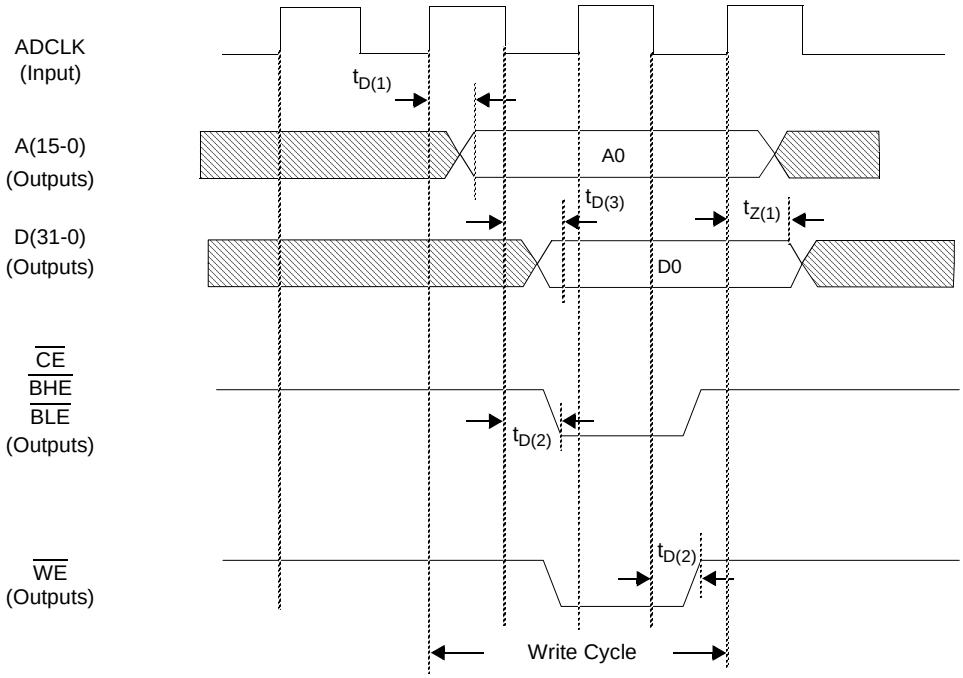
Parameter	Symbol	Min	Typ	Max	Unit
AUCLK clock cycle time	t_{CYC}	40			ns
AUCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
MITD(7-0), MITPRTY, MITSOC, MITCLAV setup time to AUCLK↑	$t_{SU(1)}$	7.5			ns
MITD(7-0), MITPRTY, MITSOC, MITCLAV hold time after AUCLK↑	$t_{H(1)}$	1.0			ns
MITADDR(4-0), $\overline{\text{MITENB}}$ delay from AUCLK↑	$t_{D(1)}$	2.0		14	ns

Figure 12. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 16-bit)



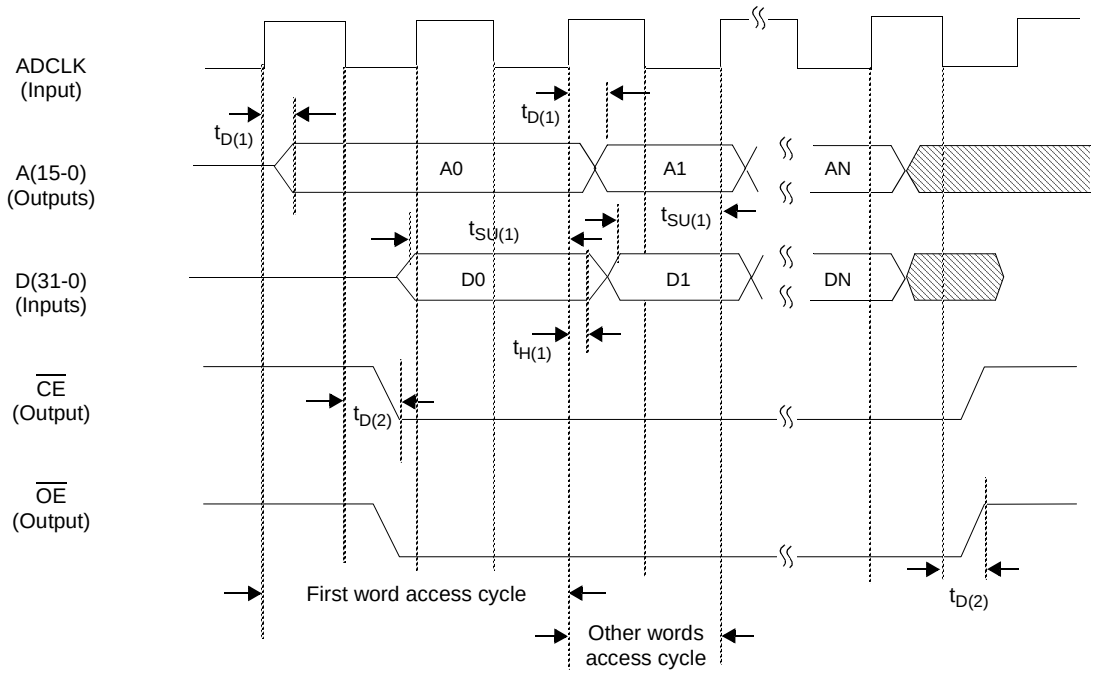
Parameter	Symbol	Min	Typ	Max	Unit
AUCLK clock cycle time	t_{CYC}	40			ns
AUCLK duty cycle, t_{PWH}/t_{CYC}		40		60	%
MITD(15-0), MITPRTY, MITSOC, MITCLAV setup time to AUCLK↑	$t_{SU(1)}$	7.5			ns
MITD(15-0), MITPRTY, MITSOC, MITCLAV hold time after AUCLK↑	$t_{H(1)}$	1.0			ns
MITADDR(4-0), $\overline{\text{MITENB}}$ delay from AUCLK↑	$t_{D(1)}$	2.0		14	ns

Figure 13. External Asynchronous SRAM - Write Timing



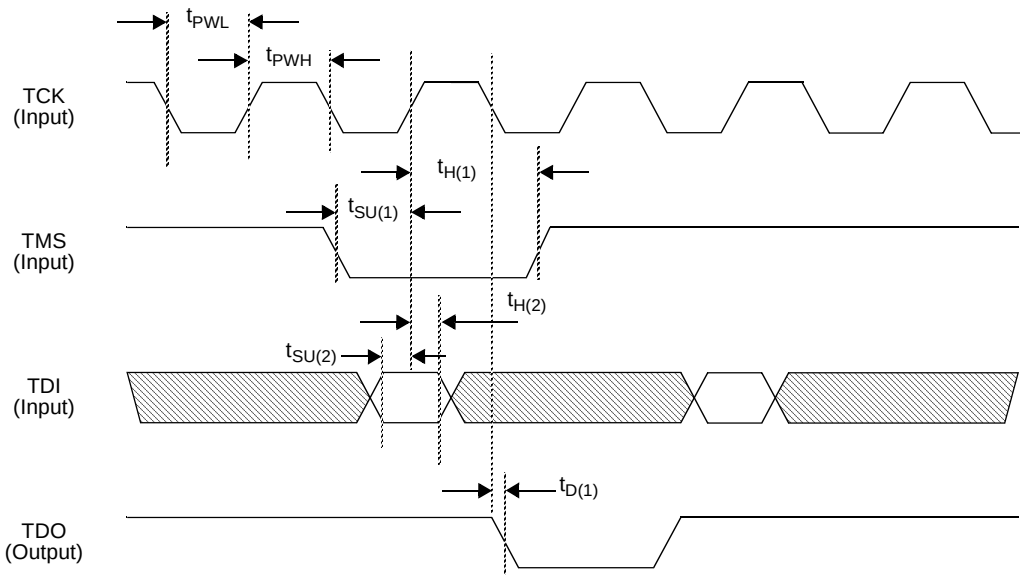
Parameter	Symbol	Min	Typ	Max	Unit
A(15-0) delay after ADCLK↑	$t_{D(1)}$	2.0		14.5	ns
$\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$, $\overline{WE}$ delay after ADCLK↓	$t_{D(2)}$	2.0		14.5	ns
D(31-0) delay from Tristate after ADCLK↓	$t_{D(3)}$	2.0		14.5	ns
D(31-0) delay to Tristate after ADCLK↑	$t_{Z(1)}$	2.0		14.5	ns

Figure 14. External Asynchronous SRAM - Read Timing



Parameter	Symbol	Min	Typ	Max	Unit
A(15-0) delay after ADCLK↑	$t_{D(1)}$	2.0		14.5	ns
$\overline{CE}$, $\overline{OE}$ delay after ADCLK↓	$t_{D(2)}$	2.0		14.5	ns
D(31-0) setup time before ADCLK↑	$t_{SU(1)}$	7.5			ns
D(31-0) hold time after ADCLK↑	$t_{H(1)}$	1.0			ns

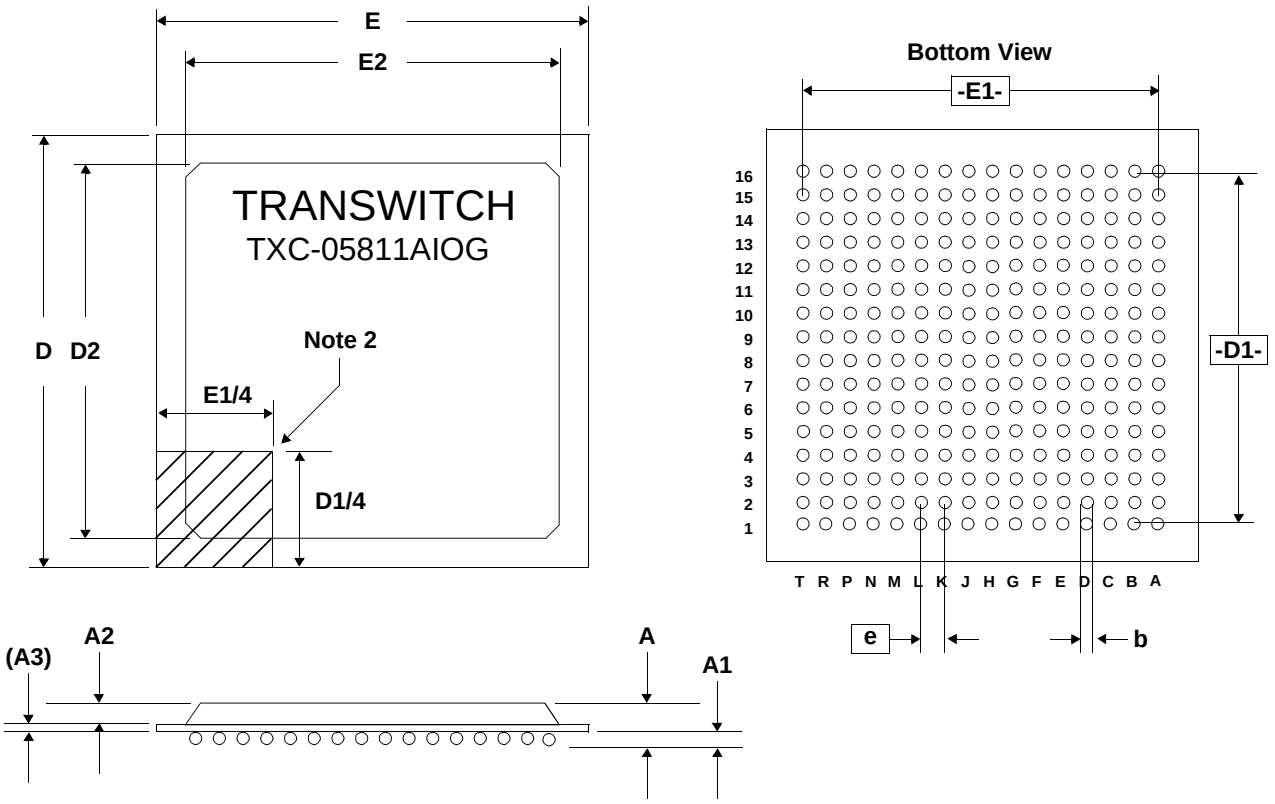
Figure 15. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock frequency	-	-	10	MHz
TCK clock high time	t_{PWH}	40	60	ns
TCK clock low time	t_{PWL}	40	60	ns
TMS setup time before TCK↑	$t_{SU(1)}$	7.5	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	7.5	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	7.5	-	ns
TDO delay from TCK↓	$t_{D(1)}$	-	16	ns

PACKAGE INFORMATION

The ASPEN-PX device is available in a 256-lead plastic ball grid array (PBGA) suitable for surface mounting, as shown in Figure 16.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 16 x 16, JEDEC code MO-151-AAF-1

Dimension (Note 1)	Min	Max
A	1.50	2.00
A1	0.30	0.50
A2	0.70	0.90
A3 (Ref.)	0.56	
b	0.40	0.60
D	17.00	
D1 (BSC)	15.00	
D2	15.00	15.70
E	17.00	
E1 (BSC)	15.00	
E2	15.00	15.70
e (BSC)	1.00	

Figure 16. ASPEN-PX TXC-05811 256-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-05811AIOG 256-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

TXC-05810B, ASPEN Device (*CellBus* Access Processor). The ASPEN is a revolutionary, RISC-based processor designed to support the requirements of next generation multi-service access systems. ASPEN supports *CellBus* operation in both Cell and Packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation or alternatively, to provide greater system throughput. Line interface is via UTOPIA 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables is stored in an external synchronous SRAM.

TXC-05806, ASPEN Express Device (Multi-PHY *CellBus* Access Switch). The ASPEN Express is a single-chip solution for implementing cost-effective ATM multiplexing and switching systems, based on the *CellBus* architecture. The ASPEN Express provides enhanced traffic management to the *CellBus* family of ATM switching devices, including OAM Fault Management, Policing, and EPD/PPD. ASPEN Express supports unicast and multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing, policing, and inlet/outlet cell queuing. The ASPEN Express offers dual *CellBus* interfaces to support load sharing or redundancy and utilizes SDRAM memory greatly reducing the total board cost.

TXC-06203, PHAST-3P Device (STM-1/STS-3c SDH/SONET Overhead Terminator). The PHAST-3P is an STM-1/STS-3c section, line and path overhead termination device that performs ATM and PPP PHY-layer processing. It provides either a SDH/SONET pseudo-ECL bit-serial interface or a byte-wide parallel interface on the line side. The serial interface provides 155 MHz clock recovery and clock synthesis. The terminal interface is UTOPIA level 2 for ATM cells or level 2P for packets.

TXC-06212, PHAST-12E Device (Programmable, High-Performance ATM/PPP/TDM/SONET/SDH Overhead Terminator). The PHAST-12E is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12E device can terminate four individual STS-3c or STM-1 lines or a single STS-12/12c or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s signals or single 622.08 Mbit/s serial operation.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118

Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England

Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112

Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France

Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

JEDEC (International):

Joint Electron Device Engineering Council
2500 Wilson Boulevard
Arlington, VA 22201-3834

Tel: (703) 907-7559
Fax: (703) 907-7583
Web: www.jedec.org

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated ASPEN-PX Data Sheet that have significant differences relative to the previous and now superseded ASPEN-PX Data Sheet:

Updated ASPEN-PX device Data Sheet: *PRELIMINARY* Edition 6, August 2003

Previous ASPEN-PX device Data Sheet: *PRELIMINARY* Edition 5, April 2002

The page numbers indicated below of this updated Data Sheet include changes relative to the previous Data Sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
1	Changed Features section. Changed Description section.
3	Changed diagram of Figure 1.
4 - 21	Changed Block Diagram Description, ASPEN-PX Configuration/Status, System Overview, ASPEN-PX (TXC-05811)/ASPEN (TXC-05810B) Communication, ASPEN Driver API Functions (Host) and ASPEN-PX Messages sections.
26	Changed Name/Function for Symbol $\overline{\text{HIGHZ}}$.
40	Changed Related Products section.
41	Changed Standards Documentation Sources section.
43	Updated List of Data Sheet Changes section.

- NOTES -

- NOTES -

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