# ASPEN® Device
## *CellBus*® Access Processor
## TXC-05810B

**DATA SHEET**

## FEATURES

- 155 Mbit/s bidirectional throughput
- RISC-based hardware architecture
- Dual independent *CellBus* interfaces for increased bandwidth or redundancy
- UTOPIA Level 2P interface for cell and packet transport
- 64-bit synchronous SRAM port for data storage
- Utilizes ASPEN ATM AccessEDGE™ firmware for design and field upgrades
- Cell insertion/extraction through host interface
- Message-based interface for host-ASPEN communication
- Interoperable with ASPEN-PX (TXC-05811) enabling ASPEN to address up to 64 UTOPIA Level 2 ports
- TranSwitch *CellBus*® switch fabric compliant, interoperable with CUBIT® family and ASPEN® family of *CellBus* products
- +3.3 V and +2.5 V power supplies
- Test Access Port for IEEE 1149.1 boundary scan
- 503-lead Plastic Ball Grid Array (PBGA) package, 40 mm x 40 mm

## DESCRIPTION

The ASPEN device (TXC-05810B) is a revolutionary, RISC-based processor designed to support the requirements of next generation multi-service access systems.

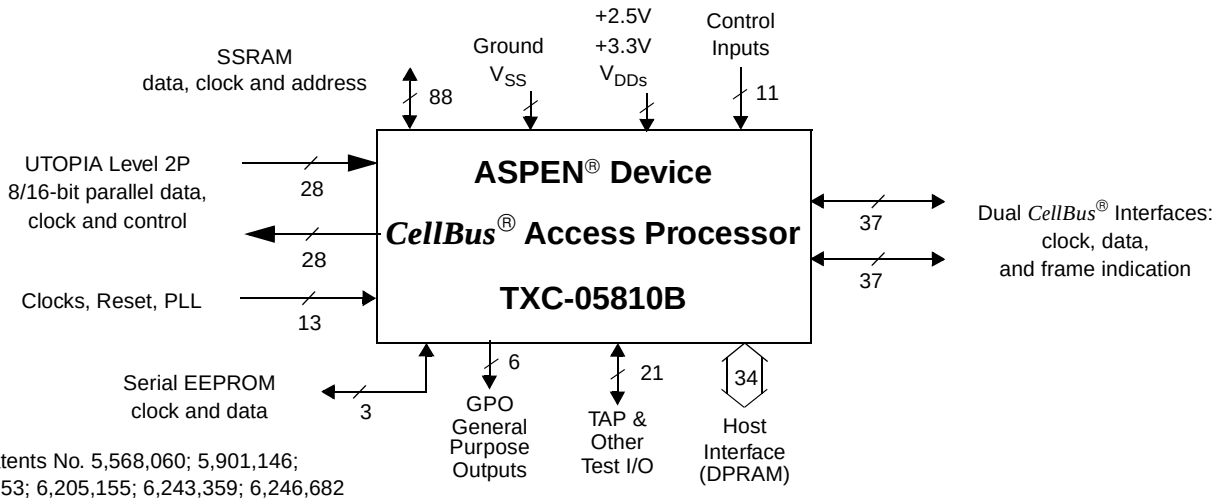
The ASPEN supports *CellBus*® operation in both cell and packet modes via two independent *CellBus* ports. The ASPEN and *CellBus* may be configured to support redundant system operation or, alternatively, to provide greater system throughput. Line interface is via UTOPIA Level 2 for ATM cells or Level 2P for variable length packets. Buffering of data traffic and control information, such as connection tables, is stored in an external synchronous SRAM. Communication to a local host, is message based and via an external Dual Port RAM.

The flexible nature of the ASPEN device architecture supports a variety of cell, packet, and cell/packet interworking modes. The ASPEN device's mode of operation is determined by firmware downloaded into the device instruction memory.

Contact TranSwitch for details of UTOPIA Level 2P interface specifications and information on available operational firmware.

## APPLICATIONS

- ATM Access Multiplexers
- DSLAM Applications
- Multi-Service Access Multiplexers
- ATM LAN Switch
- VoIP/VoATM Voice Gateways
- Frame Relay Switch



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# TABLE OF CONTENTS



*Note: For ease of reading, references to the *CellBus*® switch fabric or a *CellBus*® bus may be abbreviated to *CellBus* throughout this document.

## TABLE OF CONTENTS (cont.)



## LIST OF FIGURES

## LIST OF FIGURES (cont.)

## BLOCK DIAGRAM

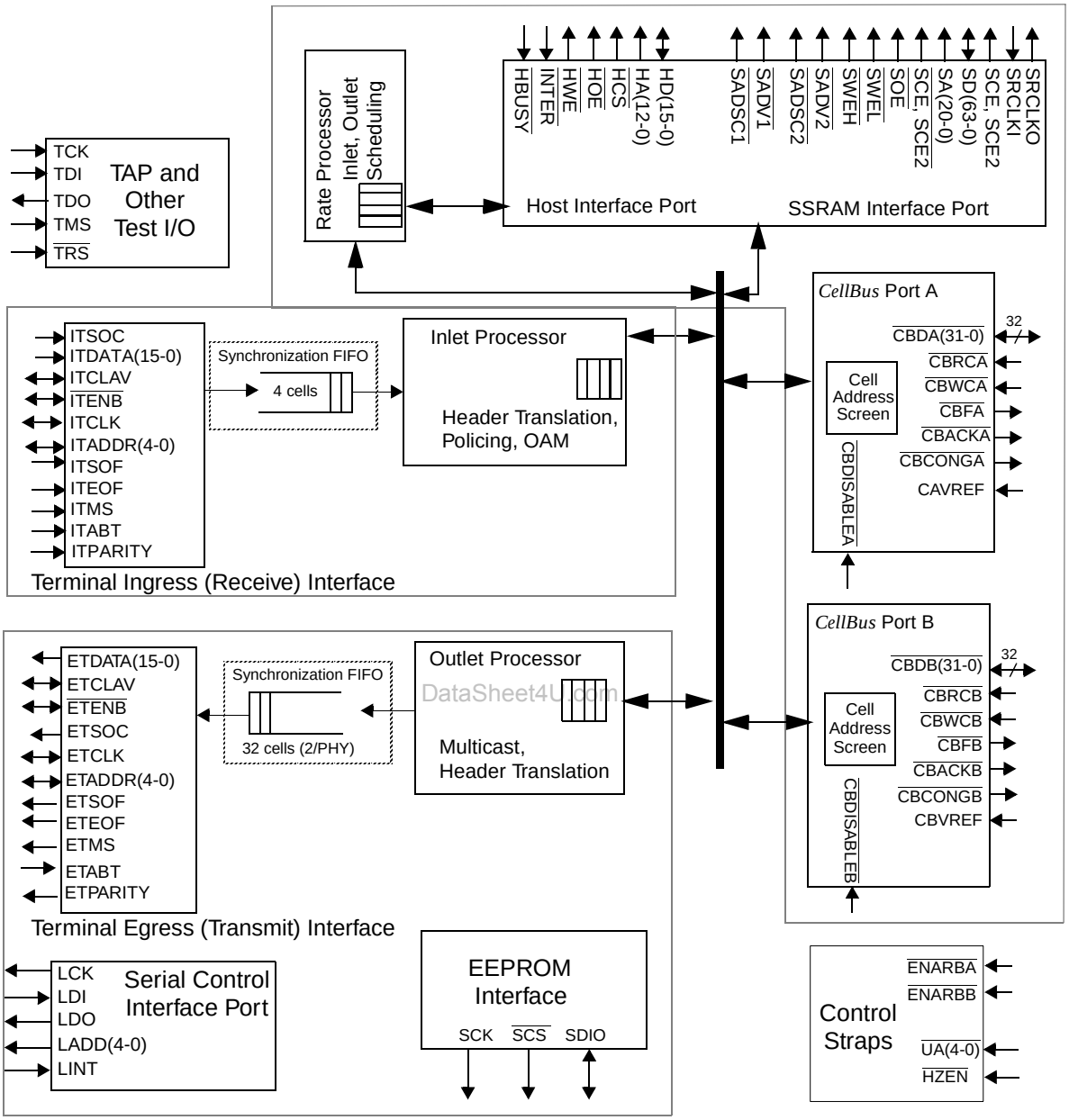



**Figure 1. ASPEN Device (TXC-05810B) Block Diagram**

## BLOCK DIAGRAM DESCRIPTION

A simplified block diagram of the ASPEN device is shown in Figure 1. Device functionality is defined by operational firmware running on the three internal RISC processors (Inlet, Outlet, and Rate - IP, OP and RP). This firmware is downloaded into the processor's instruction RAM via a Dual Port RAM (DPRAM) connected to the Host Interface Port.

Supplemental information on the operation, control and configuration of the ASPEN device is provided in a separate User's Guide specific to each operational firmware load. Contact TranSwitch for further details.

## THE *CELLBUS* INTERFACE

### *CellBus* Operation

The ASPEN device is a versatile CMOS VLSI device for implementing ATM switching and traffic management functions. Various ATM cell switching or multiplexing structures can be formed by interconnection of a number of ASPEN devices over each of two 37-line parallel buses with 32 data bits, the *CellBus*. Since the interconnect structure is a bus, communications between any of the devices on the bus is possible. Each cell placed onto either *CellBus* by an ASPEN device can be routed either to one single *CellBus* device port (unicast addressing), or to multiple *CellBus* device ports (multicast or broadcast addressing). Depending upon the needs of an application, up to 32 *CellBus* devices may be interconnected on either *CellBus*. When using the ASPEN device (TXC-05810B), the maximum bus clock frequency is 40 MHz and the raw bandwidth of each *CellBus* exceeds 1.25 Gbit/s.

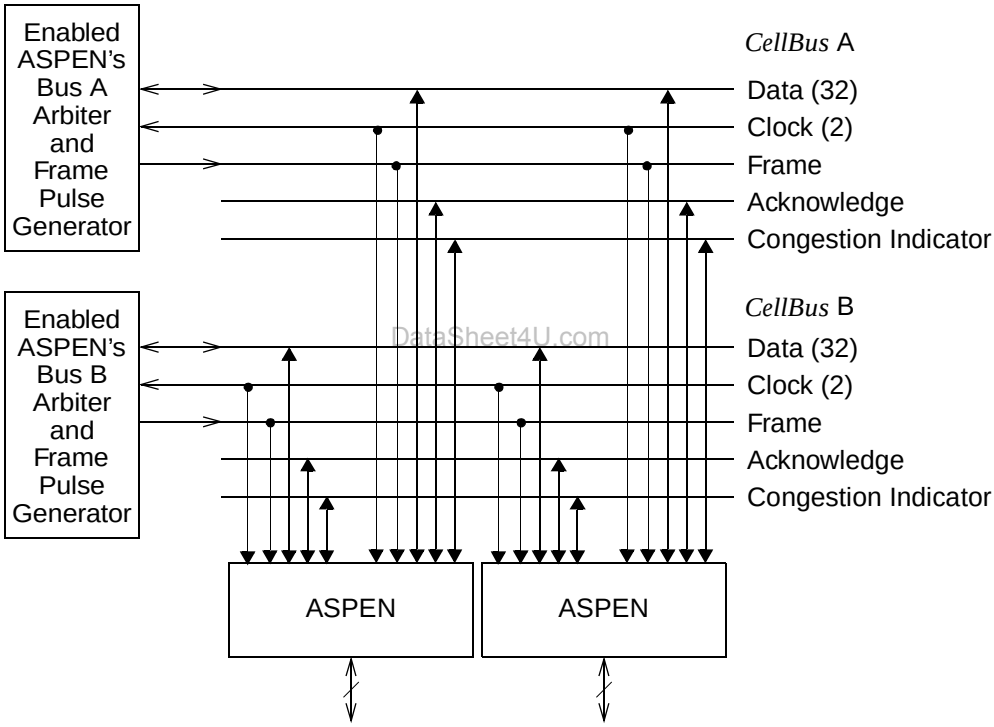



**Figure 2. *CellBus* Interconnection Diagram**

*CellBus*, shown in Figure 2, is a shared bus, and can be implemented either on a single circuit card, or in a backplane configuration among multiple circuit cards. Since multiple ASPEN devices share the same bus, bus access contention must be resolved. This access contention is resolved by use of a central arbitration function. ASPEN devices will request bus access, and the central Bus Arbiter will grant access back, in response. The circuitry for this Bus Arbiter is included inside the ASPEN device, with separate circuits for each of the two buses. Any one ASPEN device on a given bus in a system may be selected to perform the bus arbitration function. The selected ASPEN device will also generate the frame pulse for the arbitrated bus.

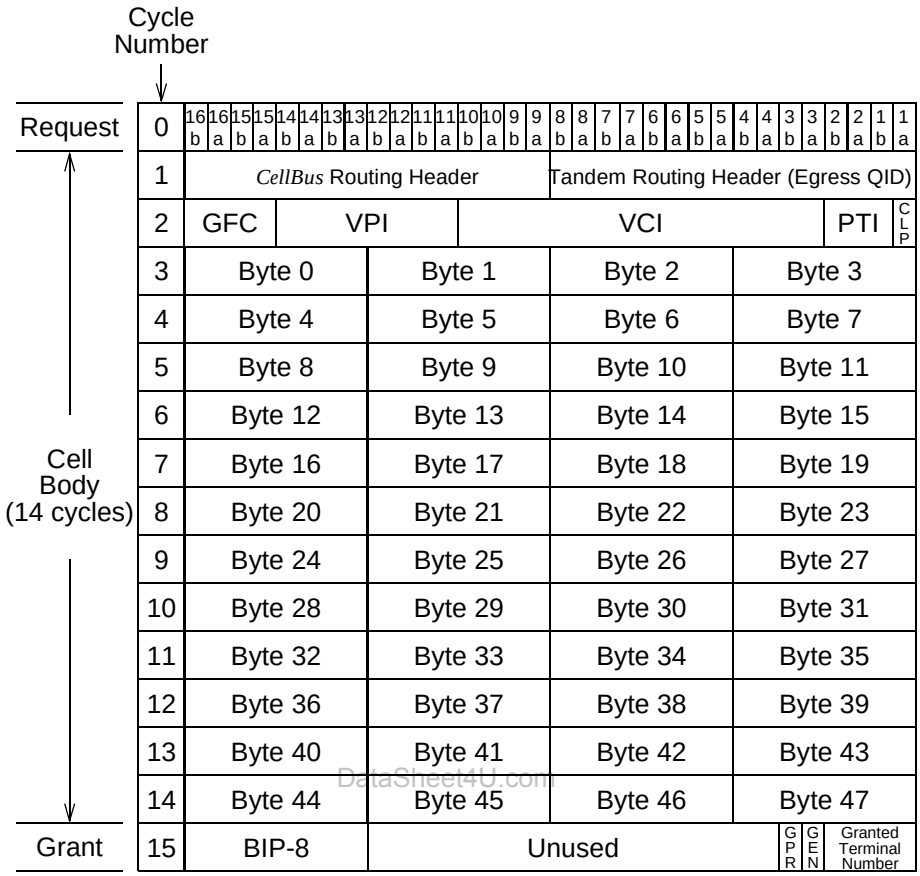



**Figure 3. *CellBus* Frame Format**

*CellBus* has a framed format 16 clock cycles long and 32 bits wide, which is illustrated in Figure 3. The first cycle of each frame is the Request cycle (Cycle 0), during which those ASPEN devices which have a cell to send to the bus each make an access request by asserting one or two assigned bits on the bus. The device address assigned to each ASPEN device by control straps bits $\overline{UA(4\text{-}0)}$ and mirrored by control bits UA(4-0) uniquely specifies which two bits it may assert during the bus Request cycle time. By asserting one of its assigned bits, or the other, or both, access requests of three different priorities may be made. A central Bus Arbiter accepts these access requests, executes an arbitration algorithm, and issues a bus access grant during the final cycle of the frame, the Grant cycle (Cycle 15). Each grant issued by the arbiter is for one ASPEN device to send one cell to the bus. Whichever ASPEN device is issued a grant during one cell will transmit its cell during the 14 Cell Body clock cycles of the next bus frame, and will also drive an 8-bit cell parity check during the Grant cycle of the same bus frame. Each cell sent can be of unicast, multicast, or broadcast type. ASPEN devices will accept single-address cells routed to an address defined by their address straps, all broadcast cells, and selected multicast cells. Thus, cells may be sent from any one ASPEN device to any one ASPEN device or to multiple ASPEN devices.

The ASPEN device can be operated in either 16-user or 32-user mode for each *CellBus* by setting the two control bits U16/$\overline{32}$A and U16/$\overline{32}$B in RP register 0/6/2. For the 16-user mode, each *CellBus* frame occurs between framing pulses, as shown on the left side of Figure 4. However, in 32-user mode, two frames occur between framing pulses, the first for even frames (users 0-15) and the second for odd frames (users 16-31), as shown on the right side of Figure 4. The request cycle in the even frame coincides with the frame pulse, whereas in

the odd frame the pulse is not present. In the even frame ASPEN devices 0-15 (lower 16 users) request access to the bus and in the odd frame ASPEN devices 16-31 (upper 16 users) request access to the bus. The full bus bandwidth is available to be shared among all the users of the bus in both 16-user and 32-user modes.

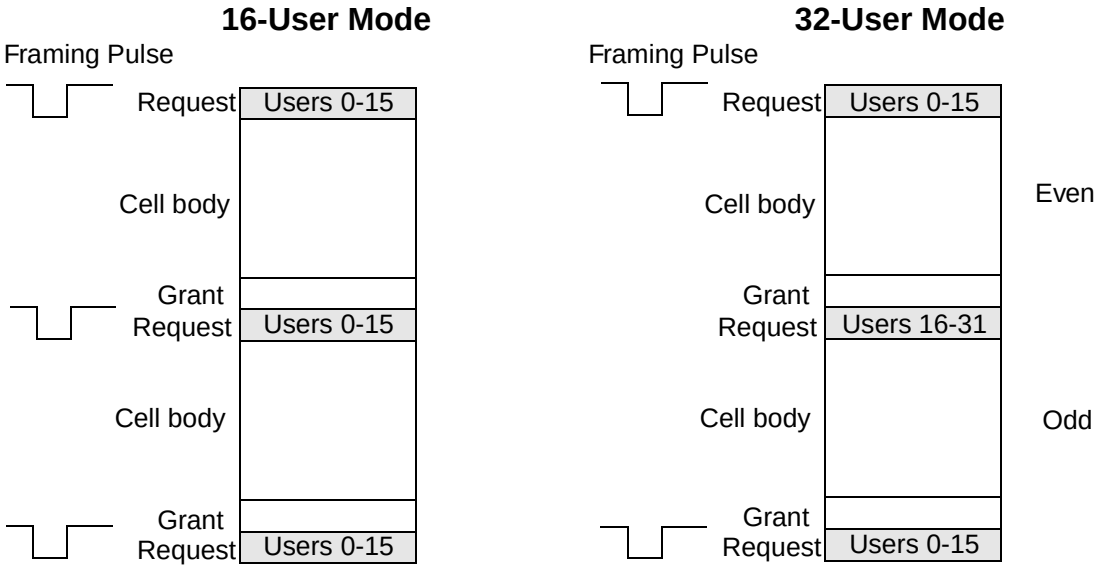



**Figure 4. *CellBus* 16/32-User Frame Format**



To detect *CellBus* errors, a BIP-8 (Bit Interleave Parity byte) is calculated over the 54-byte data field that extends from the first Tandem Routing Header byte through the final payload data byte, Byte 47. The BIP-8 is generated by the transmitting ASPEN device using the following algorithm. The first byte of the Tandem Routing Header is exclusive-or gated with an all-ones byte, creating a starting seed value. This seed value is then exclusive-or gated with the second byte of the Tandem Routing Header. The result is then exclusive-or gated with the next byte in the cell. This process is repeated with every successive byte in the cell, through Byte 47 of the payload, and the final result is transmitted as the BIP-8 byte in cycle 15. The receiving ASPEN device performs the same process and compares the generated BIP-8 with the received BIP-8. If no errors are detected the receiving ASPEN device pulls $\overline{\text{CBACKA}}$ or $\overline{\text{CBACKB}}$ low, acknowledging receipt of a cell. All ASPEN devices calculate the BIP-8 value for each cell transferred across the *CellBus*, allowing every device to detect and report a BIP-8 error. The *CellBus* Routing Header has its own CRC-4 field and is not included in the BIP-8 calculation.

The only signals required to operate each bus that are not sourced by an ASPEN device are two transfer clocks per *CellBus*: write clocks ($\overline{\text{CBWCA}}$, $\overline{\text{CBWCB}}$), and read clocks ($\overline{\text{CBRCA}}$, $\overline{\text{CBRCB}}$). These clock signals are of the same frequency, but may be slightly phase-offset to allow for reliable bus operation. The framing pulse used to define the bus frame cycle is sent out by one of the ASPEN devices, and the arbitration function is also performed by the same ASPEN device. Each ASPEN device contains the circuitry for both the Bus Arbiter and the Frame Pulse Generator. Only one ASPEN device per *CellBus* will have this circuitry enabled, by setting the $\overline{\text{ENARBA}}$/$\overline{\text{ENARBB}}$ leads on the device to the active low level.

### *CellBus* Cell Routing

The *CellBus* architecture allows several types of cell routing:

Point-to-Point Routing: In Unicast or Single Address cell routing a cell coming into an input port is transferred to a single output port. The ASPEN device can address a cell to itself, effectively implementing both the input and output ports.

Point-to-Multipoint (Broadcast): A cell coming into the input port is routed to all the output ports (ASPEN devices) in the *CellBus*.

Point-to-Multipoint (Multicast): In multicast routing the cell arriving at the input port is sent to the subset of output ports that belong to the specific multicast session.

For each of the routing methods the cells can be sent to different output queues according to a queue index stored in the 18-bit extended tandem routing header. The encoding rules for the two-byte *CellBus* Routing Header in Bits 31-16 of Cycle 1 are summarized in Figure 5 below:

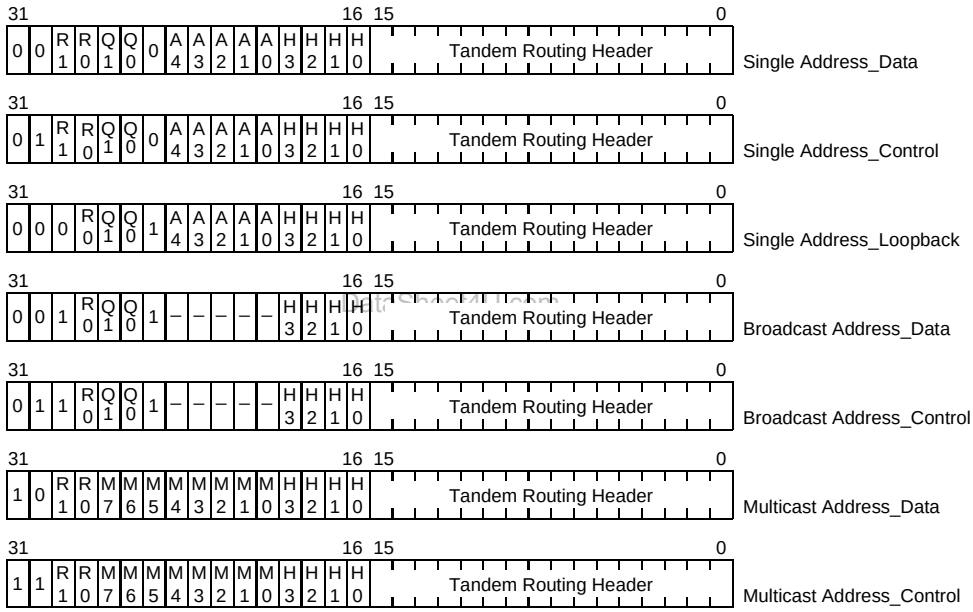



**Figure 5. *CellBus* Routing Header Formats**

*CellBus* Routing Header Format

The *CellBus* Routing Header contains the following fields:

**R**: Multicast Extension field (2 bits). This field was unused by the CUBIT and CUBIT-*Pro.* The following are the 7 *CellBus* addressing modes and the **R** bit usage for each mode.

**SAD:** In Single Address Data: R1, R0 is used to indicate class type. This information is used to index per class counters.

**BAD:** In Broadcast Address Data: R0 is used to indicate class type. This information is used to index per class counters.

**MAD:** In Multicast Address Data: R0 is used to indicate class type. This information is used to index per class counters. Usage of multicast is restricted to CBR or VBR-rt queues to allow proper monitoring of the multicast cell buffer utilization within a service category. R1 is used to indicate the location of the queue index for multicast. R1 = 0 for QID in the M field or R1 = 1 for QID in the extended Tandem Routing Header (TRH), as described below.

**SAC:** In Single Address Control: R1, R0 are used to indicate class type. This information is used to index per class counters.

**SAL:** In Single Address Loopback: R0 is used to indicate class type. This information is used to index per class counters.

**BAC:** In Broadcast Address Control: R0 is used to indicate class type. This information is used to index per class counters.

**MAC:** In Multicast Address Control: R0 is used to indicate class type. This information is used to index per class counters. Usage of multicast is restricted to CBR or VBR-rt queues to allow proper monitoring of the multicast cell buffer utilization within a service category. R1 is used to indicate the location of the queue index for multicast. R1 = 0 for QID in the M field or R1 = 1 for QID in the extended Tandem Routing Header (TRH), as described below.

**Q**: Queue selection field (2 bits). This field is used by the ASPEN device to extend the TRH from 16 to 18 bits, TRH(17-0). Q0 is TRH16 and Q1 is TRH17 in the Single Address Data and Control formats and in the Broadcast Address Data and Control formats.

**A**: ASPEN device single address field (5 bits, for 32 addresses). A0 is the LSB.

**M**: Multicast number field (8 bits for 256 multicast sessions). M0 is the LSB.

**H**: CRC-4 field. This field is generated and terminated by the ASPEN device. It is used for error protection across the *CellBus*. The calculation of the CRC-4 field (H3-H0) over the 12-bit word (X11-X0) in bits 31-20 of the routing header is calculated using the following logic:

$$H3 = \overline{(X7 \oplus X9 \oplus X3 \oplus X10 \oplus X8 \oplus X5 \oplus X2)}$$

$$H2 = (X6 \oplus X8 \oplus X2 \oplus X9 \oplus X7 \oplus X4 \oplus X1)$$

$$H1 = \overline{(X5 \oplus X7 \oplus X1 \oplus X8 \oplus X6 \oplus X3 \oplus X0)}$$

$$H0 = (X8 \oplus X10 \oplus X4 \oplus X11 \oplus X9 \oplus X6 \oplus X3 \oplus X0)$$

where $\oplus$ represents logical exclusive-or. The CRC-4 calculated by the ASPEN device can be inverted to purposely force an incorrect value for testing by setting CRC4I = 1. Each ASPEN will verify the correct CRC-4 on all *CellBus* cells regardless of the destination of the transfer. This allows every ASPEN to detect and report a CRC-4 error in the CBRH. The ASPEN device will calculate the correct CRC-4 on all outgoing cells toward the *CellBus*.

Tandem Routing Header Format

The two-byte Tandem Routing Header (TRH) format in Bits 15-0 of Cycle 1 is used in the ASPEN device in conjunction with the Q field to direct the *CellBus* frame to the proper outlet-side queue. Bits 3-0 contain an optional CRC-4 field to protect the upper 12 bits of the TRH. The CRC-4 is calculated using the same mechanism as specified above in the H field of the *CellBus* Routing Header. All ASPEN devices will verify the correct CRC-4 on all *CellBus* cells regardless of the destination of the transfer. This allows every ASPEN to detect and report a CRC-4 error in the TRH. When the optional CRC-4 generation is not used over the TRH field, these four bits are used to indicate the end of a packet for packet-based traffic as noted below.

**Bit 3:** EP: Used to indicate the end of packet cell.

**Bit 2-0:** Reserved

| TRH Format | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cell | Tandem Routing Header | | | | | | | | | | | | CRC-4 | | | |
| Packet | Tandem Routing Header | | | | | | | | | | | | EP | Reserved | | |

**Figure 6. Tandem Routing Header Format**

### *CellBus* Status Signals and Monitoring

The ASPEN device provides the capability to monitor the activity in the *CellBus*. The essential signals that determine whether the bus is active (in the absence of any cell traffic) are the clock signals and the frame pulse.

The *CellBus* clocks (read and write) are generated externally to the ASPEN device and in the event that these clocks fail, the entire bus will cease any operation. The ASPEN device provides the capability to detect the absence of a clock signal within 32 processor clock cycles. The failure detection is performed independently for each *CellBus* Read Clock ($\overline{\text{CBRCA}}$, $\overline{\text{CBRCB}}$) and *CellBus* Write Clock ($\overline{\text{CBWCA}}$, $\overline{\text{CBWCB}}$).

The ASPEN device will detect and report loss of *CellBus* read and write clocks on both *CellBus* buses (CBLORCA, CBLORCB, CBLOWCA and CBLOWCB), as well as detection of loss of frame. The detection mechanism looks for two consecutive missing *CellBus* frame pulses in 32-user mode (i.e., U16/$\overline{32}$A or U16/$\overline{32}$B = 0), and four consecutive missing *CellBus* frame pulses in 16-user mode (i.e., U16/$\overline{32}$A or U16/$\overline{32}$B = 1). The *CellBus* Read Clock must be present to detect Loss of Frame Pulse. If *CellBus* Read Clock is present and *CellBus* Write Clock is not, then both loss of *CellBus* write clock and loss of frame for that particular *CellBus* will be set. The ASPEN device will report these events via error messages to the host processor.



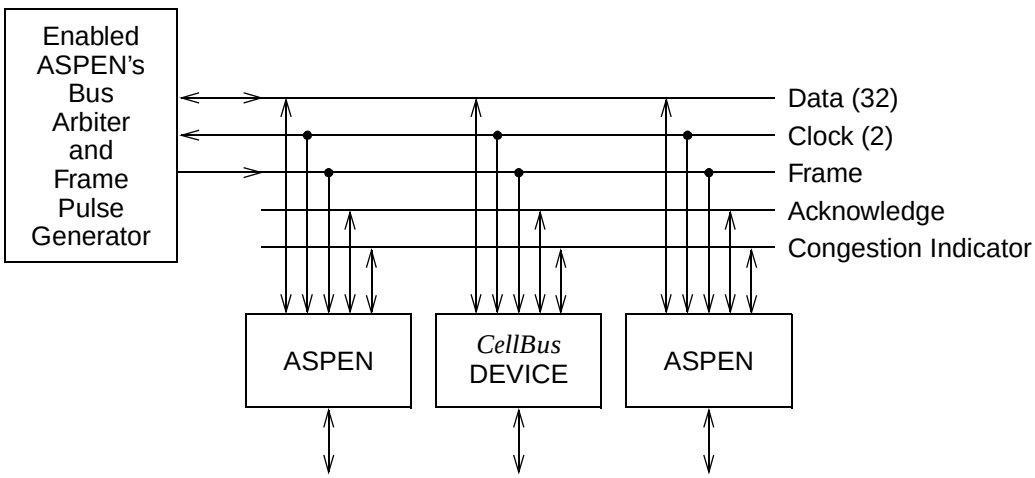



**Figure 7. *CellBus* Bus Structure**

Thirty-seven lines comprise the *CellBus* interface, as shown in Figure 7. There are thirty-two Data lines, with Frame, Acknowledge, and Congestion Indicator lines, all sourced by an ASPEN device, and two Clock lines sourced by external drivers.

### *CellBus* Bus Arbiter Selection

Two *CellBus* Bus Arbiters are included inside each ASPEN device, one arbiter for each independent *CellBus*. Enabling of the arbiter on a particular *CellBus* is done by connecting either of the $\overline{\text{ENARBA}}$, $\overline{\text{ENARBB}}$ leads of that device to ground ($V_{SS}$). Normally, one arbiter per *CellBus* is turned on and the remaining arbiters on that

bus are turned off. It is the responsibility of the overall system control to decide which ASPEN device will have its arbiter enabled, and to enable it. Failure of an arbiter can be detected by using the CBNACK interrupt with the NOGRT status indications. If multiple ASPEN devices are indicating NOGRT failures, an arbiter failure is indicated. It is again the responsibility of system control to enable another arbiter. Upon switching from one arbiter to another, the receiving devices on the bus will automatically re-align to the new frame position within one *CellBus* frame.

### *CellBus* Burst Reduction Algorithm

*CellBus* arbitration has been enhanced with the selectable Burst Arrest Arbitration feature. This feature allows the arbiter to make use of information from the Burst Monitor to determine how the *CellBus* should be allocated. Each *CellBus* Arbiter has its own independent monitoring function for both buses, A and B.

The Burst Monitor monitors the bursts into the two devices currently believed to be experiencing the most congestion, as viewed from a burst length point of view. The Monitor keeps two counters, CBBURSTLEN0 and CBBURSTLEN1. Each *CellBus* Routing Header which traverses the bus is examined. If the CBRH matches one of the identifiers stored in CBBURSTID0 or 1, the corresponding counter is incremented, and the other counter is decremented by 2 (saturating at 0).

If the CBRH does not match either of the two IDs being tracked, a determination needs to be made whether to start tracking it. This is done by checking to see if either of the two currently tracked IDs have a length of 2 or less, indicating a short burst, or a burst which ended a number of frames earlier. If CBBURSTLEN0, for instance, is less than or equal to 2, it will be tossed out after this frame anyway because it will be decremented to 0. The newcomer is then tracked as CBBURSTID0 with a CBBURSTLEN0 of 1.

The Arbiter uses the information in the Burst Monitor by inserting non-granted frames on IDs which have reached threshold levels. When an ID reaches the threshold level, from 0-7 non-granted frames may be inserted, as determined by the value of control bits BURST_BACKOFF(2-0).

### *CellBus* Congestion Indication

The *CellBus* signal format includes a congestion indication signal ($\overline{\text{CBCONGA}}$, $\overline{\text{CBCONGB}}$). This is an active low signal indicating that the current cell being transferred is headed toward a queue experiencing congestion. Status bits CONGm (m=0-255, determined by CONG(15-0) and CNRAMADDR(3-0) in memory map, 16 x 16 = 256 status indications) will be set to 1 indicating that queue m is in a congested state. When a cell arrives from the *CellBus* for queue m, the *CellBus* congestion indication returns the value of CONGm to the sending device. The upper 8 bits of the tandem routing header will be used as index m into the CONGm status bits.
**Note**: *CellBus* control cells designated for queues 0-3, which are the processors' internal queues, will not respond with a congestion indication when CONG0 is in a congested state.

### *CellBus* NACK Indication

The *CellBus* signal format includes an acknowledge indication signal ($\overline{\text{CBACKA}}$, $\overline{\text{CBACKB}}$). This is an active low signal indicating that the current cell being transferred was accepted. Internal status bits NACKm (m=0-255, determined by NACK(15-0) and CNRAMADDR(3-0) in memory map, 16 x 16 = 256 status indications) will be set to 1 indicating that queue m is in a congested state and cannot accept a cell. When a cell arrives from the *CellBus* for queue m, the *CellBus* acknowledge indication returns the value of NACKm to the sending device. The upper 8 bits of the extended tandem routing header will be used as index m into the NACKm status bits.
**Note**: *CellBus* control cells headed for queues 0-3 which are processors' internal queues will respond with an acknowledge when NACK0 is in a congested state.

### *CellBus* Electrical Interface

Operation with Internal GTL+ Transceivers

Gunning Transceiver Logic (GTL+) transceivers for *CellBus* Data, Frame, Acknowledge, and Congestion Indicator lines are contained internally in the ASPEN device, along with two clock line GTL+ receivers. Each of the drivers has a maximum current sink capability of 48 mA and is capable of driving a bus on a card or on a backplane directly. Each of the GTL lines is to be pulled up at each of its ends by a 50 ohm (± 5%) resistor (metal film or carbon composition) to a +1.5 V low-impedance supply. Each end of each line should have a filtering capacitor connected from the +1.5 V supply to ground, as shown in Figure 8 below.

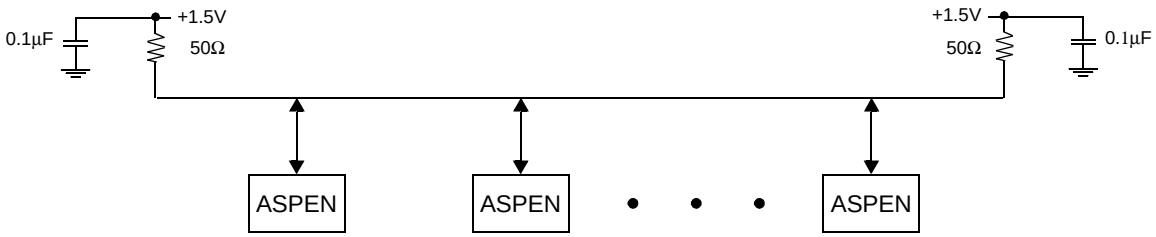



**Figure 8. External Circuit Requirements for GTL+ Transceivers**



In the ASPEN device lead configuration, all of the leads involved with each bus interface are aligned along one side of the package. This side of the package must be aligned toward the board connector, or toward the bus, with as little board trace length as possible between the leads and the connector or bus, to maximize operating speed.

Clock Source

Two GTL+ level clock signals must be driven to the *CellBus* from an external source. These are the write clock, $\overline{\text{CBWC}}$, and the read clock, $\overline{\text{CBRC}}$. A phase relationship keeping the write clock between 0.5 and 4 nanoseconds behind the read clock is needed to ensure proper synchronous bus operation. In any *CellBus* implementation, on the backplane and on each card, care must be taken to ensure that these two lines are routed together. The capacitive and inductive loadings of the two lines should be as nearly equal as possible, to maintain performance. At the drive point, a delay line should be used to maintain a stable delay, and the read and write clock drivers must be units of the same integrated circuit package. All of these precautions will ensure the most stable clocks and permit the highest possible operating speed.

### UTOPIA LEVEL 2P INTERFACE

**Note**: Use of this interface is restricted by application firmware. Contact the TranSwitch Applications Engineering department for additional information regarding the use of this interface.

The UTOPIA Level 2P ports provide for transport of both cells and frames between the physical and ATM layers. The ports are UTOPIA Level 1 and Level 2 compatible with an extension for frame transport. Both 8-bit and 16-bit configurations are supported.

The possible UTOPIA configurations in cell mode are shown in Figures 9, 10, 11 and 12.

Note: All physical layer devices must be initialized prior to configuring and enabling the UTOPIA interface on ASPEN, to ensure proper signaling startup.

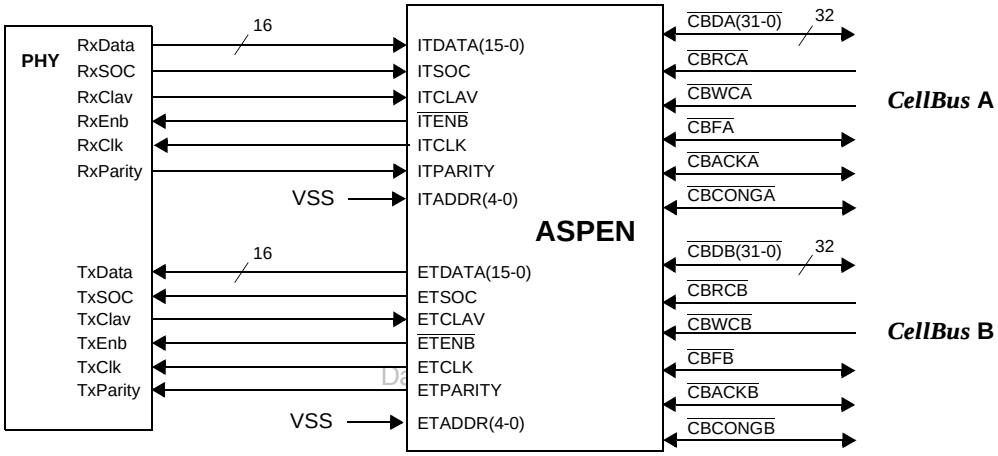



**Figure 9. ASPEN Device in ATM Layer, Single-PHY Mode Configuration**

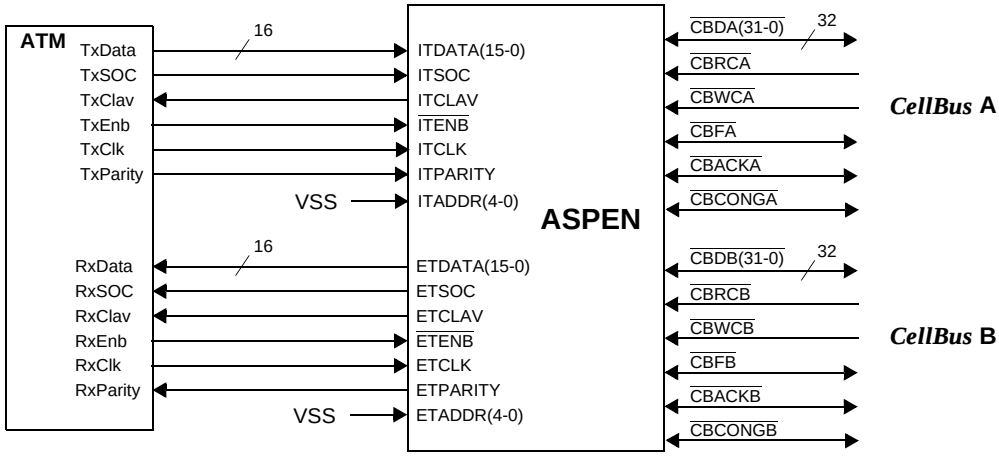



**Figure 10. ASPEN Device in PHY Layer, Single-PHY Mode Configuration**

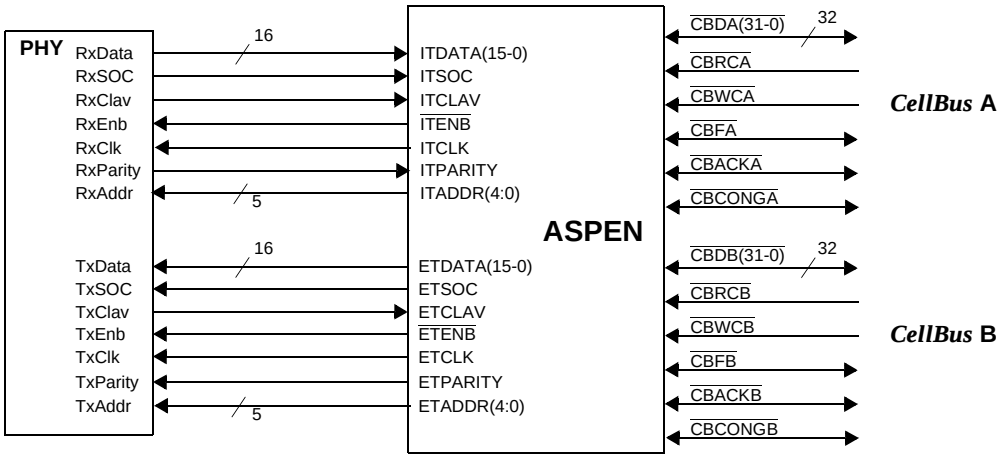



**Figure 11. ASPEN Device in ATM Layer, Multi-PHY Mode Configuration**

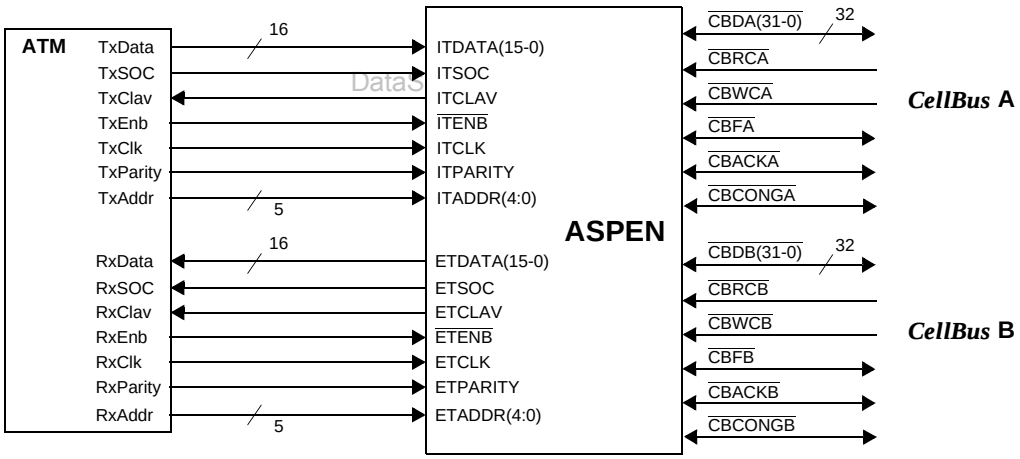



**Figure 12. ASPEN Device in PHY Layer, Multi-PHY Mode Configuration**

### Ingress UTOPIA Level 2P Interface

The Terminal Ingress port constitutes the main inlet interface for the cell traffic between the ASPEN device and other devices in either the upper ATM or Physical Layers. Several interfaces are supported by the device: UTOPIA (Level 1 and 2), and packet. The modes are selectable via control bit ITLMODE (IP register 0/6/1, bit 21). The encoding for the line mode is as follows.

0: UTOPIA Mode

1: Packet Mode

Control bit ITONLINE (IP register 0/6/1, bit 13), when set to one, enables the Ingress UTOPIA Level 2P Interface. If it is set to zero then no data will be accepted via the UTOPIA Level 2P interface.

Cell Mode

There is a 4-cell buffer at the Inlet UTOPIA interface for rate decoupling on the inlet and a 2 cell/port buffer at the outlet (for up to 16 ports). Typical signal connections for the ASPEN device when operating in UTOPIA mode are illustrated in Figures 9, 10, 11 and 12. The operating mode options for UTOPIA mode are selected by the control bits ITU1, ITPHYEN, ITCELLSIZE(3-0), UNI, IT16b, and ITPHYnADDR(4-0) in IP registers 0/6/1 to 0/6/5. The UTOPIA modes are described in more detail below. Differences between Single-PHY and Multi-PHY functions in a given mode, if any, are highlighted. In UTOPIA mode, ITPHYEN determines whether the ASPEN device emulates an ATM or PHY device. ITU1 determines either UTOPIA Level 1 or Level 2 support. ITCELLSIZE sets the cell inlet cell size. The inlet cell size can vary between 52 bytes and 64 bytes in 8-bit mode. The cell sizes supported in 16-bit mode are 27 - 32 words. The setting of UNI causes the upper nibble of the Cell header (GFC field) to be ignored for cell header lookup. In UTOPIA Level 2 mode, the ITADDR(3-0) field is used during header lookup instead of the GFC field. In UTOPIA Level 2 mode in ATM layer emulation, the ATM layer device is required to poll the various physical layer devices to determine the availability of cells which can be transferred. The polling mechanism implemented in the ASPEN device is round robin-based. The address of each enabled physical device is set by control bits ITE(15-0), and the UTOPIA addresses are set via control bits PHYnADDR(4-0). In Multi-PHY mode where ASPEN device is in PHY-layer emulation, PHY number 0 is used to carry the required information for controlling the interface, i.e. control bits ITPHY(0), ADDR(4-0) and IE0 are used to control the interface. Control bit IT16b enables the ASPEN device to receive 16-bit wide data.

The ingress UTOPIA interface keeps track of the byte count on the incoming cell stream. Cells that do not have the full byte count are discarded. Received long cells are transmitted with the extra bytes dropped. An ingress terminal parity error is detected by the inlet processor when the incoming parity bit ITPARITY does not match the odd parity calculated over the incoming data word. Reporting of this error condition is firmware dependent.



Packet Interface Mode



**Note**: Use of this interface is restricted by application firmware. Contact the TranSwitch Applications Engineering department for additional information regarding the use of this interface.

Packet mode is enabled by setting control bit ITLMODE to 1. The Terminal Ingress Frame interface mode reuses the standard UTOPIA interface leads in the manner described below. The packets are transferred across using the UTOPIA data leads. The byte arrangement is big-endian. Additional control information is passed across using four additional leads, ITSOF, ITEOF, ITMS, and ITABT. Framing information is transferred via the ITSOF for start of frame, ITSOC start of chunk, and ITEOF for end of frame. ITMS is used in 16-bit mode to indicate which byte contains the last byte of the packet. ITABT, if asserted, indicates that the current packet being transferred has invalid information, and should be dropped. In Multi-PHY mode, packets are transferred in either 16 or 48-byte frame chunks. UTOPIA Level 2 protocols for polling are followed. The flow control mechanism used is UTOPIA octet-level flow control for Single-PHY operation, and UTOPIA cell-level flow control for Multi-PHY operation where the chunk size is either 16 or 48 bytes.

The operating mode options for packet mode are selected by the control bits ITCHNK16, DMINF and ITPARDATA. ITCHNK16 sets the interface to accept packet chunk sizes of either 16-bytes (ITCHNK16 = 1) or 48-bytes (ITCHNK16 = 0). Received frames with length less than MINFL bytes may be discarded by setting control bit DMINF. The control bit ITPARDATA is used to select over which bits odd parity is calculated. When set to 1 odd parity is calculated over ITDATA only, when set to 0 odd parity is calculated over ITDATA, ITSOF, ITEOF, ITMS, ITABT and compared to ITPARITY.

In packet mode, the BRF and BMFL error conditions are reported on a per physical device basis. Bad Receive Frame (BRF) is signalled if the ITABT lead is asserted during a frame transfer, and the partially segmented packet is discarded. Below Minimum Frame Length (BMFL) is indicated when the number of bytes of an incoming packet is less than the minimum frame length specified by control bits MINFL(4-0).

Single-PHY Handshake

Data is transferred from the PHY emulation layer to the ATM emulation layer via the following procedure. The PHY emulation layer indicates it has valid data by asserting ITCLAV (in frame mode this signal indicates availability of a frame or frame chunk), then the ATM emulation layer asserts $\overline{\text{ITENB}}$ to indicate it wants to read the data. $\overline{\text{ITENB}}$ may be asserted or deasserted at any time.

The cycles during which $\overline{\text{ITENB}}$ are asserted is defined as a read window. During a read window, the PHY emulation layer reads data from its internal buffer and sends it out via ITDATA, ITSOF, ITSOC, and ITEOF on the rising edge of ITCLK. Asserting $\overline{\text{ITENB}}$ while ITCLAV is deasserted is allowed, but the data on ITDATA is undefined.

An example of Receive Single-PHY Handshake is shown in Figure 13.

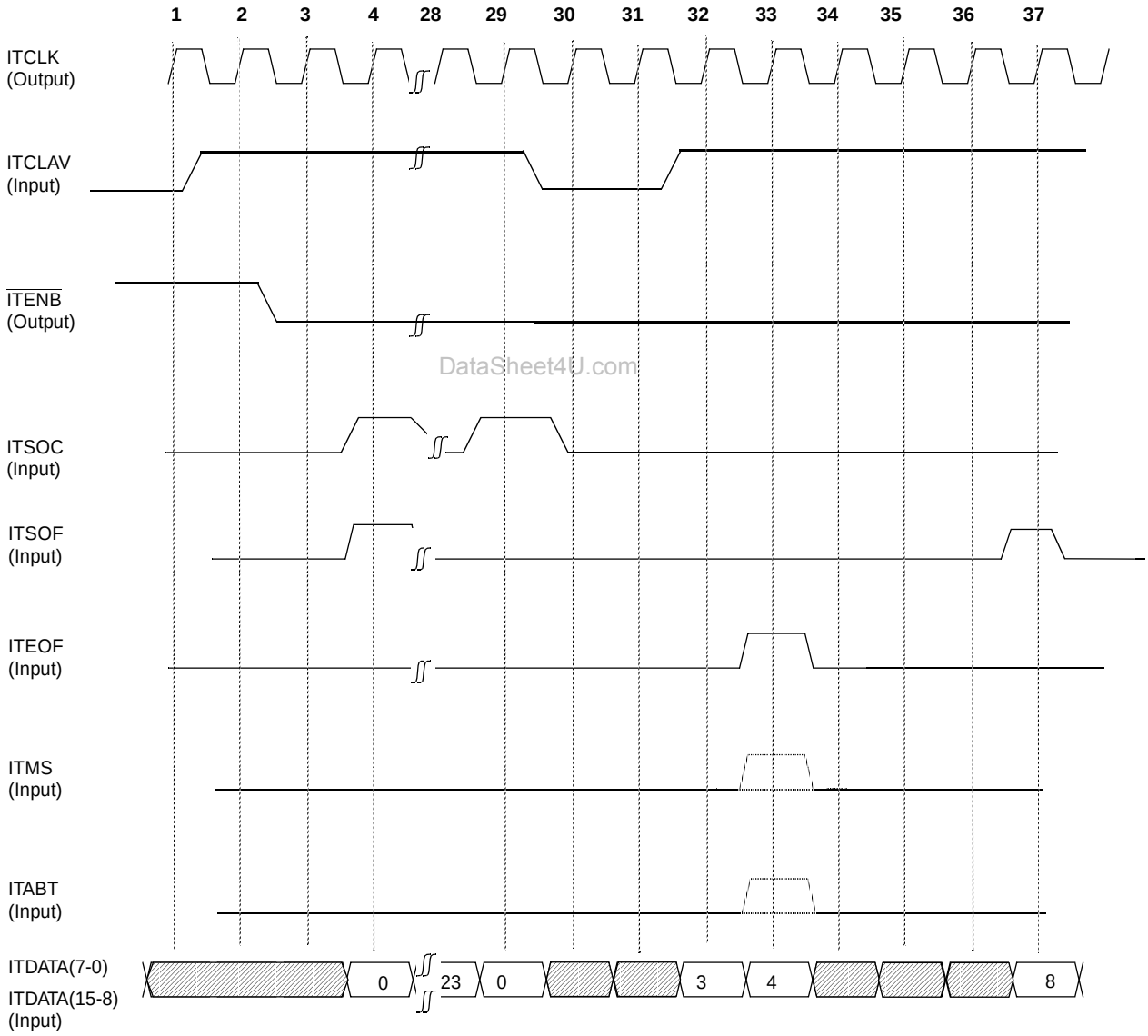



**Figure 13. Timing of Receive Frame Interface, Single-PHY (ASPEN Device in ATM Layer Emulation)**

Figure 13 shows the handshaking between the PHY and ATM emulation layers. At clock edge #2, the ATM emulation layer recognizes that the PHY emulation layer has data to send. The ATM emulation layer responds by asserting $\overline{\text{ITENB}}$. At clock edge #3, the PHY emulation layer detects the assertion of $\overline{\text{ITENB}}$, and responds by starting the transmission of the frame. At clock edge #29, the PHY emulation layer has run out of data to transmit, but is not yet at the end of a frame, so it deasserts ITCLAV until it has valid data to transmit. At clock edge #30, the ATM emulation layer detects the deassertion of ITCLAV, and invalidates the data received at clock edge #30. After clock edge #31, the PHY emulation layer again has data to transmit, so it reasserts ITCLAV. At clock edge #32, the ATM emulation layer detects the assertion of ITCLAV, and starts accepting data again. At clock edge #33, the ATM emulation layer detects ITEOF has been asserted, and the frame transfer is completed. If the transfer was over the 16-bit optional version of the interface, then the value of ITMS would have been sampled, to determine if the last byte of the packet fell on the upper or lower byte of the transfer.

Multi-PHY Handshake

In Single-PHY operation there is a point-to-point link between a PHY emulation device and an ATM layer emulation device. In Multi-PHY, transfer is from one selected PHY emulation layer (of Multiple-PHY emulation devices) to a single ATM emulation layer device. Out of band polling is used in the selection of the next PHY emulation layer device.

The ATM emulation layer device polls the PHY emulation layer by placing the address of a given device on ITADDR. The PHY emulation device responds by driving ITCLAV on the next clock cycle. The state of ITCLAV is based on the ability of the PHY emulation layer device to transfer a frame segment's worth of information, or an amount of data less than a frame segment which contains the last byte of the current frame, from the given PHY emulation layer device with the remainder of the chunk padded.

The selection of the PHY emulation layer is accomplished by placing the desired address onto ITADDR when $\overline{\text{ITENB}}$ is deasserted during the current cycle and reasserted during the next consecutive clock cycle. All Multi-PHY emulation layer devices only examine the value of ITADDR for selection purposes when $\overline{\text{ITENB}}$ is deasserted. The selected PHY emulation layer is selected from the cycle after its address is on the ITADDR leads and $\overline{\text{ITENB}}$ is deasserted until a new PHY emulation layer is selected per standard UTOPIA Level 2 protocol.

Once a PHY emulation layer is selected it must be able to transfer either an entire frame segment, or an amount of data less than a frame segment which contains the last byte of the current frame. If the latter, then the padding must be added to fill out the frame segment.

If the current frame chunk being transferred is aborted, it will maintain length integrity, and will pad the words after the abort signal is sent with arbitrary data.

An example of Receive Multi-PHY Handshake is shown in Figure 14.

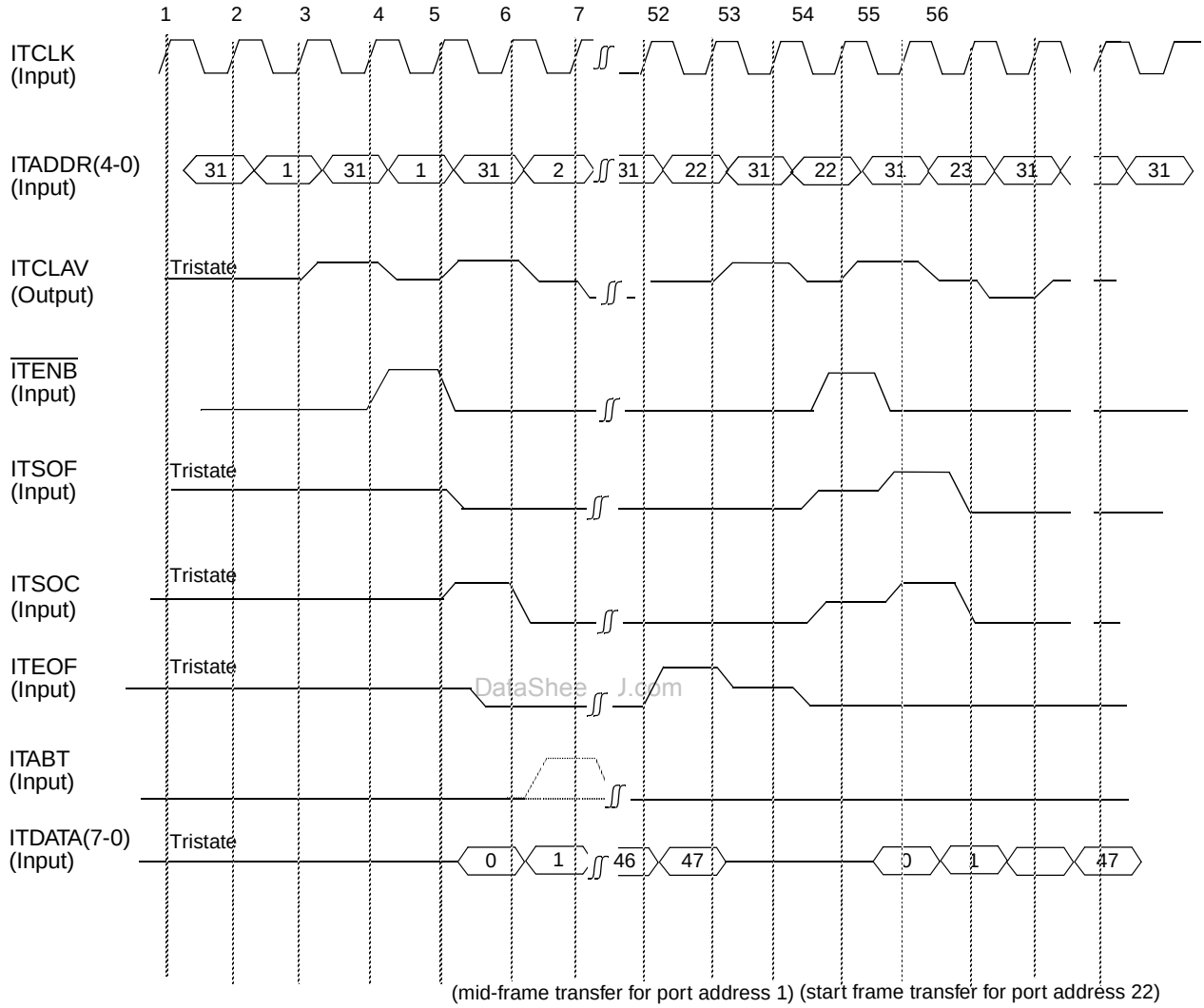



**Figure 14. Timing of Receive Frame Interface, Multi-PHY (ASPEN Device in PHY Layer Emulation)**

Figure 14 shows the handshaking and polling between the PHY and ATM emulation layers. At clock edge #2, the ATM emulation layer places address 1 on ITADDR. At clock edge #3, the Multi-PHY emulation device detects the address. The specific Multi-PHY address port, which matches PHY address 1, responds by asserting ITCLAV. Devices that did not match the address have their outputs set to tristate. At clock edge #4, the ATM emulation layer detects the assertion of ITFAV, and selects port address 1 by a) setting ITADDR port address 1, and b) deasserting $\overline{\text{ITENB}}$. At clock edge #5, the Multi-PHY emulation devices detect that $\overline{\text{ITENB}}$ has been deasserted, and then the selected Multi-PHY device whose address has been selected must start sending data. At clock edge #6, the PHY emulation device starts sampling data.

### Egress UTOPIA Level 2P Interface

The Terminal Egress port constitutes the main outlet interface for the cell traffic between the ASPEN device and other devices in either the ATM or Physical Layers. Several interfaces are supported by the device: UTOPIA (Level 1 and 2), and packet. The modes are selectable via control bit ETLMODE in OP register 0/6/1, bit 21. The encoding for ETLMODE is as follows:

0: UTOPIA Mode

1: Packet Mode

Control bit ETONLINE, when set to one, is used to enable the UTOPIA Level 2P interface. If it is set to zero, then the status that no cell is available for transmission is reported via the UTOPIA Level 2P interface.

Control bits UTCLKSRC(1-0) are used to select the clock used in the UTOPIA interface when in ATM layer emulation, i.e., sourcing the clock for the interface. The encoding follows:

00: LUCLK

01: PCLK

10: PCLK divided by 2

11: Reserved

Cell Mode

There is a 2-cell buffer per port at the UTOPIA interface for decoupling the cell output from the internal or the external cell buffers. The organization of the FIFO will be 2 cells per physical device. Typical signal connections for the ASPEN device when operating in UTOPIA mode are illustrated in Figures 9 - 12. The operating mode options for UTOPIA mode are selected by the control bits ETU1, ETPHYEN, ETCELLSIZE(3-0), ET16b, and ETPHYnADDR (4-0) in OP registers 0/6/1 to 0/6/5. The UTOPIA modes are described in more detail below. Differences between Single-PHY and Multi-PHY functions in a given mode, if any, are highlighted. ETPHYEN determines whether the ASPEN device emulates an ATM or PHY device. ETU1 determines either UTOPIA Level 1 or Level 2 support. ETCELLSIZE sets the outlet cell size, which can vary between 53 bytes and 62 bytes in 8-bit mode or 27 to 32 sixteen bit words in 16-bit mode. The extra bytes are prepended to the ATM cell. In UTOPIA Level 2 mode in ATM layer emulation, the ATM layer device is required to poll the various physical layer devices to determine the availability of cell space in a given PHY device. The polling mechanism implemented in the ASPEN device is round robin-based. The physical and logical address correlation is set via control bits ETPHYnADDR(4-0). Control bit ET16b enables the ASPEN device to transfer 16-bit wide data.

Packet Interface Mode

**Note**: Use of this interface is restricted by application firmware. Contact the TranSwitch Applications Engineering department for additional information regarding the use of this interface.

The Terminal Egress interface block in packet mode reuses the UTOPIA Level 2 interface leads in the following manner. The packets are transferred across using the UTOPIA data leads. The byte arrangement is big-endian. Additional control information is passed across using four leads, ETSOF, ETEOF, ETMS, and ETABT. Framing information is transferred via the ETSOF lead for start of frame and ETEOF for end of frame. ETMS is used in 16-bit mode to indicate which byte contains the last byte of the packet. ETABT, if asserted, indicates that the current packet being transferred has been aborted. In Multi-PHY mode, packets are transferred in 48-byte frames. The signal ETSOC is used to indicate the start of chunk. UTOPIA Level 2 protocols for polling are followed. The lead descriptions can be found in the section headed “Terminal Egress Interface” on page 35.

Single-PHY Handshake

During the transmit window, the PHY emulation layer stores data from ETDATA on the rising edge of ETCLK, if $\overline{\text{ETENB}}$ is asserted. The transmit window exists from the time that the PHY emulation layer indicates it can accept data by asserting ETCLAV (this is a reuse of the UTOPIA signal ETCLAV, Cell Available, in frame mode,

where this signal indicates availability of a frame or frame segment), until four valid write cycles after the PHY layer deasserts ETCLAV. After being asserted this indicates that the ATM emulation layer may transfer only four data words on ETDATA until ETCLAV is reasserted.

An example of Transmit Single-PHY Handshake is shown in Figure 15.

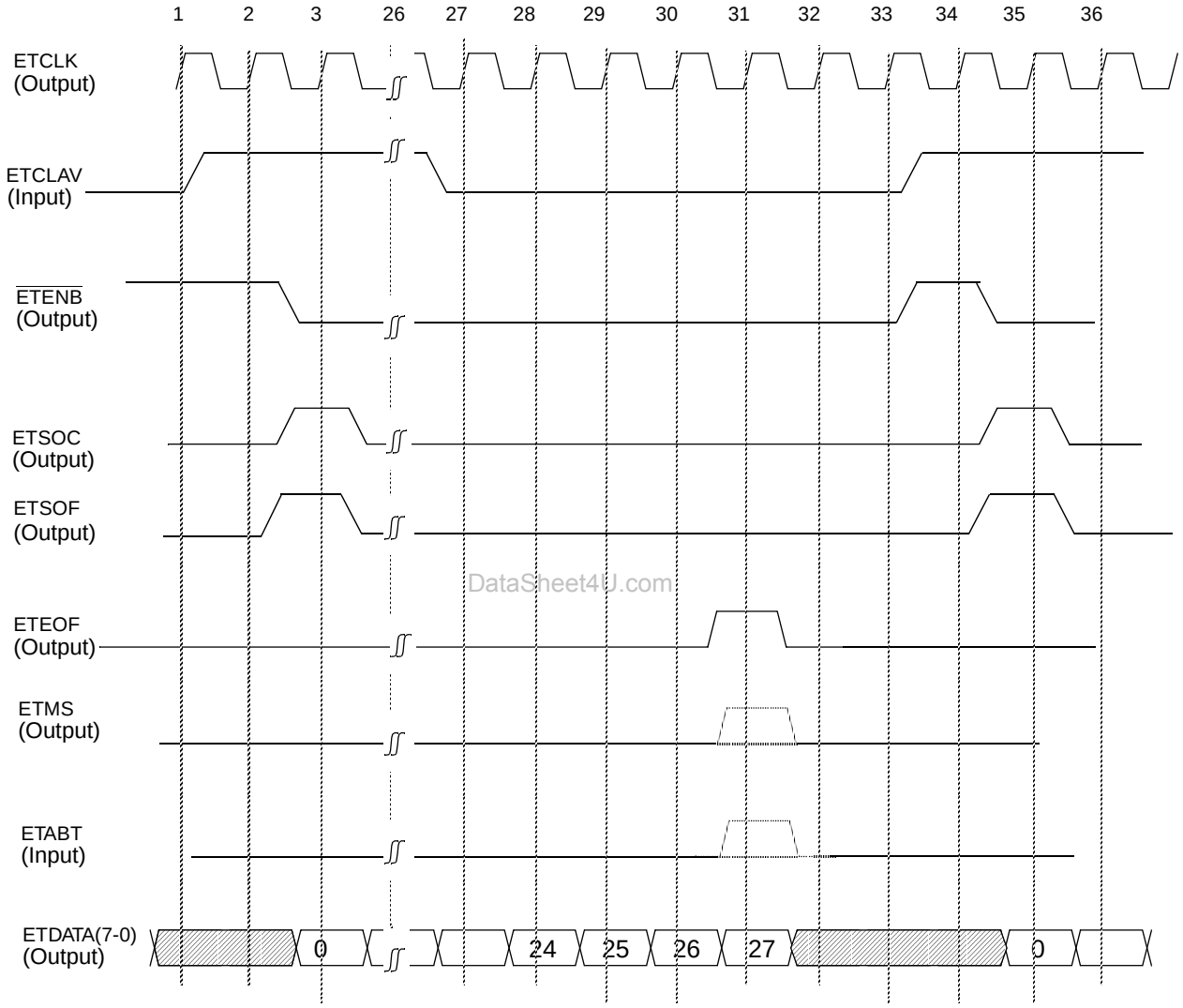



**Figure 15. Timing of Transmit Frame Interface, Single-PHY (ASPEN Device in ATM Layer Emulation)**

Figure 15 shows the handshaking between the PHY and ATM emulation layers. At clock edge #2, the ATM emulation layer recognizes that the PHY emulation layer is able to receive data. The ATM emulation layer responds by asserting $\overline{\text{ETENB}}$, and starting the transmission of data. At clock edge #3, the PHY emulation layer detects the assertion of $\overline{\text{ETENB}}$, and responds accepting the transmission of the frame chunk. At clock edge #26, the PHY emulation layer has only four words of space to accept data, but is not yet at the end of a frame, so it deasserts ETCLAV. At clock edge #27, the ATM emulation layer detects the deassertion of ETCLAV, and only sends a maximum of four new words of data. After clock edge #33, the PHY emulation layer again has sufficient space to accept data, so it reasserts ETCLAV. At clock edge #34, the ATM emulation layer detects the assertion of ETCLAV, and starts transferring data again.

Multi-PHY Handshake

In Single-PHY operation there is a point-to-point link between a PHY emulation device and an ATM layer emulation device. In Multi-PHY, data is transferred from one selected PHY emulation layer to a single ATM emulation layer device. Out of band polling is used in the selection of the next PHY emulation layer device.

The ATM emulation layer device polls the PHY emulation layer by placing the address of a given device on ETADDR. The PHY emulation device responds by driving ETCLAV on the next clock cycle. The state of ETCLAV is based on the ability of the PHY emulation layer device to transfer a frame chunk's worth of information, or an amount of data less than a frame chunk which contains the last byte of the current frame.

The selection of the PHY emulation layer is accomplished by placing the desired address onto ETADDR(4-0) when $\overline{\text{ETENB}}$ is deasserted during the current cycle and reasserted during the next consecutive clock cycle. All Multi-PHY emulation layer devices only examine the value of ETADDR(4-0) for selection purposes when $\overline{\text{ETENB}}$ is deasserted. The selected PHY emulation layer is selected from the cycle after its address is on the ETADDR(4-0) leads and $\overline{\text{ETENB}}$ is deasserted until a new PHY emulation layer is selected.

Once a PHY emulation layer is selected it must be able to transfer either an entire frame chunk, or an amount of data less than a frame chunk which contains the last byte of the current frame. If the latter, then the padding must be added to fill out the frame chunk.

An example of Transmit Multi-PHY Handshake is shown Figure 16.

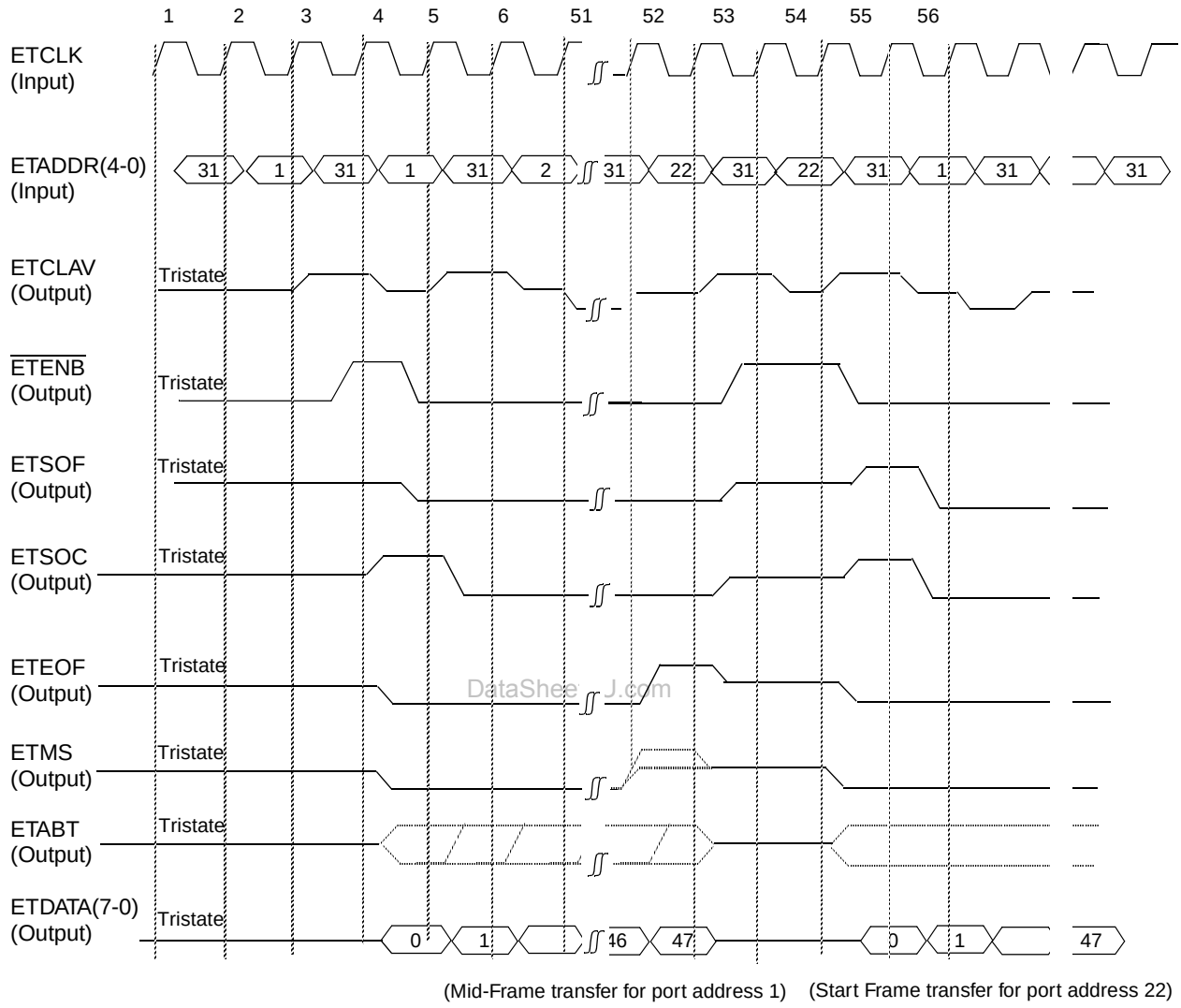



**Figure 16. Timing of Transmit Frame Interface, Multi-PHY (ASPEN Device in PHY Layer Emulation)**

Figure 16 shows the handshaking and polling between the PHY and ATM emulation layers. At clock edge #2, the ATM emulation layer places address 1 on the ETADDR(4-0) leads. At clock edge #3, the Multi-PHY emulation device detects the address. The specific Multi-PHY address port, which matches PHY address 1, responds by asserting ETCLAV. Devices which did not match the address have their outputs set to tristate. At clock edge #4, the ATM emulation layer detects the assertion of ETCLAV, and selects port address 1 by setting ETADDR(4-0) to port address 1, and deselecting $\overline{\text{ETENB}}$. At clock edge #5, the Multi-PHY emulation devices detect that $\overline{\text{ETENB}}$ has been deasserted, and then the specific Multi-PHY address which matches the address on the ETADDR(4-0) leads is selected and must start sending data. At clock edge #6, the ATM emulation starts sampling data.

### SERIAL CONTROL INTERFACE

**Note**: Use of this interface is restricted by application firmware. Contact the TranSwitch Applications Engineering department for additional information regarding the use of this interface.

The nine-lead Serial Control Interface port is a serial line interface composed of a five-bit Line Interface Address enable output bus for selecting one from up to 31 xDSL transceivers, a clock output lead, a data input, a data output and an interrupt input. There are eight dead cycles in between data and address transmission where the data output lead is in tristate. The control bits LDATA(15-0), LADD(14-0), LR/$\overline{W}$, LDIV, LN(4-0), and the status bits LSTATUS, LSCAN(15-0) are located in Outlet Processor registers 0/6/7 - 0/6/10.

### HOST INTERFACE

**Note**: AccessEDGE firmware supports only 64 word offsets using an 8-bit wide dual port RAM interface, as shown in the mailbox organization diagram of Figure 17.

The ASPEN device contains an integrated 8/16-bit Host Interface for transferring data and control information. The Host Interface is a message-based interface between the host and the ASPEN device. Data transfer is performed via mailboxes in the externally mapped memory. An external asynchronous dual-port static RAM is used to hold the mailbox entries, as shown in Figure 18. The six unidirectional mailboxes support variable size message transfers in each direction up to 16 words (64 bytes) in length. Each mailbox starts at an offset of 64 words (256 bytes) or 256 words (1024 bytes) from each other.

A number of operational and failure conditions can be reported to the host processor via messages. The Host Interface incorporates several FIFO buffers to allow masking of latency and significant improvement in throughput.

The communications procedure is as follows: The host or ASPEN device writes a message to a mailbox. The corresponding bit (i.e., for the IP, OP or RP mailbox) in the corresponding (i.e., host or ASPEN) 3-bit write status field (AW/HW) in the mailbox SRAM locations 7FEh and 7FFh is toggled to indicate the presence of the message and then the DPSRAM asserts $\overline{INTER}$(R) (towards the ASPEN device) or $\overline{INTER}$(L) (towards the host). The reading entity reads the write status field, and then the message, from the mailbox. The reading of the status field locations will deassert the $\overline{INTER}$ lead. After the complete message is read, the reader toggles the appropriate read status field (AR/HR in 7FEh and 7FFh), and then the DPSRAM signals the writing entity via the $\overline{INTER}$ (L, R) leads. The original writer will then read the read status field to update the availability of the mailbox.

The default size of the host mailboxes is loaded from EEPROM and is reflected in configuration register HSTSZ (size can be either 64 or 256 words). The default width of the host dual port RAM is loaded from EEPROM and is reflected in configuration control bit HSTWD. HSTWD is used to specify the width of the host dual port SRAM. When set to 0, 8-bit wide data is selected. A 1 selects 16-bit wide data. Please note that ASPEN AccessEDGE firmware supports 8-bit mode. The default dual port memory size is loaded from EEPROM and is reflected in configuration control bit $\overline{HST16K}$, which is used to specify the size of the host dual port SRAM. When set to 0, 16k is selected. 1 selects 64k.

There are six unidirectional mailboxes, which correspond to read and write between each of the three individual internal RISC processors and the host. The location of the messages is based on $\overline{HST16K}$, and HSTDW. The following table fully describes the locations. Each mailbox is located at an offset of either 64 or 256 32-bit words. The example below is using 64-word offsets with 8-bit memory ($\overline{HST16K}$ = 0, HSTDW = 0). Maximum message transfer size to/from ASPEN is 16 words (64 bytes) aligned at the lowest offset address in the mailbox. Only one message is allowed in a mailbox at any given time.

| Byte Offset | Port Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| HOST -> Rate Processor Mailbox (000h - 0FFh) (64 words) | | | | | | | | | |
| 000h<br>03Fh | Host Write/ ASPEN Read | Word #0 to Word 15 Message | | | | | | | |
| 040h ~<br>~ 0FFh | | Word #16 to Word #63 Unused | | | | | | | |
| Rate Processor -> HOST Mailbox (100h - 1FFh) (64 words) | | | | | | | | | |
| 100h<br>13Fh | Host Read/ ASPEN Write | Word #0 to Word #15 Message | | | | | | | |
| 140h ~<br>~1FFh | | Word #16 to Word #63 Unused | | | | | | | |
| HOST -> Ingress Processor Mailbox (200h - 2FFh) (64 words) | | | | | | | | | |
| 200h<br>23Fh | Host Write/ ASPEN Read | Word #0 to Word 15 Message | | | | | | | |
| 240h ~<br>~ 2FFh | | Word #16 to Word #63 Unused | | | | | | | |
| Ingress Processor -> HOST Mailbox (300h - 3FFh) (64 words) | | | | | | | | | |
| 300h<br>33Fh | Host Read/ ASPEN Write | Word #0 to Word 15 Message | | | | | | | |
| 340h ~<br>~ 3FFh | | Word #16 to Word #63 Unused | | | | | | | |
| HOST -> Egress Processor Mailbox (400h - 4FFh) (64 words) | | | | | | | | | |
| 400h<br>43Fh | Host Write/ ASPEN Read | Word #0 to Word 15 Message | | | | | | | |
| 440h ~<br>~ 4FFh | | Word #16 to Word #63 Unused | | | | | | | |
| Egress Processor -> HOST Mailbox (500h - 5FFh) (64 words) | | | | | | | | | |
| 500h<br>53Fh | Host Read/ ASPEN Write | Word #0 to Word 15 Message | | | | | | | |
| 540h ~<br>~ 5FFh | | Word #16 to Word #63 Unused | | | | | | | |
| 600h<br><br><br>7FDh | | Unused | | | | | | | |
| 7FEh | Host Read/ ASPEN Write | AW | | | | | AR | | |
| 7FFh | Host Write/ ASPEN Read | HW | | | | | HR | | |

**Figure 17. Dual Port RAM Mailbox Organization**

**AW:** 3-bits indicates current write status of ASPEN to HOST mailboxes. Bits change on event basis i.e. are toggled. Organization is Ingress, Egress, Rate. ASPEN updates this field.

**AR:** 3-bits indicates current read status of HOST to ASPEN mailboxes. Bits change on event basis i.e. are toggled. Organization is Ingress, Egress, Rate. ASPEN updates this field.

**HW:** 3-bits indicates current write status of HOST to ASPEN mailboxes. Bits change on event basis i.e. are toggled. Organization is Ingress, Egress, Rate. Host updates this field.

**HR:** 3-bits indicates current read status of ASPEN to HOST mailboxes. Bits change on event basis i.e. are toggled. Organization is Ingress, Egress, Rate. Host updates this field.

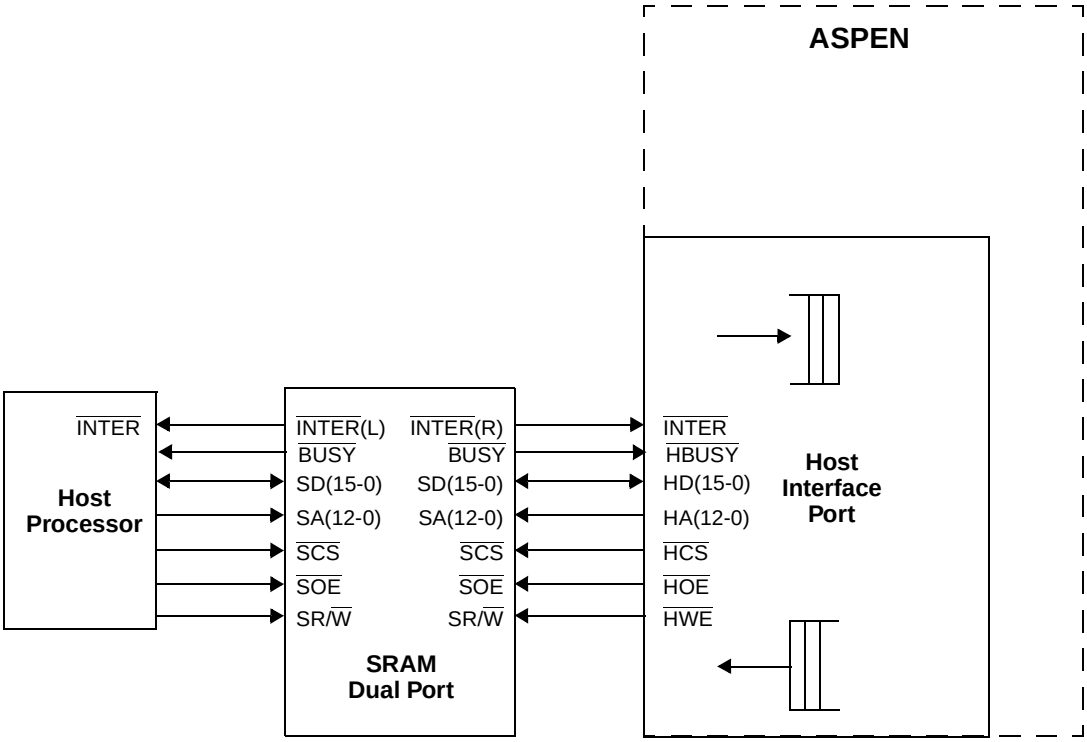



**Figure 18. Host Processor Interface**

### Host Control Logic

The Host Interface control logic allows the external host processor to access on-chip control/status registers, and external control memory data structures. This allows the host software to configure, control and poll the ASPEN device, and to communicate with firmware running on the ASPEN device RISC cores. The control logic also implements read and write FIFO buffers that interface between the control logic and DMA controller and internal registers. The FIFO buffers allow burst writes and reads to be performed from the off-chip mailboxes to the local memory or on-chip registers. The ASPEN device Host Interface uses a 16-word write command/data FIFO, and a 16-word read command FIFO. These two FIFOs permit the Host Interface to implement a write-behind/fetch-ahead behavior: memory commands are buffered and memory read data words are pre-fetched to hide memory access latencies.

Microprocessor interrupt lead $\overline{\text{INTER}}$ is asserted when the appropriate status field is written, and deasserted when the status field is read.

Before initiating ASPEN reset via the $\overline{\text{RESET}}$, $\overline{\text{FWRST}}$ sequence, (see Figure 68), the host should insure that no messages are pending to ASPEN in order to avoid messages being trapped in the dual port RAM. The ASPEN firmware download can be initiated 20ms after the $\overline{\text{RESET}}$, $\overline{\text{FWRST}}$ sequence.

### Message Format

Detailed message formats are described in the appropriate User's Guide for AccessEDGE firmware.

### SERIAL EEPROM INTERFACE

The non-volatile serial EEPROM interface is used to access boot firmware, stored in an external EEPROM, required for booting up the ASPEN device. A 16 kbit minimum device is required. The external EEPROM will be accessed upon hardware and firmware reset (see timing in Figure 68).

This interface requires 3 leads: SCK (Serial EEPROM Clock), SDIO (Serial EEPROM Address Output/Data Input), and $\overline{SCS}$ (Serial EEPROM Chip Select). The serial clock lead SCK is an output, and has a rate of approximately 0.03 x PCLK. Data transfer is performed through SPI protocol over SDIO, as defined by commercial serial EEPROM devices. The control bits SEADD(15-0), and status bits SEDATA(31-0) and SESTATUS, are located in the Outlet Processor registers 0/6/A- 0/6/12. The timing diagram is shown in Figure 65. The memory map is shown below:

**Table 1. Serial EEPROM Configuration Register Map**

| ADDR | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Configuration Space | | | | | | | |
| 254 | | | | | | | | |
| 255 | Reserved (Set to 0) | | | | | | | |
| 256 | OP Boot Code | | | | | | | |
| 767 | | | | | | | | |
| 768 | IP Boot Code | | | | | | | |
| 1279 | | | | | | | | |
| 1280 | RP Boot Code | | | | | | | |
| 1791 | | | | | | | | |
| 1792 | General Purpose Space | | | | | | | |
| 65535 | | | | | | | | |



### SSRAM MEMORY INTERFACE

**Note**: AccessEDGE Firmware only supports a 64-bit SSRAM interface.

An external local memory is required by the ASPEN device to hold data structures and queues. The ASPEN device integrates a complete memory controller to support this local memory. The ASPEN device supports a synchronous SRAM configuration where all data structures and queues are accessed via this interface. The on-chip memory controller provides a 'glueless' interface to high speed synchronous SRAM. No external timing or control logic is required. The external memory may be partitioned only using similar size memory configurations i.e., all 1 Mbit, 4 Mbit, 8 Mbit or 16 Mbit. The control bits SBZ(1-0) specify the function of the SCE2 and $\overline{SCE2}$ output leads, which are used as chip select or extended memory address outputs, as shown in Table 2.

**Table 2. SCE2, $\overline{SCE2}$ functional mapping**

| SBZ1 | SBZ0 | SCE2 | $\overline{SCE2}$ |
|---|---|---|---|
| 0 | 0 | SA16 | $\overline{SA16}$ |
| 0 | 1 | SA20 | $\overline{SA20}$ |
| 1 | 0 | SA18 | $\overline{SA18}$ |
| 1 | 1 | Reserved | |

The SRAM memory controller directly addresses up to 16 MBytes of external memory. The memory controller uses a 64-bit memory datapath running at 100 MHz to allow sustained transfers of up to 6400 Mbit/s.
Note: Refer to Figures 58, 59 and 60, as well as notes on page 100, when designing the SSRAM memory interface.

Example SSRAM configurations are shown in Figures 19, 20 and 21.

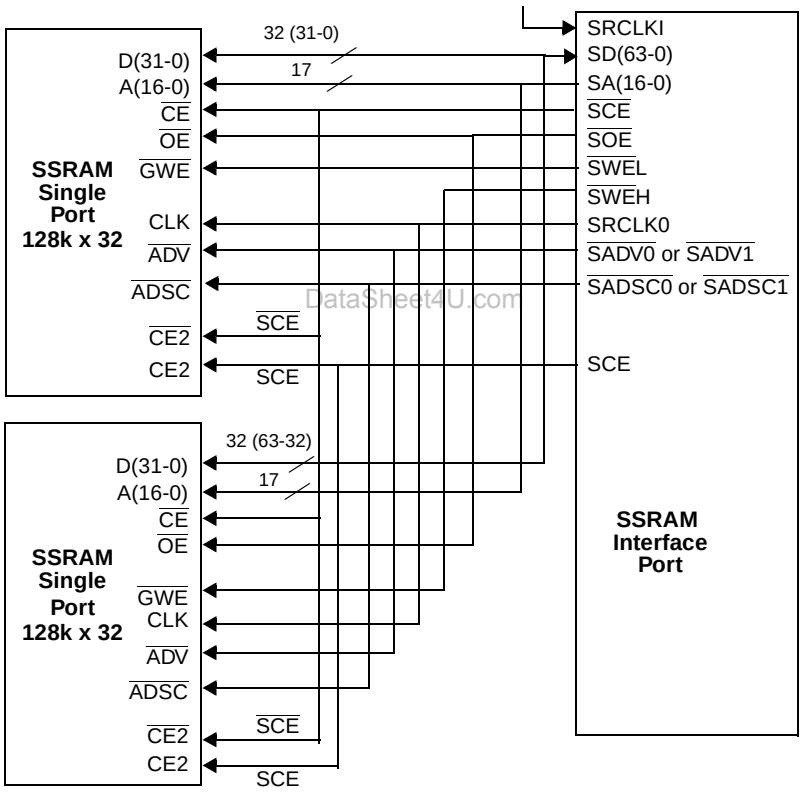



**Figure 19. SSRAM Example Configuration - 64-bit wide, depth = 1, 4 Mbit memories used**

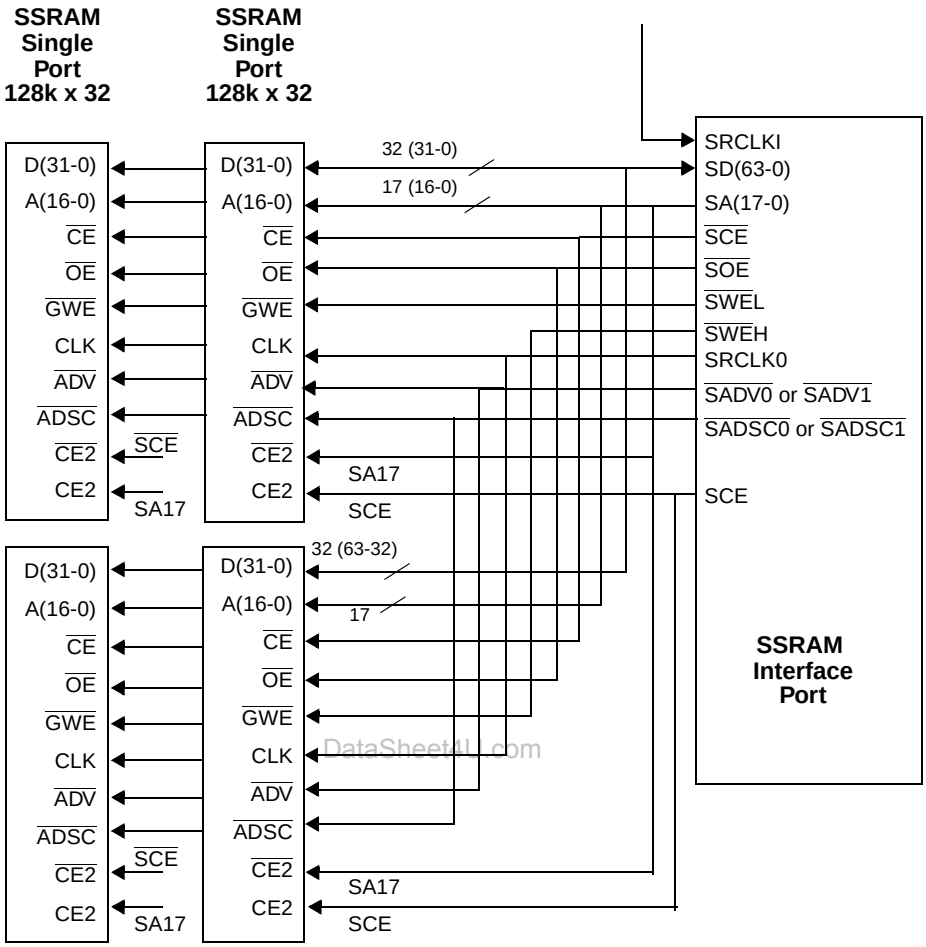



**Figure 20. SSRAM Example Configuration - 64-bit wide, depth = 2, 4 Mbit memories used**

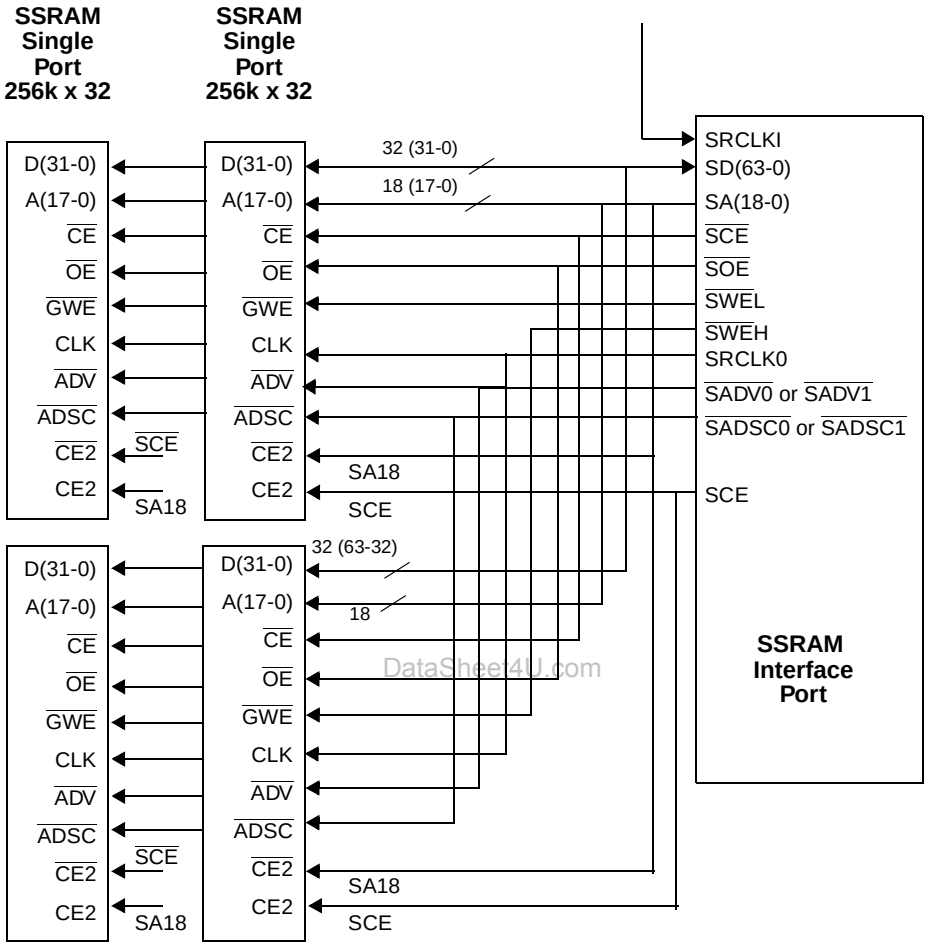



**Figure 21. SSRAM Example Configuration - 64-bit wide, depth = 2, 8 Mbit memories used**

### JTAG BOUNDARY SCAN BACKGROUND INFORMATION

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 22. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{\text{TRS}}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{\text{TRS}}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a 16-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers, LSB first. A timing diagram for the boundary scan feature is provided in Figure 66.



#### Boundary Scan Support



The ASPEN device executes the following boundary scan test instructions:

- EXTEST
- SAMPLE/PRELOAD
- BYPASS

EXTEST Test Instruction

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads.

SAMPLE/PRELOAD Test Instruction

When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction

When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay. When JTAG test reset ($\overline{\text{TRS}}$) is asserted, the BYPASS instruction is loaded by default.

### BSDL File

A Boundary Scan Description Language (BSDL) file for the ASPEN device is available for download from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

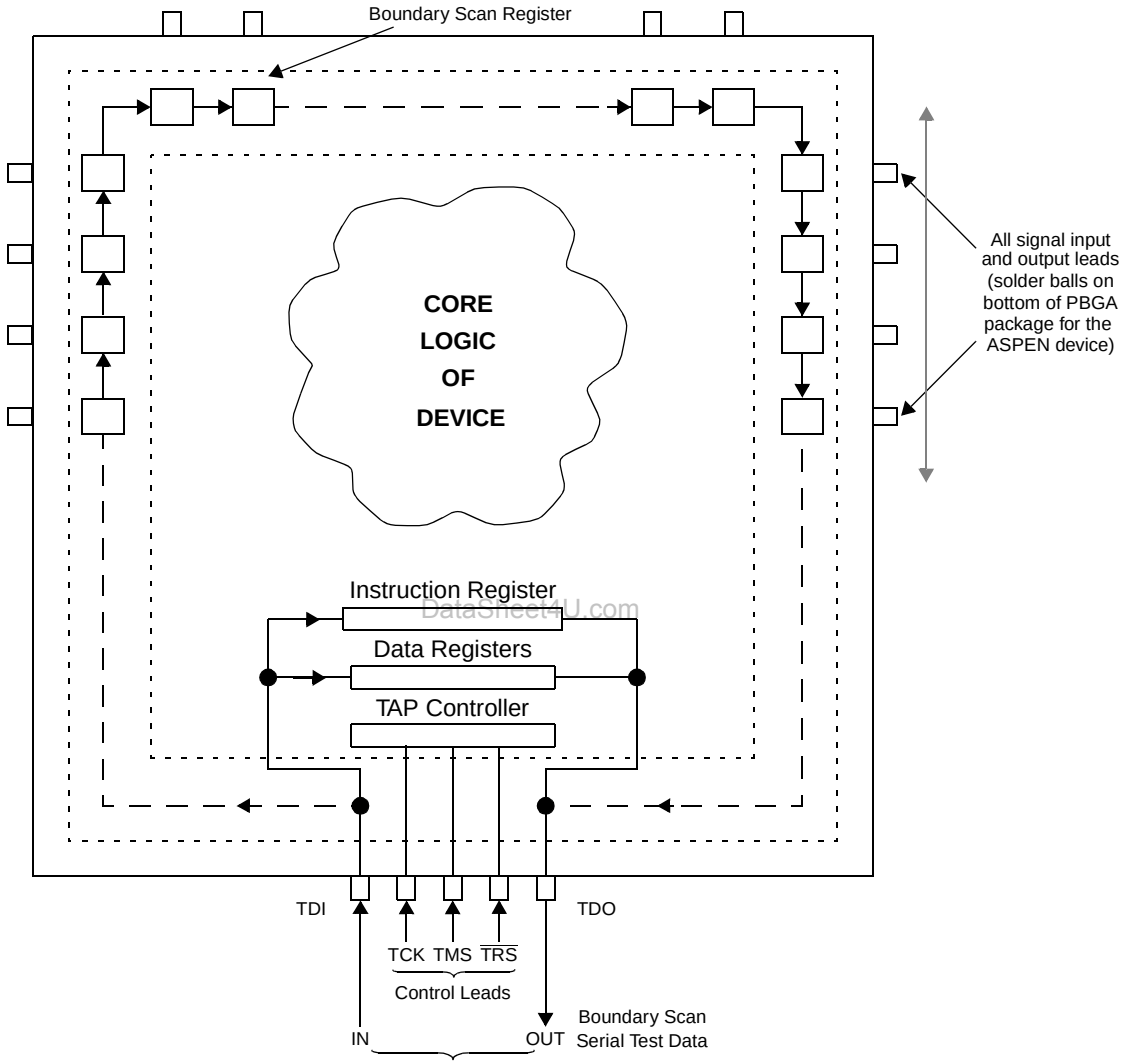



**Figure 22. Boundary Scan Top-Level Block Diagram**

## LEAD DESCRIPTIONS

### POWER SUPPLY, GROUND AND NO CONNECT

| Symbol | Lead No. | I/O/P * | Type | Name/Function |
|---|---|---|---|---|
| VDD3 | C02, E26, F29, H04, K05, K26, M27, P05, P28, R04, R26, T26, U01, V26, W04, Y26, AA25, AB02, AC26, AD01, AE15, AE18, AE23, AF09, AF12, AG07, AG17, AH21, AH23, AH26 | P | | **$V_{DD3}$:** +3.3 volt, ±5% input/output supply. Refer to Note 5 under "Power Requirements" section, on page 46, for the required power-up/power-down sequence of the device. |
| VDD2.5 | A03, A05, A10, A11, A14, A16, A19, A20, A27, A29, B02, C01, C29, E05, E25, K01, K29, L01, L29, P01, P29, T01, V29, W01, W29, Y01, Y29, AC29, AE05, AE25, AG01, AH03, AH29, AJ01, AJ03, AJ05, AJ10, AJ11, AJ14, AJ16, AJ19, AJ20, AJ27, AJ29 | P | | **$V_{DD2.5}$:** +2.5 volt, ±5% CMOS core supply. Refer to Note 5 under "Power Requirements" section, on page 46, for the required power-up/power-down sequence of the device. |

* Note: I = Input; O = Output; P = Power

| Symbol | Lead No. | I/O/P * | Type | Name/Function |
|---|---|---|---|---|
| VSS | A02, A04, A07, A08, A09, A12, A15, A18, A21, A22, A23, A25, A26, A28, B01, B29, D01, D26, D29, E01, E06, E29, G01, G29, H01, H29, J01, J29, L11, L13, L15, L17, L19, M01, M29, N11, N13, N15, N17, N19, R01, R11, R13, R17, R19, R29, T29, U11, U13, U15, U17, U19, V01, W11, W13, W15, W17, W19, AA01, AA29, AB01, AB29, AC01, AD05, AD25, AE01, AE29, AF01, AF29, AG29, AH01, AH02, AH28, AJ02, AJ04, AJ07, AJ08, AJ09, AJ12, AJ15, AJ18, AJ21, AJ22, AJ23, AJ25, AJ26, AJ28 | P | | **$V_{SS}$:** Ground**,** 0 volt reference. |
| VDDBOOTA | E10 | P | | **VDDBOOTA:** +2.5V, ± 5%, supply voltage, which must be present for the *CellBus* A disable function to work. |
| VDDBOOTB | D18 | P | | **VDDBOOTB:** +2.5V, ± 5%, supply voltage, which must be present for the *CellBus* B disable function to work. |
| NC | B26, C03, D04, D05, E07, E24, L03, L05 | - | | **No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. Some NC leads may be assigned functions in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these leads having been left floating. |

* Note: I = Input; O = Output; P = Power, T = Tristate

**TERMINAL EGRESS INTERFACE**

| Symbol | Lead No. | I/O/P | Type * | Name/Function |
|---|---|---|---|---|
| ETCLK | AE12 | I/O (T) | LVTTL/ CMOS 12mA | **Egress Terminal UTOPIA Clock:** 50 MHz UTOPIA interface clock |
| $\overline{\text{ETENB}}$ | AH10 | I/O (T) | LVTTL/ CMOS 8mA | **Egress Terminal Enable:**<br>**UTOPIA mode** - Egress terminal input in PHY mode, output in ATM mode. Active low read enable signal for cell output.<br>**Packet mode** - Active low read enable signal for packet output. Input in PHY emulation mode, output in ATM emulation mode. |
| ETCLAV | AH09 | I/O (T) | LVTTL/ CMOS 8mA | **Egress Terminal Cell/Packet Available:**<br>**UTOPIA mode** - Egress terminal input in ATM mode, output in PHY mode. Active high signal indicating a cell space is available in the external PHY device to receive a cell when in ATM mode. In PHY mode it indicates that a cell is available to be sent to the ATM device.<br>**Packet mode** - Active high signal indicating buffer space is available to receive a packet chunk when in ATM mode. In PHY mode it indicates that a packet chunk is available to be sent to the ATM device. |
| ETDATA(0-15) | AE11, AF10 AG09, AH08 AE10, AG08 AJ06, AE09 AF08, AH07 AH06, AE08 AG06, AH05 AF07, AE06 | O (T) | CMOS 8mA | **Egress Terminal Data:** Output data bus |
| ETSOC | AG10 | O (T) | CMOS 8mA | **Egress Terminal Start of Cell/ Start of chunk:**<br>**UTOPIA mode** - Start of Cell indicator.<br>**Packet mode** - Start of Chunk indicator. |
| ETSOF | AF14 | O (T) | CMOS 8mA | **Egress Terminal Start of Frame:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - Start of Frame Indicator. |
| ETADDR(0-4) | AG12, AH11 AE14, AE13 AG11 | I/O (T) | LVTTL/ CMOS 8mA | **Egress Terminal Multi-PHY Address:**<br>**UTOPIA mode** - Used for polling each port to determine the availability of a cell in PHY mode, and availability of a cell space for transfer in ATM mode. Input in PHY emulation mode, output in ATM emulation mode.<br>**Packet mode** - Used for polling each port to determine the availability of a space available for transfer in Multi-PHY mode. Input in PHY emulation mode, output in ATM emulation mode. |

* See Input, Output and Input/Output Parameters section for Type descriptions.

| Symbol | Lead No. | I/O/P | Type * | Name/Function |
|---|---|---|---|---|
| ETPARITY | AF11 | O (T) | CMOS 8mA | **Egress Terminal Parity:**<br>**UTOPIA Mode** - Odd parity over ETDATA.<br>**Packet mode** - Odd Parity over ETDATA, ETSOF, ETEOF, and ETMS. |
| ETEOF | AG13 | O (T) | CMOS 8mA | **Egress Terminal End of Frame:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - End of Frame Indicator. |
| ETMS | AH12 | O (T) | CMOS 8mA | **Egress Terminal Most Significant Byte:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - Active high signal indicates the most significant byte is the last byte of the outgoing frame. This signal is valid only in 16-bit mode. |
| ETABT | AF13 | I | LVTTL | **Egress Terminal Abort Transmission:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - Active high signal indicates an error in the current packet being sent. |

**SERIAL CONTROL INTERFACE**

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| LADD(0-4) | AB03, AC02, AB05, AC03, AD03 | O (T) | CMOS 4 mA | **Line Interface Address:** These signals enable a given xDSL transceiver on the first falling edge of LCK. When asserted, data can be written to, or read from, the line interface from/to any of the 31 potential devices. |
| LCK | AC04 | O (T) | CMOS 4 mA | **Line Interface Clock:** This signal is used to shift data to and from the line interface serial port. Data out, LDO, is updated on the falling edge of LCK. Data in, LDI, is sampled on the rising edge of LCK. LCK rate is a division of PCLK. When control bit LDIV = 0, the LCK rate is PCLK÷4 and when LDIV = 1, the LCK rate is PCLK÷2. |
| LDO | AD04 | O (T) | CMOS 4 mA | **Line Interface Data Out:** This is the serial data output to the xDSL component. This output is shared among the multiple components. This output is updated on the falling edge of LCK using the following format. The first bit is Read/$\overline{\text{Write}}$ followed by fifteen address bits. |
| LDI | AD02 | I | LVTTL | **Line Interface Data In:** This is the serial data input from the xDSL components. This input is shared among the multiple transceivers. This input is sampled on the rising edge of LCK. |
| LINT | AE02 | I | LVTTL | **Line Interface Interrupt:** This is the interrupt lead from the xDSL components. This input is shared among the multiple transceivers. This active high signal indicates an interrupt is pending. LINT becomes inactive when the interrupt has been serviced. |

**TERMINAL INGRESS INTERFACE**

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| ITCLK | R03 | I/O (T) | LVTTL/ CMOS 12mA | **Ingress Terminal UTOPIA Clock:** 50 MHz UTOPIA interface clock |
| $\overline{\text{ITENB}}$ | N01 | I/O (T) | LVTTL/ CMOS 8mA | **Ingress Terminal Enable:**<br>**UTOPIA mode** - Ingress terminal input in PHY mode, output in ATM mode. Active low read enable signal for cell transfer in ATM mode. Active low write enable in PHY mode.<br>**Packet mode** - Active low read enable signal for packet transfer in ATM mode. This signal is an input in PHY emulation mode, which indicates write enable. |
| ITCLAV | N02 | I/O (T) | LVTTL/ CMOS 8mA | **Ingress Terminal Cell/Packet Available:**<br>**UTOPIA mode** - Ingress terminal input in ATM mode, output in PHY mode. Active high signal indicating that space is available to receive a cell (PHY mode) or that a cell is available to be sent by the PHY device (ATM mode).<br>**Packet mode** - Active high output signal indicating a packet chunk space is available to receive a packet chunk in PHY mode. Input in ATM emulation mode, indicating that a cell is available to be sent by the PHY device. |
| ITDATA(0-15) | Y02, W03, V05, U05, W02, V03, V04, U04, V02, U02, U03, T02, R02, T04, T03, T05 | I | LVTTL | **Ingress Terminal Data:** Input data bus |
| ITSOC | R05 | I | LVTTL | **Ingress Terminal Start of Cell/ Start of Chunk:**<br>**UTOPIA mode** - Start of Cell indicator.<br>**Packet mode** - Start of Chunk indicator. |
| ITSOF | AA03 | I | LVTTL | **Ingress Terminal Start of Frame:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - Start of Frame Indicator. |
| ITADDR(0-4) | Y05<br>AA02<br>Y03<br>Y04<br>W05 | I/O (T) | LVTTL/ CMOS 8mA | **Ingress Terminal Multi-PHY Address:**<br>**UTOPIA mode** - Used for polling each port to determine the availability of cell space in PHY mode, and availability of a cell for transfer in ATM mode. Input in PHY emulation mode, output in ATM emulation mode.<br>**Packet mode** - Used for polling each port to determine the availability of a chunk which is ready for transfer in Multi-PHY mode. Input in PHY emulation mode, output in ATM emulation mode. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| ITPARITY | P02 | I | LVTTL | **Ingress Terminal Parity:**<br>**UTOPIA Mode** - Odd parity over ITDATA.<br>**Packet mode** - Odd parity over ITDATA, ITSOF, ITEOF, ITMS, and ITABT or over ITDATA alone, based on control bit ITPARDATA. |
| ITEOF | AB04 | I | LVTTL | **Ingress Terminal End of Frame:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - End of Frame Indicator. |
| ITMS | AA05 | I | LVTTL | **Ingress Terminal Most Significant Byte:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - Active high signal indicates the most significant byte is the last byte of the incoming frame. This signal is valid only in 16-bit mode. |
| ITABT | AA04 | I | LVTTL | **Ingress Terminal Abort:**<br>**UTOPIA mode** - This signal is not used in UTOPIA mode.<br>**Packet mode** - Active high signal indicates the current packet being received has an error. |

***CellBus* Interface**

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| $\overline{\text{CBRCA}}$ | B03 | I | GTL+ | ***CellBus* A Read Clock:** Used to clock in data from A bus. Falling edge used for data transfer. The maximum frequency of the read and write clocks is 40 MHz. |
| $\overline{\text{CBRCB}}$ | C15 | I | GTL+ | ***CellBus* B Read Clock:** Used to clock in data from B bus. Falling edge used for data transfer. The maximum frequency of the read and write clocks is 40 MHz. |
| $\overline{\text{CBWCA}}$ | B06 | I | GTL+ | ***CellBus* A Write Clock:** Used to drive data on the A bus. Falling edge used for data transfer. The maximum frequency of the read and write clocks is 40 MHz. |
| $\overline{\text{CBWCB}}$ | D15 | I | GTL+ | ***CellBus* B Write Clock:** Used to drive data on the B bus. Falling edge used for data transfer. The maximum frequency of the read and write clocks is 40 MHz. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| $\overline{\text{CBDA(0-31)}}$ | D14, C13, B13, A13, E12, D12, C12, B12, E11, D11, C11, B11, D10, C10, B10, E09, D09, B09, E08, D08, C08, B08, D07, C07, B07, D06, C06, C05, B05, A06, C04, B04 | I/O (T) | GTL+ | ***CellBus* A Data:** Active low 32-bit parallel data input/output bus for *CellBus* A. |
| $\overline{\text{CBDB(0-31)}}$ | B25, C23 B23, D22 C22, B22 E21, D21 C21, B21 E20, D20 C20, B20 E19, D19 B19, E18 C18, B18 E17, D17 C17, B17 A17, E16 D16, C16 B16, E15 B15, E14 | I/O (T) | GTL+ | ***CellBus* B Data:** Active low 32-bit parallel data input/output bus for *CellBus* B. |
| $\overline{\text{CBFA}}$ | D13 | I/O (T) | GTL+ | ***CellBus* A Frame Pulse:** Active low pulse that occurs once for every 16 or 32 *CellBus* A clock cycles, corresponding to selection of 16-user or 32-user modes. |
| $\overline{\text{CBFB}}$ | A24 | I/O (T) | GTL+ | ***CellBus* B Frame Pulse:** Active low pulse that occurs once for every 16 or 32 *CellBus* B clock cycles, corresponding to selection of 16-user or 32-user modes. |
| $\overline{\text{CBACKA}}$ | E13 | I/O (T) | GTL+ | ***CellBus* A Acknowledge:** Active low acknowledge for each cell received on *CellBus* A. |
| $\overline{\text{CBACKB}}$ | B24 | I/O (T) | GTL+ | ***CellBus* B Acknowledge:** Active low acknowledge for each cell received on *CellBus* B. |
| $\overline{\text{CBCONGA}}$ | B14 | I/O (T) | GTL+ | ***CellBus* A Congestion:** Active low congestion indicator set by receiving device for *CellBus* A. |
| $\overline{\text{CBCONGB}}$ | C24 | I/O (T) | GTL+ | ***CellBus* B Congestion:** Active low congestion indicator set by receiving device for *CellBus* B. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| $\overline{\text{CBDISABLEA}}$ | C14 | I | CMOS2.5 | ***CellBus* A Disable:** Active low signal to tristate all outputs of the device to *CellBus* A, regardless of the state of the $V_{DD2.5}$ and $V_{DD3}$ power supplies. (This signal is not part of the *CellBus*.)<br>Note: VDDBOOTA must be present at all times. |
| $\overline{\text{CBDISABLEB}}$ | E22 | I | CMOS2.5 | ***CellBus* B Disable:** Active low signal to tristate all outputs of the device to *CellBus* B, regardless of the state of the $V_{DD2.5}$ and $V_{DD3}$ power supplies. (This signal is not part of the *CellBus*.)<br>Note: VDDBOOTB must be present at all times. |
| CAVREF | C09 | I | Reference Voltage | **CAVREF:** Reference voltage for GTL+ receivers on *CellBus* A. CAVREF is approximately 2/3 $V_{tt}$, where $V_{tt}$ is the backplane termination voltage (nominally $V_{tt}$ = +1.5V). (This signal is not part of the *CellBus*.)<br>Note: CAVREF must be present at all times. |
| CBVREF | C19 | I | Reference Voltage | **CBVREF:** Reference voltage for GTL+ receivers on *CellBus* B. CBVREF is approximately 2/3 $V_{tt}$, where $V_{tt}$ is the backplane termination voltage (nominally Vtt = +1.5V). (This signal is not part of the *CellBus*.)<br>Note: CBVREF must be present at all times. |



**MISCELLANEOUS LEADS**



| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| $\overline{\text{RESET}}$ | P03 | I | LVTTLp | **Hardware Reset:** An active low pulse with minimum width of 200 ns which must be applied after power-up to reset all registers, counters, and FIFOs. The reset is asynchronous going into the reset state, but requires all external clocks to be stable when coming out of the reset state. |
| $\overline{\text{FWRST}}$ | N03 | I | LVTTLp | **Firmware Reset:** An active low pulse, used in conjunction with the $\overline{\text{RESET}}$ lead, that triggers a firmware reload from the serial EEPROM. See the timing diagram in Figure 68. |
| $\overline{\text{RESERVEH}}$ | M02 | I | LVTTLp | **Reserve:** Tied to VDD3 for normal operation. |
| RESERVEL | P04 | I | LVTTLpd | **Reserve:** Tied to VSS for normal operation. |
| PCLK_BP | AG04 | I | LVTTL | **Processor Clock Bypass:** Used only when internal PLL is bypassed during production testing. Tied to ground for customer applications. |
| PCLK | AF05 | I | LVTTL | **Processor Clock:** Up to 50 MHz PLL clock reference. Internally, speed is multiplied by 2 in a PLL to generate the internal system clock. |
| LUCLK | AG02 | I | LVTTL | **Local UTOPIA Clock:** This is a clock that is used for UTOPIA interfaces when in ATM Layer emulation mode. The maximum clock frequency is 50 MHz. |
| PLLVDD | AF04 | P | VDD | **PLL VDD:** Filtered 2.5 volt VDD power input for PLL block. See Figure 78. Refer to Note 5 under “Power Requirements” section, on page 46, for the required power-up/power-down sequence of the device. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| PLLEN | AH04 | I | LVTTLp | **PLL Enable:** An active high input to enable the PLL. |
| PLLVSS | AF06 | P | GND | **PLL VSS:** Separate 0 volt reference input for PLL block. See Figure 78. |
| $\overline{\text{PLLTEST}}$ | AG05 | I | LVTTLp | **PLL Test:** Used to bypass PLL. When set to 0, PCLK_BP is used directly as a system clock. When set to 1, PCLK x 2 is used as system clock. |
| PLLRATIO (3-0) | AE04, AE07, AG03, AC05 | I | LVTTLp | **PLL Current Ratios (3-0):** Used to program current ratios for two PLL charge pumps. Normally set to 1111. |

**SSRAM INTERFACE PORT**

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| SD(0-63) | B27, C26<br>C25, E23<br>D25, G25<br>C27, B28<br>C28, D27<br>E27, F25<br>D28, E28,<br>F26, G26<br>F27, G27<br>H25, F28<br>G28, H26<br>H28, H27<br>J26, K25<br>J28, J27<br>L25, K28<br>K27, L26<br>P25, R28<br>R25, R27<br>U29, T28<br>U28, T27<br>U27, V28<br>U26, V27<br>V25, T25<br>U25, W27<br>W25, W28<br>W26, Y27<br>Y25, Y28<br>AA27, AB28<br>AA28, AA26<br>AB27, AB25<br>AB26, AC28<br>AD28, AD29 | I/O (T) | LVTTL/<br>CMOS<br>8mA | **SSRAM Data:** Bidirectional 64-bit data bus used for reading input and writing output data from/to the external SSRAM. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| SA(0-20) | AJ24, AG24<br>AF24, AH25<br>AE24, AG25<br>AG26, AF25<br>AF26, AH27<br>AG27, AC25<br>AE26, AF27<br>AG28, AE27<br>AF28, AD26<br>AD27, AE28<br>AC27 | O (T) | CMOS<br>8mA | **SSRAM Address:** 21-bit address output bus used to select external SSRAM address for read or write access. |
| $\overline{SCE}$ | P27 | O (T) | CMOS<br>8mA | **SSRAM Chip Select:** Active low output signal enables the interface to SSRAM and allows the transfer of information between the ASPEN device and the selected SSRAM. |
| SCE | P26 | O (T) | CMOS<br>8mA | **SSRAM Chip Select:** Active high output signal mirrors $\overline{SCE}$ lead functionality. |
| $\overline{SCE2}$ | N28 | O (T) | CMOS<br>8mA | **SSRAM Chip Select 2:** Active low output signal used in conjunction with $\overline{SCE}$, SCE to expand the depth of the address space. |
| SCE2 | N29 | O (T) | CMOS<br>8mA | **SSRAM Chip Select 2:** Active high output signal used in conjunction with $\overline{SCE}$, SCE to expand the depth of the address space. |
| $\overline{SOE}$ | N27 | O (T) | CMOS<br>8mA | **SSRAM Output (Read) Enable:** This output signal is asserted low to enable the SSRAM to drive the data bus. |
| $\overline{SWEL}$ | M28 | O (T) | CMOS<br>8mA | **SSRAM Write Enable Low:** This output signal is asserted low to initiate an SSRAM write cycle for the lower 32 bits of the data bus (i.e., 31-0). Separate enables are used for the lower and upper 32-bit words. |
| $\overline{SWEH}$ | N26 | O (T) | CMOS<br>8mA | **SSRAM Write Enable High:** This output signal is asserted low to initiate an SSRAM write cycle for the upper 32 bits of the data bus (i.e., 63-32). Separate enables are used for the lower and upper 32-bit words. |
| SRCLKI | L27 | I | LVTTL | **SSRAM Clock Input:** Clock input for DMA interface and external SSRAM interface |
| SRCLKO | M26 | O (T) | CMOS<br>12 mA | **SSRAM Clock Output:** Clock output for external SSRAM interface |
| $\overline{SADV0}$<br>$\overline{SADV1}$ | N25<br>D23 | O (T) | CMOS<br>8mA | **SSRAM Address Advance**: This is a duplicated output to double load drive capability. Active low output used to advance the internal burst counter, controlling burst access after the external address is loaded. A high causes wait states to be generated. |
| $\overline{SADSC0}$<br>$\overline{SADSC1}$ | M25<br>D24 | O (T) | CMOS<br>8mA | **SSRAM Address Controller**: This is a duplicated output to double load drive capability. Active low output that causes a new external address to be registered at the SSRAM. A write cycle is initiated if $\overline{SWEL}$ or $\overline{SWEH}$ is low, otherwise a read cycle will be initiated. |

### HOST INTERFACE PORT

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| HD(0-15) | AE22, AG23<br>AF22, AE21<br>AH22, AG22<br>AF21, AE20<br>AG21, AF20<br>AE19, AH20<br>AG20, AF19<br>AG19, AH19 | I/O (T) | LVTTL/<br>CMOS<br>8mA | **Host Data:** Bidirectional 16-bit data bus used for reading and writing data from/to the external host dual port SRAM. |
| HA(0-12) | AJ13, AH14<br>AF15, AG15<br>AH15, AE16<br>AG16, AF16<br>AH16, AH17<br>AJ17, AG18<br>AH18 | O (T) | CMOS<br>8mA | **Host Address:** 13-bit address output bus used to select the external host dual port SRAM address for read or write access. |
| $\overline{\text{HCS}}$ | AF17 | O (T) | CMOS<br>6mA | **Host Chip Select:** Active low output signal enables the interface to the host dual port SRAM and allows the transfer of information between the ASPEN device and the SRAM. |
| $\overline{\text{HOE}}$ | AE17 | O (T) | CMOS<br>8mA | **Host Output (Read) Enable:** This output signal is asserted low to initiate a read cycle of the host dual port SRAM. |
| $\overline{\text{HWE}}$ | AF18 | O (T) | CMOS<br>8mA | **Host Write Enable:** This output signal is asserted low to initiate a write cycle of the host dual port SRAM. |
| $\overline{\text{INTER}}$ | AG14 | I | LVTTL | **Interrupt:** This active low input signal is used by the dual port SRAM to indicate a change in the host to ASPEN device status bits. |
| $\overline{\text{HBUSY}}$ | AH13 | I | LVTTL | **Host Busy:** This active low input signal will cause the ASPEN device to insert wait states during read or write cycles of the dual port SRAM. It is an indication that the host is simultaneously accessing the same address. This is not applicable when both are performing reads. |

### BOUNDARY SCAN AND OTHER TEST LEADS

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| TDO | G05 | O (T) | CMOS<br>2 mA | **Test Data Output:** Boundary scan output for data and test instructions from internal test registers. |
| $\overline{\text{TRS}}$ | E04 | I | LVTTLp | **Test Mode Reset:** A 1 microsecond (minimum) low on this lead resets the boundary scan; recommended for use after power-up initialization as well. |
| TMS | D03 | I | LVTTLp | **Test Mode Select:** Boundary scan test mode select. |
| TDI | D02 | I | LVTTLp | **Test Data Input:** Boundary scan input for data and test instructions. |

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| TCK | E03 | I | LVTTLp | **Test Clock:** Boundary scan clock. Input signals are clocked in on its rising edge. |
| IPRT(0-2) | F04<br>G04<br>F05 | O (T) | CMOS<br>4mA | **Inlet Processor Real-time Trace:** These leads indicate changes in the inlet processor program counter on a cycle by cycle basis. Used in conjunction with serial event history port to give real-time view into internal system. This lead is intended only for use by the manufacturer. |
| OPRT(0-2) | F03<br>G03<br>H05 | O (T) | CMOS<br>4mA | **Outlet Processor Real-time Trace:** These leads indicate changes in the outlet processor program counter on a cycle by cycle basis. This lead is intended only for use by the manufacturer. |
| RPRT(0-2) | E02<br>F02<br>F01 | O (T) | CMOS<br>4mA | **Rate Processor Real-time Trace:** These leads indicate changes in the rate processor program counter on a cycle by cycle basis. This lead is intended only for use by the manufacturer. |
| EPC | J02 | O (T) | CMOS<br>8mA | **Event History Port Clock:** Output clock used to drive out the contents of the internal event history buffer. This lead is intended only for use by the manufacturer. |
| EPD(0-3) | K03<br>J03<br>K04<br>J04 | O (T) | CMOS<br>4mA | **Event History Port Data:** Output data from the internal event history buffer. This lead is intended only for use by the manufacturer. |
| EPE | H03 | O (T) | CMOS<br>4mA | **Event History Port Enable:** Active high output signal indicates that valid data is being transferred from the internal event history buffer. This lead is intended only for use by the manufacturer. |
| IP(0-1) | H02<br>G02 | O (T) | CMOS<br>4mA | **Inlet Processor Status:** 2-bit status controlled through the timer coprocessor interface. |
| OP(0-1) | AH24<br>AF23 | O (T) | CMOS<br>4mA | **Outlet Processor Status:** 2-bit status controlled through the timer coprocessor interface. |
| RP0 | L28 | O (T) | CMOS<br>4mA | **Rate Processor Status:** 1-bit status controlled through the timer coprocessor interface. |
| ASPEN_<br>BOOTED | J25 | O (T) | CMOS<br>4mA | **ASPEN Booted:** When high, this lead indicates that the operational firmware is loaded. When this lead is low, it indicates that the operational firmware is not loaded. |
| BRK | J05 | O (T) | CMOS<br>4mA | **Breakpoint Encountered:** Active high signal indicating a debug breakpoint was encountered, or a toggle-based signal indicating an exception was encountered. This lead is intended only for use by the manufacturer. |

### SERIAL EEPROM INTERFACE PORT

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| SCK | AF03 | O (T) | CMOS 8 mA | **Serial EEPROM Clock:** This clock lead is used for the serial EEPROM interface. |
| $\overline{SCS}$ | AE03 | O (T) | CMOS 8 mA | **Serial EEPROM Chip Select:** Chip select lead for the serial EEPROM interface. |
| SDIO | AF02 | I/O (T) | LVTTL/ CMOS 8mA | **Serial EEPROM Address Output/Data Input:** Address and Data lead for the serial EEPROM interface. |

### STRAPS

| Symbol | Lead No. | I/O/P | Type | Name/Function |
|---|---|---|---|---|
| $\overline{ENARBA}$ | L04 | I | LVTTLp | **Enable Arbiter *CellBus* A:** Active low signal to enable Bus Arbiter and Frame Pulse Generator for *CellBus* A. |
| $\overline{ENARBB}$ | M05 | I | LVTTLp | **Enable Arbiter *CellBus* B:** Active low signal to enable Bus Arbiter and Frame Pulse Generator for *CellBus* B. |
| $\overline{UA(0\text{-}4)}$ | M04<br>N05<br>K02<br>M03<br>N04 | I | LVTTLp | **Unit Address:** Five active low device identity straps, used to identify each *CellBus* device in a system containing up to 32 devices (binary numbers from 0 to 31, $\overline{UA4}$ is MSB). This unit address may be overridden through a host command that writes a different unit address value to the corresponding UA bits in RP configuration register 0/6/2. |
| $\overline{HZEN}$ | L02 | I | LVTTL | **High Impedance Enable:** Active low signal that causes all tristateable output leads to assume the tristate condition, including input/output leads functioning as outputs but excluding TDO.<br>**Note:** This input lead **must** be connected to an external pullup resistor, powered by VDD3, that will maintain a logic 1 level at this lead. |

## ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

| Parameter | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Supply voltage (I/O) | $V_{DD3}$ | -0.3 | +3.9 | V | Note 1 |
| Supply voltage (Core) | $V_{DD2.5}$ | -0.3 | +3.1 | V | Note 1 |
| Supply voltage (PLLVDD) | $V_{PLL}$ | -0.3 | +3.1 | V | Note 1 |
| DC input voltage | $V_{IN}$ | -1.0 | $V_{DD3}$ + 0.3 | V | Note 1 |
| Storage temperature range | $T_S$ | -40 | 125 | $^oC$ | Note 1 |
| Ambient operating temperature | $T_A$ | -40 | 85 | $^oC$ | 0 ft/min linear airflow |
| Operating junction temperature | $T_J$ | -40 | 125 | $^oC$ | Note 1 |
| Moisture Exposure Level | ME | 5 | | Level | per EIA/JEDEC JESD22-A112-A |
| Relative Humidity, during assembly | RH | 30 | 60 | % | Note 2 |
| Relative Humidity, in-circuit | RH | 0 | 100 | % | non-condensing |
| ESD Classification | ESD | Absolute value 2000 | | V | Note 3 |
| Latch-up | LU | | | | Meets JEDEC STD-78 |

Notes:
1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, method 3015.7.



## THERMAL CHARACTERISTICS



| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Thermal Resistance - junction to ambient | $\theta_{JA}$ | | 13.0 | | $^oC/W$ | 0 ft/min airflow |
| Thermal Resistance - junction to case | $\theta_{JC}$ | | 5.3 | | $^oC/W$ | 0 ft/min airflow |

## POWER REQUIREMENTS

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{DD3}$ | 3.14 | 3.3 | 3.46 | V | Note 5 |
| $V_{DD2.5}$, $V_{PLL}$ (PLL voltage) | 2.375 | 2.5 | 2.625 | V | Note 5 |
| $I_{DD3}$ | | 130 | 150 | mA | Notes 1, 2, 3 |
| $I_{DD2.5}$, $I_{PLL}$ (PLL current) | | 670 | 700 | mA | Notes 1, 2, 3 |
| $V_{DDBOOT\ A,\ B}$ | 2.375 | 2.5 | 2.625 | V | |
| $I_{DDBOOT\ A,\ B}$ | | 0.01 | 0.02 | mA | |
| $P_{DD\ (Total)}$ | | 2.10 | 2.35 | W | Notes 1, 2, 3, 4 |

Notes:
1. With inputs switching and output load of 25 pF.
2. All $I_{DD}$ and $P_{DD}$ values are dependent upon $V_{DD}$ and the bus operation.
3. Conditions: SSRAM = 100 MHz, UTOPIA = 25 MHz, *CellBus* A = 40 MHz, *CellBus* B = 40 MHz, PCLK = 50 MHz (internal system clock = 100 MHz).
4. Maximum power is at minimum operating temperature.
5. During power-up, I/O Supply Voltage (VDD3) must lead the PLLVDD (2.5V) and the Core Supply Voltage (VDD2.5). After power-up, the I/O Supply Voltage must not go below the PLLVDD and the Core Supply Voltage by more than 0.5V at any time, including power-down.

## INPUT, OUTPUT, AND INPUT/OUTPUT PARAMETERS

### Input Parameters For CMOS2.5

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | 1.3 | | | V | $2.375 \leq V_{DD2.5} \leq 2.625$ |
| $V_{IL}$ | | | 0.9 | V | $2.375 \leq V_{DD2.5} \leq 2.625$ |
| Input leakage current | -10 | | 10 | µA | $V_{IN} = V_{DD2.5}$ or $V_{SS}$ |
| Input capacitance | | | 5 | pF | |

### Input Parameters For LVTTL

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | 2.0 | | | V | $3.14 \leq V_{DD3} \leq 3.46$ |
| $V_{IL}$ | | | 0.8 | V | $3.14 \leq V_{DD3} \leq 3.46$ |
| Input leakage current | -15 | | 15 | µA | $V_{IN} = V_{DD3}$ or $V_{SS}$ |
| Input capacitance | | | 6 | pF | |



### Input Parameters For LVTTLp (these leads have an internal pull-up resistor)



| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | 2.0 | | | V | $3.14 \leq V_{DD3} \leq 3.46$ |
| $V_{IL}$ | | | 0.8 | V | $3.14 \leq V_{DD3} \leq 3.46$ |
| Input current | -150 | -180 | -250 | µA | $V_{IN} = V_{SS}$ |
| Input leakage current | | | 15 | µA | $V_{IN} = V_{DD3}$ |
| Input capacitance | | | 6 | pF | |

### Input Parameters For LVTTLpd (these leads have an internal pull-down resistor)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | 2.0 | | | V | $3.14 \leq V_{DD3} \leq 3.46$ |
| $V_{IL}$ | | | 0.8 | V | $3.14 \leq V_{DD3} \leq 3.46$ |
| Input current | 80 | 117 | 180 | µA | $V_{IN} = V_{DD3}$ |
| Input leakage current | -15 | | | µA | $V_{IN} = V_{SS}$ |
| Input capacitance | | | 6 | pF | |

**Input and Input/Output Parameters For GTL+**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | $V_{REF}$+0.05 | | | V | |
| $V_{IL}$ | | | $V_{REF}$-0.05 | V | |
| Input leakage current | | | 10 | µA | |
| GTL+ lead capacitance | | | 6 | pF | |
| $V_{OL}$ | | | 0.5 | V | $I_{OL}$ = 48 mA |
| $I_{OL}$ | | | 48 | mA | Loaded with 21 Ω to +1.5 V |

**Output Parameters For CMOS 2mA**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -2 mA |
| $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 2 mA |
| $I_{OL}$ | | | 2.0 | mA | |
| $I_{OH}$ | | | -2.0 | mA | |
| Leakage Tristate | -10 | | 10 | µA | |

**Output Parameters For CMOS 4mA**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -4 mA |
| $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 4 mA |
| $I_{OL}$ | | | 4.0 | mA | |
| $I_{OH}$ | | | -4.0 | mA | |
| Leakage Tristate | -10 | | 10 | µA | |

**Output Parameters For CMOS 6mA**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -6 mA |
| $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 6 mA |
| $I_{OL}$ | | | 6.0 | mA | |
| $I_{OH}$ | | | -6.0 | mA | |
| Leakage Tristate | -10 | | 10 | µA | |

**Output Parameters For CMOS 8mA**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -8 mA |
| $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 8 mA |
| $I_{OL}$ | | | 8.0 | mA | |
| $I_{OH}$ | | | -8.0 | mA | |
| Leakage Tristate | -10 | | 10 | µA | |

**Output Parameters For CMOS 12mA**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 12 mA |
| $I_{OL}$ | | | 12.0 | mA | |
| $I_{OH}$ | | | -12.0 | mA | |
| Leakage Tristate | -10 | | 10 | µA | |



**Input/Output Parameters For LVTTL/CMOS 8mA**



| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | 2.0 | | | V | $3.14 \le V_{DD3} \le 3.46$ |
| $V_{IL}$ | | | 0.8 | V | $3.14 \le V_{DD3} \le 3.46$ |
| Input leakage current | | | 10 | µA | $V_{DD3}$ = 3.46 |
| Input capacitance | | 9 | | pF | |
| $V_{OH}$ | 2.4 | | | V | $V_{DD3}$= 3.14; $I_{OH}$ = -8 mA |
| $V_{OL}$ | | | 0.4 | V | $V_{DD3}$= 3.14; $I_{OL}$ = 8 mA |
| $I_{OL}$ | | | 8.0 | mA | |
| $I_{OH}$ | | | -8.0 | mA | |

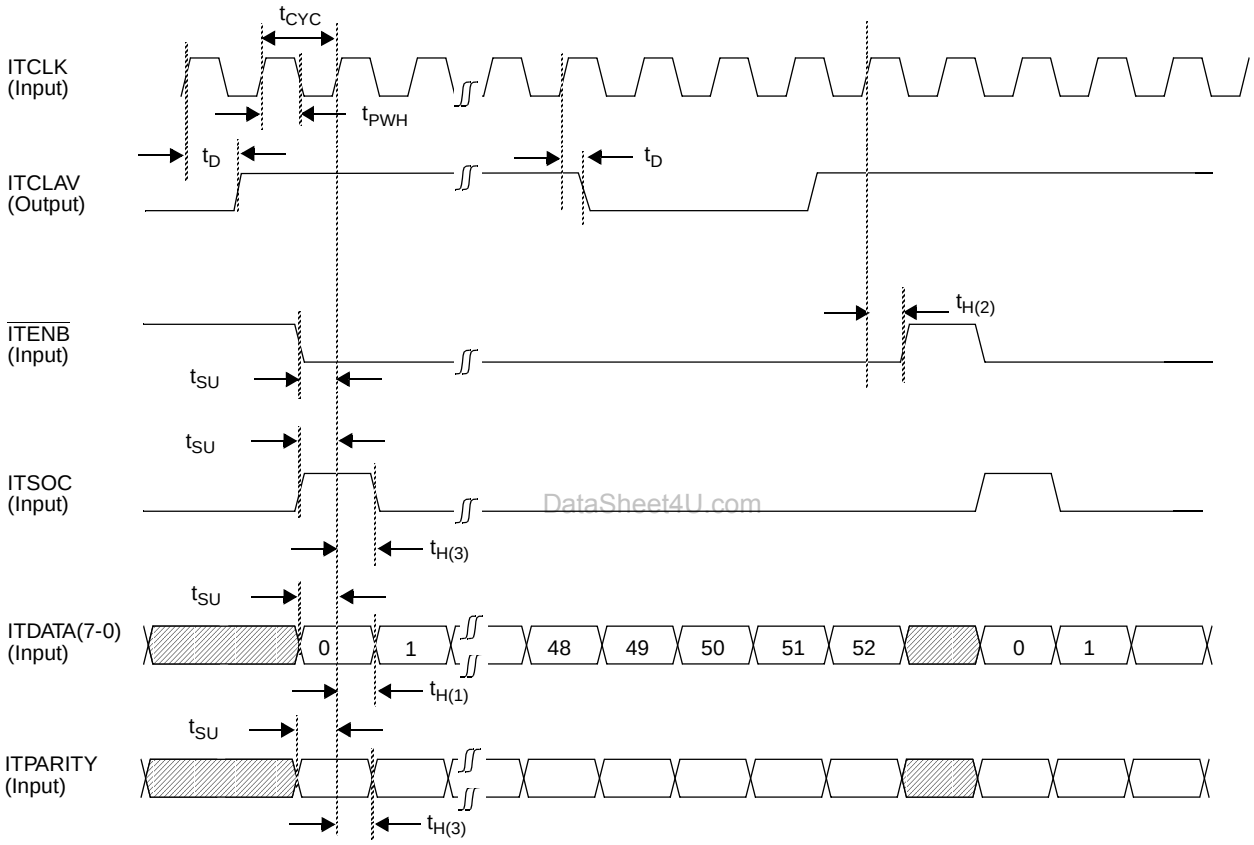
**Input/Output Parameters For LVTTL/CMOS 12mA**

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | 2.0 | | | V | $3.14 \le V_{DD3} \le 3.46$ |
| $V_{IL}$ | | | 0.8 | V | $3.14 \le V_{DD3} \le 3.46$ |
| Input leakage current | | | 10 | µA | $V_{DD3}$ = 3.46 |
| Input capacitance | | 6 | | pF | |
| $V_{OH}$ | 2.4 | | | V | $V_{DD3}$= 3.14; $I_{OH}$ = -12 mA |
| $V_{OL}$ | | | 0.4 | V | $V_{DD3}$= 3.14; $I_{OL}$ = 12 mA |
| $I_{OL}$ | | | 12.0 | mA | |
| $I_{OH}$ | | | -12.0 | mA | |

## TIMING CHARACTERISTICS

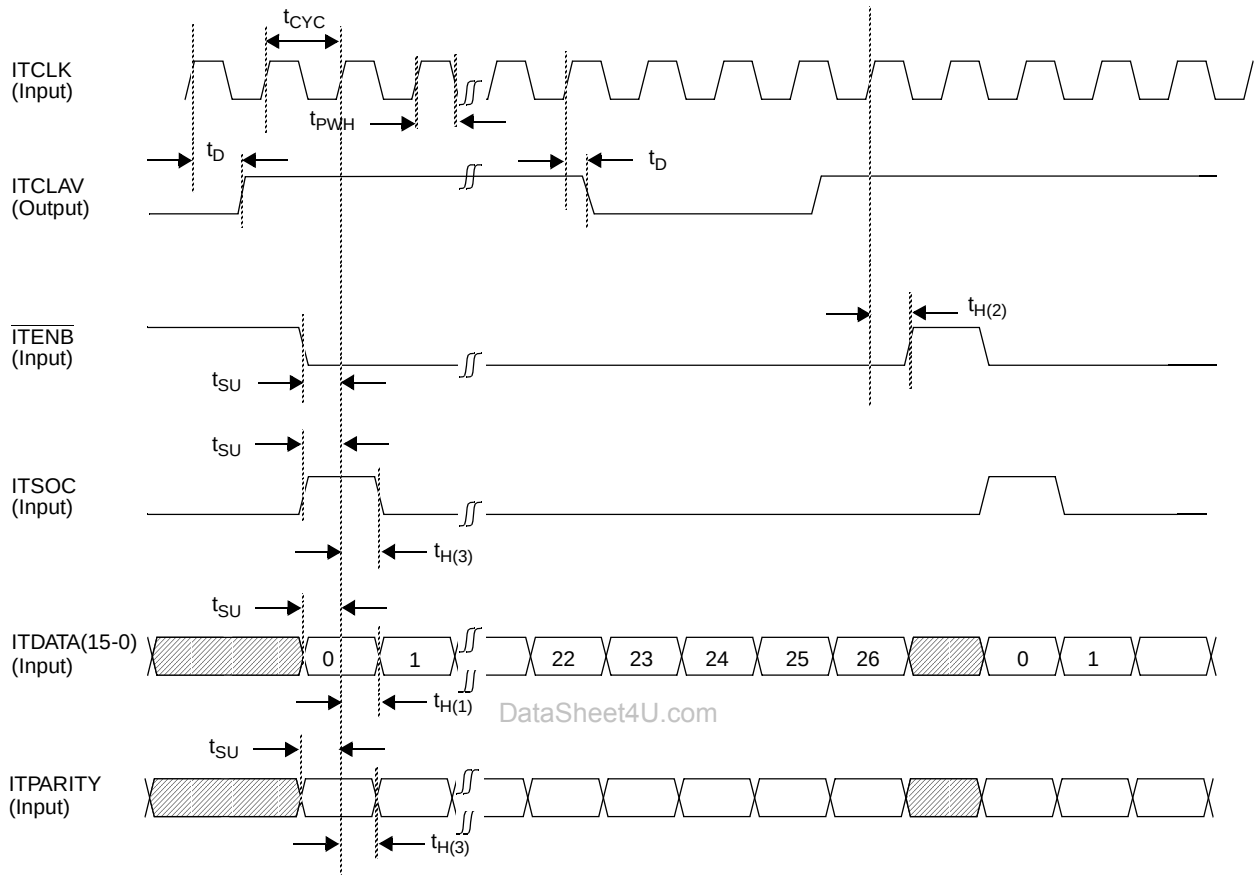
Detailed timing diagrams for the ASPEN device are provided in Figures 23 through 67, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum 25 pF load capacitance, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ and $(V_{OH}+V_{OL})/2$, for input and output signals, respectively.

**Figure 23. Timing of Receive Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 8-bit)**



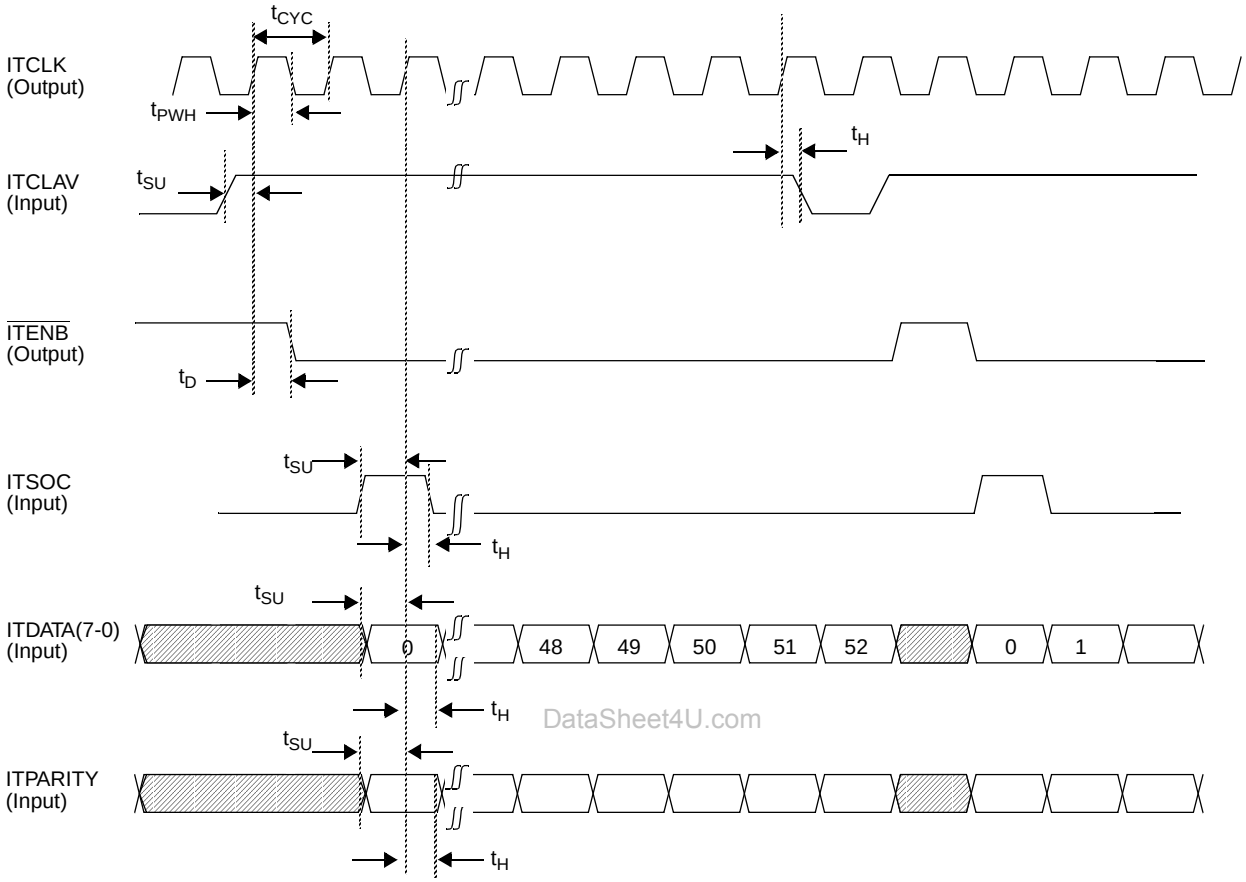

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(7-0), ITSOC, $\overline{\text{ITENB}}$, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(7-0) hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| $\overline{\text{ITENB}}$ hold time after ITCLK↑ | $t_{H(2)}$ | 1.5 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |
| ITSOC, ITPARITY hold time after ITCLK↑ | $t_{H(3)}$ | 2.0 | | | ns |

**Figure 24. Timing of Receive Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(15-0), ITSOC, $\overline{\text{ITENB}}$, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(15-0) hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| $\overline{\text{ITENB}}$ hold time after ITCLK↑ | $t_{H(2)}$ | 1.5 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |
| ITSOC, ITPARITY hold time after ITCLK↑ | $t_{H(3)}$ | 2.0 | | | ns |

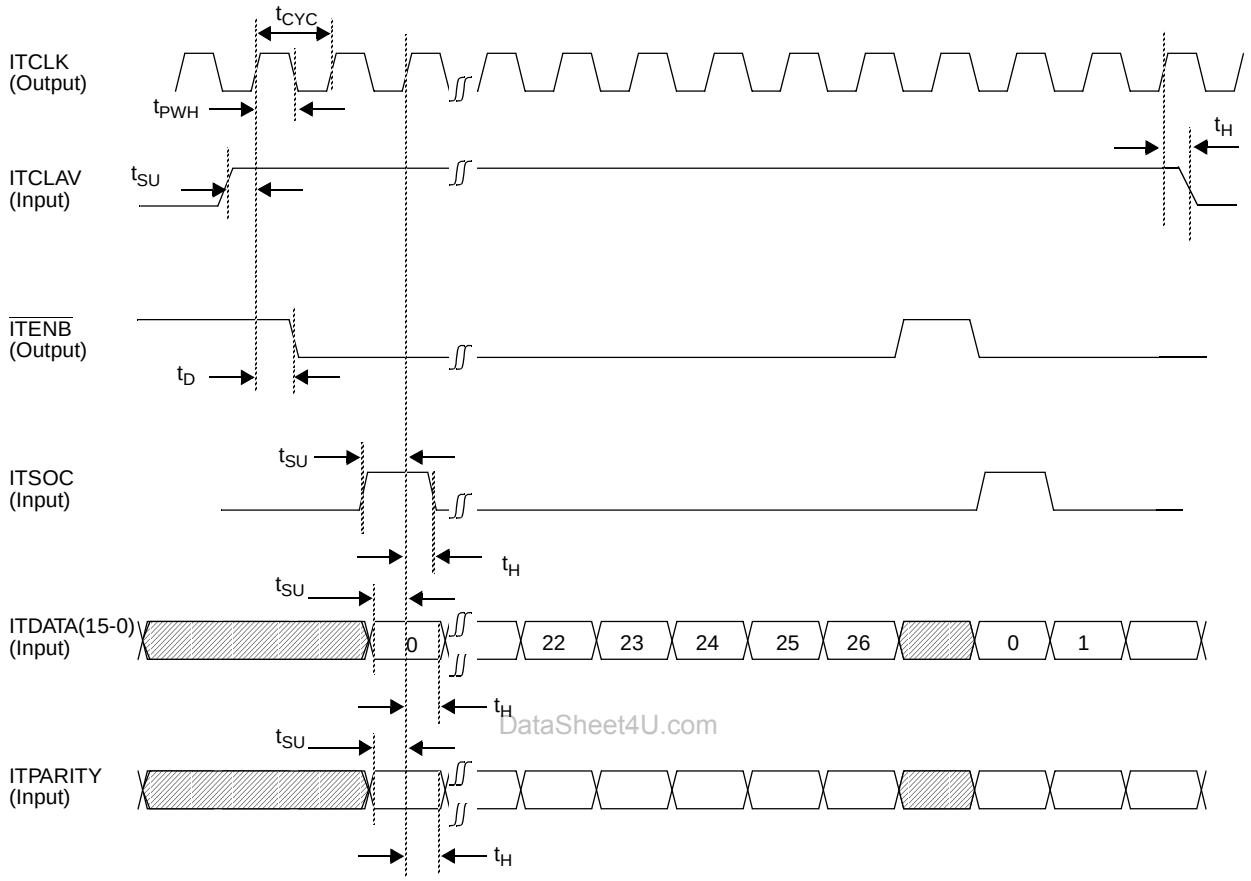
**Figure 25. Timing of Receive Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 8-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA (7-0), ITSOC, ITCLAV, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 6.0 | | | ns |
| ITDATA (7-0), ITSOC, ITCLAV, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| $\overline{\text{ITENB}}$ delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

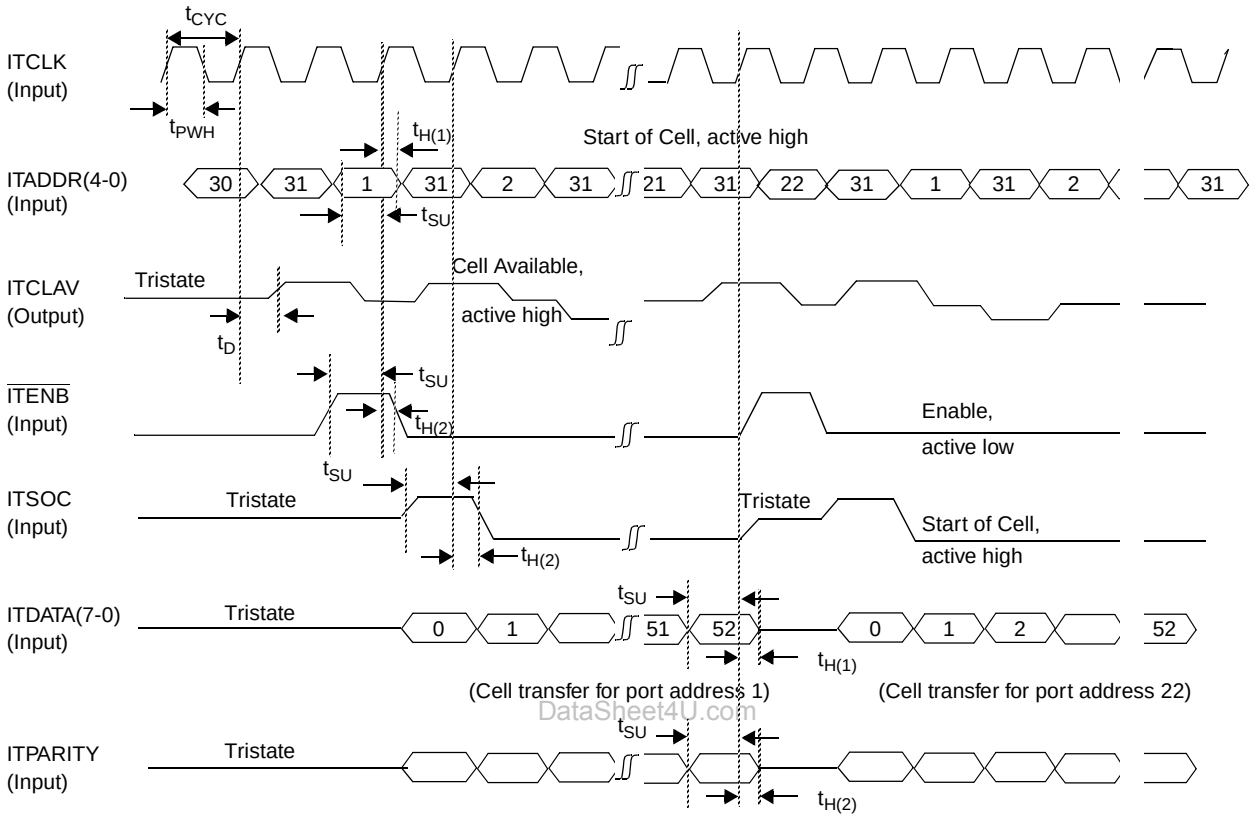
**Figure 26. Timing of Receive Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(15-0), ITSOC, ITCLAV, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 6.0 | | | ns |
| ITDATA(15-0), ITSOC, ITCLAV, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| $\overline{\text{ITENB}}$ delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

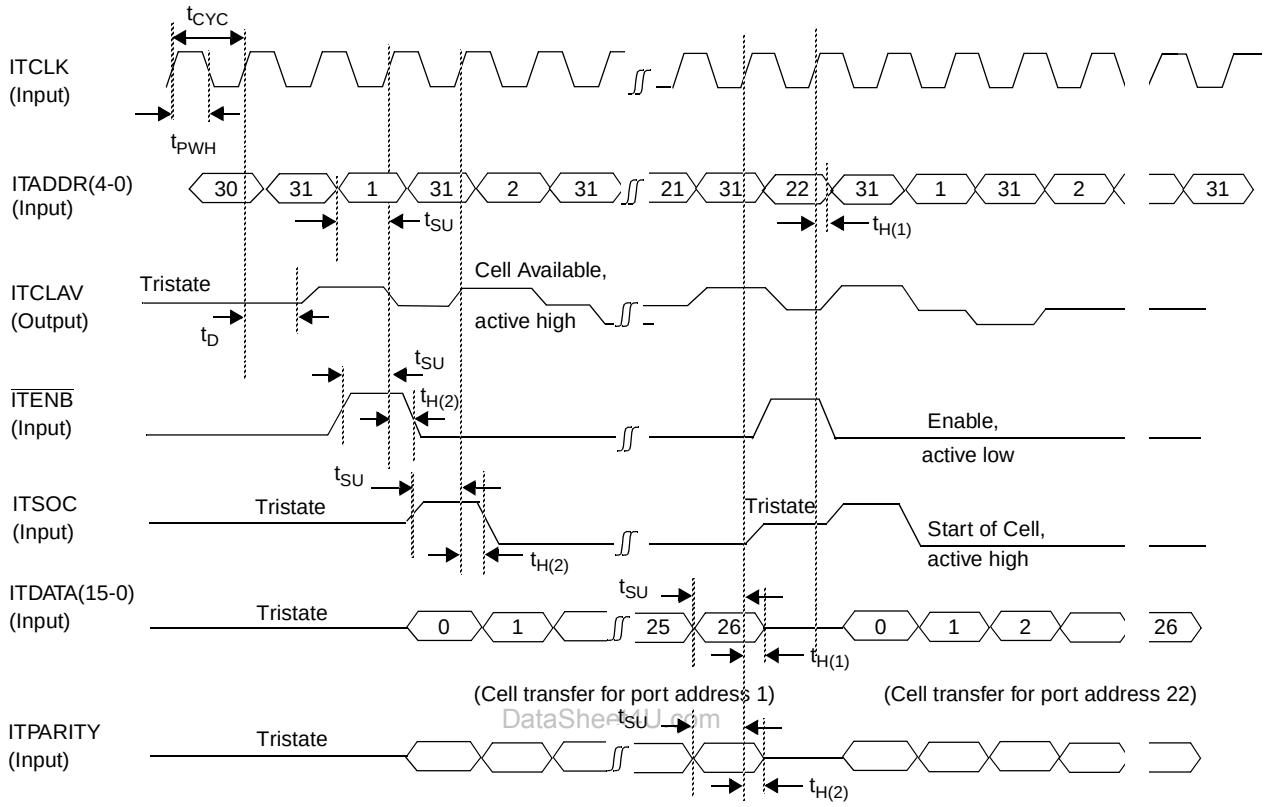
Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 27. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 8-bit)**



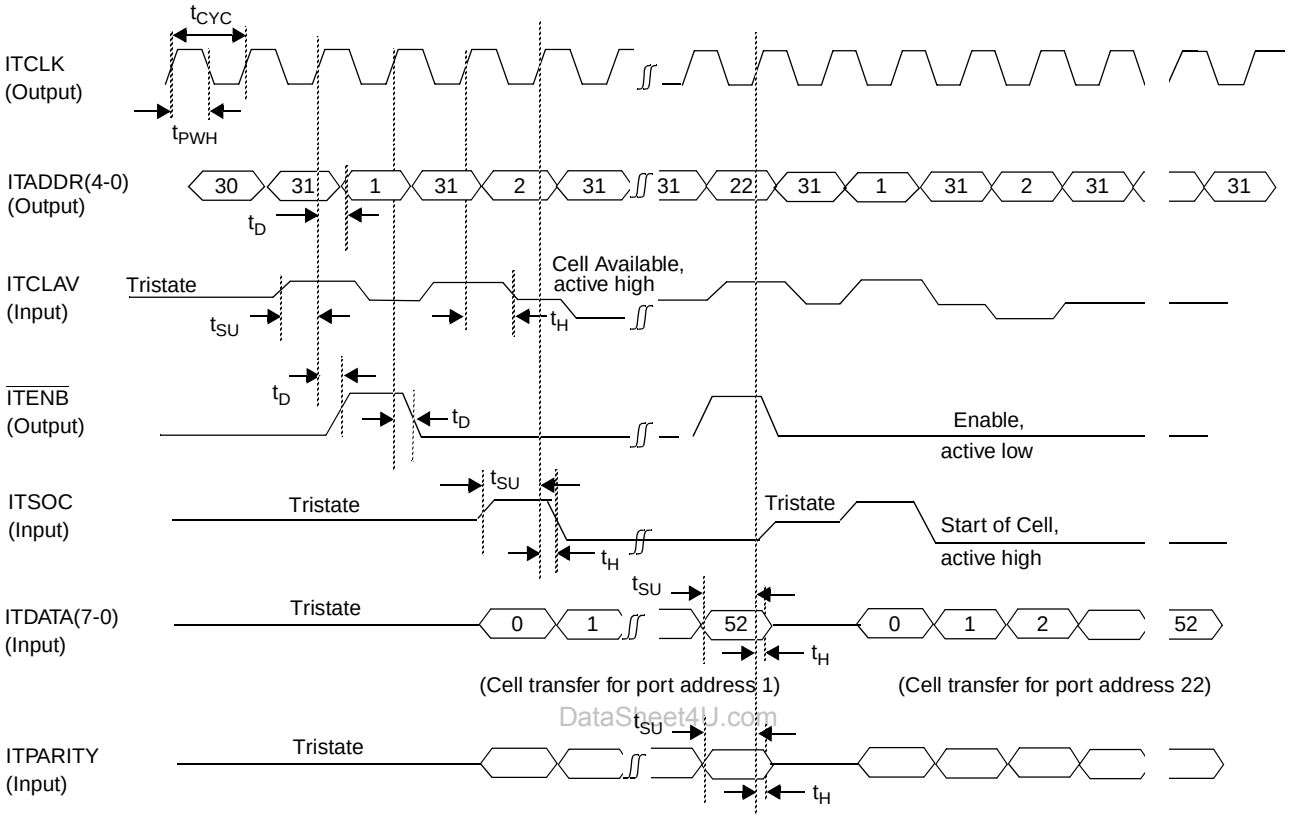

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(7-0), ITSOC, ITADDR(4-0), $\overline{\text{ITENB}}$, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(7-0), ITADDR(4-0) hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| ITSOC, $\overline{\text{ITENB}}$, ITPARITY hold time after ITCLK↑ | $t_{H(2)}$ | 2.0 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

**Figure 28. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(15-0), ITSOC, ITADDR(4-0), $\overline{\text{ITENB}}$, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(15-0), ITADDR(4-0) hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| ITSOC, $\overline{\text{ITENB}}$, ITPARITY hold time after ITCLK↑ | $t_{H(2)}$ | 2.0 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

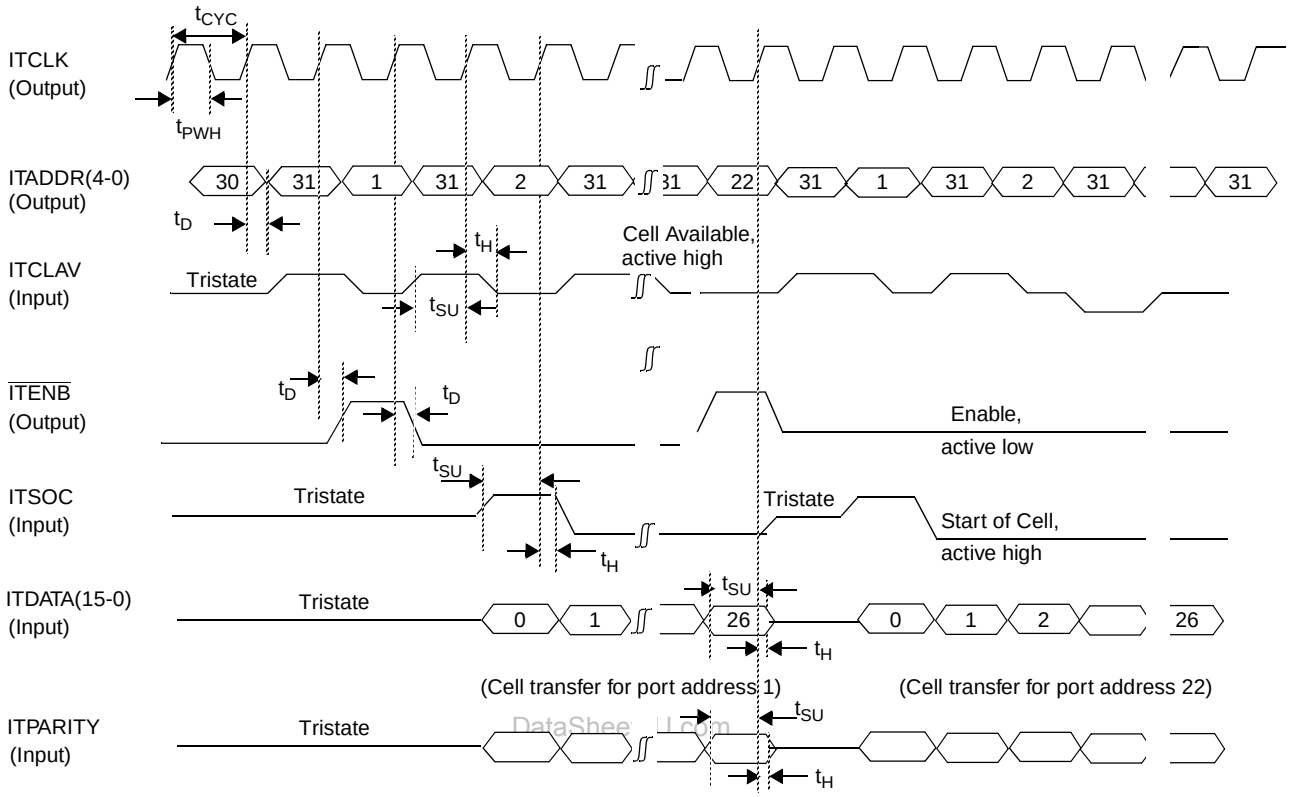
**Figure 29. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 8-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(7-0), ITSOC, ITCLAV, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 6.0 | | | ns |
| ITDATA(7-0), ITSOC, ITCLAV, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| ITADDR(4-0), $\overline{\text{ITENB}}$ delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 30. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(15-0), ITSOC, ITCLAV, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 6.0 | | | ns |
| ITDATA(15-0), ITSOC, ITCLAV, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| ITADDR(4-0), $\overline{\text{ITENB}}$ delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 31. Timing of Receive Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 8-bit)**

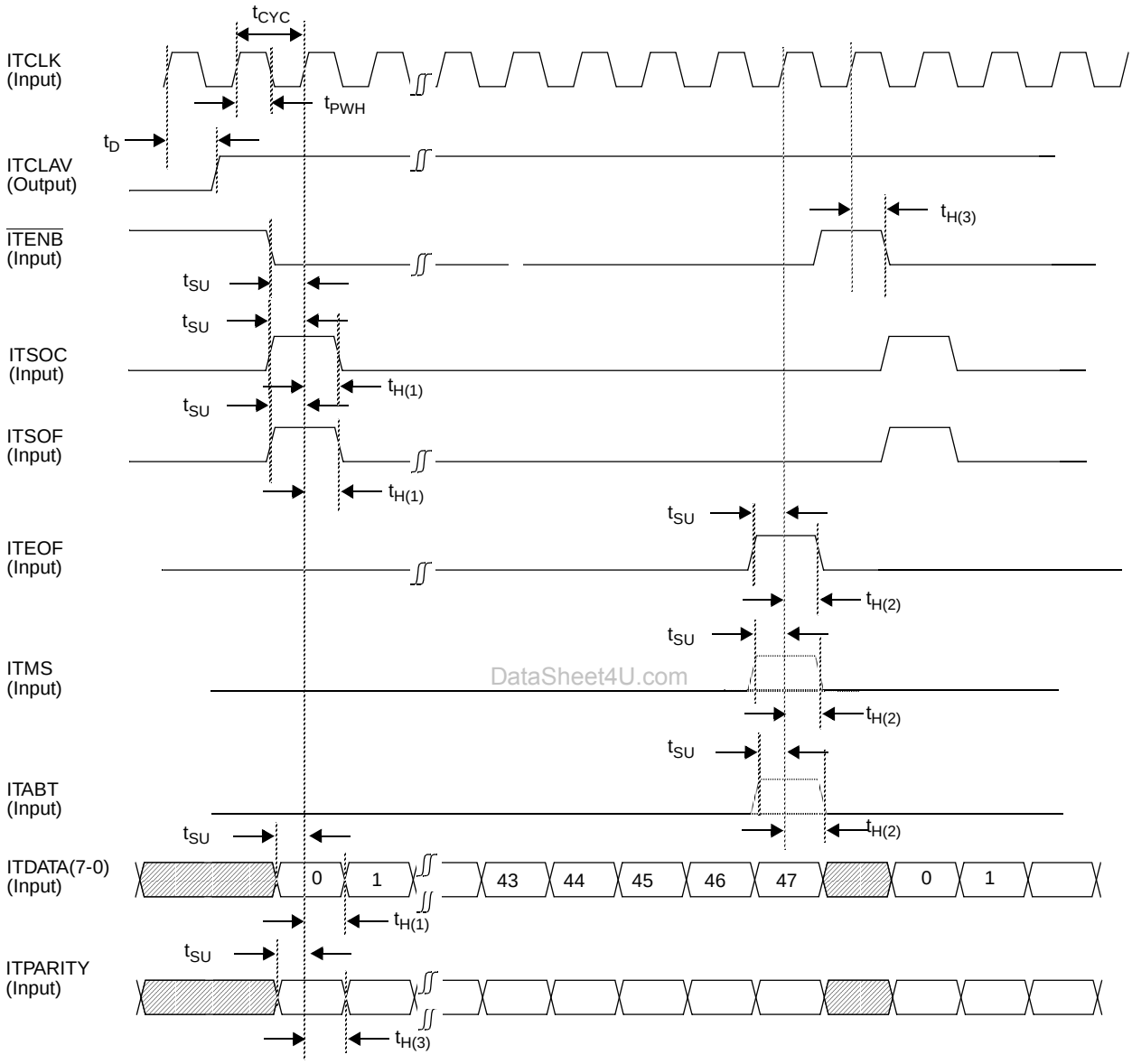


**Figure 31. Timing of Receive Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(7-0), ITSOF, ITSOC, ITEOF, $\overline{\text{ITENB}}$, ITMS, ITABT, ITPARITY setup to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(7-0), ITSOF, ITSOC, $\overline{\text{ITENB}}$ hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| ITEOF, ITMS, ITABT hold time after ITCLK↑ | $t_{H(2)}$ | 2.5 | | | ns |
| $\overline{\text{ITENB}}$, ITPARITY hold time after ITCLK↑ | $t_{H(3)}$ | 1.0 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

**Figure 32. Timing of Receive Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 16-bit)**

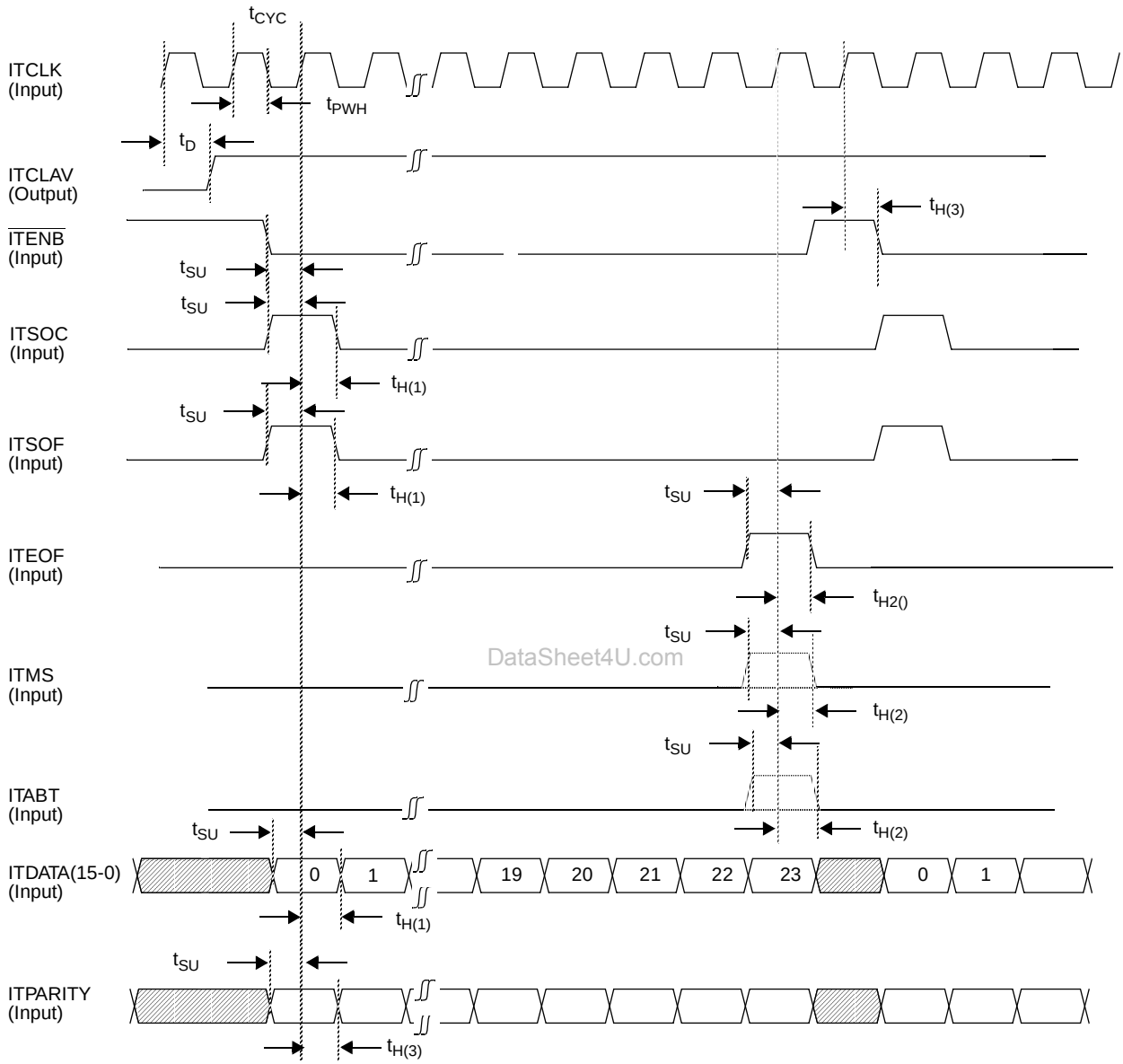


**Figure 32. Timing of Receive Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(15-0), ITSOF, ITSOC, ITEOF, ITABT, ITMS, $\overline{\text{ITENB}}$, ITPARITY setup to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(15-0), ITSOF, ITSOC hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| ITEOF, ITABT, ITMS hold time after ITCLK↑ | $t_{H(2)}$ | 2.5 | | | ns |
| $\overline{\text{ITENB}}$, ITPARITY hold time after ITCLK↑ | $t_{H(3)}$ | 2.0 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

**Figure 33. Timing of Receive Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 8-bit)**

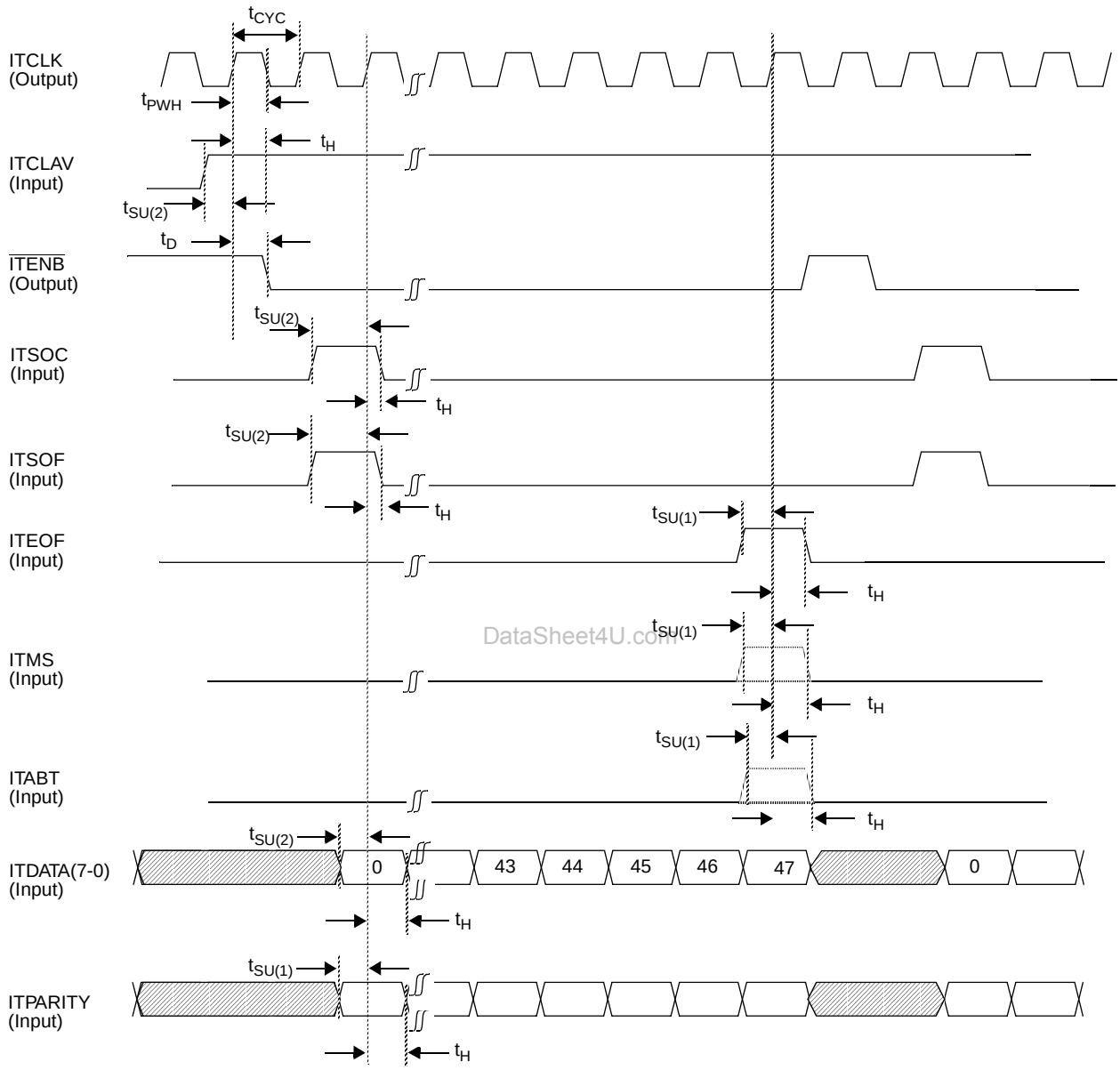


**Figure 33. Timing of Receive Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITEOF, ITMS, ITABT, ITPARITY setup time to ITCLK↑ | $t_{SU(1)}$ | 5.5 | | | ns |
| ITDATA(7-0), ITCLAV, ITSOF, ITSOC setup time to ITCLK↑ | $t_{SU(2)}$ | 6.0 | | | ns |
| ITDATA(7-0), ITSOF, ITSOC, ITEOF, ITMS, ITABT, ITCLAV, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| $\overline{\text{ITENB}}$ delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 34. Timing of Receive Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 16-bit)**

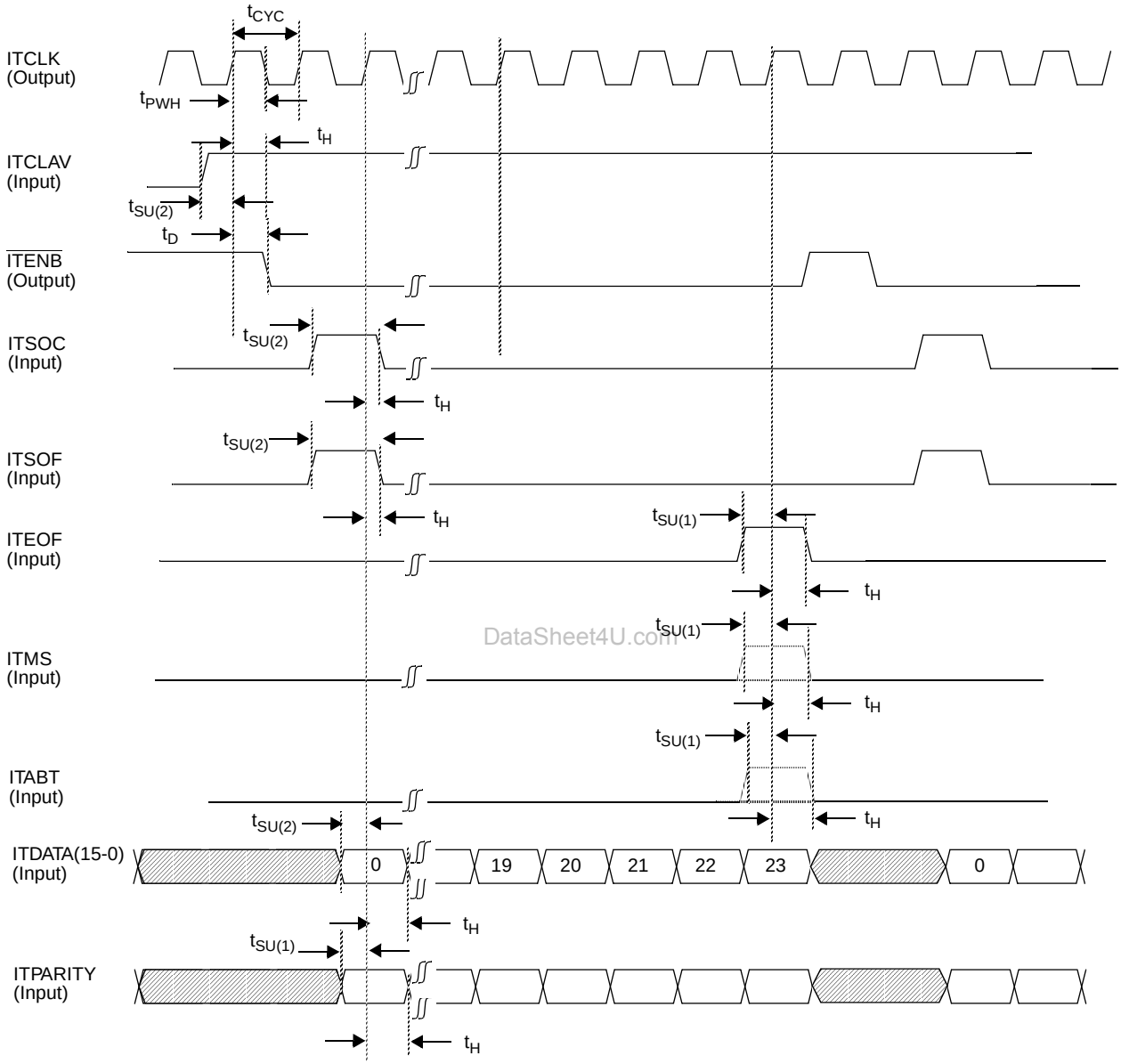


**Figure 34. Timing of Receive Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITEOF, ITMS, ITABT, ITPARITY setup time to ITCLK↑ | $t_{SU(1)}$ | 5.5 | | | ns |
| ITDATA(15-0), ITCLAV, ITSOF, ITSOC setup time to ITCLK↑ | $t_{SU(2)}$ | 6.0 | | | ns |
| ITDATA(15-0), ITSOF, ITSOC, ITEOF, ITMS, ITABT, ITCLAV, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| $\overline{\text{ITENB}}$ delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 35. Timing of Receive Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 8-bit)**

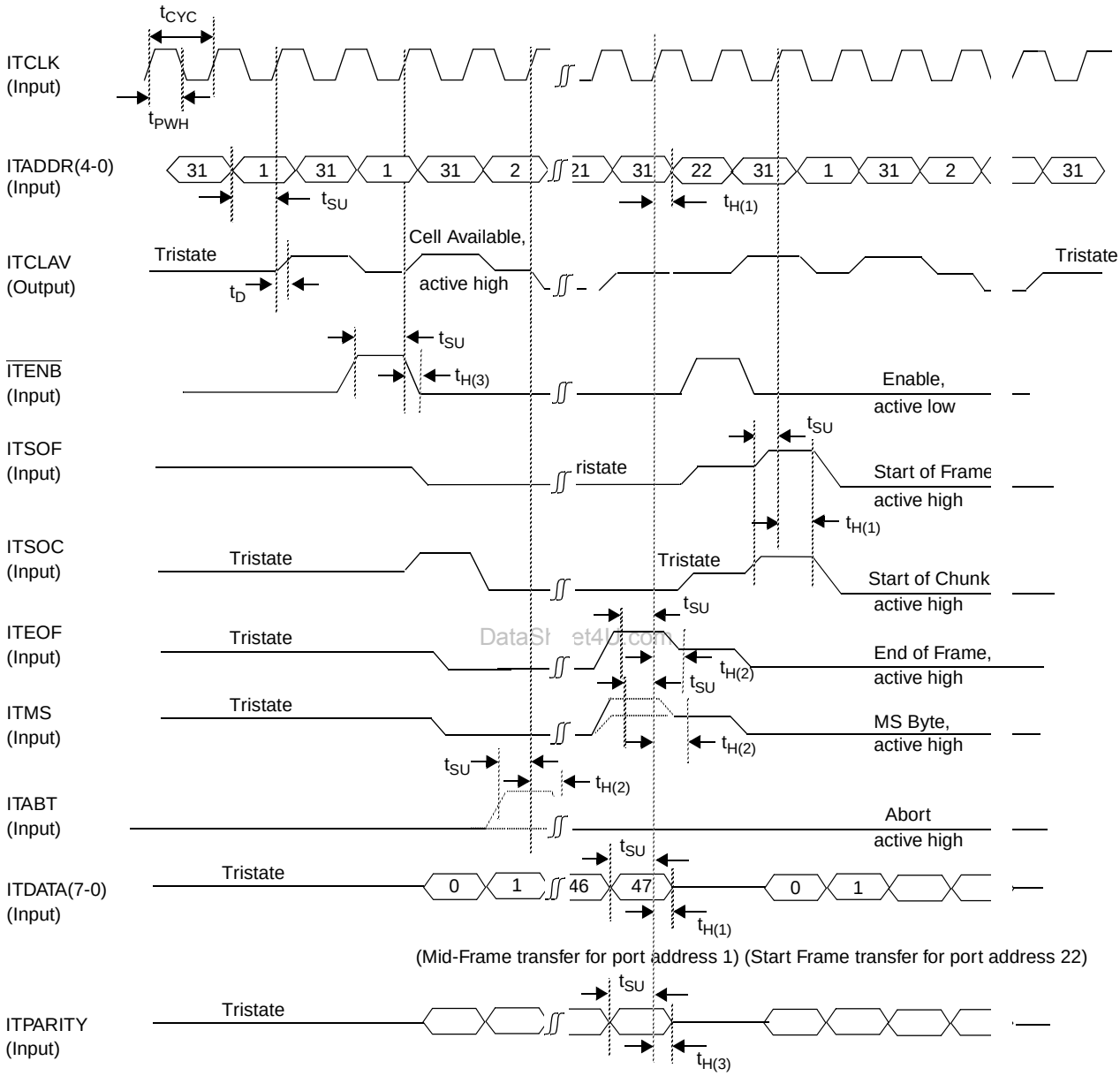


**Figure 35. Timing of Receive Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(7-0), ITSOF, ITSOC, ITEOF, ITMS, ITABT, ITADDR(4-0), $\overline{\text{ITENB}}$, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(7-0), ITSOF, ITSOC, ITADDR(4-0) hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| ITEOF, ITMS, ITABT hold time after ITCLK↑ | $t_{H(2)}$ | 2.5 | | | ns |
| $\overline{\text{ITENB}}$, ITPARITY hold time after ITCLK↑ | $t_{H(3)}$ | 1.5 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

**Figure 36. Timing of Receive Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 16-bit)**

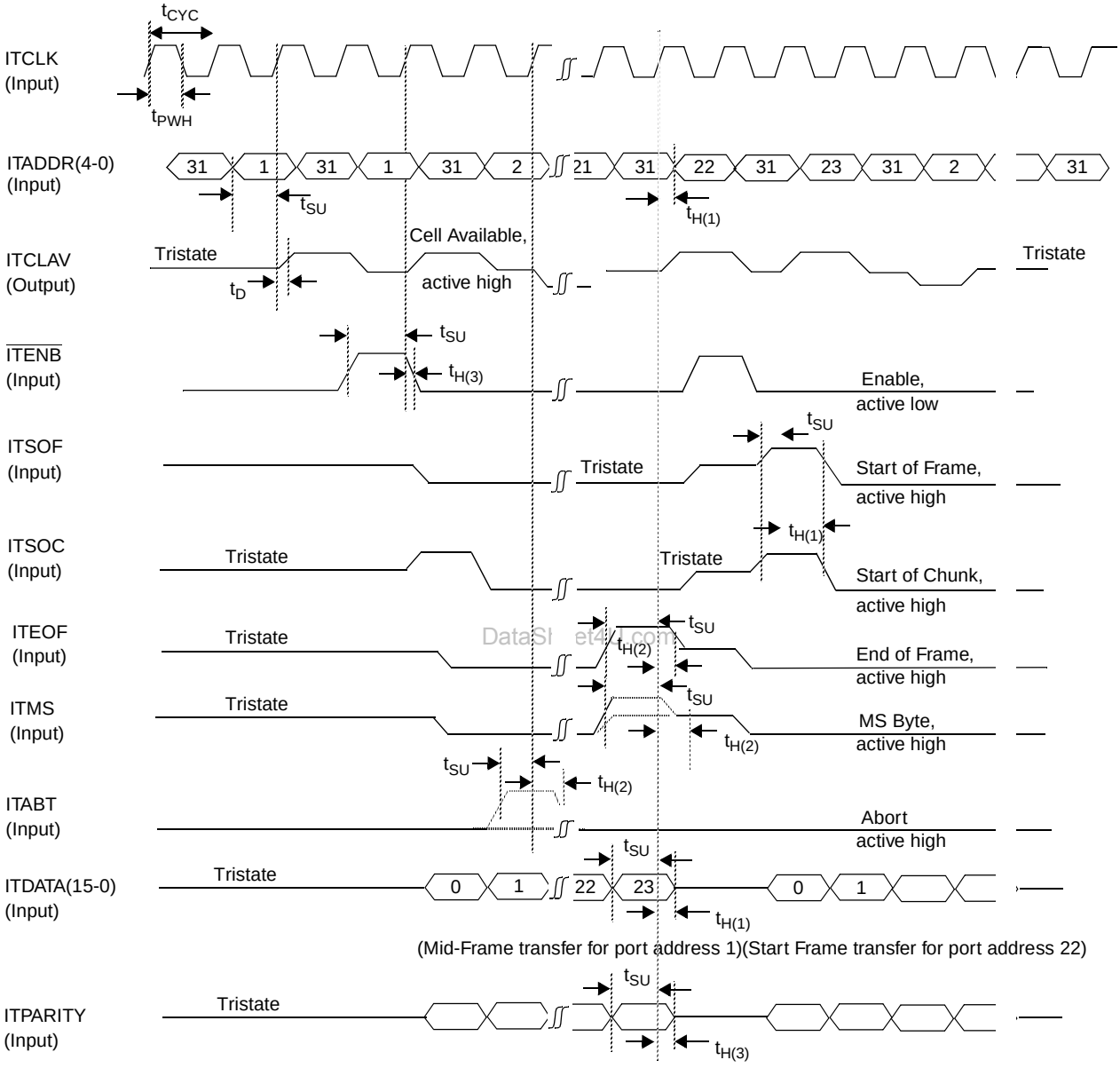


**Figure 36. Timing of Receive Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITDATA(15-0), ITSOF, ITSOC, ITEOF, ITMS, ITABT, ITADDR(4-0), $\overline{\text{ITENB}}$, ITPARITY setup time to ITCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| ITDATA(15-0), ITSOF, ITSOC, ITADDR(4-0) hold time after ITCLK↑ | $t_{H(1)}$ | 2.5 | | | ns |
| ITEOF, ITMS, ITABT hold time after ITCLK↑ | $t_{H(2)}$ | 2.5 | | | ns |
| $\overline{\text{ITENB}}$, ITPARITY hold time after ITCLK↑ | $t_{H(3)}$ | 1.5 | | | ns |
| ITCLAV delay from ITCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

**Figure 37. Timing of Receive Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 8-bit)**

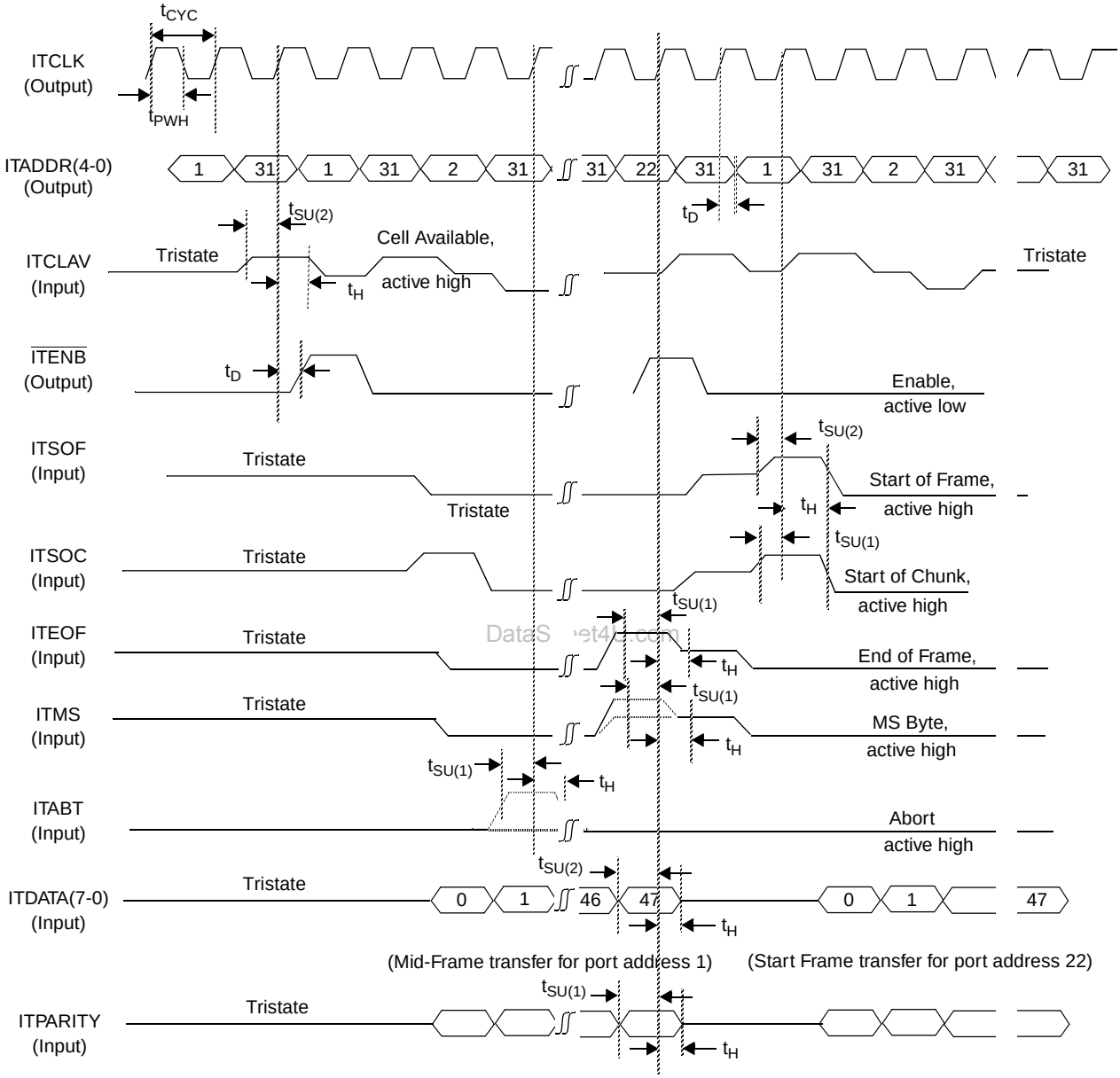


**Figure 37. Timing of Receive Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITEOF, ITMS, ITSOC, ITABT, ITPARITY setup time to ITCLK↑ | $t_{SU(1)}$ | 5.5 | | | ns |
| ITDATA(7-0), ITCLAV, ITSOF setup time to ITCLK↑ | $t_{SU(2)}$ | 6.0 | | | ns |
| ITDATA(7-0), ITSOF, ITEOF, ITCLAV, ITMS, ITSOC, ITABT, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| $\overline{\text{ITENB}}$, ITADDR(4-0) delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 38. Timing of Receive Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 16-bit)**

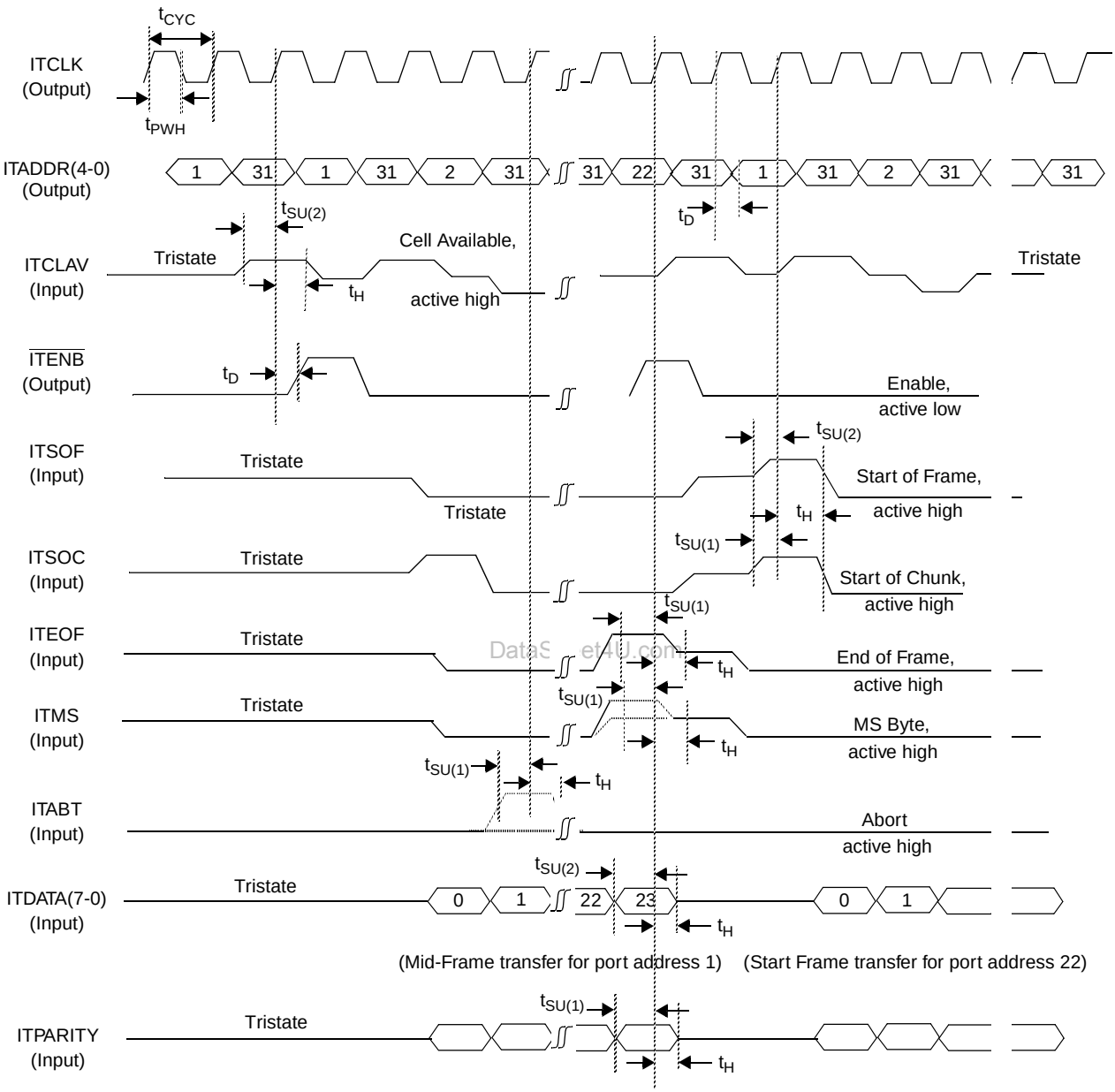
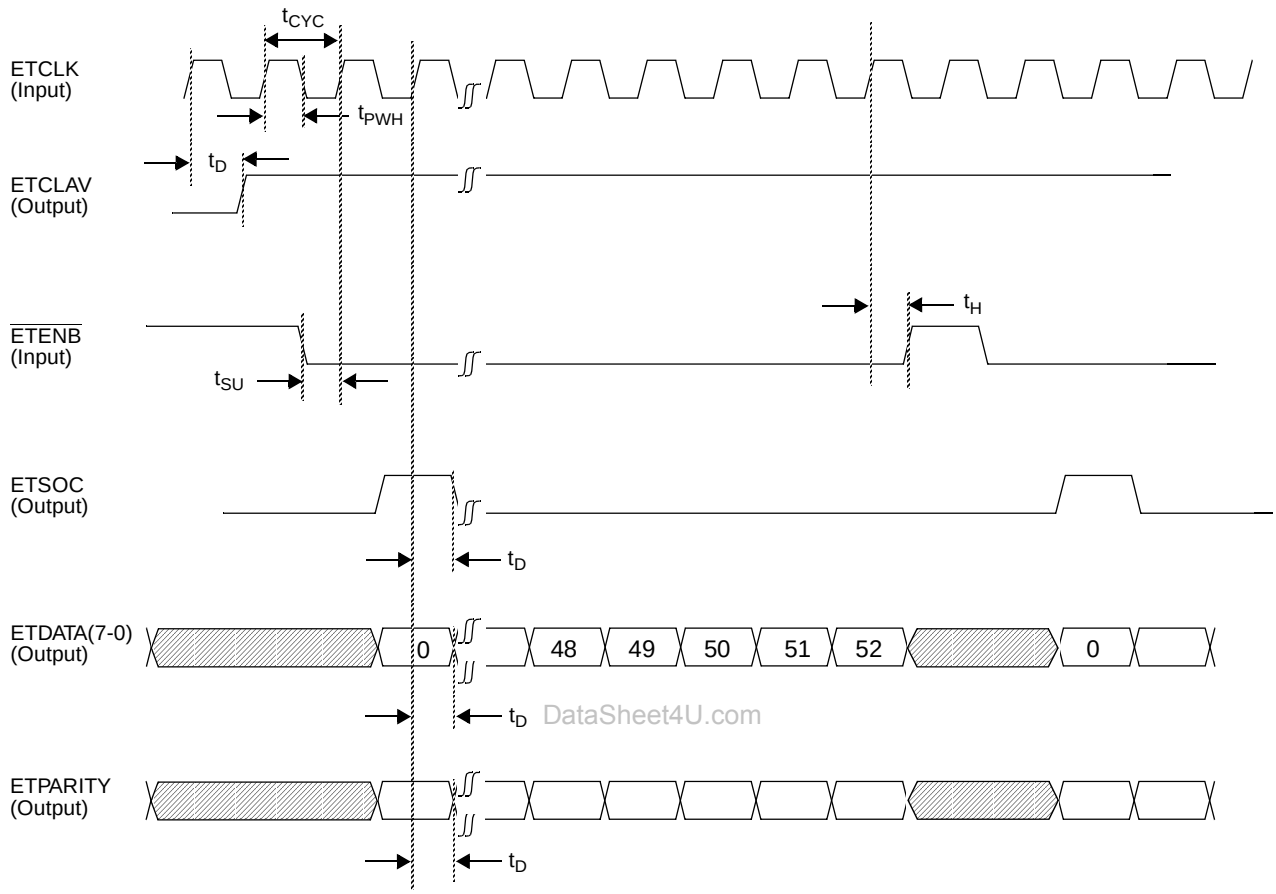


**Figure 38. Timing of Receive Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ITCLK clock period, UTCLKSRC = 00<br>ITCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ITCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ITEOF, ITMS, ITSOC, ITABT, ITPARITY setup time to ITCLK↑ | $t_{SU(1)}$ | 5.5 | | | ns |
| ITDATA(15-0), ITCLAV, ITSOF setup time to ITCLK↑ | $t_{SU(2)}$ | 6.0 | | | ns |
| ITDATA(15-0), ITSOF, ITEOF, ITCLAV, ITMS, ITSOC, ITABT, ITPARITY hold time after ITCLK↑ | $t_H$ | 1.0 | | | ns |
| $\overline{\text{ITENB}}$, ITADDR(4-0) delay from ITCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

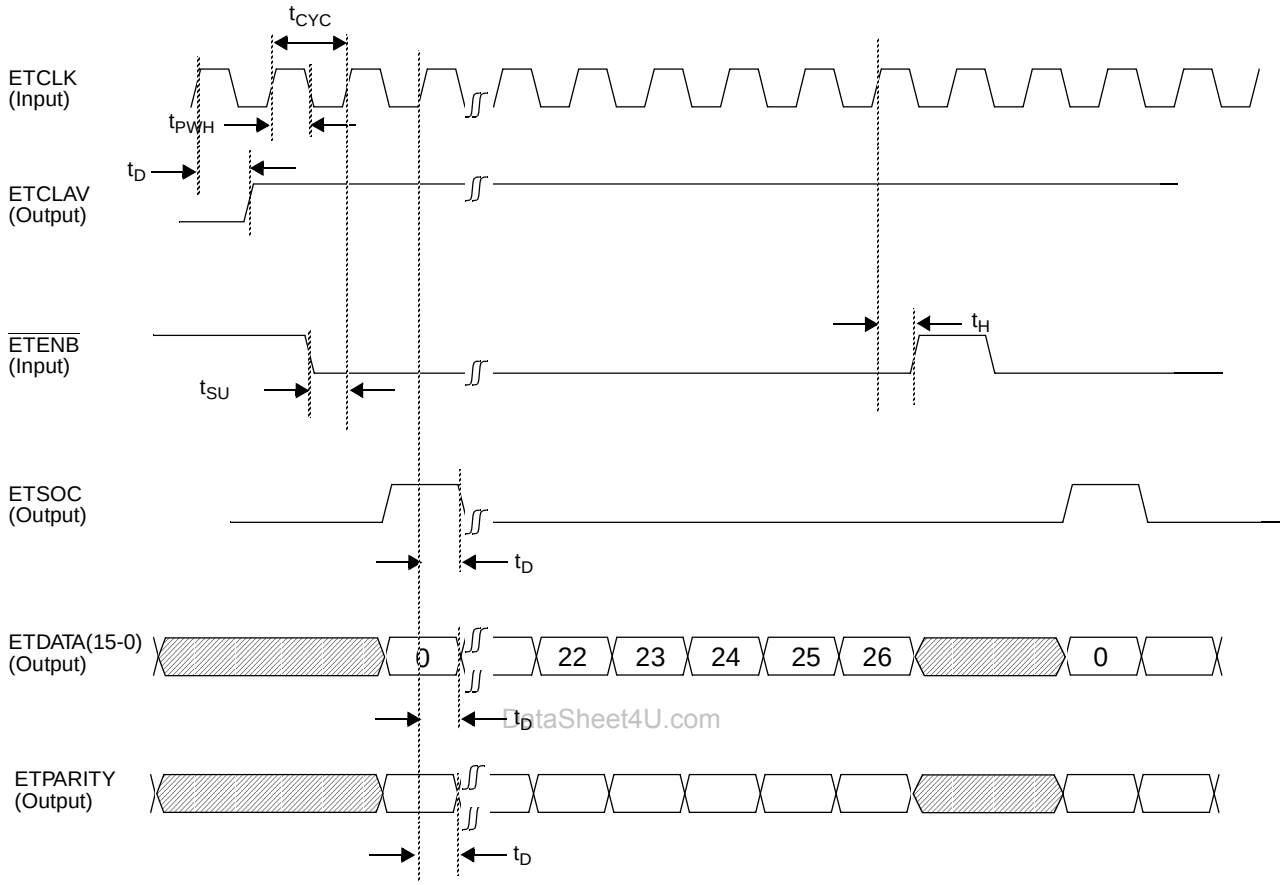
Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 39. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 8-bit)**



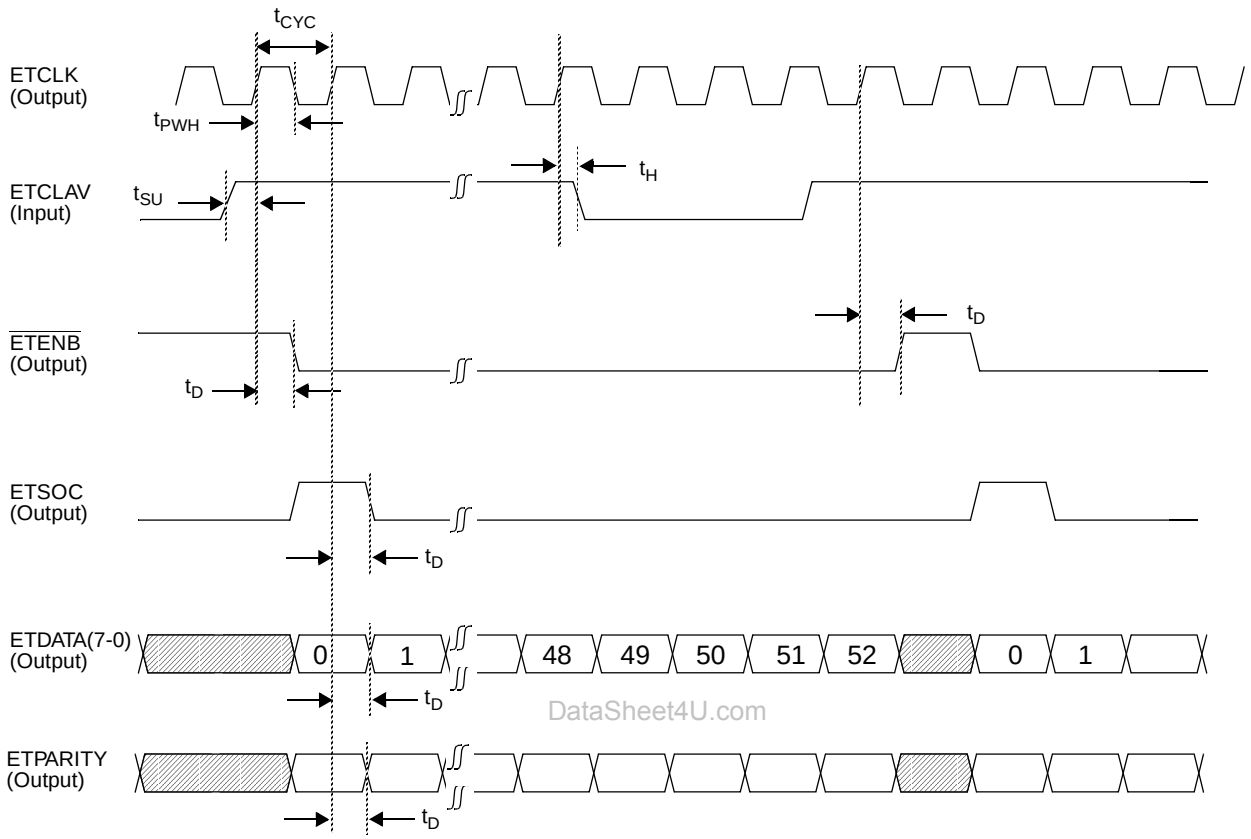

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{\text{ETENB}}$ setup time to ETCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| $\overline{\text{ETENB}}$ hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(7-0), ETSOC, ETCLAV, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.0 | ns |

**Figure 40. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{\text{ETENB}}$ setup time to ETCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| $\overline{\text{ETENB}}$ hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(15-0), ETSOC, ETCLAV, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.0 | ns |

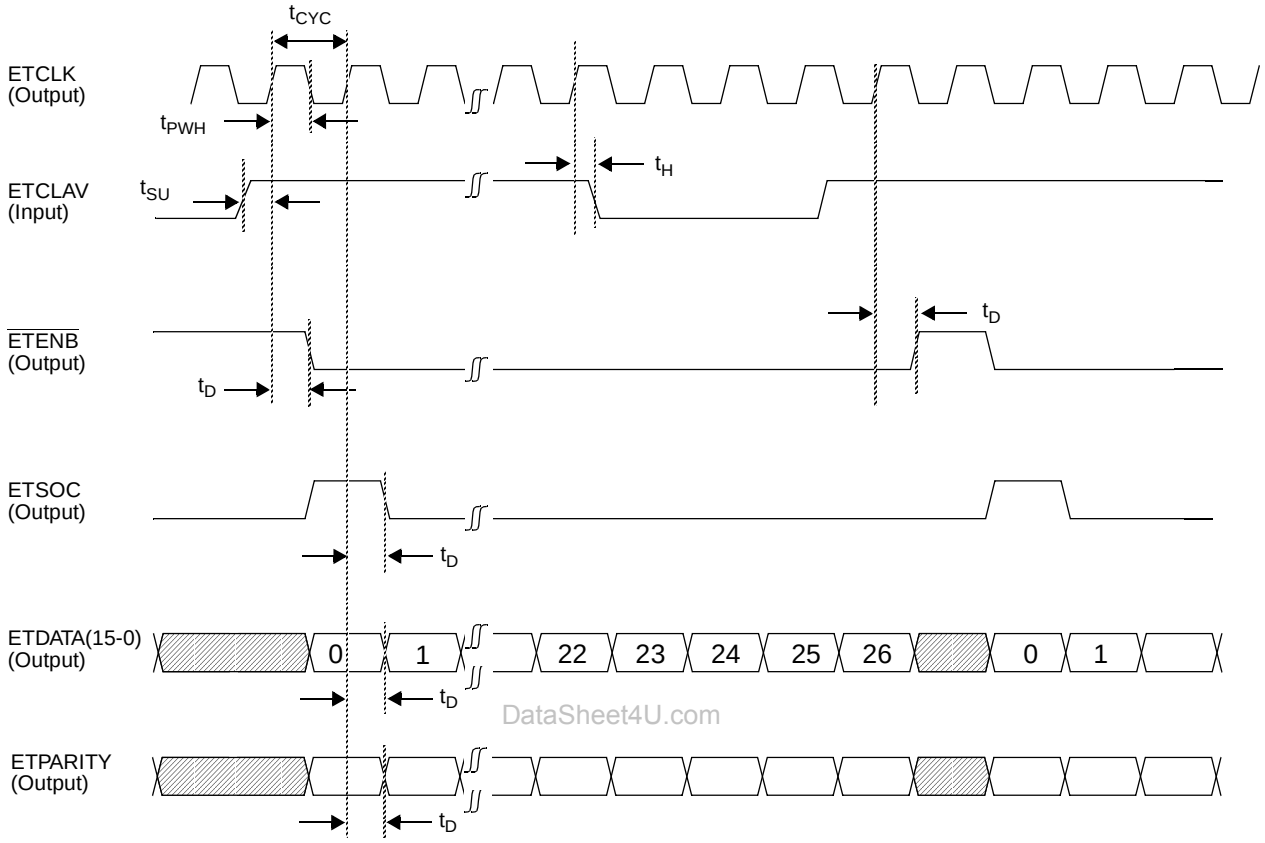
**Figure 41. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 8-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU}$ | 8.5 | | | ns |
| ETCLAV hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(7-0), ETSOC, $\overline{\text{ETENB}}$, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.0 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

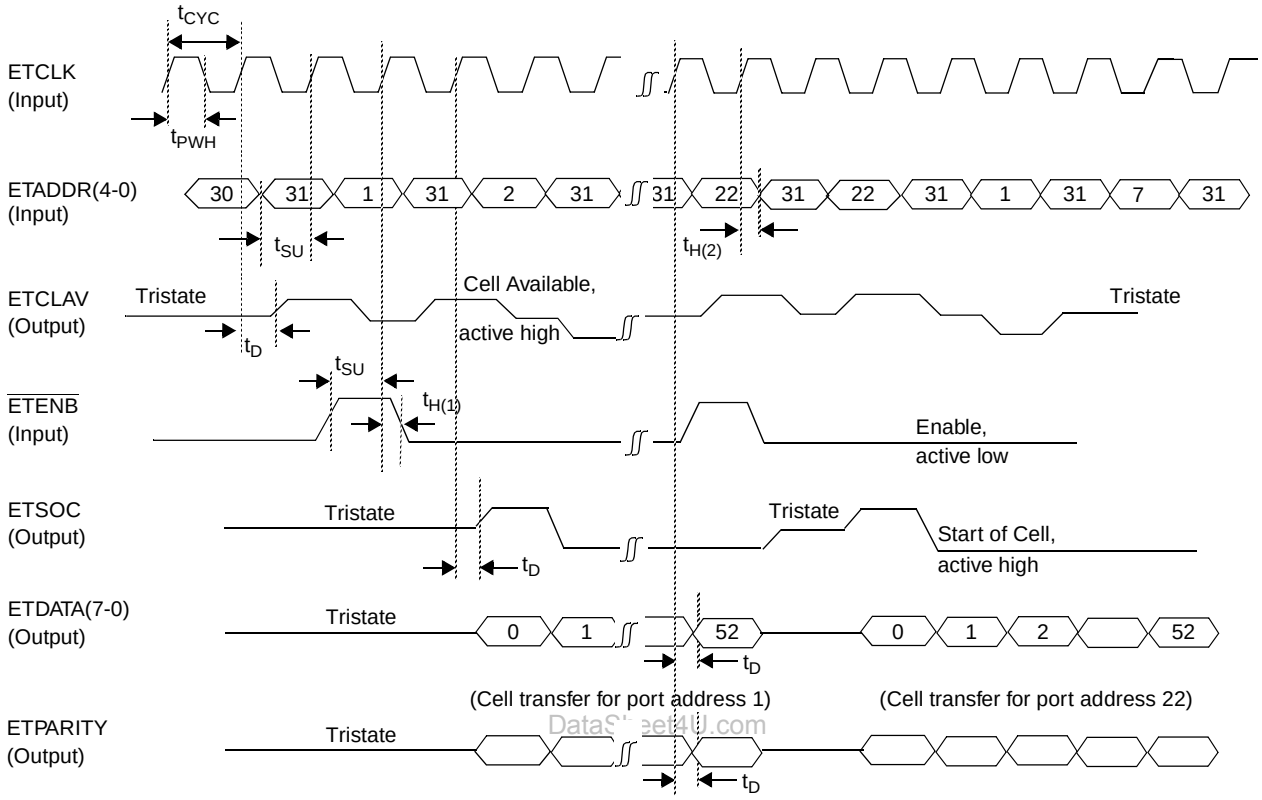
**Figure 42. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU}$ | 8.5 | | | ns |
| ETCLAV hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(15-0), ETSOC, $\overline{\text{ETENB}}$, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.0 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

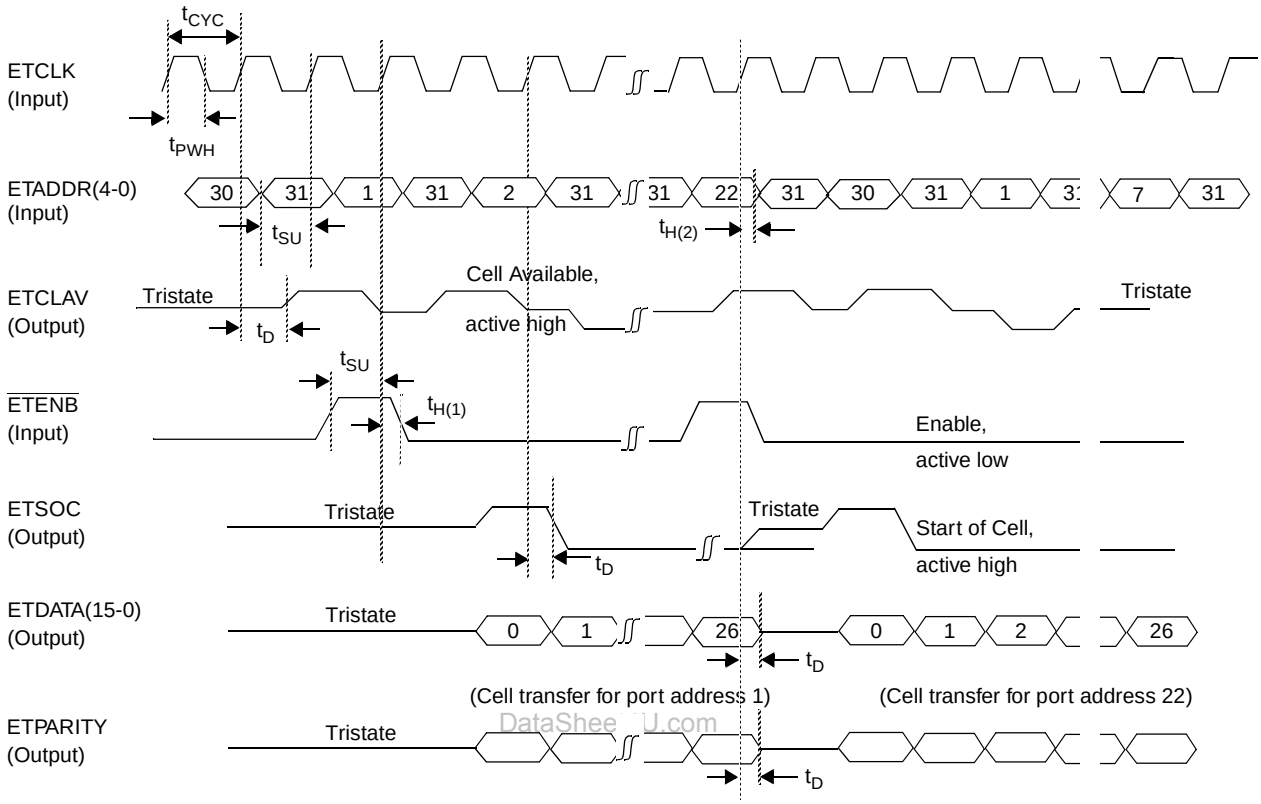
Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 43. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 8-bit)**



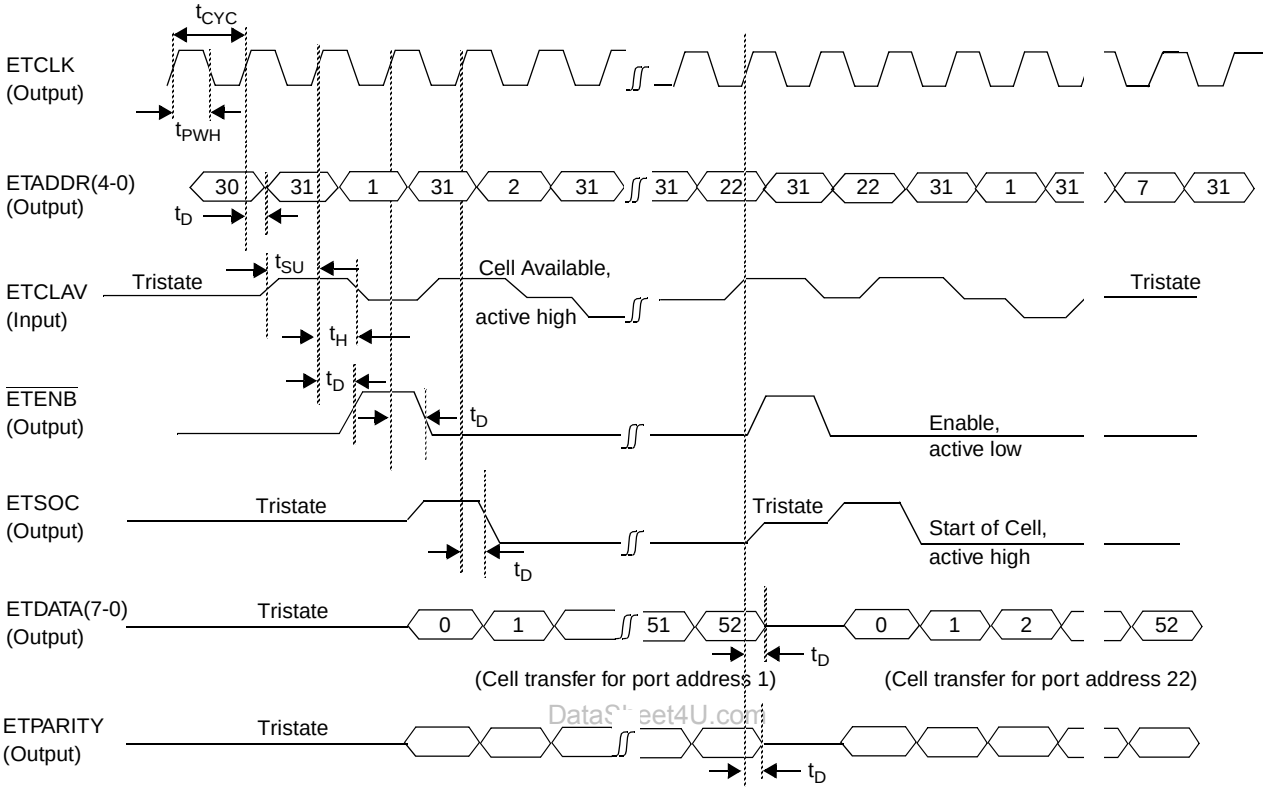

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{ETENB}$, ETADDR(4-0) setup time to ETCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| $\overline{ETENB}$ hold time after ETCLK↑ | $t_{H(1)}$ | 1.0 | | | ns |
| ETADDR(4-0) hold time after ETCLK↑ | $t_{H(2)}$ | 2.0 | | | ns |
| ETDATA(7-0), ETSOC, ETCLAV, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

**Figure 44. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{ETENB}$, ETADDR(4-0) setup time to ETCLK↑ | $t_{SU}$ | 4.0 | | | ns |
| $\overline{ETENB}$ hold time after ETCLK↑ | $t_{H(1)}$ | 1.0 | | | ns |
| ETADDR(4-0) hold time after ETCLK↑ | $t_{H(2)}$ | 2.0 | | | ns |
| ETDATA(15-0), ETSOC, ETCLAV, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |

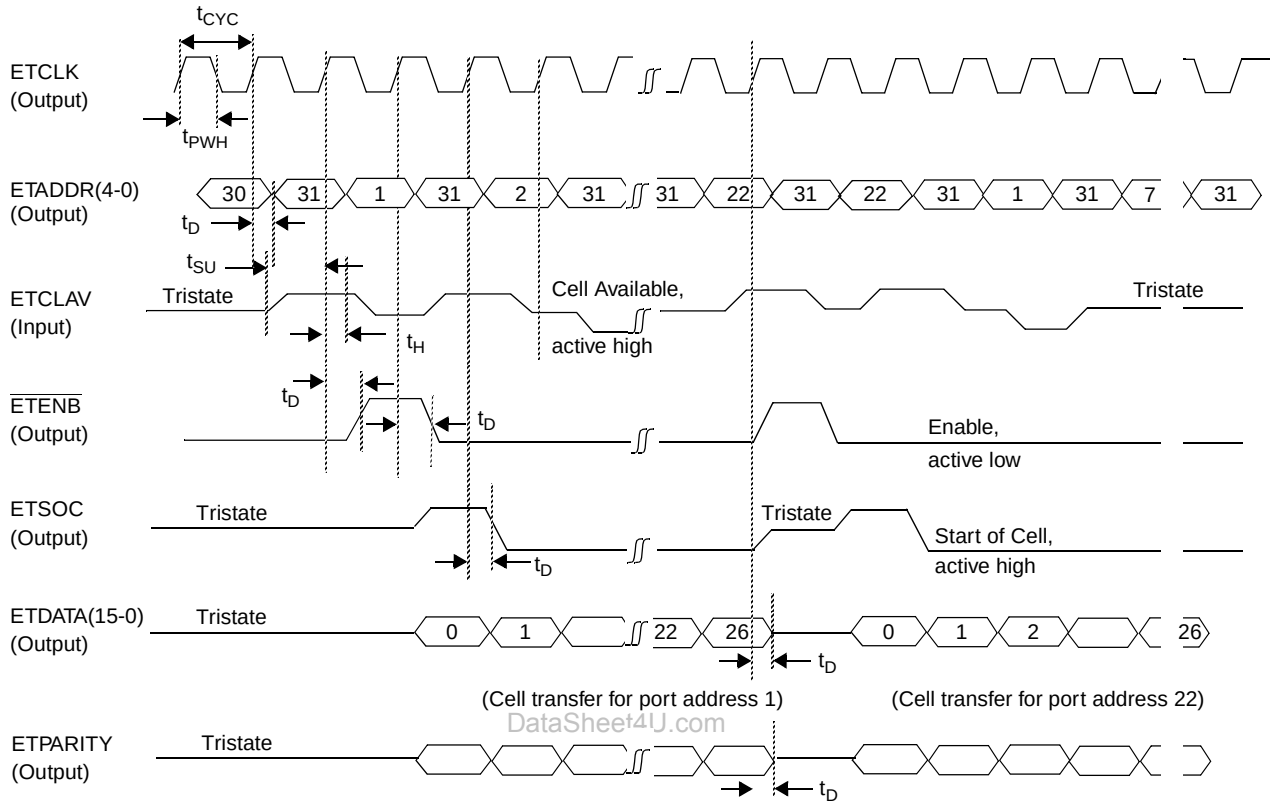
**Figure 45. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 8-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU}$ | 7.0 | | | ns |
| ETCLAV hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(7-0), ETSOC, ETADDR(4-0), $\overline{\text{ETENB}}$, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 46. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 16-bit)**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU}$ | 7.0 | | | ns |
| ETCLAV hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(15-0), ETSOC, ETADDR(4-0), $\overline{\text{ETENB}}$, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 47. Timing of Transmit Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 8-bit)**

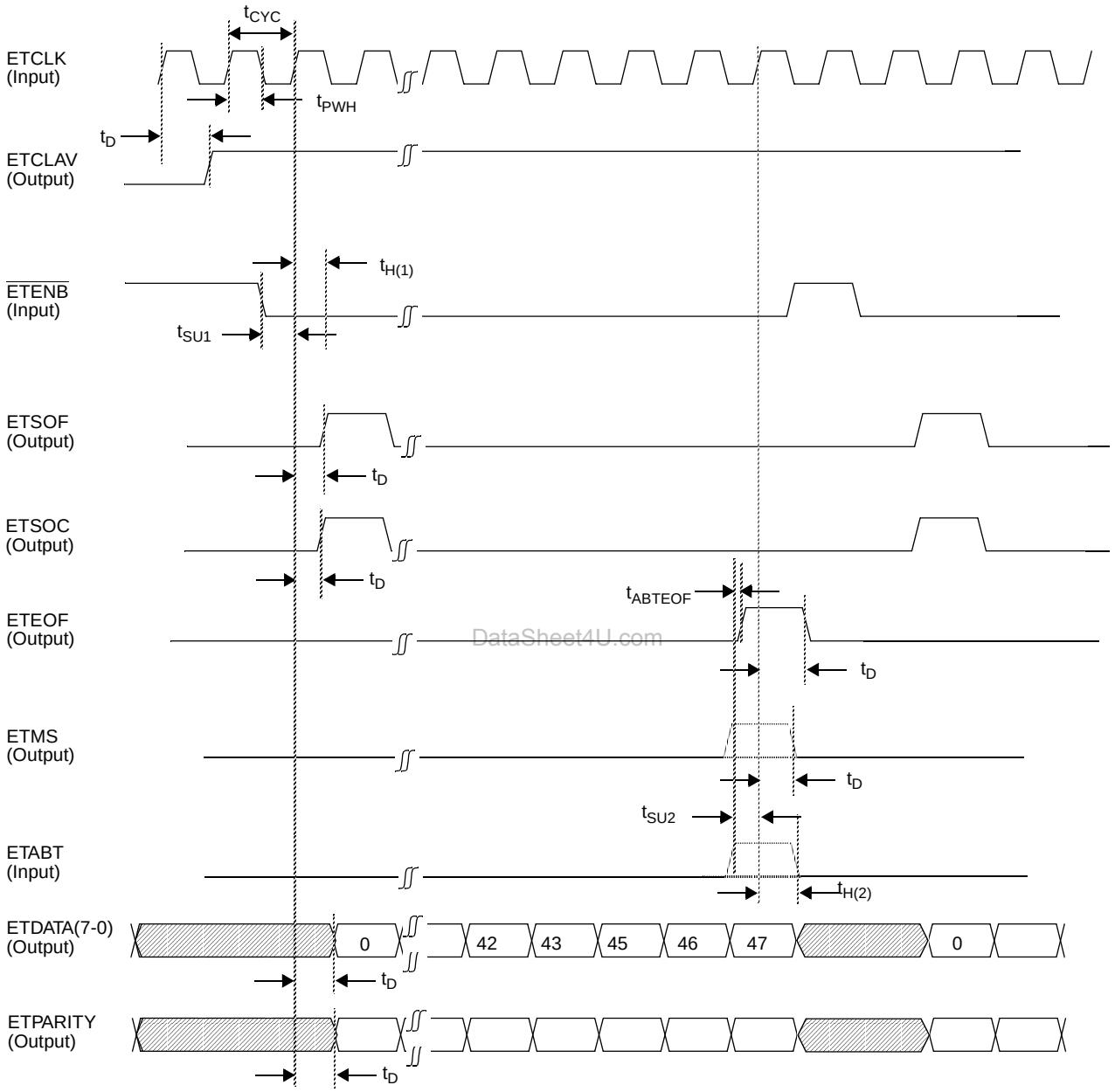


**Figure 47. Timing of Transmit Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{\text{ETENB}}$ setup time to ETCLK↑ | $t_{SU(1)}$ | 12.0 | | | ns |
| ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 4.0 | | | ns |
| $\overline{\text{ETENB}}$ hold time after ETCLK↑ | $t_{H(1)}$ | 1.0 | | | ns |
| ETABT hold time after ETCLK↑ | $t_{H(2)}$ | 1.5 | | | ns |
| ETDATA(7-0), ETSOF, ETEOF, ETSOC, ETCLAV, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

**Figure 48. Timing of Transmit Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 16-bit)**

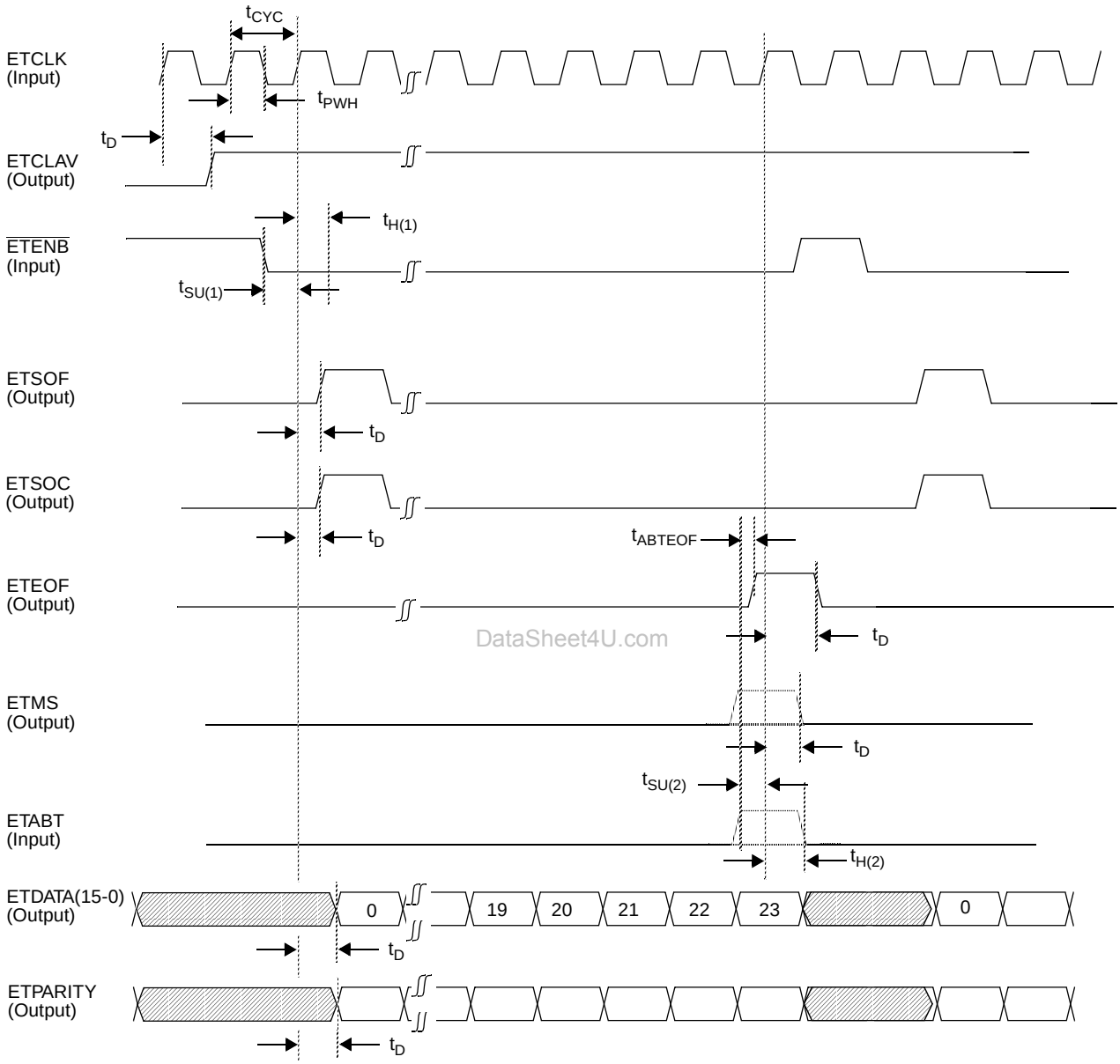


**Figure 48. Timing of Transmit Interface for Packet Mode, Single-PHY (PHY Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{\text{ETENB}}$ setup time to ETCLK↑ | $t_{SU(1)}$ | 12.0 | | | ns |
| ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 4.0 | | | ns |
| $\overline{\text{ETENB}}$ hold time after ETCLK↑ | $t_{H(1)}$ | 1.0 | | | ns |
| ETABT hold time after ETCLK↑ | $t_{H(2)}$ | 1.5 | | | ns |
| ETDATA(15-0), ETSOF, ETEOF, ETCLAV, ETMS, ETSOC, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

**Figure 49. Timing of Transmit Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 8-bit)**

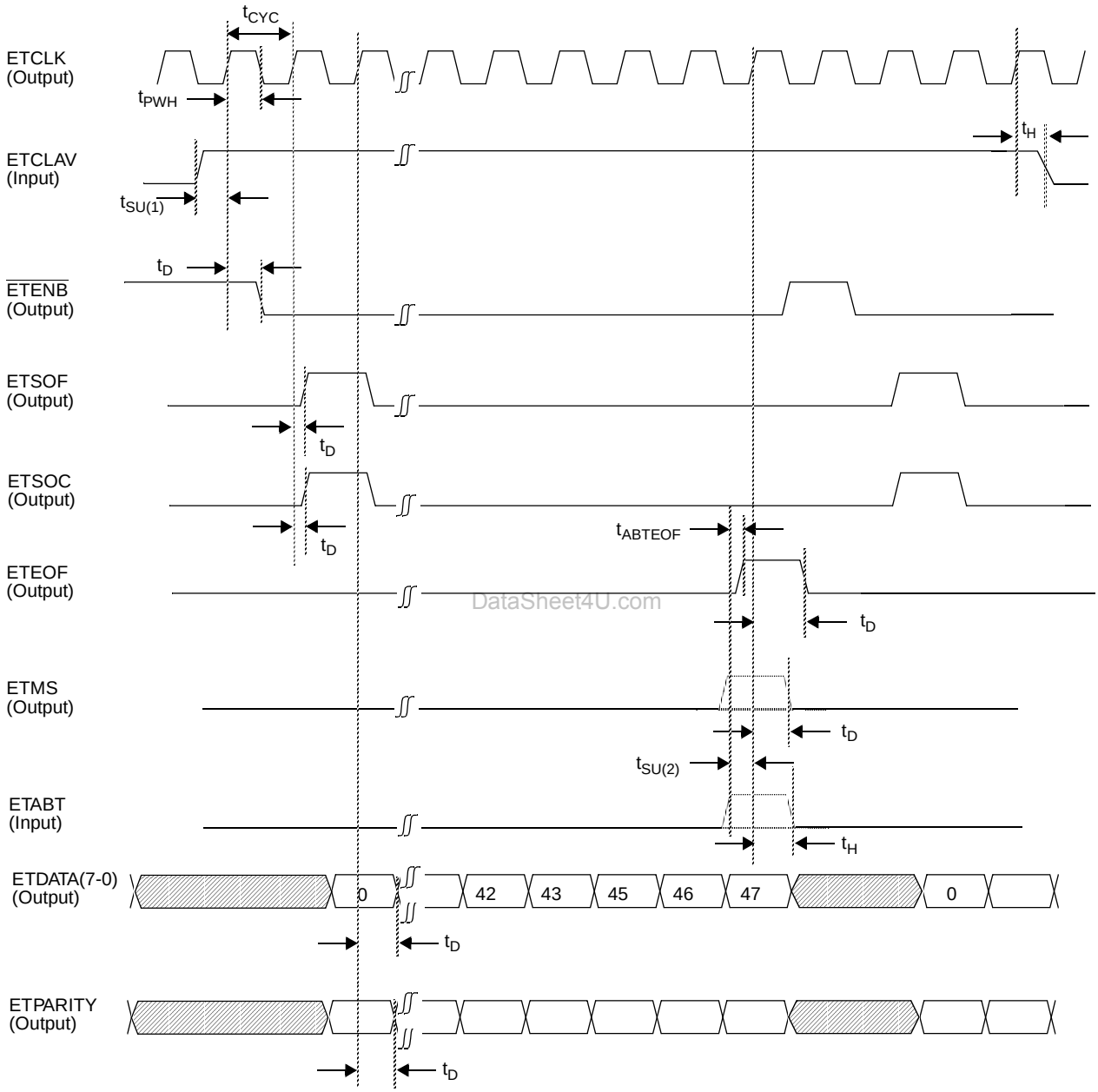


**Figure 49. Timing of Transmit Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU(1)}$ | 16.0 | | | ns |
| ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 5.0 | | | ns |
| ETCLAV, ETABT hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(7-0), ETSOF, ETEOF, $\overline{\text{ETENB}}$, ETSOC, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 50. Timing of Transmit Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 16-bit)**

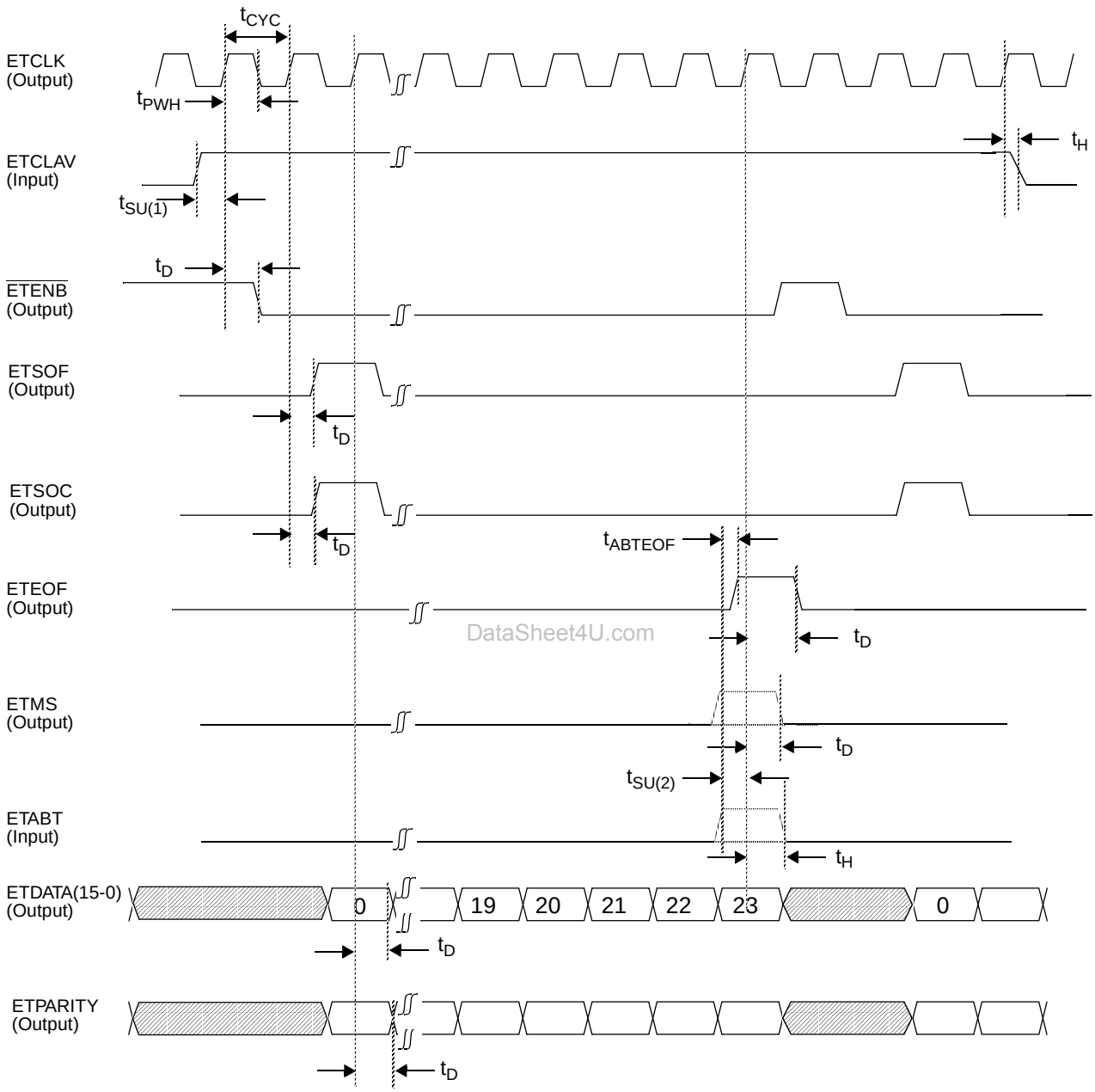


**Figure 50. Timing of Transmit Interface for Packet Mode, Single-PHY (ATM Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU(1)}$ | 16.0 | | | ns |
| ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 5.0 | | | ns |
| ETCLAV, ETABT hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(15-0), ETSOF, ETEOF, $\overline{\text{ETENB}}$, ETSOC, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 51. Timing of Transmit Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 8-bit)**

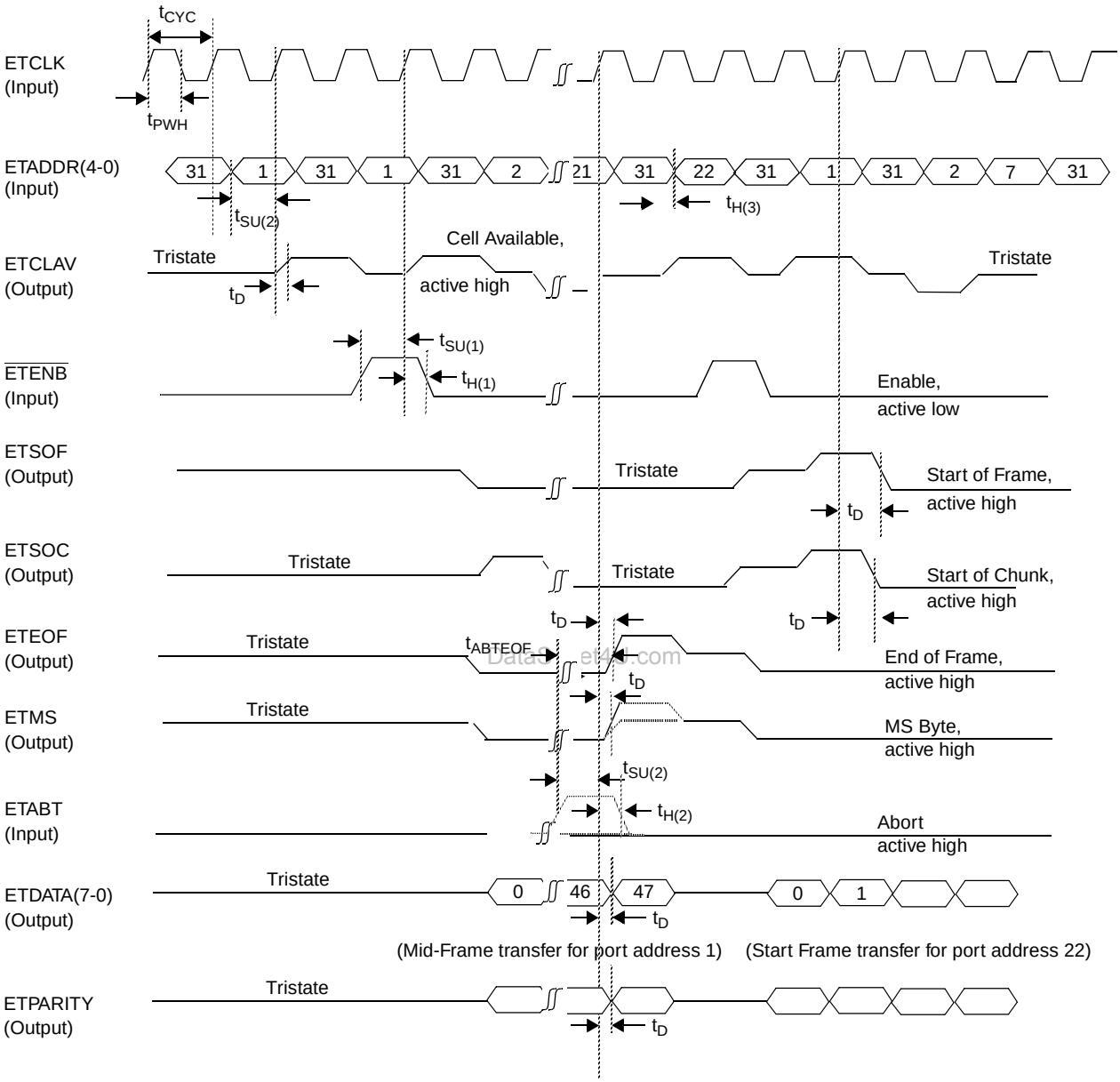


**Figure 51. Timing of Transmit Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{ETENB}$ setup time to ETCLK↑ | $t_{SU(1)}$ | 12.0 | | | ns |
| ETADDR(4-0), ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 4.0 | | | ns |
| $\overline{ETENB}$ hold time after ETCLK↑ | $t_{H(1)}$ | 1.5 | | | ns |
| ETABT hold time after ETCLK↑ | $t_{H(2)}$ | 1.5 | | | ns |
| ETADDR(4-0) hold time after ETCLK↑ | $t_{H(3)}$ | 2.0 | | | ns |
| ETDATA(7-0), ETSOF, ETEOF, ETCLAV, ETSOC, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

**Figure 52. Timing of Transmit Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 16-bit)**

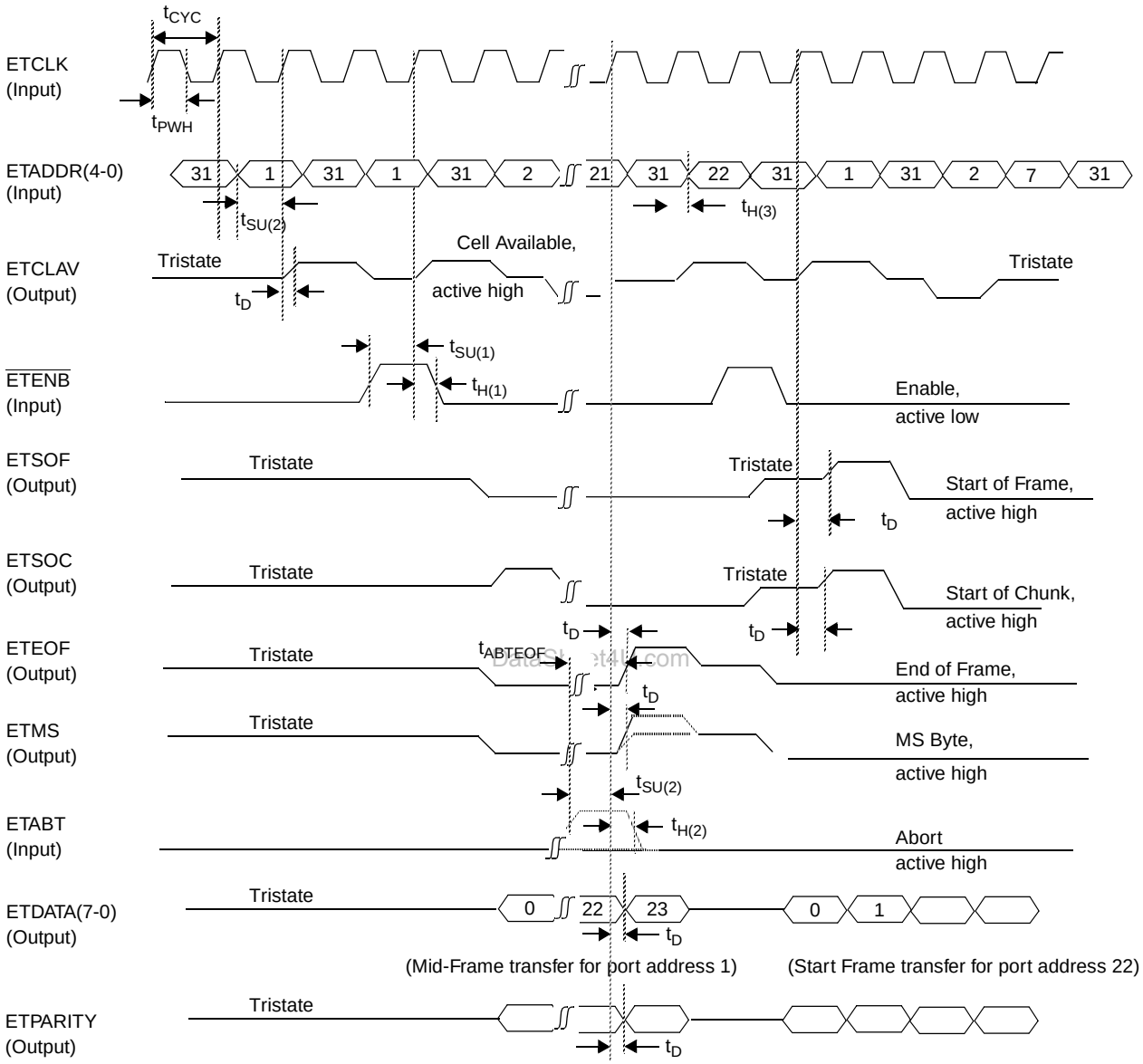


**Figure 52. Timing of Transmit Interface for Packet Mode, Multi-PHY (PHY Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period | $t_{CYC}$ | 20 | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| $\overline{\text{ETENB}}$ setup time to ETCLK↑ | $t_{SU(1)}$ | 12.0 | | | ns |
| ETADDR(4-0), ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 4.0 | | | ns |
| $\overline{\text{ETENB}}$ hold time after ETCLK↑ | $t_{H(1)}$ | 1.0 | | | ns |
| ETABT hold time after ETCLK↑ | $t_{H(2)}$ | 1.5 | | | ns |
| ETADDR(4-0) hold time after ETCLK↑ | $t_{H(3)}$ | 2.0 | | | ns |
| ETDATA(15-0), ETSOF, ETEOF, ETCLAV, ETSOC, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 11.5 | ns |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

**Figure 53. Timing of Transmit Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 8-bit)**

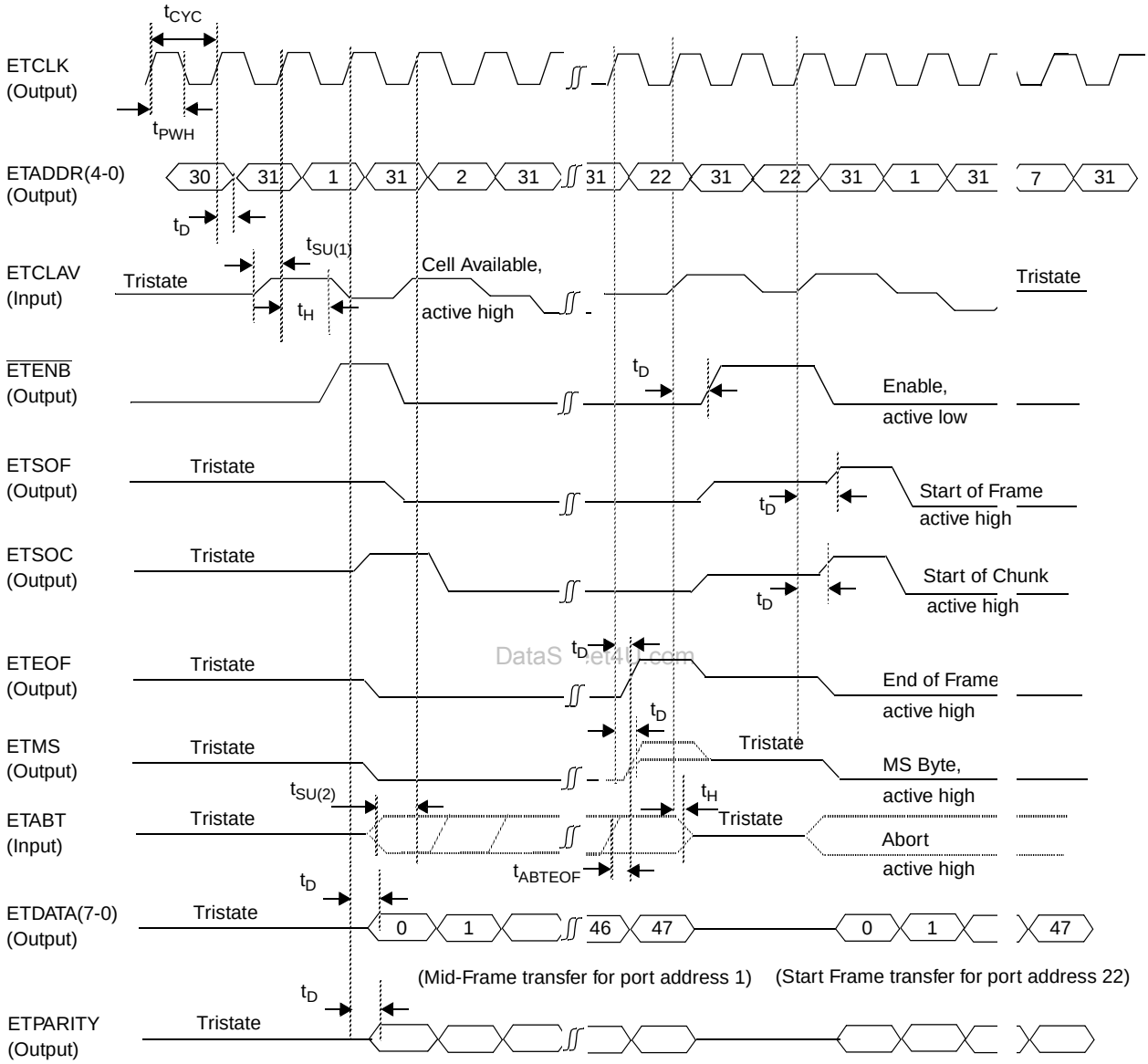


**Figure 53. Timing of Transmit Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 8-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU(1)}$ | 16.0 | | | ns |
| ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 5.0 | | | ns |
| ETCLAV, ETABT hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(7-0), ETSOF, ETEOF, ETADDR (4-0), $\overline{\text{ETENB}}$, ETSOC, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 54. Timing of Transmit Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 16-bit)**

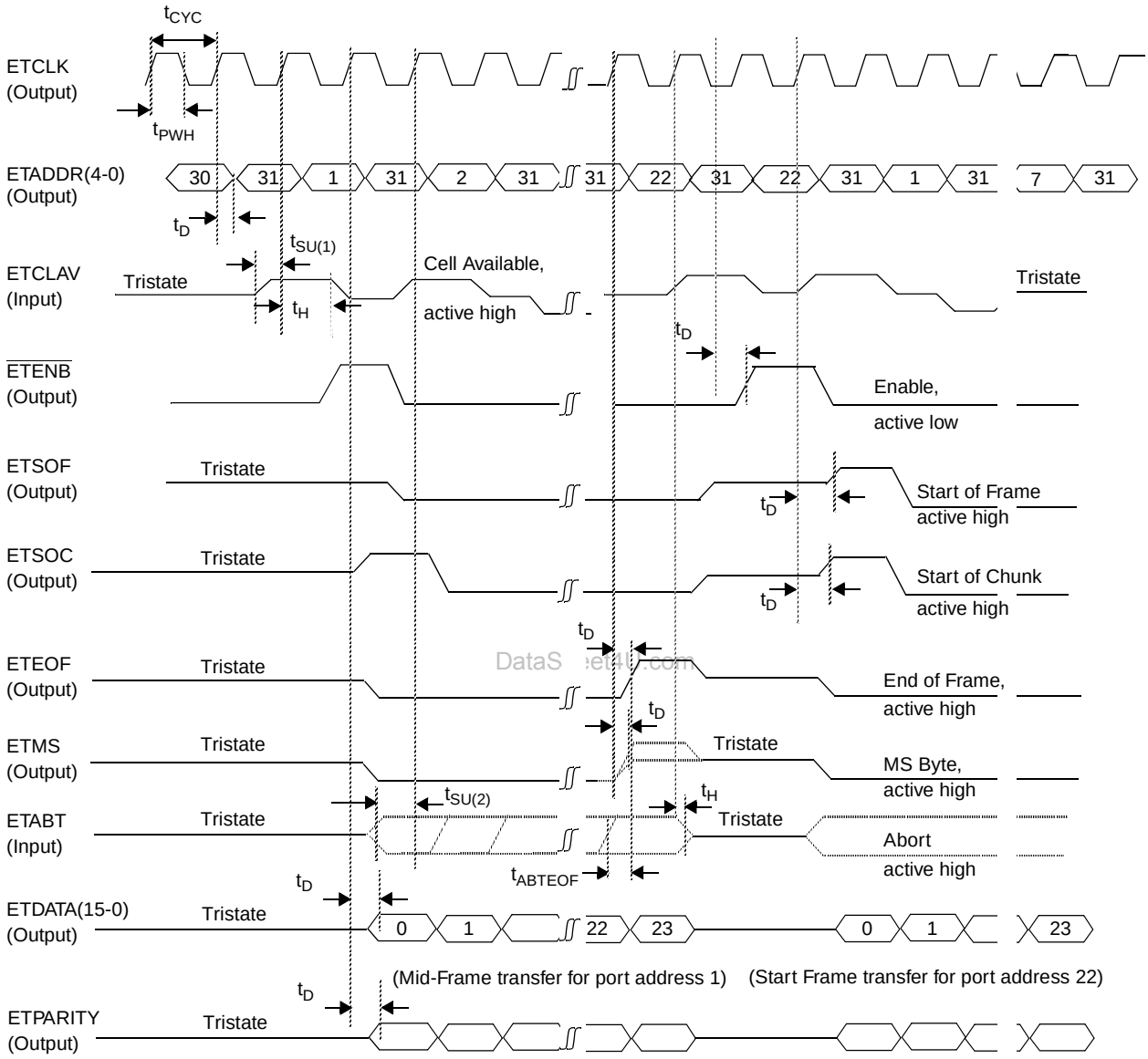
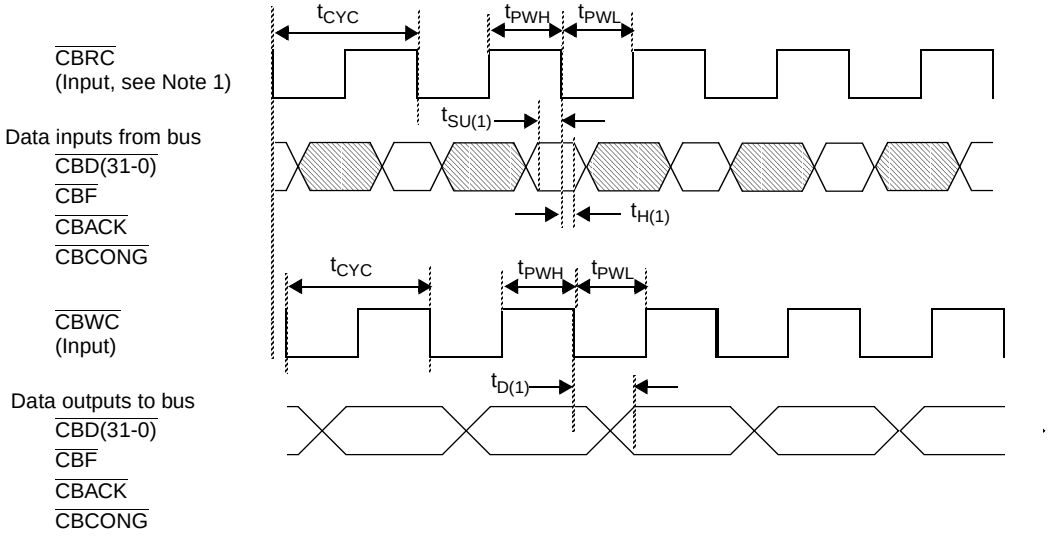


**Figure 54. Timing of Transmit Interface for Packet Mode, Multi-PHY (ATM Layer Emulation, 16-bit) (Cont.)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ETCLK clock period, UTCLKSRC = 00<br>ETCLK clock period, UTCLKSRC = 01 or 10 | $t_{CYC}$ | 20<br>$t_{CYCIN(PCLK)}$ | | | ns |
| ETCLK duty cycle, $t_{PWH}/t_{CYC}$ | | 40 | | 60 | % |
| ETCLAV setup time to ETCLK↑ | $t_{SU(1)}$ | 16.0 | | | ns |
| ETABT setup time to ETCLK↑ | $t_{SU(2)}$ | 5.0 | | | ns |
| ETCLAV, ETABT hold time after ETCLK↑ | $t_H$ | 1.0 | | | ns |
| ETDATA(15-0), ETSOF, ETEOF, ETADDR(4-0), $\overline{\text{ETENB}}$, ETSOC, ETMS, ETPARITY delay from ETCLK↑ | $t_D$ | 1.0 | | 6.5 | ns |
| LUCLK duty cycle (See Note) | | 45 | | 55 | % |
| ETABT to ETEOF | $t_{ABTEOF}$ | 2.0 | | 8.0 | ns |

Note: When UTCLKSRC = 00, LUCLK is used for Ingress and Egress UTOPIA interfaces.

**Figure 55. Timing of Signals for *CellBus* Interfaces**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $\overline{\text{CBRC}}$, $\overline{\text{CBWC}}$ cycle time | $t_{CYC}$ | 25 | | | ns |
| $\overline{\text{CBRC}}$, $\overline{\text{CBWC}}$ duty cycle | $t_{PWH}/t_{CYC}$ | 40 | | 60 | % |
| *CellBus* inputs setup time before $\overline{\text{CBRC}}\downarrow$ | $t_{SU(1)}$ | 1.0 | | | ns |
| *CellBus* inputs hold time after $\overline{\text{CBRC}}\downarrow$ | $t_{H(1)}$ | 3.0 | | | ns |
| *CellBus* outputs delay after $\overline{\text{CBWC}}\downarrow$ | $t_{D(1)}$ | See Note 2 | | See Note 2 | ns |

Notes:

1. The timing shown applies to the signals of both *CellBus* A and *CellBus* B, identified by A or B appended to all of the signal names shown in this Figure.
2. The ASPEN device *CellBus* write clock to *CellBus* data out time delay $t_{D(1)}$ has two components, internal delay and GTL+ driver delay. The internal delay consists of the delay from the $\overline{\text{CBWC}}$ input, through the GTL+ receiver, internal ASPEN device circuitry and into the (internal) input lead of the GTL+ driver. This internal delay is dependent solely on temperature, voltage and process variation and has minimum and maximum values of 2.0 ns and 7.0 ns, respectively. The GTL+ driver delay includes the effects of the (internal) GTL+ driver and all external loading, from the chip bond wire inductance onwards. For the purposes of specification, a test load is used which consists of a 10.7 nH bond wire inductance from the VLSI device output pad to the package output lead, and a 50 ohm resistor to +1.5 volts with a 1.0 pF capacitor to ground from the package output lead. The total value of $t_{D(1)}$ is increased to the following minimum and maximum values (shown below) when using this load.

| ***CellBus* Output Transition** | **$t_{D(1)}$ Minimum Delay (ns) Internal + GTL+ = Total Pad** | **$t_{D(1)}$ Maximum Delay (ns) Internal + GTL+ = Total Pad** |
|---|---|---|
| Z to Low | 2.0 + 0.5 = 2.5 | 7.0 + 2.0 = 9.0 |
| Low to Z | 2.0 + 3.0 = 5.0 | 7.0 + 4.2 = 11.2 |

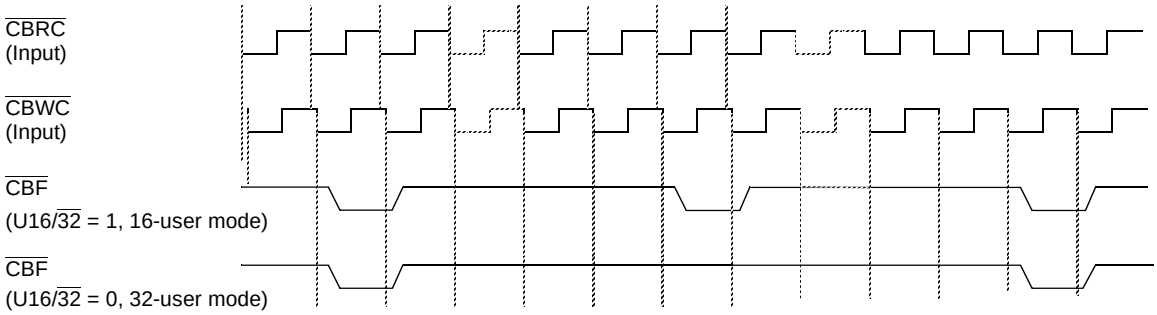
These output delay values by themselves may be inadequate to complete a system design. TranSwitch strongly recommends that all *CellBus* applications should be analyzed by high speed backplane and simulation specialists, using such tools as HSpice® analog circuit simulation.

These simulations can model timing from one ASPEN device, through various levels of system interconnect, to another ASPEN device, and include the effects of the device package, printed circuit board, connectors and backplane. The results of these simulations, when added to the internal delay, will provide the actual value of $t_{D(1)}$ for a given system. TranSwitch is able to support simulations by providing up-to-date models of the GTL+ transceiver used within the ASPEN device.

Please contact the TranSwitch Applications Engineering Department for additional information, a list of proven high speed simulation consultants, and support.

HSpice is a registered trademark of Meta-Software, Inc.

**Figure 56. Timing of *CellBus* Frame Position**

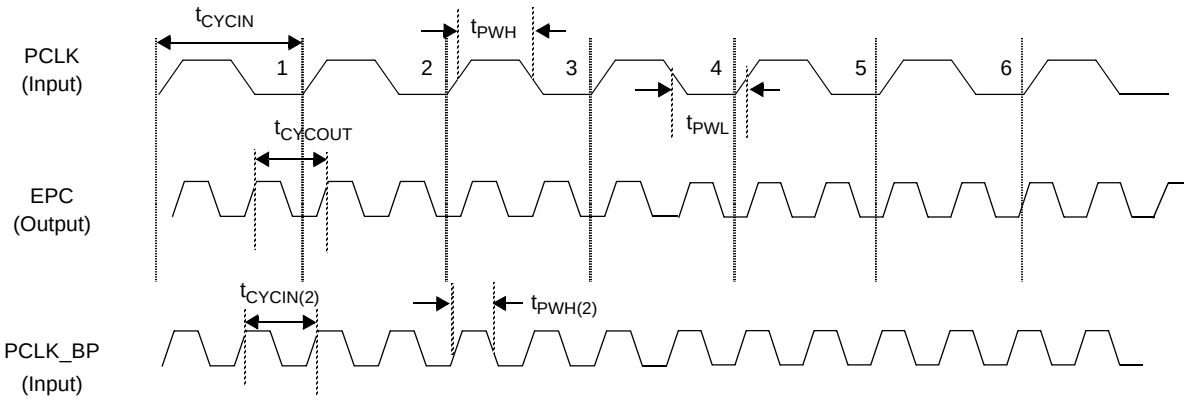



Note: The timing shown applies to the signals of both *CellBus* A and *CellBus* B, identified by A or B appended to all of the signal names shown in this Figure.



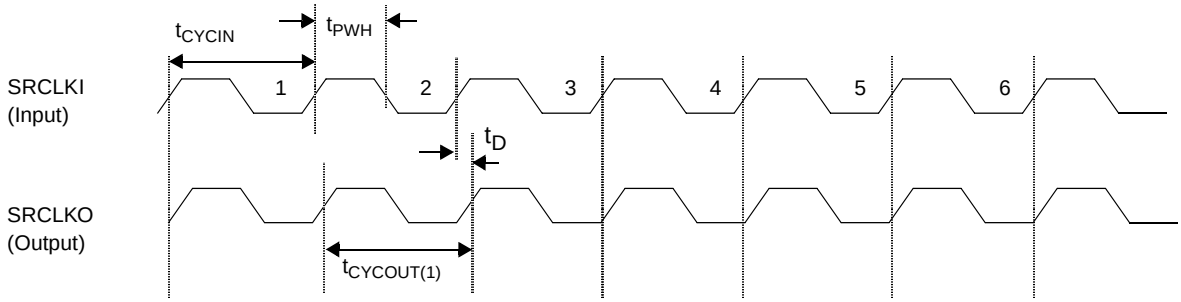
**Figure 57. Timing Relationship Between PCLK and EPC Clocks**






| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PCLK cycle time | $t_{CYCIN}$ | 20 | | 28.57 (see Note 3 on page 100) | ns |
| PCLK duty cycle, $t_{PWH}/t_{CYCIN}$ | | 25 | | 75 | % |
| EPC cycle time | $t_{CYCOUT}$ | $t_{CYCIN(PCLK)}$ x 0.5 | | | ns |
| PCLK_BP cycle time | $t_{CYCIN(2)}$ | 10 | | 14.28 (see Note 3 on page 100) | ns |
| PCLK_BP duty cycle, $t_{PWH(2)}/t_{CYCIN(2)}$ | | 48 | | 52 | % |

**Figure 58. Timing Relationship Between SRCLKI and SRCLKO Clocks**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SRCLKI Cycle Time | $t_{CYCIN}$ | 10 | | 14.28 (see Note 3 on page 100) | ns |
| SRCLKI duty cycle, $t_{PWH}/t_{CYCIN}$ | | 45 | | 55 | % |
| SRCLKO Cycle Time | $t_{CYCOUT(1)}$ | $t_{CYCIN(SRCLKI)}$ | | | ns |
| SRCLKO↑ delay from SRCLKI↑ | $t_D$ | 1.6 | | 3.8 | ns |

Notes:

1. The ASPEN device SSRAM SRCLKO output clock to data out time delay ($t_{D(1)}$ - $t_{D(6)}$ in Figures 59 and 60) has two components, internal delay and pad driver delay. The internal delay consists of the delay from the SRCLKI input, through the pad receiver, internal ASPEN device circuitry and into the (internal) input lead of the pad driver. This internal delay is dependent solely on temperature, voltage and process variation and it has the minimum and maximum values, respectively, that are shown below for each signal:



| Symbol | Min | Max | Unit |
|---|---|---|---|
| SRCLKO | 0.5 | 1.4 | ns |
| $\overline{\text{SADSC0}}$ or $\overline{\text{SADSC1}}$ | 2.7 | 7.5 | ns |
| SA(0-20) | 2.5 | 9.9 | ns |
| SD(0-63) | 2.4 | 7.8 | ns |
| $\overline{\text{SOE}}$ | 2.6 | 6.4 | ns |
| $\overline{\text{SADV0}}$ or $\overline{\text{SADV1}}$ | 2.7 | 7.2 | ns |
| $\overline{\text{SWEL}}$ or $\overline{\text{SWEH}}$ | 2.5 | 6.3 | ns |
| SCE, SCE2, $\overline{\text{SCE}}$, $\overline{\text{SCE2}}$ | 2.5 | 6.3 | ns |

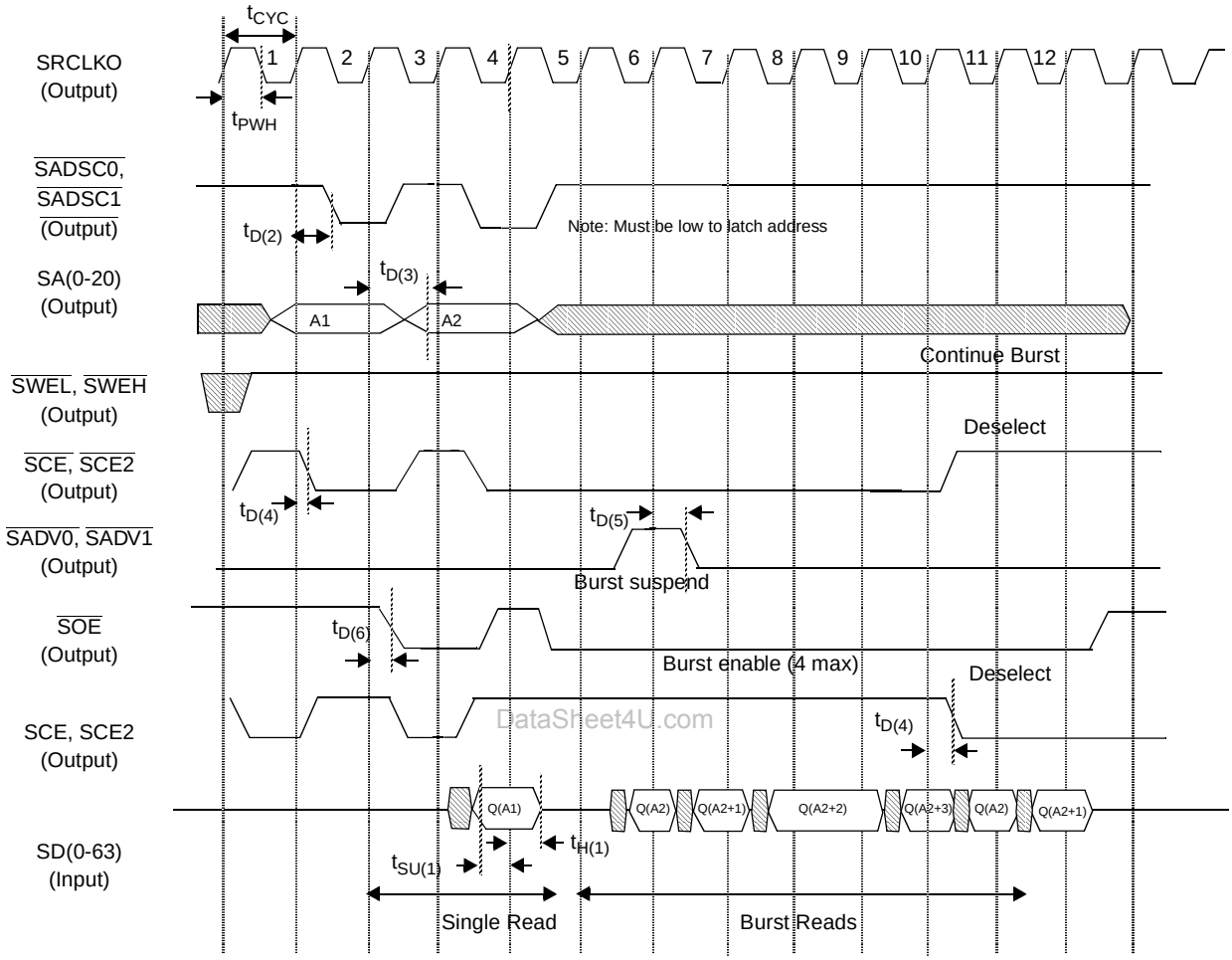
The pad driver delay includes the effects of the (internal) pad driver and all external loading. Based upon output loading for each system design, the pad driver delay should be calculated and the values combined to the internal delay values to determine system performance. The SSRAM timing shown in Figures 58, 59, and 60 applies when there is a 37pF load to ground (4 SSRAM load) on outputs SA(0-20), SRCLKO, $\overline{\text{SADSC0}}$, $\overline{\text{SADSC1}}$, $\overline{\text{SCE}}$, $\overline{\text{SCE2}}$, SCE, SCE2, $\overline{\text{SADV0}}$, $\overline{\text{SADV1}}$, $\overline{\text{SOE}}$, $\overline{\text{SWEL}}$, $\overline{\text{SWEH}}$ and a 35pF load to ground on outputs SD(0-63).

2. TranSwitch strongly recommends that all ASPEN SSRAM memory interface designs be analyzed using an analog simulation tool such as HSpice® analog circuit simulation. These simulations can model timing from an ASPEN device, to the SSRAM memories, and include the effect of PCB traces and vias.

   Please contact the TranSwitch Applications Engineering department for additional information and support. HSpice is a registered trademark of Meta-Software, Inc.

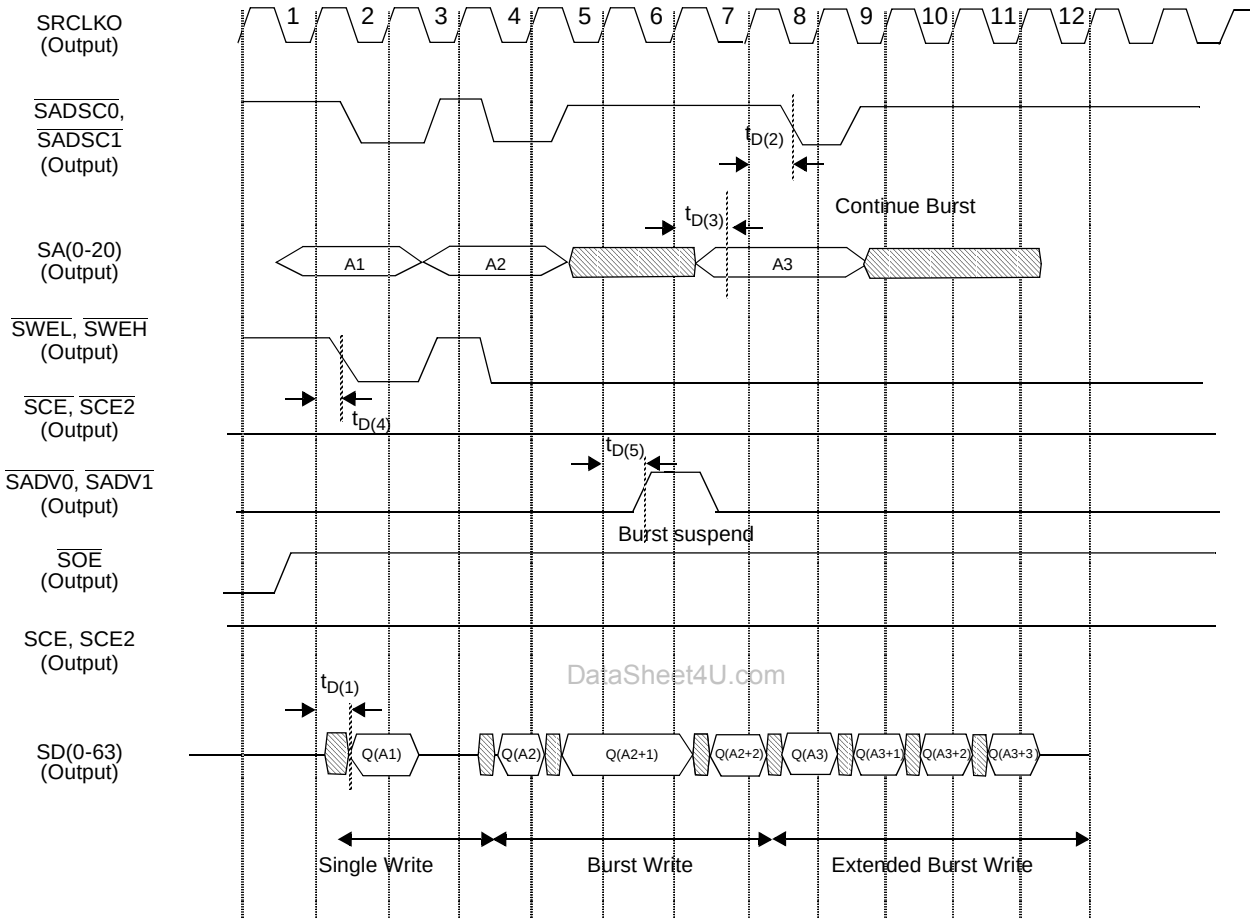
3. The maximum cycle time (minimum clock frequency) for the PCLK, PCLK_BP and SRCLKI input clocks is determined by the performance requirements of your design. Consult the TranSwitch Applications Engineering department for assistance in determining the maximum cycle time for these inputs if your design does not require maximum ASPEN performance.

**Figure 59. Timing of SSRAM Read Cycle**



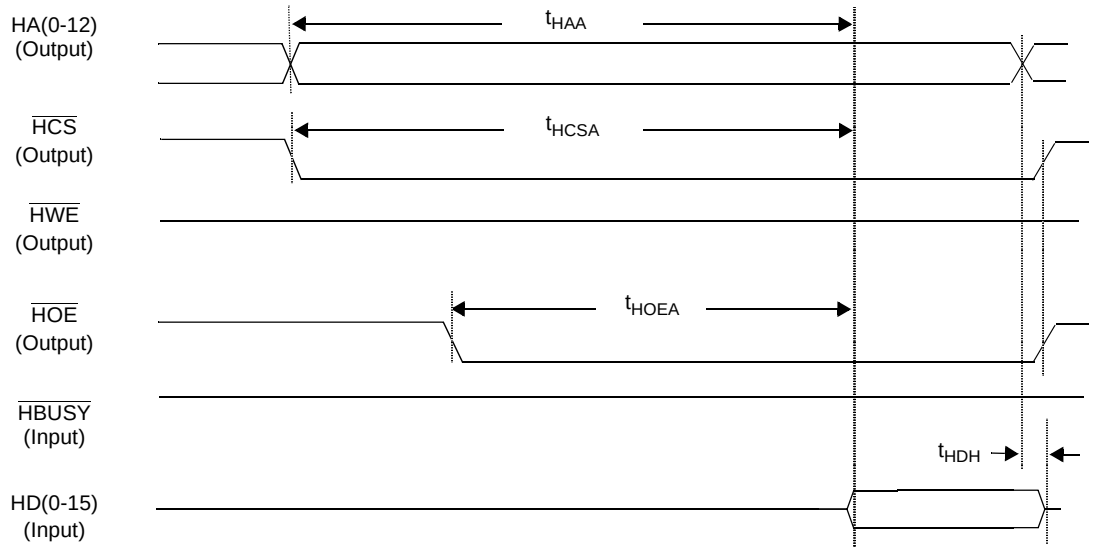

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SRCLKO cycle time | $t_{CYC}$ | 10 | | 14.28 (see Note 3 on page 100) | ns |
| SRCLKO duty cycle | $t_{PWH}/t_{CYC}$ | 38 | | 62 | % |
| $\overline{SADSC0}$, $\overline{SADSC1}$ delay from SRCLKO↑ | $t_{D(2)}$ | 1.0 | | 6.6 | ns |
| SA(0-20) delay from SRCLKO↑ | $t_{D(3)}$ | 1.0 | | 9.1 | ns |
| $\overline{SCE}$, $\overline{SCE2}$ delay from SRCLKO↑ | $t_{D(4)}$ | 1.0 | | 5.5 | ns |
| SCE, SCE2 delay from SRCLKO↑ | $t_{D(4)}$ | 1.0 | | 5.5 | ns |
| $\overline{SADV0}$, $\overline{SADV1}$ delay from SRCLKO↑ | $t_{D(5)}$ | 1.0 | | 6.5 | ns |
| $\overline{SOE}$ delay from SRCLKO↑ | $t_{D(6)}$ | 1.0 | | 5.6 | ns |
| SD(0-63) setup time to SRCLKO↑ | $t_{SU(1)}$ | 2.8 | | | ns |
| SD(0-63) hold time after SRCLKO↑ | $t_{H(1)}$ | 0.0 | | | ns |

**Figure 60. Timing of SSRAM Write Cycle**



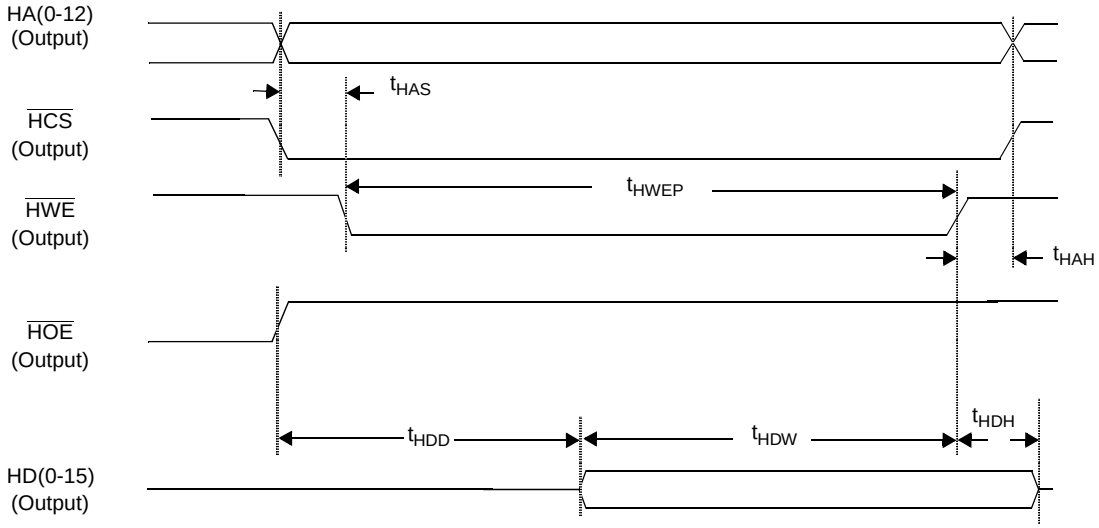

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SD(0-63) delay from SRCLKO↑ | $t_{D(1)}$ | 1.0 | | 6.9 | ns |
| $\overline{SADSC0}$, $\overline{SADSC1}$ delay from SRCLKO↑ | $t_{D(2)}$ | 1.0 | | 6.6 | ns |
| SA(0-20) delay from SRCLKO↑ | $t_{D(3)}$ | 1.0 | | 9.1 | ns |
| $\overline{SWEL}$, $\overline{SWEH}$ delay from SRCLKO↑ | $t_{D(4)}$ | 1.0 | | 5.5 | ns |
| $\overline{SADV0}$, $\overline{SADV1}$ delay from SRCLKO↑ | $t_{D(5)}$ | 1.0 | | 6.5 | ns |

**Figure 61. Timing of Host Interface Read Cycle for Non-Status Location**



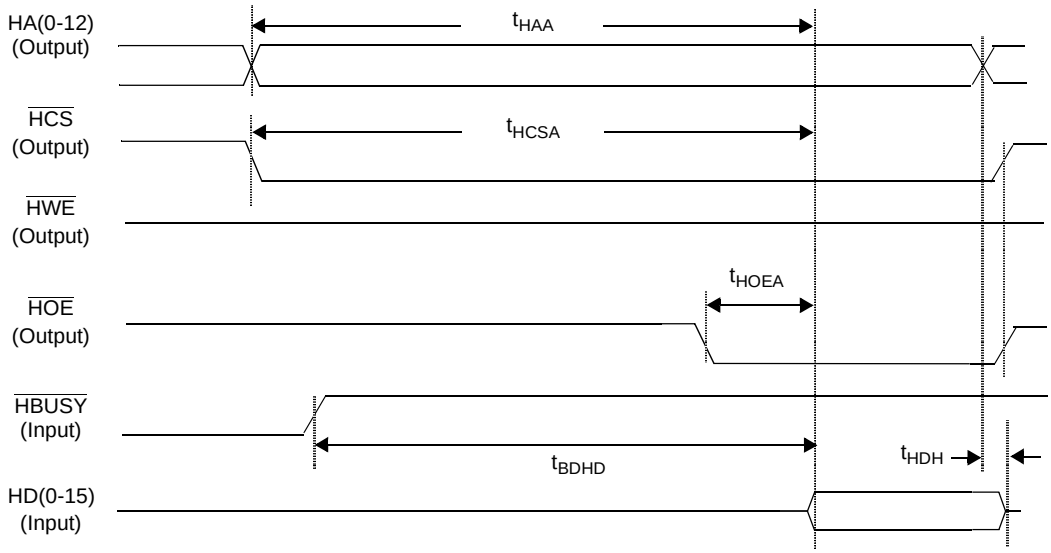

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| HA(0-12) to HD(0-15) valid | $t_{HAA}$ | | | 45 | ns |
| $\overline{HCS}$ to HD(0-15) valid | $t_{HCSA}$ | | | 45 | ns |
| $\overline{HOE}$ to HD(0-15) valid | $t_{HOEA}$ | | | 30 | ns |
| HD(0-15) hold time after HA(0-12) change | $t_{HDH}$ | 0.0 | | | ns |

**Figure 62. Timing of Host Interface Write Cycle for Non-Status Location**



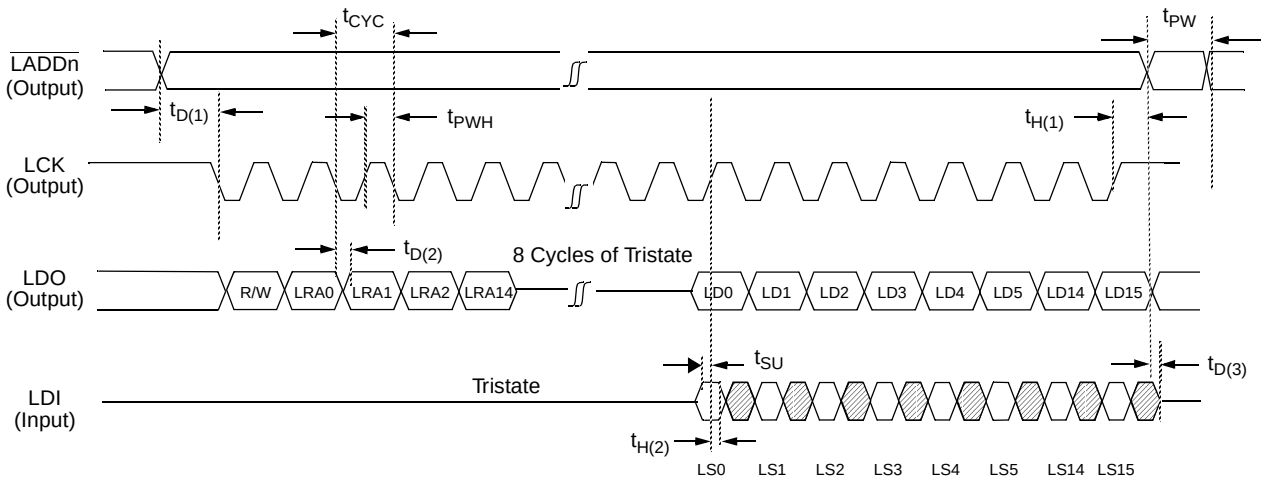

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| HA(0-12), $\overline{HCS}$ to $\overline{HWE}\downarrow$ | $t_{HAS}$ | 0 | | | ns |
| $\overline{HWE}$ pulse width | $t_{HWEP}$ | 40 | | | ns |
| HD(0-15) valid to $\overline{HWE}\uparrow$ | $t_{HDW}$ | 30 | | | ns |
| HD(0-15) hold time after $\overline{HWE}\uparrow$ | $t_{HDH}$ | ($t_{CYCIN(PCLK)}$ x 0.5) | | | ns |
| HA(0-12), $\overline{HCS}$ hold time after $\overline{HWE}\uparrow$ | $t_{HAH}$ | ($t_{CYCIN(PCLK)}$ x 0.5) | | | ns |
| $\overline{HOE}\uparrow$ to HD(0-15) valid | $t_{HDD}$ | ($t_{CYCIN(PCLK)}$ x 0.5) - 1 | | | ns |

**Figure 63. Timing of Host Interface Read Cycle for Status Location**



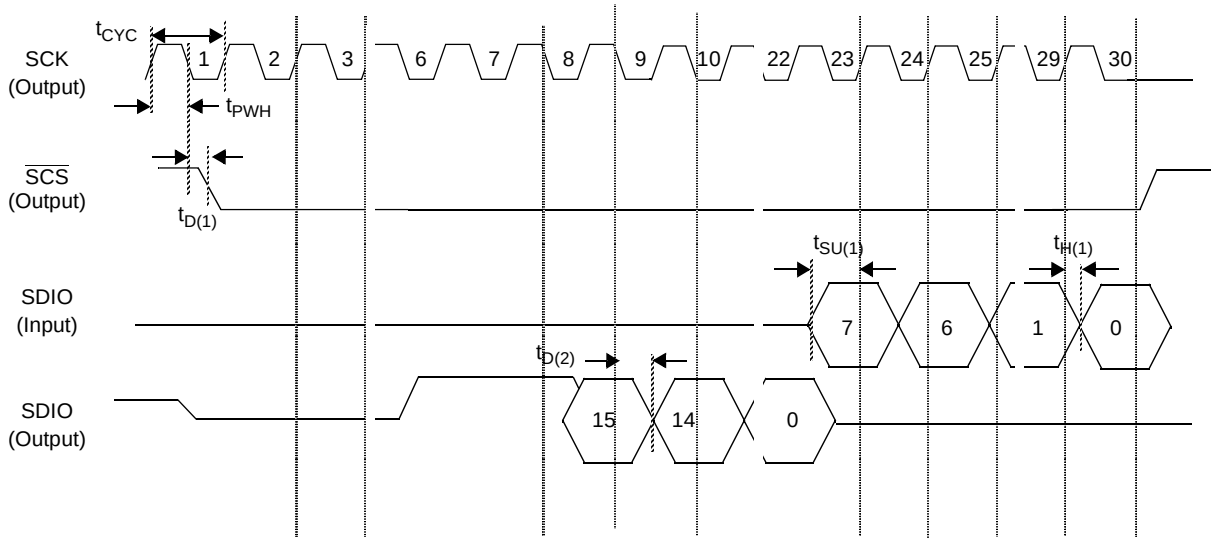

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| HA(0-12) to HD valid | $t_{HAA}$ | | | 45 | ns |
| $\overline{HCS}$ to HD(0-15) valid | $t_{HCSA}$ | | | 45 | ns |
| $\overline{HOE}$ to HD(0-15) valid | $t_{HOEA}$ | | | 30 | ns |
| HD(0-15) Hold Time after HA change | $t_{HDH}$ | 0.0 | | | ns |
| $\overline{HBUSY}$ disable to HD(0-15) valid | $t_{BDHD}$ | | | $t_{CYCIN(PCLK)}$ x 3 | ns |

**Figure 64. Timing of Serial Line Control Interface**



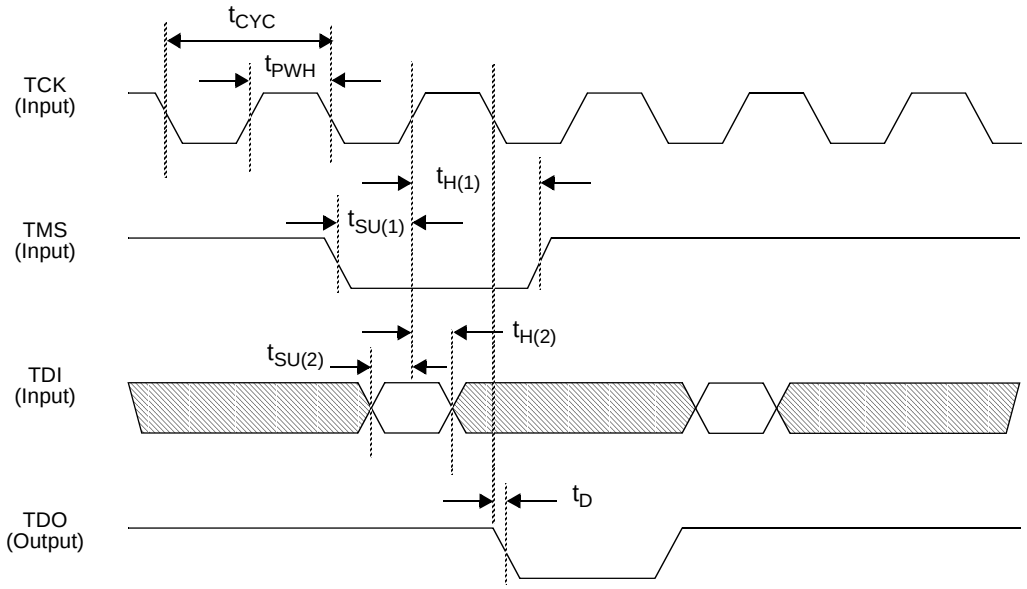

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LCK clock cycle time | $t_{CYC}$ | $t_{CYCIN(PCLK)}$ x 2 | | $t_{CYCIN(PCLK)}$ x 4 | ns |
| LCK duty cycle | $t_{PWH}/t_{CYC}$ | 40 | | 60 | % |
| $\overline{\text{LADDn}}$ active delay after LCK↓ | $t_{D(1)}$ | $t_{CYC}$ | | | ns |
| LDO valid delay after LCK↓ | $t_{D(2)}$ | | | 4.0 | ns |
| LDI high-Z delay after $\overline{\text{LADDn}}$ inactive | $t_{D(3)}$ | | | $t_{CYC}$ | ns |
| LDI setup time before LCK↑ | $t_{SU}$ | 10.0 | | | ns |
| LDI hold time after LCK↑ | $t_{H(2)}$ | 0.0 | | | ns |
| $\overline{\text{LADDn}}$ hold time after LCK↑ | $t_{H(1)}$ | $t_{CYC}$ | | | ns |
| $\overline{\text{LADDn}}$ inactive pulse width | $t_{PW}$ | $t_{CYC}$ | | | ns |

**Figure 65. Timing of Serial EEPROM Interface**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCK cycle time | $t_{CYC}$ | $t_{CYCIN(PCLK)}$ x 33 | | | ns |
| SCK duty cycle | $t_{PWH}/t_{CYC}$ | 45 | | 55 | % |
| $\overline{SCS}$ active delay after SCK↓ | $t_{D(1)}$ | 1.0 | | 5.0 | ns |
| SDIO valid delay after SCK↓ | $t_{D(2)}$ | 1.0 | | 5.0 | ns |
| SDIO setup time before SCK↑ | $t_{SU(1)}$ | 10.0 | | | ns |
| SDIO hold time after SCK↑ | $t_{H(1)}$ | 10.0 | | | ns |

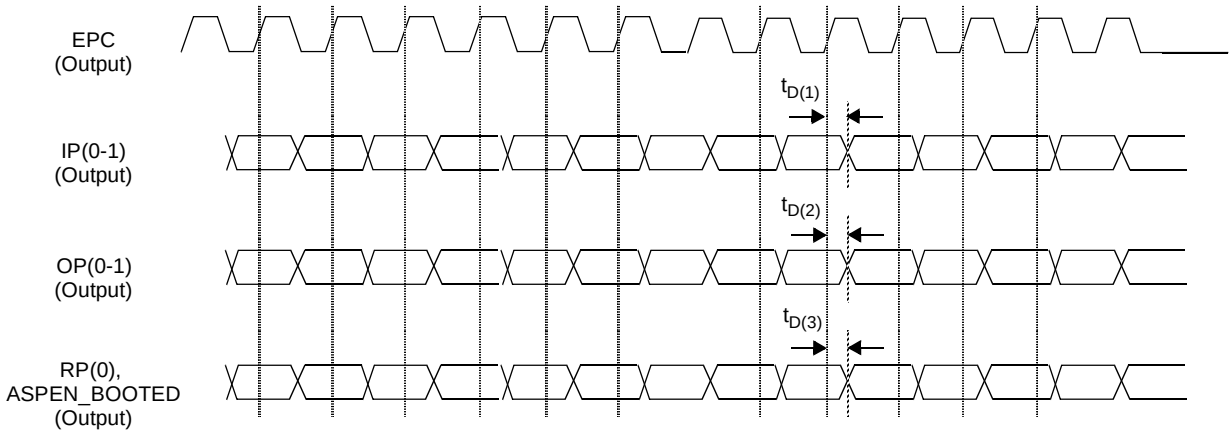
**Figure 66. Boundary Scan Timing Diagram**






| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| TCK clock cycle time | $t_{CYC}$ | 50 | | ns |
| TCK clock duty cycle | $t_{PWH}/t_{CYC}$ | 40 | 60 | % |
| TMS setup time before TCK↑ | $t_{SU(1)}$ | 4.0 | | ns |
| TMS hold time after TCK↑ | $t_{H(1)}$ | 0.0 | | ns |
| TDI setup time before TCK↑ | $t_{SU(2)}$ | 4.0 | | ns |
| TDI hold time after TCK↑ | $t_{H(2)}$ | 0.0 | | ns |
| TDO delay after TCK↓ | $t_D$ | | 12.0 | ns |

**Figure 67. Timing of General Purpose Outputs**

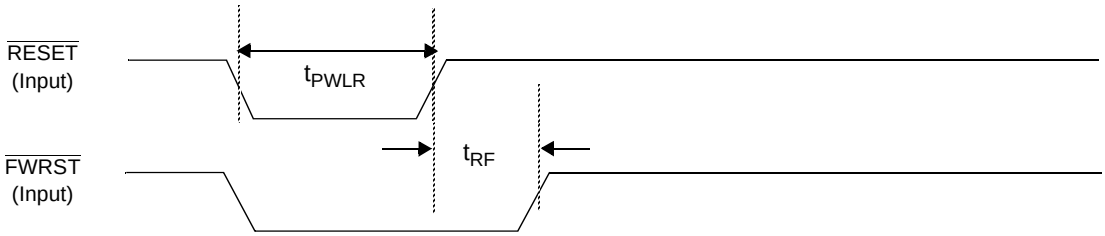



| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IP(0-1) delay after EPC rise | $t_{D(1)}$ | 1.0 | | 7.0 | ns |
| OP(0-1) delay after EPC rise | $t_{D(2)}$ | 1.0 | | 7.0 | ns |
| RP(0), ASPEN_BOOTED delay after EPC rise | $t_{D(3)}$ | 1.0 | | 7.0 | ns |



Note: Load on outputs EPC, IP(0-1), OP(0-1), RP(0), ASPEN_BOOTED is 15pF for the above timing.

**Figure 68. Timing Relationship of $\overline{\text{RESET}}$ and $\overline{\text{FWRST}}$**




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $\overline{\text{FWRST}}\uparrow$ delay after $\overline{\text{RESET}}\uparrow$ | $t_{RF}$ | $t_{CYCIN(PCLK)}$ x 5 | | $t_{CYCIN(PCLK)}$ x 1000 | ns |
| $\overline{\text{RESET}}$ pulse width | $t_{PWLR}$ | $t_{CYCIN(PCLK)}$ x 10 | | | ns |

## MESSAGING FORMATS

### CONTROL REGISTER ACCESS:

The ASPEN device provides a messaging interface for communication with a host processor, rather than using a direct address/data/control interface to its internal memory for control input and status output. This is supported through an external asynchronous dual port static RAM (DPSRAM) mapped as six unidirectional mailboxes, three for host-to-ASPEN messages and three for ASPEN-to-host messages. The last two bytes of the DPSRAM contain control registers to facilitate the handshaking required for bidirectional message exchange (For details of Host-ASPEN messaging, see "Host Interface" on page 24).

**Figure 69. Control Register WRITE Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00100 | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 6H | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST(4-2) See Note 1 | | |
| | 0 | DEST(1-0) See Note 1 | | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | 00H | | | | | | | |
| | 2 | 00H | | | | | | | |
| | 1 | 00H | | | | | | | |
| | 0 | 00H | | | | | | | |
| 2 | 3 | 00H (future use, CBRH) | | | | | | | |
| | 2 | 00H (future use, CBRH) | | | | | | | |
| | 1 | 00H (future use, TRH) | | | | | | | |
| | 0 | 00H (future use, TRH) | | | | | | | |
| 3 | 3 | FFH (ATM Cell Header) See Note 2 | | | | | | | |
| | 2 | FFH (ATM Cell Header) See Note 2 | | | | | | | |
| | 1 | FFH (ATM Cell Header) See Note 2 | | | | | | | |
| | 0 | F0H (ATM Cell Header) See Note 2 | | | | | | | |
| 4 | 3 | 00H (future use) | | | | | | | |
| | 2 | 00H (future use) | | | | | | | |
| | 1 | Message ID=03H | | | | | | | |
| | 0 | Message Sub ID=01H | | | | | | | |
| 5 | 3 | 0 | 1 | PP | Page# (3-1) | | | 0 | 0 |
| | 2 | Write = 1 | Page# (0) | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | Register Address | | | | | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6 | 3 | Mask value for register write - MSB | | | | | | | |
| | 2 | Mask value for register write | | | | | | | |
| | 1 | Mask value for register write | | | | | | | |
| | 0 | Mask value for register write - LSB | | | | | | | |
| 7 | 3 | Register value - MSB | | | | | | | |
| | 2 | Register value | | | | | | | |
| | 1 | Register value | | | | | | | |
| | 0 | Register value - LSB | | | | | | | |

Notes:
1. Five-bit DEST(4-0) field indicates the related RISC processor: 00001=IP, 00101=OP, 01001=RP.
2. Cell Header of FFFFFFF0H represents an ASPEN device control plane cell for ASPEN device management.

Writing and reading to/from control registers located in the internal memory space of the ASPEN device requires the use of a “Control Register Write” request message and a “Control Register Read” request message (see Figures 69 and 70 for the formats of these messages). The write or read requests are written by the host into one of the three ASPEN device input mailboxes based on the functional domain within the ASPEN device to which the message is related. This Data Sheet defines these control registers for each functional domain within the ASPEN device. The three domains are (IP) covering the UTOPIA Inlet Processor, (OP) covering the UTOPIA Outlet Processor, and (RP) covering the *CellBus* interface Rate Processor.

The word size of the both the request messages and the ASPEN device control registers is 32 bits. The Length field in word 0, byte 2 of each message applies only to the number of words in the message payload and does not cover the “control words” in word 0 and word 1.

**Figure 70. Control Register READ Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00100 | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 5H | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST(4-2) See Note 1 | | |
| | 0 | DEST(1-0) See Note 1 | | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | 00H | | | | | | | |
| | 2 | 00H | | | | | | | |
| | 1 | 00H | | | | | | | |
| | 0 | 00H | | | | | | | |
| 2 | 3 | 00H (future use CBRH) | | | | | | | |
| | 2 | 00H (future use CBRH) | | | | | | | |
| | 1 | 00H (TRH) | | | | | | | |
| | 0 | 00H (TRH) | | | | | | | |
| 3 | 3 | FFH (ATM Cell Header) See Note 2 | | | | | | | |
| | 2 | FFH (ATM Cell Header) See Note 2 | | | | | | | |
| | 1 | FFH (ATM Cell Header) See Note 2 | | | | | | | |
| | 0 | F0H (ATM Cell Header) See Note 2 | | | | | | | |
| 4 | 3 | 00H (future use) | | | | | | | |
| | 2 | 00H (future use) | | | | | | | |
| | 1 | Message ID=03H | | | | | | | |
| | 0 | Message Sub ID=02H | | | | | | | |
| 5 | 3 | 0 | 1 | PP | Page# (3-1) | | | 0 | 0 |
| | 2 | Read = 0 | Page# (0) | 0 | 0 | 0 | 0 | 0 | 0 |
| | 1 | Register Address | | | | | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6 | 3 | Register value - MSB | | | | | | | |
| | 2 | Register value | | | | | | | |
| | 1 | Register value return message only | | | | | | | |
| | 0 | Register value - LSB | | | | | | | |

Notes:
1. Five-bit DEST(4-0) field indicates the related RISC processor: 00001=IP, 00101=OP, 01001=RP.
2. Cell Header of FFFFFFF0H represents an ASPEN device control plane cell for ASPEN device management.

Response messages for register reads will have the same format as the read request message and will be returned in one of the ASPEN-to-host mailboxes. Values to be written to a control register may be masked (in word 6 of the write message) so that only the specified bits are written to the register (a zero masks the corresponding bit position from being updated, while a one enables updating).

## CONTROL REGISTER FORMATS

The functions of the ASPEN device control register memory locations related to the Inlet Processor (IP), Outlet Processor (OP) and Rate Processor (RP) are described in separate sections below. Each ASPEN device control register is identified by a hexadecimal address structure expressed as 'PP/Page#/Register Address'. These three fields are defined in the first column of each control register description.

In the following sections, the functions of a group of related control register words are first indicated in a 'map' table that shows four byte rows and eight bit columns for each 32-bit word, so that each bit can be identified by a description or Symbol name in the 32 cells shown for the word. The four bytes of a word are numbered from 3 (MSB, bits 31-24, listed first) to 0 (LSB, bits 7-0, listed last). After the map table, a 'description' table provides a description of the function of each bit, presented in the same order as in the map table. Reserved bytes and bits are not included in the 'description' tables. Reserved fields should not be written to by the host processor. An appropriate mask value should be used in control register write messages to avoid writing Reserved fields.

### INLET PROCESSOR (IP)-RELATED PARAMETERS

**IP Register Map No. 1**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/D/0 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | ITACTLD |
| 1/D/1 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | FLIF |
| 1/D/2 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | ARCN(2-0) | | |
| 1/D/3 | R/W | C0QID(15-8) | | | | | | | |
| | R/W | C0QID(7-0) | | | | | | | |
| | R/W | C0PCSDN | C0CLDIS | C0ENDST | C0DEST(4-0) | | | | |
| | R/W | C0IRH(5-0) | | | | | | C0SC4 | C0C/T |
| 1/D/4 | R/W | C1QID(15-8) | | | | | | | |
| | R/W | C1QID(7-0) | | | | | | | |
| | R/W | C1PCSDN | C1CLDIS | C1ENDST | C1DEST(4-0) | | | | |
| | R/W | C1IRH(5-0) | | | | | | C1SC4 | C1C/T |
| 1/D/5 | R/W | C2QID(15-8) | | | | | | | |
| | R/W | C2QID(7-0) | | | | | | | |
| | R/W | C2PCSDN | C2CLDIS | C2ENDST | C2DEST(4-0) | | | | |
| | R/W | C2IRH(5-0) | | | | | | C2SC4 | C2C/T |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/D/6 | R/W | C3QID(15-8) | | | | | | | |
| | R/W | C3QID(7-0) | | | | | | | |
| | R/W | C3PCSDN | C3CLDIS | C3ENDST | C3DEST(4-0) | | | | |
| | R/W | C3IRH(5-0) | | | | | | C3SC4 | C3C/T |
| 1/D/7 | R/W | C4QID(15-8) | | | | | | | |
| | R/W | C4QID(7-0) | | | | | | | |
| | R/W | C4PCSDN | RESERVED | C4ENDST | C4DEST(4-0) | | | | |
| | R/W | C4IRH(5-0) | | | | | | CRCG | C4C/T |
| 1/D/8 | R/W | GFC(3-0) | | | | VPI(7-4) | | | |
| | R/W | VPI(3-0) | | | | VCI(15-12) | | | |
| | R/W | VCI(11-4) | | | | | | | |
| | R/W | VCI(3-0) | | | | RESERVED | | | |
| 1/D/9 | R/W | TR | VP/VC | RESERVED | | | | | |
| | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/D/A | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | ASHIFT(1-0) | |
| 1/D/B | R/W | Residual Word (31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/D/C | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | IA | BN(1-0) | |
| 1/D/D | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | RSTPKTIDX |

**IP Bit Descriptions No. 1**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/0:0 | 0 | ITACTLD | **Automatic Connection Table Lookup Disable:** When set to 1, this bit disables the hardware mechanism for automatically requesting a connection table lookup when the ATM cell header is written into the ingress rate decoupling buffer. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/1:0 | 0 | FLIF | **Flush Ingress FIFO:** When set to 1, this bit flushes the ingress rate decoupling FIFO. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/2:0 | 2-1 | ARCN(2-0) | **Alternate Read Cell Number:** These bits are used to indirectly address ingress rate decoupling FIFO and IP control registers 1/C/1-1/C/7. When set to a value '000' => '100', allows the rate decoupling FIFO's addresses 0-15 to be used to indicate address space ARCN*16 +0 => ARCN*16+15. These bits are for internal TranSwitch use only. |
| 1/D/3:3<br>1/D/3:2 | 7-0<br>7-0 | C0QID(15-8)<br>C0QID(7-0) | **Cell 0 Queue Identifier:** 16-bit queue identification field used by the DMA to properly store the cell. These bits are for internal TranSwitch use only. |
| 1/D/3:1 | 7 | C0PCSDN | **Cell 0 Processing Done:** Setting this bit to 1 initiates the data controller to transfer Cell 0 from the Data Buffer to its destination specified by C0QID The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/3:1 | 6 | C0CLDIS | **Cell 0 Discard:** Setting this bit to 1 initiates the data controller to discard the cell stored in this location. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/3:1 | 5 | C0ENDST | **Cell 0 Enable Alternate Destination:** When this bit is set to 0, transfer destination is DMA controller for queuing. When set to 1 destination is specified by C0DEST. This bit is for internal TranSwitch use only. |
| 1/D/3:1 | 4-0 | C0DEST(4-0) | **Cell 0 Destination:** 5-bit destination value. These bits are for internal TranSwitch use only. |
| 1/D/3:0 | 7-2 | C0IRH(5-0) | **Cell 0 Internal Routing Header:** 6-bit internal bus routing field used in internal transfers. These bits are for internal TranSwitch use only. |
| 1/D/3:0 | 1 | C0SC4 | **Cell 0 Send Cell location 4:** When set to 1, the processor-generated cell in cell location 4 is queued immediately after this cell. This bit is for internal TranSwitch use only. |
| 1/D/3:0 | 0 | C0C/T | **Cell 0 *CellBus* Egress of Terminal Egress Queue Space:** When set to 1, the cell will be enqueued in Terminal Egress (outlet) queue space. Default is 0, i.e., the cell being enqueued to *CellBus* Egress (inlet) queue space. This bit is for internal TranSwitch use only. |
| 1/D/4:3<br>1/D/4:2 | 7-0<br>7-0 | C1QID(15-8)<br>C1QID(7-0) | **Cell 1 Queue Identifier:** 16-bit queue identification field used by the DMA to properly store the cell. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/4:1 | 7 | C1PCSDN | **Cell 1 Processing Done:** Setting this bit to 1 initiates the data controller to transfer Cell 1 from the Data Buffer to its destination specified by C1QID. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/4:1 | 6 | C1CLDIS | **Cell 1 Discard:** Setting this bit to 1 initiates the data controller to discard the cell stored in this location. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/4:1 | 5 | C1ENDST | **Cell 1 Enable Alternate Destination:** When this bit is set to 0, transfer destination is DMA controller for queuing. When set to 1 destination is specified by C1DEST. This bit is for internal TranSwitch use only. |
| 1/D/4:1 | 4-0 | C1DEST(4-0) | **Cell 1 Destination:** 5-bit destination value. These bits are for internal TranSwitch use only. |
| 1/D/4:0 | 7-2 | C1IRH(5-0) | **Cell 1 Internal Routing Header:** 6-bit internal bus routing field used in internal transfers. These bits are for internal TranSwitch use only. |
| 1/D/4:0 | 1 | C1SC4 | **Cell 1 Send Cell location 4:** When set to 1, the processor-generated cell in cell location 4 is queued immediately after this cell. This bit is for internal TranSwitch use only. |
| 1/D/4:0 | 0 | C1C/T | **Cell 1 *CellBus* Egress of Terminal Egress Queue Space:** When set to 1, the cell will be enqueued in Terminal Egress (outlet) queue space. Default is 0, i.e., the cell being enqueued to *CellBus* Egress (inlet) queue space. This bit is for internal TranSwitch use only. |
| 1/D/5:3<br>1/D/5:2 | 7-0<br>7-0 | C2QID(15-8)<br>C2QID(7-0) | **Cell 2 Queue Identifier:** 16-bit queue identification field used by the DMA to properly store the cell. These bits are for internal TranSwitch use only. |
| 1/D/5:1 | 7 | C2PCSDN | **Cell 2 Processing Done:** Setting this bit to 1 initiates the data controller to transfer Cell 2 from the Data Buffer to its destination specified by C2QID. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/5:1 | 6 | C2CLDIS | **Cell 2 Discard:** Setting this bit to 1 initiates the data controller to discard the cell stored in this location. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/5:1 | 5 | C2ENDST | **Cell 2 Enable Alternate Destination:** When this bit is set to 0, transfer destination is DMA controller for queuing. When set to 1 destination is specified by C2DEST. This bit is for internal TranSwitch use only. |
| 1/D/5:1 | 4-0 | C2DEST(4-0) | **Cell 2 Destination:** 5-bit destination value. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/5:0 | 7-2 | C2IRH(5-0) | **Cell 2 Internal Routing Header:** 6-bit internal bus routing field used in internal transfers. These bits are for internal TranSwitch use only. |
| 1/D/5:0 | 1 | C2SC4 | **Cell 2 Send Cell location 4:** When set to 1, processor generated cell in cell location 4 is queued immediately after this cell. This bit is for internal TranSwitch use only. |
| 1/D/5:0 | 0 | C2C/T | **Cell 2 *CellBus* Egress of Terminal Egress Queue Space:** When set to 1, the cell will be enqueued in Terminal Egress (outlet) queue space. Default is 0, i.e. the cell being enqueued to *CellBus* Egress (inlet) queue space. This bit is for internal TranSwitch use only. |
| 1/D/6:3<br>1/D/6:2 | 7-0<br>7-0 | C3QID(15-8)<br>C3QID(7-0) | **Cell 3 Queue Identifier:** 16-bit queue identification field used by the DMA to properly store the cell. These bits are for internal TranSwitch use only. |
| 1/D/6:1 | 7 | C3PCSDN | **Cell 3 Processing Done:** Setting this bit to 1 initiates the data controller to transfer Cell 3 from the Data Buffer to its destination specified by C3QID. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/5:1 | 6 | C3CLDIS | **Cell 3 Discard:** Setting this bit to 1 initiates the data controller to discard the cell stored in this location. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/6:1 | 5 | C3ENDST | **Cell 3 Enable Alternate Destination:** When this bit is set to 0, transfer destination is DMA controller for queuing. When set to 1 destination is specified by C3DEST. This bit is for internal TranSwitch use only. |
| 1/D/6:1 | 4-0 | C3DEST(4-0) | **Cell 3 Destination:** 5-bit destination value. These bits are for internal TranSwitch use only. |
| 1/D/6:0 | 7-2 | C3IRH(5-0) | **Cell 3 Internal Routing Header:** 6-bit internal bus routing field used in internal transfers. These bits are for internal TranSwitch use only. |
| 1/D/6:0 | 1 | C3SC4 | **Cell 3 Send Cell location 4:** When set to 1, the processor-generated cell in cell location 4 is queued immediately after this cell. This bit is for internal TranSwitch use only. |
| 1/D/6:0 | 0 | C3C/T | **Cell 3 *CellBus* Egress of Terminal Egress Queue Space:** When set to 1, the cell will be enqueued in Terminal Egress (outlet) queue space. Default is 0, i.e., the cell being enqueued to *CellBus* Egress (inlet) queue space. This bit is for internal TranSwitch use only. |
| 1/D/7:3<br>1/D/7:2 | 7-0<br>7-0 | C4QID(15-8)<br>C4QID(7-0) | **Cell 4 Queue Identifier:** 16-bit queue identification field used by the DMA to properly store the cell. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/7:1 | 7 | C4PCSDN | **Cell 4 Processing Done:** Setting this bit to 1 initiates an independent transfer of cell 4 from the Data Buffer to its destination specified by C4QID(15-0). The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This control bit is not used when cell buffer 4 transfers are initiated in "piggyback" mode using bit C3SC4. This bit is for internal TranSwitch use only. |
| 1/D/7:1 | 5 | C4ENDST | **Cell 4 Enable Alternate Destination:** When this bit is set to 0, transfer destination is DMA controller for queuing. When set to 1 destination is specified by C4DEST. This bit is for internal TranSwitch use only. |
| 1/D/7:1 | 4-0 | C4DEST(4-0) | **Cell 4 Destination:** 5-bit destination value. These bits are for internal TranSwitch use only. |
| 1/D/7:0 | 7-2 | C4IRH(5-0) | **Cell 4 Internal Routing Header:** 6-bit internal bus routing field used in internal transfers. These bits are for internal TranSwitch use only. |
| 1/D/7:0 | 1 | CRCG | When set to 1, CRC-10 generation and insertion is performed on Cell location 4 before a cell is queued. This bit is for internal TranSwitch use only. |
| 1/D/7:0 | 0 | C4C/T | **Cell 4 *CellBus* Egress of Terminal Egress Queue Space:** When set to 1, the cell will be enqueued in Terminal Egress (outlet) queue space. Default is 0, i.e., the cell being enqueued to *CellBus* Egress (inlet) queue space. This bit is for internal TranSwitch use only. |
| 1/D/8:3 | 7-4 | GFC(3-0) | **Generic Flow Control:** Used in header translation function to replace GFC field in the outgoing cell. Used in conjunction with VP/VC, TR, and COP3 control bit UNI. When UNI is 0, TR is 1, and VP/VC is 0, then GFC replaces the GFC of the cell which has completed processing. Note: CnPCSDN (n=3-0) must be set to 1 after this field, TR, and VP/VC are written. These bits are for internal TranSwitch use only. |
| 1/D/8:3<br>1/D/8:2 | 3-0<br>7-4 | VPI(7-4)<br>VPI(3-0) | **Virtual Path Identifier:** Used in header translation function to replace VPI field in the outgoing cell. Used in conjunction with VP/VC, and TR. When TR is 1, and VP/VC is 0, then VPI replaces the VPI of the cell which has completed processing. Note: CnPCSDN (n=3-0) must be set to 1 after this field, TR, and VP/VC is written. These bits are for internal TranSwitch use only. |
| 1/D/8:2<br>1/D/8:1<br>1/D/8:0 | 3-0<br>7-0<br>7-4 | VCI(15-12)<br>VCI(11-4)<br>VCI(3-0) | **Virtual Connection Identifier:** Used in Header translation function to replace VCI field in the outgoing cell. Used in conjunction with VP/VC, and TR. When TR is 1, and VP/VC is 1, then VCI replaces the VCI of the cell which has completed processing. Note: CnPCSDN (n=3-0) must be set to 1 after this field, TR, and VP/VC is written. These bits are for internal TranSwitch use only. |
| 1/D/9:3 | 7 | TR | **Translate:** When this bit is set to 1, this indicates that a translation function should be performed before the cell currently being processed is enqueued. Used in conjunction with VP/VC. This bit is reset to 0 after the operation is completed. This bit is for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/9:3 | 6 | VP/VC | **Virtual Path/Virtual Connection:** When this bit is set to 1, this indicates that a virtual connection translation is to be done before the cell currently being processed is enqueued. When set to 0, this indicates that a virtual path translation is to be done before the cell currently being processed is enqueued. Used in conjunction with VP/VC. This bit is for internal TranSwitch use only. |
| 1/D/A:0 | 1-0 | ASHIFT(1-0) | **Alignment Shift:** Number of octets to right shift residual with top word of ingress rate decoupling FIFO. These bits are for internal TranSwitch use only. |
| 1/D/B:3<br>1/D/B:2<br>1/D/B:1<br>1/D/B:0 | 7-0<br>7-0<br>7-0<br>7-0 | Residual Word<br>(31-24)<br>(23-16)<br>(15-8)<br>(7-0) | **Residual Word:** These bits are for internal TranSwitch use only. |
| 1/D/C:0 | 2 | IA | **Initiate Alignment:** Align the residual amount with top of ingress rate decoupling FIFO to create an octet aligned word. This bit is for internal TranSwitch use only. |
| 1/D/C:0 | 1-0 | BN(1-0) | **Bytes Needed for Packet Processing:** Used only when a final result needs less than a full word, i.e., a three-octet packet. These bits are for internal TranSwitch use only. |
| 1/D/D:0 | 0 | RSTPKTIDX | **Reset Index to Packet Information FIFO:** Set to 1 to reset, set to 0 to release. This bit is for internal TranSwitch use only. |



**IP Register Map No. 2**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/C/0 | R/W | NXT CELL (2-0) | | | CL CNT (2-0) | | | CTSS | RESERVED |
| | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/C/1 | R/W | C0 BIP-16 (15-8) | | | | | | | |
| | R/W | C0 BIP-16 (7-0) | | | | | | | |
| | R/W | C0 UDF2 (7-0) | | | | | | | |
| | R/W | C0 UDF1 (7-0) | | | | | | | |
| 1/C/2 | R/W | C0 PID (3-0) | | | | C0 TYPE (2-0) | | | C0 CRCE |
| | R/W | C0 INF (1-0) | | C0 PSC (4-0) | | | | | C0 PERR |
| | R/W | C0 SHPC | CO CTSS | RESERVED | | | | | |
| | R/W | RESERVED | | | | | | | |
| 1/C/3 | R/W | C1 BIP-16 (15-8) | | | | | | | |
| | R/W | C1 BIP-16 (7-0) | | | | | | | |
| | R/W | C1 UDF2 (7-0) | | | | | | | |
| | R/W | C1 UDF1 (7-0) | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/C/4 | R/W | C1 PID (3-0) | | | | C1 TYPE (2-0) | | | C1 CRCE |
| | R/W | C1 INF (1-0) | | C1 PSC (4-0) | | | | | C1 PERR |
| | R/W | C1 SHPC | C1 CTSS | RESERVED | | | | | |
| | R/W | RESERVED | | | | | | | |
| 1/C/5 | R/W | C2 BIP-16 (15-8) | | | | | | | |
| | R/W | C2 BIP-16 (7-0) | | | | | | | |
| | R/W | C2 UDF2 (7-0) | | | | | | | |
| | R/W | C2 UDF1 (7-0) | | | | | | | |
| 1/C/6 | R/W | C2 PID (3-0) | | | | C2 TYPE (2-0) | | | C2 CRCE |
| | R/W | C2 INF (1-0) | | C2 PSC (4-0) | | | | | C2 PERR |
| | R/W | C2 SHPC | C2 CTSS | RESERVED | | | | | |
| | R/W | RESERVED | | | | | | | |
| 1/C/7 | R/W | C3 BIP-16 (15-8) | | | | | | | |
| | R/W | C3 BIP-16 (7-0) | | | | | | | |
| | R/W | C3 UDF2 (7-0) | | | | | | | |
| | R/W | C3 UDF1 (7-0) | | | | | | | |
| 1/C/8 | R/W | C3 PID (3-0) | | | | C3 TYPE (2-0) | | | C3 CRCE |
| | R/W | C3 INF (1-0) | | C3 PSC (4-0) | | | | | C3 PERR |
| | R/W | C3 SHPC | C3 CTSS | RESERVED | | | | | |
| | R/W | RESERVED | | | | | | | |
| 1/C/9 | R/W | OA(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/C/A | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | PSIT2 |
| | R/W | PSIT(1-0) | | PSL(5-0) | | | | | |

**IP Bit Descriptions No. 2**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/0:3 | 7-5 | NXT CELL (2-0) | **Next Cell:** 3-bit Field indicating location of next cell to be processed by Inlet Processor:<br>000 - Cell 0<br>001 - Cell 1<br>010 - Cell 2<br>011 - Cell 3<br>111 - No cells in Buffer<br>These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/0:3 | 4-2 | CL CNT (2-0) | **Cell Count:** 3-bit counter (range 0-4) indicates number cells in rate decoupling FIFO. These bits are for internal TranSwitch use only. |
| 1/C/0:3 | 1 | CTSS | **Connection Table Search Status:** 1-bit<br>0 - Connection Table not available in CT scratchpad<br>1 - Connection Table available in CT scratchpad<br>This bit is for internal TranSwitch use only. |
| 1/C/1:3<br>1/C/1:2 | 7-0<br>7-0 | C0 BIP-16 (15-8)<br>C0 BIP-16 (7-0) | **Cell 0 Even Parity BIP-16 over cell payload:** These bits are for internal TranSwitch use only. |
| 1/C/1:1 | 7-0 | C0 UDF2 (7-0) | **Cell 0 User Defined Field 2:** Available only in Cell Mode using 16-bit wide interface. These bits are for internal TranSwitch use only. |
| 1/C/1:0 | 7-0 | C0 UDF1 (7-0) | **Cell 0 User Defined Field 1:** Available only in Cell Mode, commonly referred as HEC field. These bits are for internal TranSwitch use only. |
| 1/C/2:3 | 7-4 | C0 PID (3-0) | **Cell 0 PHYID**: Indicates which PHY layer device sent this cell. Field valid only in Multi-PHY ATM-layer emulation mode for both packets and cells. These bits are for internal TranSwitch use only. |
| 1/C/2:3 | 3-1 | C0 TYPE (2-0) | **3-bit Field indicating type of cell residing in this location:**<br>000 - Empty<br>001 - User Cell<br>010 - OAM Cell F4 Segment (VCI = 3)<br>011 - OAM Cell F4 End-to-End (VCI = 4)<br>100 - OAM Cell F5 Segment (PTI = 4)<br>101 - OAM Cell End-to-End (PTI = 5)<br>110 - OAM Cell Other (VCI <= 31, but not equal to 3 or 4 and PTI not equal to 4 or 5)<br>111 - Boot Cell (GFC =F, VPI = FF, VCI = FFFF in NNI mode and GFC ignored in UNI mode)<br>These bits are for internal TranSwitch use only. |
| 1/C/2:3 | 0 | C0 CRCE | **Cell 0 CRC-10 Error:** Indicates that the CRC-10 calculated across the payload of the ATM cell is incorrect. Information valid only for ATM OAM cells. This bit is for internal TranSwitch use only. |
| 1/C/2:2 | 7-6 | C0 INF (1-0) | **Cell 0 Information:**<br>00 - User Cell<br>01 - Reserved<br>10 - End of Message (AAL5), PTI=1 or 3<br>11 - Reserved<br>These bits are for internal TranSwitch use only. |
| 1/C/2:2 | 5-1 | C0 PSC (4-0) | **Cell 0 Packet Segment Count:** Number of Packet Segments inside Frame Chunk. Used in conjunction with PSIT, PSL, PSI. These bits are for internal TranSwitch use only. |
| 1/C/2:2 | 0 | C0 PERR | **Cell 0 Parity Error:** Indicates odd parity failure across the UTOPIA 2P interface. This bit is for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/2:1 | 7 | C0 SHPC | **Cell 0:** The current cell has the same header as previous cell. This bit is for internal TranSwitch use only. |
| 1/C/2:1 | 6 | C0 CTSS | Duplicate of CTSS in 1/C/0:3. |
| 1/C/3:3<br>1/C/3:2 | 7-0<br>7-0 | C1 BIP-16 (15-8)<br>C1 BIP-16 (7-0) | **Cell 1 Even Parity BIP-16 over cell payload:** These bits are for internal TranSwitch use only. |
| 1/C/3:1 | 7-0 | C1 UDF2 (7-0) | **Cell 1 User Defined Field 2:** Available only in Cell Mode using 16-bit wide interface. These bits are for internal TranSwitch use only. |
| 1/C/3:0 | 7-0 | C1 UDF1 (7-0) | **Cell 1 User Defined Field 1:** Available only in Cell Mode, commonly referred as HEC field. These bits are for internal TranSwitch use only. |
| 1/C/4:3 | 7-4 | C1 PID (3-0) | **Cell 1 PHYID**: Indicates which PHY layer device sent this cell. Field valid only in Multi-PHY ATM-layer emulation mode for both packets and cells. These bits are for internal TranSwitch use only. |
| 1/C/4:3 | 3-1 | C1 TYPE (2-0) | **3-bit Field indicating type of cell residing in this location:**<br>000 - Empty<br>001 - User Cell<br>010 - OAM Cell F4 Segment (VCI = 3)<br>011 - OAM Cell F4 End-to-End (VCI = 4)<br>100 - OAM Cell F5 Segment (PTI = 4)<br>101 - OAM Cell End-to-End (PTI = 5)<br>110 - OAM Cell Other (VCI <= 31, but not equal to 3 or 4 and PTI not equal to 4 or 5)<br>111 - Boot Cell (GFC =F, VPI = FF, VCI = FFFF in NNI mode and GFC ignored in UNI mode)<br>These bits are for internal TranSwitch use only. |
| 1/C/4:3 | 0 | C1 CRCE | **Cell 1 CRC-10 Error:** Indicates that the CRC-10 calculated across the payload of the ATM cell is incorrect. Information valid only for ATM OAM cells. This bit is for internal TranSwitch use only. |
| 1/C/4:2 | 7-6 | C1 INF (1-0) | **Cell 1 Information:**<br>00 - User Cell<br>01 - Reserved<br>10 - End of Message (AAL5), PTI=1 or 3<br>11 - Reserved<br>These bits are for internal TranSwitch use only. |
| 1/C/4:2 | 5-1 | C1 PSC (4-0) | **Cell 1 Packet Segment Count:** Number of Packet Segments inside Frame Chunk. Used in conjunction with PSIT, PSL, PSI. These bits are for internal TranSwitch use only. |
| 1/C/4:2 | 0 | C1 PERR | **Cell 1 Parity Error:** Indicates odd parity failure across the UTOPIA 2P interface. This bit is for internal TranSwitch use only. |
| 1/C/4:1 | 7 | C1 SHPC | **Cell 1:** The current cell has the same header as previous cell. This bit is for internal TranSwitch use only. |
| 1/C/4:1 | 6 | C1 CTSS | Duplicate of CTSS in 1/C/0:3. |
| 1/C/5:3<br>1/C/5:2 | 7-0<br>7-0 | C2 BIP-16 (15-8)<br>C2 BIP-16 (7-0) | **Cell 2 Even Parity BIP-16 over cell payload:** These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/5:1 | 7-0 | C2 UDF2 (7-0) | **Cell 2 User Defined Field 2:** Available only in Cell Mode using 16-bit wide interface. These bits are for internal TranSwitch use only. |
| 1/C/5:0 | 7-0 | C2 UDF1 (7-0) | **Cell 2 User Defined Field 1:** Available only in Cell Mode, commonly referred as HEC field. These bits are for internal TranSwitch use only. |
| 1/C/6:3 | 7-4 | C2 PID (3-0) | **Cell 2 PHYID**: Indicates which PHY layer device sent this cell. Field valid only in Multi-PHY ATM-layer emulation mode for both packets and cells. These bits are for internal TranSwitch use only. |
| 1/C/6:3 | 3-1 | C2 TYPE (2-0) | **3-bit Field indicating type of cell residing in this location:**<br>000 - Empty<br>001 - User Cell<br>010 - OAM Cell F4 Segment (VCI = 3)<br>011 - OAM Cell F4 End-to-End (VCI = 4)<br>100 - OAM Cell F5 Segment (PTI = 4)<br>101 - OAM Cell End-to-End (PTI = 5)<br>110 - OAM Cell Other (VCI <= 31, but not equal to 3 or 4 and PTI not equal to 4 or 5)<br>111 - Boot Cell (GFC =F, VPI = FF, VCI = FFFF in NNI mode and GFC ignored in UNI mode)<br>These bits are for internal TranSwitch use only. |
| 1/C/6:3 | 0 | C2 CRCE | **Cell 2 CRC-10 Error:** Indicates that the CRC-10 calculated across the payload of the ATM cell is incorrect. Information valid only for ATM OAM cells. This bit is for internal TranSwitch use only. |
| 1/C/6:2 | 7-6 | C2 INF (1-0) | **Cell 2 Information:**<br>00 - User Cell<br>01 - Reserved<br>10 - End of Message (AAL5), PTI=1 or 3<br>11 - Reserved<br>These bits are for internal TranSwitch use only. |
| 1/C/6:2 | 5-1 | C2 PSC (4-0) | **Cell 2 Packet Segment Count:** Number of Packet Segments inside Frame Chunk. Used in conjunction with PSIT, PSL, PSI. These bits are for internal TranSwitch use only. |
| 1/C/6:2 | 0 | C2 PERR | **Cell 2 Parity Error:** Indicates odd parity failure across the UTOPIA 2P interface. This bit is for internal TranSwitch use only. |
| 1/C/6:1 | 7 | C2 SHPC | **Cell 2:** The current cell has the same header as previous cell. This bit is for internal TranSwitch use only. |
| 1/C/7:3<br>1/C/7:2 | 7-0<br>7-0 | C3 BIP-16 (15-8)<br>C3 BIP-16 (7-0) | **Cell 3 Even Parity BIP-16 over cell payload:** These bits are for internal TranSwitch use only. |
| 1/C/7:1 | 7-0 | C3 UDF2 (7-0) | **Cell 3 User Defined Field 2:** Available only in Cell Mode using 16-bit wide interface. These bits are for internal TranSwitch use only. |
| 1/C/7:0 | 7-0 | C3 UDF1 (7-0) | **Cell 3 User Defined Field 1:** Available only in Cell Mode, commonly referred as HEC field. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/8:3 | 7-4 | C3 PID (3-0) | **Cell 3 PHYID**: Indicates which PHY layer device sent this cell. Field valid only in Multi-PHY ATM-layer emulation mode for both packets and cells. These bits are for internal TranSwitch use only. |
| 1/C/8:3 | 3-1 | C3 TYPE (2-0) | **3-bit Field indicating type of cell residing in this location:**<br>000 - Empty<br>001 - User Cell<br>010 - OAM Cell F4 Segment (VCI = 3)<br>011 - OAM Cell F4 End-to-End (VCI = 4)<br>100 - OAM Cell F5 Segment (PTI = 4)<br>101 - OAM Cell End-to-End (PTI = 5)<br>110 - OAM Cell Other (VCI <= 31, but not equal to 3 or 4 and PTI not equal to 4 or 5)<br>111 - Boot Cell (GFC =F, VPI = FF, VCI = FFFF in NNI mode and GFC ignored in UNI mode)<br>These bits are for internal TranSwitch use only. |
| 1/C/8:3 | 0 | C3 CRCE | **Cell 3 CRC-10 Error:** Indicates that the CRC-10 calculated across the payload of the ATM cell is incorrect. Information valid only for ATM OAM cells. This bit is for internal TranSwitch use only. |
| 1/C/8:2 | 7-6 | C3 INF (1-0) | **Cell 3 Information:**<br>00 - User Cell<br>01 - Reserved<br>10 - End of Message (AAL5), PTI=1 or 3<br>11 - Reserved<br>These bits are for internal TranSwitch use only. |
| 1/C/8:2 | 5-1 | C3 PSC (4-0) | **Cell 3 Packet Segment Count:** Number of Packet Segments inside Frame Chunk. Used in conjunction with PSIT, PSL, PSI. These bits are for internal TranSwitch use only. |
| 1/C/8:2 | 0 | C3 PERR | **Cell 3 Parity Error:** Indicates odd parity failure across the UTOPIA 2P interface. This bit is for internal TranSwitch use only. |
| 1/C/8:1 | 7 | C3 SHPC | **Cell 3:** The current cell has the same header as previous cell. This bit is for internal TranSwitch use only. |
| 1/C/8:1 | 6 | C3 CTSS | Duplicate of CTSS in 1/C/0:3. |
| 1/C/9:3<br>1/C/9:2<br>1/C/9:1<br>1/C/9:0 | 7-0<br>7-0<br>7-0<br>7-0 | OA(31-24)<br>OA(23-16)<br>OA(15-8)<br>OA(7-0) | Result of Octet Alignment process. These bits are for internal TranSwitch use only. |
| 1/C/A:1<br>1/C/A:0 | 0<br>7-6 | PSIT2<br>PSIT(1-0) | **Packet Segment Indicator Type:** 3-bit encoding describing what type of segment is contained in the Frame Chunk(s).<br>000 - Continuation<br>001 - Start of Frame<br>010 - End of Frame<br>011 - End of Cell<br>1XX - Abort<br>These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/A:0 | 5-0 | PSL(5-0) | **Packet Segment Length:** 6-bit length of PBIT segment, this is the byte location with respect to the beginning of the chunk. These bits are for internal TranSwitch use only. |

**IP Register Map No. 3**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/9/0 | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | CFGGPO1(2-0) | | | CFGGPO0(2-0) | | |
| | R/W | ENT4I | ENT3I | ENT2I | ENT1I | T4DIV(1-0) | | ENT4 | T3DIV1 |
| | R/W | T3DIV0 | ENT3 | T2DIV(1-0) | | ENT2 | T1DIV(1-0) | | ENT1 |

**IP Bit Descriptions No. 3**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:2 | 5-3 | CFGGPO1(2-0) | **Configure General Purpose Output 1:** These bits 5-3 contain a binary code that controls the signal on Inlet Processor Status output lead IP1, as follows:<br>000: Timer 1 rollover: IP1 held high when Timer 1 is all 1s<br>001: Timer 2 rollover: IP1 held high when Timer 2 is all 1s<br>010: Timer 3 rollover: IP1 held high when Timer 3 is all 1s<br>011: Timer 4 rollover: IP1 held high when Timer 4 is all 1s<br>100: Internal Test Point 0:<br>101: Internal Test Point 1:<br>110: IP1 held low<br>111: IP1 held high |
| 1/9/0:2 | 2-0 | CFGGPO0(2-0) | **Configure General Purpose Output 0:** These bits 2-0 contain a binary code that controls the signal on Inlet Processor Status output lead IP0, as follows:<br>000: Timer 1 rollover: IP0 held high when Timer 1 is all 1s<br>001: Timer 2 rollover: IP0 held high when Timer 2 is all 1s<br>010: Timer 3 rollover: IP0 held high when Timer 3 is all 1s<br>011: Timer 4 rollover: IP0 held high when Timer 4 is all 1s<br>100: Internal Test Point 0:<br>101: Internal Test Point 1:<br>110: IP0 held low<br>111: IP0 held high |
| 1/9/0:1 | 7 | ENT4I | **Enable Timer 4 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 4 is all ones. |
| 1/9/0:1 | 6 | ENT3I | **Enable Timer 3 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 3 is all ones. |
| 1/9/0:1 | 5 | ENT2I | **Enable Timer 2 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 2 is all ones. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:1 | 4 | ENT1I | **Enable Timer 1 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 1 is all ones. |
| 1/9/0:1 | 3-2 | T4DIV(1-0) | **Timer 4 Division Mode:** These bits 3-2 contain a binary code that controls the clock division ratio for Timer 4, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:1 | 1 | ENT4 | **Enable Timer 4:** When set to 1, this bit enables Timer 4. |
| 1/9/0:1<br>1/9/0:0 | 0<br>7 | T3DIV(1-0) | **Timer 3 Division Mode:** These bits 0 and 7 contain a binary code that controls the clock division ratio for Timer 3, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 6 | ENT3 | **Enable Timer 3:** When set to 1, this bit enables Timer 2. |
| 1/9/0:0 | 5-4 | T2DIV(1-0) | **Timer 2 Division Mode:** These bits 5-4 contain a binary code that controls the clock division ratio for Timer 2, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 3 | ENT2 | **Enable Timer 4:** When set to 1, this bit enables Timer 2. |
| 1/9/0:0 | 2-1 | T1DIV(1-0) | **Timer 1 Division Mode:** These bits 2-1 contain a binary code that controls the clock division ratio for Timer 1, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 0 | ENT1 | **Enable Timer 1:** When set to 1, this bit enables Timer 1. |



**IP Register Map No. 4**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/8/0 | R/W | Timer 1 (32 bits) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/1 | R/W | Timer 2 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/8/2 | R/W | Timer 2 (32 bits) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/3 | R/W | Timer 3 Preload Value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Timer 3 (16 bits) | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/4 | R/W | Timer 4 Preload Value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Timer 4 (16 bits) | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/5 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | Timer Status | | | |

**IP Bit Descriptions No. 4**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/8/0:3-0 | 7-0 | Timer 1 | **Timer 1:** This is a 32-bit rollover timer. |
| 1/8/1:3-0 | 7-0 | Timer 2 Preload | **Timer 2 Preload Value:** The 32-bit Timer 2 will initially start with this value, and loads this value in after rollover. |
| 1/8/2:3-0 | 7-0 | Timer 2 | **Timer 2:** This is a 32-bit rollover timer. |
| 1/8/3:3-2 | 7-0 | Timer 3 Preload | **Timer 3 Preload Value:** The 16-bit Timer 3 will initially start with this value, and loads this value in after rollover. |
| 1/8/3:1-0 | 7-0 | Timer 3 | **Timer 3:** This is a 16-bit rollover timer. |
| 1/8/4:3-2 | 7-0 | Timer 4 Preload | **Timer 4 Preload Value:** The 16-bit Timer 4 will initially start with this value, and loads this value in after rollover. |
| 1/8/4:1-0 | 7-0 | Timer 4 | **Timer 4:** This is a 16-bit rollover timer. |
| 1/8/5:0 | 3-0 | Timer Status | **Timer Status:** These four bits (3-0) indicate the rollover events of the four Timers (4-1). A 1 indicates Timer rollover. These status bits do not clear automatically but must be reset to 0 by writing to the register. |

**IP Register Map No. 5**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/7/1D | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | | | WDTIMER(19-16) | | | |
| | R/W | WDTIMER(15-8) | | | | | | | |
| | R/W | WDTIMER(7-0) | | | | | | | |
| 0/7/1E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | WDCLR | WDEXP | WDENT |
| 0/7/1F | R/W | S/C | Update Mask (14-8) | | | | | | |
| | R/W | Update Mask (7-0) | | | | | | | |
| | R/W | RESERVED | Event (14-8) | | | | | | |
| | R/W | Event (7-0) | | | | | | | |

**IP Bit Descriptions No. 5**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/7/1D:2<br>0/7/1D:1<br>0/7/1D:0 | 3-0<br>7-0<br>7-0 | WDTIMER(19-16)<br>WDTIMER(15-8)<br>WDTIMER(7-0) | **Watchdog Timer:** This field is a 20-bit timer. When enabled (by control bit WDENT = 1, see below), the watchdog timer will count up at the PCLK clock rate. If the timer is not reset by WDCLR, the timer will expire (all 1s). When the timer expires, the ASPEN device will be forced into a restart state, and will reload boot firmware. **Note**: When debug mode is active, and the Inlet Processor is in a frozen state, the watchdog timer is also in a frozen state. |
| 0/7/1E:0 | 2 | WDCLR | **Watchdog Clear:** When this bit is set to 1, the watchdog timer is cleared, and then the bit is automatically reset to 0. This bit is initialized to 0 at device reset. |
| 0/7/1E:0 | 1 | WDEXP | **Watchdog Expired:** This bit becomes set to 1 when the watchdog timer expires (all 1s). It is reset to 0 only when a hardware reset is performed (lead $\overline{\text{RESET}}$ low). |
| 0/7/1E:0 | 0 | WDENT | **Watchdog Timer Enable:** When this bit is set to 1, the watchdog timer is enabled. Once set to 1, the watchdog timer cannot be disabled except by a hardware or firmware reset (leads $\overline{\text{RESET}}$ or $\overline{\text{FWRST}}$ low). |
| 0/7/1F:3 | 7 | S/C | **Set/Clear:** When this bit is set to 1, all Update Maskn bits (n=14-0) which are set to 0 will cause the corresponding Eventn bit to be set to 1. When this bit is set to 0, all Update Maskn bits (n=14-0) which are set to 0 will cause the corresponding Eventn bit to be set to 0. This bit is for internal TranSwitch use only. |
| 0/7/1F:3<br>0/7/1F:2 | 6-0<br>7-0 | Update Mask (14-8)<br>Update Mask (7-0) | **Update Mask:** When an individual Update Mask bit is set to 1, the corresponding Event bit is not modified. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/7/1F:1<br>0/7/1F:0 | 6-0<br>7-0 | Event (14-8)<br>Event (7-0) | **Event:** Latched Event status. These bits are for internal TranSwitch use only. |

**IP Register Map No. 6**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/0 | R/W | RESET | | | | | | | |
| | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1 | R/W | RESERVED | | | | | | | |
| | R/W | ITU1 | ITPHYEN | ITLMODE | UNI | ITCELLSIZE(3-0) | | | |
| | R/W | $\overline{\text{ITHECCHK}}$ | IT16b | ITONLINE | ITCHK16 | CTCA | RESERVED | | |
| | R/W | RESERVED | | | | | | | |
| 0/6/2 | R/W | ITE15 | | ITPHY15ADDR(4-0) | | | | | |
| | R/W | ITE14 | | ITPHY14ADDR(4-0) | | | | | |
| | R/W | ITE13 | | ITPHY13ADDR(4-0) | | | | | |
| | R/W | ITE12 | | ITPHY12ADDR(4-0) | | | | | |
| 0/6/3 | R/W | ITE11 | | ITPHY11ADDR(4-0) | | | | | |
| | R/W | ITE10 | | ITPHY10ADDR(4-0) | | | | | |
| | R/W | ITE9 | | ITPHY9ADDR(4-0) | | | | | |
| | R/W | ITE8 | | ITPHY8ADDR(4-0) | | | | | |
| 0/6/4 | R/W | ITE7 | | ITPHY7ADDR(4-0) | | | | | |
| | R/W | ITE6 | | ITPHY6ADDR(4-0) | | | | | |
| | R/W | ITE5 | | ITPHY5ADDR(4-0) | | | | | |
| | R/W | ITE4 | | ITPHY4ADDR(4-0) | | | | | |
| 0/6/5 | R/W | ITE3 | | ITPHY3ADDR(4-0) | | | | | |
| | R/W | ITE2 | | ITPHY2ADDR(4-0) | | | | | |
| | R/W | ITE1 | | ITPHY1ADDR(4-0) | | | | | |
| | R/W | ITE0 | | ITPHY0ADDR(4-0) | | | | | |
| 0/6/6 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | DMINF | ITPARDATA | RESERVED | MINFL(4-0) | | | | |
| 0/6/7 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | AVAIL |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/1C | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1D | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1F | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/20 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | IRSTUT | ICTRCHK |

**IP Bit Descriptions No. 6**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/0:3 | 7-0 | RESET | **Software Reset:** Writing a 91 Hex into this location will generate a software reset to the component. Writing other than 91 Hex to this location will remove the ASPEN device from the reset state. Reading this location will return a 00 Hex if the ASPEN device is not in reset and 01 Hex if it is in reset. Software reset will reset all ingress hardware state machines synchronously to their home state, and all FIFOs in the *CellBus* domain will be flushed. |
| 0/6/1:2 | 7 | ITU1 | **Ingress Terminal UTOPIA Level 1 Select:** Setting this bit to 1 puts the UTOPIA interface into UTOPIA Level 1 mode (Single-PHY). When this bit is set to 0, the interface is in UTOPIA Level 2 mode (Multi-PHY). |
| 0/6/1:2 | 6 | ITPHYEN | **Ingress Terminal PHY Layer Emulation Enable:** When set to 1, this bit enables PHY Layer emulation in UTOPIA modes. When set to 0, the device operates with ATM Layer emulation. |
| 0/6/1:2 | 5 | ITLMODE | **Ingress Terminal Line Mode Select:** When set to 1, this bit enables Packet Mode operation of the UTOPIA interface. When set to 0, the interface operates in Cell Mode. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/1:2 | 4 | UNI | **Upper Nibble Ignore:** When this bit is set to 1, the upper nibble of the VPI is ignored during header lookup. |
| 0/6/1:2 | 3-0 | ITCELLSIZE(3-0) | **Ingress Terminal Cell Size Select:** These bits set the cell size for the Inlet UTOPIA Interface. Actual cell size is 53 plus the decimal value of this field (bit 3 is MSB). Values of ITCELLSIZE beyond 11 will be treated as equal to 11. |
| 0/6/1:1 | 7 | $\overline{\text{ITHECCHK}}$ | **Ingress Terminal HEC Check:** When this bit is set to 0, HEC checking is enabled for the Ingress Terminal Interface. When set to 1, HEC checking is disabled. |
| 0/6/1:1 | 6 | IT16b | **Ingress Terminal 16-bit Mode Select:** When this bit is set to 1, 16-bit UTOPIA Level 2P mode is selected. When this bit is set to 0, 8-bit mode is selected. |
| 0/6/1:1 | 5 | ITONLINE | **Ingress Terminal Online:** When this bit is set to 1, the Ingress Terminal Interface is active (online). When it is set to 0, all UTOPIA-related output leads are set to the tristate condition (offline) and no cells are accepted from the interface. |
| 0/6/1:1 | 4 | ITCHK16 | **Ingress Terminal Multi-PHY Chunk Size:** When this bit is set to 1, the transfer size is 16 bytes. When set to 0, the transfer size is 48 bytes. |
| 0/6/1:1 | 3 | CTCA | **CTSA and CAVL Interrupt Combination Select:** When this bit is set to 1, the event that drives the CTSA interrupt indicates that the second of the conditions CTSA and CAVL has occurred. When set to 0, this event indicates that the connection table status information is valid and available. |
| 0/6/2:3-0<br>0/6/3:3-0<br>0/6/4:3-0<br>0/6/5:3-0 | 7<br>7<br>7<br>7 | ITE(15-12)<br>ITE(11-8)<br>ITE(7-4)<br>ITE(3-0) | **Ingress Terminal Enable for PHYs 15-0:** For each one of these bits that is set to 0, all cells going to the corresponding PHY are discarded and that PHY is no longer polled in Multi-PHY mode. |
| 0/6/2:3-0<br>0/6/3:3-0<br>0/6/4:3-0<br>0/6/5:3-0 | 4-0<br>4-0<br>4-0<br>4-0 | ITPHYnADDR(4-0)<br>(n = 15 for 0/6/2:3<br>n = 0 for 0/6/5:0) | **Ingress Terminal PHY #n Address Code:** This is a 5-bit UTOPIA Level 2 address that can be set for mapping each of 16 PHYs to a UTOPIA address value in the range 0 to 30 (bit 4 is the MSB). |
| 0/6/6:0 | 7 | DMINF | **Discard Minimum Frame:** When this bit is set to 1, frames with a length less than MINFL(4-0) bytes are discarded. |
| 0/6/6:0 | 6 | ITPARDATA | **Parity Data:** When this bit is set to 1, UTOPIA odd parity is calculated over the ITDATA bus only. When it is 0, UTOPIA odd parity is calculated over ITDATA, ITSOF, ITEOF, ITMS, and ITABT. |
| 0/6/6:0 | 4-0 | MINFL(4-0) | **Minimum Frame Length:** This 5-bit field specifies the minimum frame length for incoming frames when in UTOPIA Level 2P mode (bit 4 is MSB). If the frame length is shorter than this minimum, the frame is discarded if control bit DMINF is set to 1. |
| 0/6/7:0 | 0 | AVAIL | **Host Mailbox Available:** When this bit is set to 1, it indicates that the IP-to-host mailbox is free for the ASPEN device to send the host a message. This bit is for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/20:0 | 1 | IRSTUT | **Ingress Reset UTOPIA:** A 1 forces a reset of ingress UTOPIA interface. A 0 clears the reset condition. This bit is for internal TranSwitch use only. |
| 0/6/20:0 | 0 | ICTRCHK | **Ingress Connection Table Reference Check:** When set to 1, a comparison will be performed to see if a connection table that is returned is the same as previous by comparing the CT reference. A duplicate connection table read will result in the second fetch being discarded in order to maintain table coherency with respect to the first writeback. This bit is for internal TranSwitch use only. |

## OUTLET PROCESSOR (OP)-RELATED PARAMETERS

### OP Register Map No. 1

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/D/0 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | MGP1(3-1) | | |
| | R/W | MGP1(0) | MGP2(3-0) | | | | MGMODE | ETACTLD | F/E |
| 1/D/1 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | FLEF |
| 1/D/2 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | SPPHYID(4-0) | | | | SPONLY | CRCG | SCP |
| 1/D/3 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | PCSND | CLDIS |
| 1/D/4 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Table Offset (7-0) | | | | | | | |
| | R/W | Table Size (7-0) | | | | | | | |
| 1/D/5 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | ALTRDEN | ALTADD(4-0) | | | | |

**OP Bit Descriptions No. 1**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/0:1<br>1/D/0:0 | 2-0<br>7 | MGP1(3-1)<br>MGP1(0) | **Message Compiler Generation Parameter 1:** This 4-bit field is used in the generation of the lookup message. The first 12 bits of the message are used to index the VPI lookup table. {GFC/VPI[27:16+MGP(1)],QID[16+(MGP(1) - 1):16]}, where, if MGP(1)= 0, QID is not used in the lookup. |
| 1/D/0:0 | 6-3 | MGP2(3-0) | **Message Compiler Generation Parameter 2:** This 4-bit field is used in the generation of the lookup message. The second 16 bits of the message are used to index the connection table in direct lookup mode, and are used in the calculation of a hash index in hashing mode.<br>{VCI[15:MGP(2)],QID[(MGP(2) - 1):0]}, where, if MGP(2)=0, QID is not used in the lookup. |
| 1/D/0:0 | 2 | MGMODE | **Message Generation Mode:** In automatic connection table lookup mode, the message compiler sends a 28-bit message to the header lookup block in the DMA. MGMODE defines the format of the message content that is used in the lookup. The formats are:<br>MGMODE=1: lookup is based on VPI/VCI and QID, {GFC/ VPI[27:16+MGP(1)], QID[16+(MGP(1) - 1):16], VCI[15:MGP(2)],QID[(MGP(2) - 1):0]}, where, if MGP(1)= 0, MGP(2)=0, QID is not used in the lookup, and it defaults to {GFC[27:24],VPI[23:16],VCI[15:0]}<br>MGMODE=0: lookup is based on QID. |
| 1/D/0:0 | 1 | ETACTLD | **Automatic Connection Table Lookup Disable:** When this bit is set to 1, it disables the hardware mechanism for automatically requesting a connection table lookup when the ATM cell header is written into the egress rate decoupling buffer. |
| 1/D/0:0 | 0 | F/E | **Full/Empty Control for PFS:** When this bit is set to 1, and bit PFSn is set to 1, indicates the egress FIFO current depth is 1 cell and the second cell is being filled. When this bit is set to 1, and bit PFSn is set to 0, indicates the egress FIFO depth changes from 2 to 1. When this bit is set to 0, and bit PFSn is set to 1, indicates the egress FIFO depth is 0. When this bit is set to 0 and bit PFSn is set to 0, indicates current egress FIFO depth is 0 and first cell is being filled. This bit is for internal TranSwitch use only. |
| 1/D/1:0 | 0 | FLEF | **Flush Egress FIFO:** When set to 1, this bit flushes the egress rate decoupling FIFO. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/2:0 | 7-3 | SPPHYID(4-0) | **Scratchpad PHY ID:** Only applicable when used with SPONLY. Identifies the UTOPIA logical port number where the scratchpad should be sent. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/D/2:0 | 2 | SPONLY | **Scratchpad Only:** When set to 1, initiates a transfer of the scratchpad buffer to the UTOPIA port identified in SPPHYID. This bit is for internal TranSwitch use only. |
| 1/D/2:0 | 1 | CRCG | **CRC-10 Generate:** When this bit is set to 1, a CRC-10 will be generated over the scratchpad cell payload and inserted into the last 10 bits of cell before transmission via the UTOPIA 2P interface. This bit is for internal TranSwitch use only. |
| 1/D/2:0 | 0 | SCP | **Scratch Pad:** This bit is used to indirectly address the egress rate decoupling FIFO. When this bit is set to 1, the cell buffer for the scratch pad is available for access in the coprocessor 2 address 0-15. When this bit is set to 0, the cell buffer location pointed to by NXT PHY is available for access in coprocessor 2 address 0-15. This bit is used for code compression since the RISC instruction set does not allow indirect or relative addressing of coprocessor address space. This bit is for internal TranSwitch use only. |
| 1/D/3:0 | 1 | PCSND | **Processing Done:** Setting this bit to 1 initiates the data controller to make the cell available for transfer from the Data Buffer to the UTOPIA 2P outlet port 'n'. The data controller will indicate that the operation has been completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/3:0 | 0 | CLDIS | **Cell Discard:** Setting this bit to 1 initiates the data controller to discard the cell stored in this location. The data controller will indicate that the operation has completed successfully by resetting this bit to 0. This bit is for internal TranSwitch use only. |
| 1/D/4:1 | 7-0 | Table Offset (7-0) | **Table Offset:** These 8 bits are used when complete record transfers are not required. These bits are for internal TranSwitch use only. |
| 1/D/4:0 | 7-0 | Table Size (7-0) | **Table Size:** These 8 bits indicate the length of a table record. These bits are for internal TranSwitch use only. |
| 1/D/5:0 | 5 | ALTRDEN | **Alternate Read Enable:** This bit enables reading of Egress Data FIFO. Used for test purposes only. This bit is for internal TranSwitch use only. |
| 1/D/5:0 | 4-0 | ALTADD(4-0) | **Alternate Address:** This 5-bit address is used as an alternate read interface for Egress Data FIFO. Used in test mode only. These bits are for internal TranSwitch use only. |

**OP Register Map No. 2**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/C/0 | R/W | NXT PHY (4-0) | | | | | CTSS | RESERVED | |
| | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/C/1 | R/W | ABTINFO(20-13) | | | | | | | |
| | R/W | ABTINFO(12-5) | | | | | | | |
| | R/W | ABTINFO(4-0) | | | | | RESERVED | | |
| | R/W | RESERVED | | | | | | | |
| 1/C/2 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | PFS15 | PFS14 | PFS13 | PFS12 | PFS11 | PFS10 | PFS9 | PFS8 |
| | R/W | PFS7 | PFS6 | PFS5 | PFS4 | PFS3 | PFS2 | PFS1 | PFS0 |
| 1/C/3 | R/W | PBFL15 | | PBFL14 | | PBFL13 | | PBFL12 | |
| | R/W | PBFL11 | | PBFL10 | | PBFL9 | | PBFL8 | |
| | R/W | PBFL7 | | PBFL6 | | PBFL5 | | PBFL4 | |
| | R/W | PBFL3 | | PBFL2 | | PBFL1 | | PBFL0 | |

**OP Bit Descriptions No. 2**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/0:3 | 7-3 | NXT PHY (4-0) | **Next PHY:** This is a 5-bit field indicating location of next cell to be processed by Outlet Processor:<br>0XXXX: Cell for PHY n=XXXX<br>10000: Cell Buffer Scratch pad<br>11111: No cells in Buffer<br>These bits are for internal TranSwitch use only. |
| 1/C/0:3 | 2 | CTSS | **Connection Table Search Status:** When this bit is a 1, search status is found. When this bit is 0, search status is not found. This bit is for internal TranSwitch use only. |
| 1/C/1:3<br>1/C/1:2<br>1/C/1:1 | 7-0<br>7-0<br>7-3 | ABTINFO(20-13)<br>ABTINFO(12-5)<br>ABTINFO(4-0) | **Abort Information:** Upper 5 bits are the UTOPIA PHY ID of the port. Lower 16 bits are the Outlet Queue ID. These bits are for internal TranSwitch use only. |
| 1/C/2:1<br>1/C/2:0 | 7-0<br>7-0 | PFS15-PFS8<br>PFS7-PFS0 | **PHY FIFO Status for PHY n (n=15-0):** These bits indicate the state of the 2-cell FIFO for PHY n based on control bit F/E. When bit F/E is set to 1, and bit PFSn is set to 1, indicates Egress FIFO current depth is 1 cell and the second cell being filled. When bit F/E is set to 1, and bit PFSn is set to 0, indicates Egress FIFO depth changes from 2 to 1. When bit F/E is set to 0, and bit PFSn is set to 1, indicates Egress FIFO depth is 0. When bit F/E is set to 0, and bit PFSn is set to 0, indicates Egress FIFO current depth is 0 and first cell is being filled. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/C/3:3<br>1/C/3:2<br>1/C/3:1<br>1/C/3:0 | 7-0<br>7-0<br>7-0<br>7-0 | PBFL15-PBFL12<br>PBFL11-PBFL8<br>PBFL7-PBFL4<br>PBFL3-PBFL0 | **PHY Buffer Fill Level for PHY n (n=15-0):** These bit-pairs indicate the depth of the 2-cell FIFO for PHY n.<br>00: 1 cell present<br>01: empty<br>10: 2 cells present<br>11: not defined |

**OP Register Map No. 3**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/B/14 | R/W | CBRH for Multicast (15-8) | | | | | | | |
| | R/W | CBRH for Multicast (7-0) | | | | | | | |
| | R/W | TRH for Multicast (15-8) | | | | | | | |
| | R/W | TRH for Multicast (7-0) | | | | | | | |
| 1/B/15 | R/W | ATM Header | | | | | | | |
| | R/W | ATM Header | | | | | | | |
| | R/W | ATM Header | | | | | | | |
| | R/W | ATM Header | | | | | | | |
| 1/B/16 | R/W | Cell Payload Word 1 | | | | | | | |
| | R/W | Cell Payload Word 1 | | | | | | | |
| | R/W | Cell Payload Word 1 | | | | | | | |
| | R/W | Cell Payload Word 1 | | | | | | | |
| 1/B/17 | R/W | Cell Payload Word 2 | | | | | | | |
| | R/W | Cell Payload Word 2 | | | | | | | |
| | R/W | Cell Payload Word 2 | | | | | | | |
| | R/W | Cell Payload Word 2 | | | | | | | |
| 1/B/18 | R/W | Cell Payload Word 3 | | | | | | | |
| | R/W | Cell Payload Word 3 | | | | | | | |
| | R/W | Cell Payload Word 3 | | | | | | | |
| | R/W | Cell Payload Word 3 | | | | | | | |
| 1/B/19 | R/W | Cell Payload Word 4 | | | | | | | |
| | R/W | Cell Payload Word 4 | | | | | | | |
| | R/W | Cell Payload Word 4 | | | | | | | |
| | R/W | Cell Payload Word 4 | | | | | | | |
| 1/B/1A | R/W | Cell Payload Word 5 | | | | | | | |
| | R/W | Cell Payload Word 5 | | | | | | | |
| | R/W | Cell Payload Word 5 | | | | | | | |
| | R/W | Cell Payload Word 5 | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/B/1B | R/W | Cell Payload Word 6 | | | | | | | |
| | R/W | Cell Payload Word 6 | | | | | | | |
| | R/W | Cell Payload Word 6 | | | | | | | |
| | R/W | Cell Payload Word 6 | | | | | | | |
| 1/B/1C | R/W | Cell Payload Word 7 | | | | | | | |
| | R/W | Cell Payload Word 7 | | | | | | | |
| | R/W | Cell Payload Word 7 | | | | | | | |
| | R/W | Cell Payload Word 7 | | | | | | | |
| 1/B/1D | R/W | Cell Payload Word 8 | | | | | | | |
| | R/W | Cell Payload Word 8 | | | | | | | |
| | R/W | Cell Payload Word 8 | | | | | | | |
| | R/W | Cell Payload Word 8 | | | | | | | |
| 1/B/1E | R/W | Cell Payload Word 9 | | | | | | | |
| | R/W | Cell Payload Word 9 | | | | | | | |
| | R/W | Cell Payload Word 9 | | | | | | | |
| | R/W | Cell Payload Word 9 | | | | | | | |
| 1/B/1F | R/W | Cell Payload Word 10 | | | | | | | |
| | R/W | Cell Payload Word 10 | | | | | | | |
| | R/W | Cell Payload Word 10 | | | | | | | |
| | R/W | Cell Payload Word 10 | | | | | | | |
| 1/B/20 | R/W | Cell Payload Word 11 | | | | | | | |
| | R/W | Cell Payload Word 11 | | | | | | | |
| | R/W | Cell Payload Word 11 | | | | | | | |
| | R/W | Cell Payload Word 11 | | | | | | | |
| 1/B/21 | R/W | Cell Payload Word 12 | | | | | | | |
| | R/W | Cell Payload Word 12 | | | | | | | |
| | R/W | Cell Payload Word 12 | | | | | | | |
| | R/W | Cell Payload Word 12 | | | | | | | |
| 1/B/22 | R/W | Queue for Multicast Leaf 1 | | | | | | | |
| | R/W | Queue for Multicast Leaf 1 | | | | | | | |
| | R/W | Queue for Multicast Leaf 2 | | | | | | | |
| | R/W | Queue for Multicast Leaf 2 | | | | | | | |
| 1/B/23 | R/W | Queue for Multicast Leaf 3 | | | | | | | |
| | R/W | Queue for Multicast Leaf 3 | | | | | | | |
| | R/W | Queue for Multicast Leaf 4 | | | | | | | |
| | R/W | Queue for Multicast Leaf 4 | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/B/24 | R/W | Queue for Multicast Leaf 5 | | | | | | | |
| | R/W | Queue for Multicast Leaf 5 | | | | | | | |
| | R/W | Queue for Multicast Leaf 6 | | | | | | | |
| | R/W | Queue for Multicast Leaf 6 | | | | | | | |
| 1/B/25 | R/W | Queue for Multicast Leaf 7 | | | | | | | |
| | R/W | Queue for Multicast Leaf 7 | | | | | | | |
| | R/W | Queue for Multicast Leaf 8 | | | | | | | |
| | R/W | Queue for Multicast Leaf 8 | | | | | | | |
| 1/B/26 | R/W | Queue for Multicast Leaf 9 | | | | | | | |
| | R/W | Queue for Multicast Leaf 9 | | | | | | | |
| | R/W | Queue for Multicast Leaf 10 | | | | | | | |
| | R/W | Queue for Multicast Leaf 10 | | | | | | | |
| 1/B/27 | R/W | Queue for Multicast Leaf 11 | | | | | | | |
| | R/W | Queue for Multicast Leaf 11 | | | | | | | |
| | R/W | Queue for Multicast Leaf 12 | | | | | | | |
| | R/W | Queue for Multicast Leaf 12 | | | | | | | |
| 1/B/28 | R/W | Queue for Multicast Leaf 13 | | | | | | | |
| | R/W | Queue for Multicast Leaf 13 | | | | | | | |
| | R/W | Queue for Multicast Leaf 14 | | | | | | | |
| | R/W | Queue for Multicast Leaf 14 | | | | | | | |
| 1/B/29 | R/W | Queue for Multicast Leaf 15 | | | | | | | |
| | R/W | Queue for Multicast Leaf 15 | | | | | | | |
| | R/W | Queue for Multicast Leaf 16 | | | | | | | |
| | R/W | Queue for Multicast Leaf 16 | | | | | | | |
| 1/B/2A | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | LMST |
| 1/B/2B | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R | RESERVED | | | | | | | MIP |
| 1/B/2C | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | Enqueue Interval |
| | R/W | Enqueue Interval | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/B/2D | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | R/W | Multicast Cell Queue ID | | | | | | | |
| | R/W | Multicast Cell Queue ID | | | | | | | |

**OP Bit Descriptions No. 3**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/B/14:3<br>1/B/14:2 | 7-0<br>7-0 | CBRH for Multicast | ***CellBus* Routing Header for Multicast:** For multicast enqueues to the outlet queue space, this field is not used. If a cell is enqueued into an ingress queue from the multicast RAM, this field needs to be specified. These bits are for internal TranSwitch use only. |
| 1/B/14:1<br>1/B/14:0 | 7-0<br>7-0 | TRH for Multicast | **Tandem Routing Header:** For multicast enqueues to the outlet queue space, this field is not used. If a cell is enqueued into an ingress queue from the multicast RAM, this field needs to be specified. These bits are for internal TranSwitch use only. |
| 1/B/15:3<br>1/B/15:2<br>1/B/15:1<br>1/B/15:0 | 7-0<br>7-0<br>7-0<br>7-0 | ATM Header | **ATM Header:** ATM header word for multicast cell containing VPI, VCI, PTI, and CLP fields. Each leaf will be enqueued with the same ATM header. Egress header translation and per-vc statistics will be maintained after the cell is scheduled toward the UTOPIA initiating a header lookup based on the ATM header or QID. These bits are for internal TranSwitch use only. |
| 1/B/16:3<br>1/B/16:2<br>1/B/16:1<br>1/B/16:0<br>to<br>1/B/21:3<br>1/B/21:2<br>1/B/21:1<br>1/B/21:0 | 7-0<br>7-0<br>7-0<br>7-0<br><br>7-0<br>7-0<br>7-0<br>7-0 | Cell Payload Word 1<br><br>to<br><br>Cell Payload Word 12 | **Cell Payload Words 1 through 12:** 12 words, 48 bytes. Payload of multicast cell. These bits are for internal TranSwitch use only. |
| 1/B/22:3<br>1/B/22:2<br>1/B/22:1<br>1/B/22:0<br>to<br>1/B/29:3<br>1/B/29:2<br>1/B/29:1<br>1/B/29:0 | 7-0<br>7-0<br>7-0<br>7-0<br><br>7-0<br>7-0<br>7-0<br>7-0 | Queue for Multicast Leaf 1<br>Queue for Multicast Leaf 2<br>to<br>Queue for Multicast Leaf 15<br>Queue for Multicast Leaf 16 | **Queue for Multicast Leaves 1 through 16:** 8 words, 32 bytes. Queue ID's of multicast leaves. Queue ID's of FFFFH indicates no enqueue performed. These bits are for internal TranSwitch use only. |
| 1/B/2A:0 | 0 | LMST | **Last Multicast Session Table:** The OP writes a 1 to this bit if requiring 16 leaves or less in the "Queue for multicast leaf" registers. The OP writes a 0 to this bit if more than 16 leaves requiring another batch of queues to be stored in "Queue for multicast leaf" registers. This bit is for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/B/2B:0 | 0 | MIP | **Multicast In Progress:** A 1 indicates an enqueue action is in progress. A 0 indicates the multicast engine is ready for next action. This bit is for internal TranSwitch use only. |
| 1/B/2C:1<br>1/B/2C:0 | 0<br>7-0 | Enqueue Interval | **Enqueue Interval:** Programmable counter indicating the number of PCLK ticks to be used between successive multicast enqueues. This is a throttling control to prevent excessive bursts of multicast cells from congesting the traffic bus. The maximum delay with a 100MHz PCLK is approximately 5 µs between enqueues. These bits are for internal TranSwitch use only. |
| 1/B/2D:3<br>1/B/2D:2<br>1/B/2D:1<br>1/B/2D:0 | 7-0<br>7-0<br>7-0<br>7-0 | Multicast Cell Queue ID | **Multicast Cell Queue Identifier:** After a cell arrives in the multicast RAM after dequeue from the RP, the second command word of the dequeue request is copied into this register for use by the OP. It identifies which multicast session the cell came from. These bits are for internal TranSwitch use only. |

**OP Register Map No. 4**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/9/0 | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | CFGGPO1(2-0) | | | CFGGPO0(2-0) | | |
| | R/W | ENT4I | ENT3I | ENT2I | ENT1I | T4DIV(1-0) | | ENT4 | T3DIV1 |
| | R/W | T3DIV0 | ENT3 | T2DIV(1-0) | | ENT2 | T1DIV(1-0) | | ENT1 |

**OP Bit Descriptions No. 4**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:2 | 5-3 | CFGGPO1(2-0) | **Configure General Purpose Output 1:** These bits 5-3 contain a binary code that controls the signal on Outlet Processor Status output lead OP1, as follows:<br>000: Timer 1 rollover: OP1 held high when Timer 1 is all 1s<br>001: Timer 2 rollover: OP1 held high when Timer 2 is all 1s<br>010: Timer 3 rollover: OP1 held high when Timer 3 is all 1s<br>011: Timer 4 rollover: OP1 held high when Timer 4 is all 1s<br>100: Internal Test Point 0:<br>101: Internal Test Point 1:<br>110: OP1 held low<br>111: OP1 held high |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:2 | 2-0 | CFGGPO0(2-0) | **Configure General Purpose Output 0:** These bits 2-0 contain a binary code that controls the signal on Outlet Processor Status output lead OP0, as follows:<br>000: Timer 1 rollover: OP0 held high when Timer 1 is all 1s<br>001: Timer 2 rollover: OP0 held high when Timer 2 is all 1s<br>010: Timer 3 rollover: OP0 held high when Timer 3 is all 1s<br>011: Timer 4 rollover: OP0 held high when Timer 4 is all 1s<br>100: Internal Test Point 0:<br>101: Internal Test Point 1:<br>110: OP0 held low<br>111: OP0 held high |
| 1/9/0:1 | 7 | ENT4I | **Enable Timer 4 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 4 is all ones. |
| 1/9/0:1 | 6 | ENT3I | **Enable Timer 3 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 3 is all ones. |
| 1/9/0:1 | 5 | ENT2I | **Enable Timer 2 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 2 is all ones. |
| 1/9/0:1 | 4 | ENT1I | **Enable Timer 1 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 1 is all ones. |
| 1/9/0:1 | 3-2 | T4DIV(1-0) | **Timer 4 Division Mode:** These bits 3-2 contain a binary code that controls the clock division ratio for Timer 4, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:1 | 1 | ENT4 | **Enable Timer 4:** When set to 1, this bit enables Timer 4. |
| 1/9/0:1<br>1/9/0:0 | 0<br>7 | T3DIV(1-0) | **Timer 3 Division Mode:** These bits 0 and 7 contain a binary code that controls the clock division ratio for Timer 3, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 6 | ENT3 | **Enable Timer 3:** When set to 1, this bit enables Timer 2. |
| 1/9/0:0 | 5-4 | T2DIV(1-0) | **Timer 2 Division Mode:** These bits 5-4 contain a binary code that controls the clock division ratio for Timer 2, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 3 | ENT2 | **Enable Timer 4:** When set to 1, this bit enables Timer 2. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:0 | 2-1 | T1DIV(1-0) | **Timer 1 Division Mode:** These bits 2-1 contain a binary code that controls the clock division ratio for Timer 1, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 0 | ENT1 | **Enable Timer 1:** When set to 1, this bit enables Timer 1. |

**OP Register Map No. 5**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/8/0 | R/W | Timer 1 (32 bits) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/1 | R/W | Timer 2 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/2 | R/W | Timer 2 (32 bits) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/3 | R/W | Timer 3 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Timer 3 (16 bits) | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/4 | R/W | Timer 4 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Timer 4 (16 bits) | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/5 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | Timer Status(3-0) | | |

**OP Bit Descriptions No. 5**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/8/0:3-0 | 7-0 | Timer 1 | **Timer 1:** This is a 32-bit rollover timer. |
| 1/8/1:3-0 | 7-0 | Timer 2 Preload | **Timer 2 Preload Value:** The 32-bit Timer 2 will initially start with this value, and loads this value in after rollover. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/8/2:3-0 | 7-0 | Timer 2 | **Timer 2:** This is a 32-bit rollover timer. |
| 1/8/3:3-2 | 7-0 | Timer 3 Preload | **Timer 3 Preload Value:** The 16-bit Timer 3 will initially start with this value, and loads this value in after rollover. |
| 1/8/3:1-0 | 7-0 | Timer 3 | **Timer 3:** This is a 16-bit rollover timer. |
| 1/8/4:3-2 | 7-0 | Timer 4 Preload | **Timer 4 Preload Value:** The 16-bit Timer 4 will initially start with this value, and loads this value in after rollover. |
| 1/8/4:1-0 | 7-0 | Timer 4 | **Timer 4:** This is a 16-bit rollover timer. |
| 1/8/5:0 | 3-0 | Timer Status | **Timer Status:** These four bits (3-0) indicate the rollover events of the four Timers (4-1). A 1 indicates Timer rollover. These status bits do not clear automatically but must be reset to 0 by writing to the register. |

**OP Register Map No. 6**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/7/1D | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | | | WDTIMER(19-16) | | | |
| | R/W | WDTIMER(15-8) | | | | | | | |
| | R/W | WDTIMER(7-0) | | | | | | | |
| 0/7/1E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | WDCLR | WDEXP | WDENT |
| 0/7/1F | R/W | S/C | Update Mask (14-8) | | | | | | |
| | R/W | Update Mask (7-0) | | | | | | | |
| | R/W | RESERVED | Event (14-8) | | | | | | |
| | R/W | Event (7-0) | | | | | | | |

**OP Bit Descriptions No. 6**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/7/1D:2<br>0/7/1D:1<br>0/7/1D:0 | 3-0<br>7-0<br>7-0 | WDTIMER(19-16)<br>WDTIMER(15-8)<br>WDTIMER(7-0) | **Watchdog Timer:** This field is a 20-bit timer. When enabled (by control bit WDENT = 1, see below), the watchdog timer will count up at the PCLK clock rate. If the timer is not reset by WDCLR, the timer will expire (all 1s). When the timer expires, the ASPEN device will be forced into a restart state, and will reload boot firmware. **Note**: When debug mode is active, and the Outlet Processor is in a frozen state, the watchdog timer is also in a frozen state. |
| 0/7/1E:0 | 2 | WDCLR | **Watchdog Clear:** When this bit is set to 1, the watchdog timer is cleared, and then the bit is automatically reset to 0. This bit is initialized to 0 at device reset. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/7/1E:0 | 1 | WDEXP | **Watchdog Expired:** This bit becomes set to 1 when the watchdog timer expires (all 1s). It is reset to 0 only when a hardware reset is performed (lead $\overline{\text{RESET}}$ low). |
| 0/7/1E:0 | 0 | WDENT | **Watchdog Timer Enable:** When this bit is set to 1, the watchdog timer is enabled. Once set to 1, the watchdog timer cannot be disabled except by a hardware or firmware reset (leads $\overline{\text{RESET}}$ or $\overline{\text{FWRST}}$ low). |
| 0/7/1F:3 | 7 | S/C | **Set/Clear:** When this bit is set to 1, all Update Maskn bits (n=14-0) which are set to 0 will cause the corresponding Eventn bit to be set to 1. When this bit is set to 0, all Update Maskn bits (n=14-0) which are set to 0 will cause the corresponding Eventn bit to be set to 0. This bit is for internal TranSwitch use only. |
| 0/7/1F:3<br>0/7/1F:2 | 6-0<br>7-0 | Update Mask (14-8)<br>Update Mask (7-0) | **Update Mask:** When an individual Update Mask bit is set to 1, the corresponding Event bit is not modified. These bits are for internal TranSwitch use only. |
| 0/7/1F:1<br>0/7/1F:0 | 6-0<br>7-0 | Event (14-8)<br>Event (7-0) | **Event:** Latched Event status. These bits are for internal TranSwitch use only. |

**OP Register Map No. 7**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/0 | R/W | RESET | | | | | | | |
| | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1 | R/W | RESERVED | | | | | | | |
| | R/W | ETU1 | ETPHYEN | ETLMODE | ETCHK16 | ETCELLSIZE(3-0) | | | |
| | R/W | $\overline{\text{ETHECGEN}}$ | ET16b | ETONLINE | UTCLKSRC(1-0) | | RESERVED | | |
| | R/W | RESERVED | | | | | | | |
| 0/6/2 | R/W | ETE15 | RESERVED | | ETPHY15ADDR(4-0) | | | | |
| | R/W | ETE14 | RESERVED | | ETPHY14ADDR(4-0) | | | | |
| | R/W | ETE13 | RESERVED | | ETPHY13ADDR(4-0) | | | | |
| | R/W | ETE12 | RESERVED | | ETPHY12ADDR(4-0) | | | | |
| 0/6/3 | R/W | ETE11 | RESERVED | | ETPHY11ADDR(4-0) | | | | |
| | R/W | ETE10 | RESERVED | | ETPHY10ADDR(4-0) | | | | |
| | R/W | ETE9 | RESERVED | | ETPHY9ADDR(4-0) | | | | |
| | R/W | ETE8 | RESERVED | | ETPHY8ADDR(4-0) | | | | |
| 0/6/4 | R/W | ETE7 | RESERVED | | ETPHY7ADDR(4-0) | | | | |
| | R/W | ETE6 | RESERVED | | ETPHY6ADDR(4-0) | | | | |
| | R/W | ETE5 | RESERVED | | ETPHY5ADDR(4-0) | | | | |
| | R/W | ETE4 | RESERVED | | ETPHY4ADDR(4-0) | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/5 | R/W | ETE3 | RESERVED | | ETPHY3ADDR(4-0) | | | | |
| | R/W | ETE2 | RESERVED | | ETPHY2ADDR(4-0) | | | | |
| | R/W | ETE1 | RESERVED | | ETPHY1ADDR(4-0) | | | | |
| | R/W | ETE0 | RESERVED | | ETPHY0ADDR(4-0) | | | | |
| 0/6/6 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | LN(4-0) | | | | |
| 0/6/7 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | LDIV |
| 0/6/8 | R/W | LR/$\overline{W}$ | LADD(14-8) | | | | | | |
| | R/W | LADD(7-0) | | | | | | | |
| | R/W | LDATA(15-8) | | | | | | | |
| | R/W | LDATA(7-0) | | | | | | | |
| 0/6/9 | R/W | INST | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/A | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | SEADD(15-0) | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/B | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | READ |
| 0/6/C | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | LOAD |
| 0/6/D | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | WHPROC |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | BOOTADD(6-0) | | | | | | |
| 0/6/F | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | LSCAN(15-0) | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/10 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | LSTATUS |
| 0/6/11 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | SESTATUS |
| 0/6/12 | R/W | SEDATA(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/13 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | ETAVAIL |
| 0/6/1C | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1D | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/1F | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | OP-to-RP mailbox register (7-0) | | | | | | | |
| 0/6/20 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | ERSTUT | ECTRCHK |

**OP Bit Descriptions No. 7**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/0:3 | 7-0 | RESET | **Software Reset:** Writing a 91 Hex into this location will generate a software reset to the component. Writing other than 91 Hex to this location will remove the ASPEN device from the reset state. Reading this location will return a 00 Hex if the ASPEN device is not in reset and 01 Hex if it is in reset. Software reset will reset all egress hardware state machines synchronously to their home state, and all FIFOs in the *CellBus* domain will be flushed. |
| 0/6/1:2 | 7 | ETU1 | **Egress Terminal UTOPIA Level 1 Select:** Setting this bit to 1 puts the UTOPIA interface into UTOPIA Level 1 mode (Single-PHY). When this bit is set to 0, the interface is in UTOPIA Level 2 mode (Multi-PHY). |
| 0/6/1:2 | 6 | ETPHYEN | **Egress Terminal PHY Layer Emulation Enable:** When set to 1, this bit enables PHY Layer emulation in UTOPIA modes. When set to 0, the device operates with ATM Layer emulation. |
| 0/6/1:2 | 5 | ETLMODE | **Egress Terminal Line Mode Select:** When set to 1, this bit enables Packet Mode operation of the UTOPIA interface. When set to 0, the interface operates in Cell Mode. |
| 0/6/1:2 | 4 | ETCHK16 | **Egress Terminal Multi-PHY Chunk Size:** When this bit is set to 1, the transfer size is 16 bytes. When set to 0, the transfer size is 48 bytes. |
| 0/6/1:2 | 3-0 | ETCELLSIZE(3-0) | **Egress Terminal Cell Size Select:** These bits set the cell size for the Inlet UTOPIA Interface. Actual cell size is 53 plus the decimal value of this field (bit 3 is MSB). Values of ITCELLSIZE beyond 11 will be treated as equal to 11. |
| 0/6/1:1 | 7 | $\overline{\text{ETHECGEN}}$ | **Egress Terminal HEC Generation:** When this bit is set to 0, HEC generation is enabled for the Egress Terminal Interface. When set to 1, HEC generation is disabled. |
| 0/6/1:1 | 6 | ET16b | **Egress Terminal 16-bit Mode Select:** When this bit is set to 1, 16-bit UTOPIA Level 2P mode is selected. When this bit is set to 0, 8-bit mode is selected. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/1:1 | 5 | ETONLINE | **Egress Terminal Online:** When this bit is set to 1, the Egress Terminal Interface is active (online). When it is set to 0, all UTOPIA-related output leads are set to the tristate condition (offline). |
| 0/6/1:1 | 4-3 | UTCLKSRC(1-0) | **UTOPIA Clock Source:** These bits determine which clock will be used for the driving the UTOPIA Level 2P interface in ATM layer emulation mode. The selections for bits 4, 3 are:<br>00: LUCLK input clock.<br>01: Internal system clock÷2. This clock is generated by an internal PLL and will be the same frequency as the PCLK input. See Note below.<br>10: Internal system clock÷4. This clock is generated by an internal PLL and will be one-half the frequency of the PCLK input. See Note below.<br>11: Reserved<br>**Note:** When using either of the PLL generated internal system clocks as the UTOPIA clock source, it is **not** recommended that these clocks be used to drive external clock buffering devices that utilize internal PLL circuitry to perform clock regeneration. If the need exists to use external clock buffers that utilize internal PLL circuitry, then the LUCLK input clock must be used. |
| 0/6/2:3-0<br>0/6/3:3-0<br>0/6/4:3-0<br>0/6/5:3-0 | 7<br>7<br>7<br>7 | ETE(15-12)<br>ETE(11-8)<br>ETE(7-4)<br>ETE(3-0) | **Egress Terminal Enable for PHYs 15-0:** For each one of these bits that is set to 0, all cells going to the corresponding PHY are discarded and that PHY is no longer polled in Multi-PHY mode. |
| 0/6/2:3-0<br>0/6/3:3-0<br>0/6/4:3-0<br>0/6/5:3-0 | 4-0<br>4-0<br>4-0<br>4-0 | ETPHYnADDR(4-0)<br>(n = 15 for 0/6/2:3<br>n = 0 for 0/6/5:0) | **Egress Terminal PHY #n Address Code:** This is a 5-bit UTOPIA Level 2 address that can be set for mapping each of 16 PHYs to a UTOPIA address value in the range 0 to 30 (bit 4 is the MSB). |
| 0/6/6:0 | 7 | LN(4-0) | **Line Number:** These five bits select the line interface number for which the read/write operations are to occur. LN0 is the LSB. Writing to this location enables the corresponding LADD lead and activates the serial port read/write operation. |
| 0/6/7:0 | 0 | LDIV | **LCK divide ratio:** When this bit is set to 1, the frequency of LCK is the frequency of PCLK÷2. When set to 0, this frequency is PCLK÷4. |
| 0/6/8:3 | 7 | LR/W | **Line Control Read/Write:** Writing a 1 to this bit initiates a read operation on the selected serial line control interface. Writing a 0 to this bit initiates a write operation on the selected serial line control interface. This is the first bit shifted out on the serial port. |
| 0/6/8:3<br>0/6/8:2 | 6-0<br>7-0 | LADD(14-8)<br>LADD(7-0) | **Line Address:** These 15 bits provide the register address in the line interface device selected by LN(4-0) for which read/ write operations will occur. These bits are shifted out MSB (LADD14) first. |
| 0/6/8:1<br>0/6/8:0 | 7-0<br>7-0 | LDATA(15-8)<br>LDATA(7-0) | **Line Data:** These 16 bits provide the data that is to be written to the selected line interface, with the first bit in the MSB (LDATA15). |
| 0/6/9:3<br>0/6/9:2<br>0/6/9:1<br>0/6/9:0 | 7-0<br>7-0<br>7-0<br>7-0 | INST | **Instruction:** This register is used for the loading of instructions into the various on-chip processors, and is not user-configurable. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/A:1<br>0/6/A:0 | 7-0<br>7-0 | SEADD(15-8)<br>SEADD(7-0) | **Serial EEPROM Address:** These 16 bits provide the register address in the serial EEPROM from which read operations will occur. These bits are shifted out MSB (SEADDR15) first. |
| 0/6/B:0 | 0 | READ | **Read EEPROM:** When this bit is set to 1, it initiates a read of the EEPROM. The SESTATUS bit must be checked to see if the interface is available before initiating the read operation. |
| 0/6/C:0 | 0 | LOAD | **Load Boot RAM:** When set to 1, this bit enables loading of the Boot RAM of the processor defined by control bit WHPROC, with the instruction stored in INST to be put in address BOOTADD(6-0). |
| 0/6/D:0 | 0 | WHPROC | **Which Processor:** This bit controls which processor has its Boot RAM loaded with INST. A 1 selects the RP processor and a 0 selects the IP processor. |
| 0/6/E:0 | 6-0 | BOOTADD(6-0) | **Boot Address:** Destination address of Boot RAM into which INST value is to be loaded. |
| 0/6/F:1<br>0/6/F:0 | 7-0<br>7-0 | LSCAN(15-8)<br>LSCAN(7-0) | **Line Scan:** After a read operation from the selected line interface device, these 16 bits provide the data read from the serial line interface device, with the first bit in the MSB (LSCAN15). |
| 0/6/10:0 | 0 | LSTATUS | **Line Status:** When this bit is set to 1, it indicates that the selected line interface is in use. When it is 0, it indicates that the line interface operation has been completed. This bit may be used to avoid accessing any of the serial port registers during an operation, which would cause an error. |
| 0/6/11:0 | 0 | SESTATUS | **Serial EEPROM Status:** When this bit is set to 1, it indicates that the serial EEPROM interface is in use. When it is set to 0, it indicates that the interface operation has been completed or the interface is not in use. This bit may be used to avoid attempting access to the SEDATA register during a read operation, which may result in invalid data being read. |
| 0/6/12:3<br>0/6/12:2<br>0/6/12:1<br>0/6/12:0 | 7-0<br>7-0<br>7-0<br>7-0 | SEDATA(31-24)<br>SEDATA(23-16)<br>SEDATA(15-8)<br>SEDATA(7-0) | **Serial EEPROM Data:** After a read operation from the EEPROM, these 32 bits contain the data read from the device. Bytes read are stored in order from the MSB, with the first byte read stored in SEDATA(31-24), the second in SEDATA(23-16), and so on. |
| 0/6/13:0 | 0 | ETAVAIL | **Host Mailbox Available:** When this bit is set to 1, it indicates that the OP-to-host mailbox is free for the ASPEN device to send the host a message. This bit is for internal TranSwitch use only. |
| 0/6/1F:0 | 7-0 | OP-to-RP mailbox register (7-0) | **OP-to-RP Mailbox Register:** This is an 8-bit mailbox shadow register from OP to RP. Used to control dequeues toward egress UTOPIA. Read/Write register for OP. Value written here is reflected in RP register 0/6/1D, bits 7-0. These bits are for internal TranSwitch use only. |
| 0/6/20:0 | 1 | ERSTUT | **Egress Reset UTOPIA:** A 1 forces a reset of the egress UTOPIA interface. A 0 clears the reset condition. This bit is for internal TranSwitch use only. |
| 0/6/20:0 | 0 | ECTRCHK | **Egress Connection Table Reference Check:** When set to 1, a comparison will be performed to see if a connection table that is returned is the same as the previous by comparing the CT reference. A duplicate connection table read will result in the second fetch being discarded in order to maintain table coherency with respect to the first writeback. This bit is for internal TranSwitch use only. |

## RATE PROCESSOR (RP)-RELATED PARAMETERS

### RP Register Map No. 1

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/9/0 | R/W | RESERVED | | | | | | | |
| | R/W | | | CFGGPO1(2-0) | | | CFGGPO0(2-0) | | |
| | R/W | ENT4I | ENT3I | ENT2I | ENT1I | T4DIV(1-0) | | ENT4 | T3DIV1 |
| | R/W | T3DIV0 | ENT3 | T2DIV(1-0) | | ENT2 | T1DIV(1-0) | | ENT1 |

### RP Bit Descriptions No. 1

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:2 | 5-3 | CFGGPO1(2-0) | **Configure General Purpose Output 1:** These bits 5-3 contain a binary code that controls the signal on Rate Processor Status output lead ASPEN_BOOTED, as follows:<br>000: Timer 1 rollover: lead held high when Timer 1 is all 1s<br>001: Timer 2 rollover: lead held high when Timer 2 is all 1s<br>010: Timer 3 rollover: lead held high when Timer 3 is all 1s<br>011: Timer 4 rollover: lead held high when Timer 4 is all 1s<br>100: Internal Test Point 0:<br>101: Internal Test Point 1:<br>110: lead held low<br>111: lead held high |
| 1/9/0:2 | 2-0 | CFGGPO0(2-0) | **Configure General Purpose Output 0:** These bits 2-0 contain a binary code that controls the signal on Rate Processor Status output lead RP0, as follows:<br>000: Timer 1 rollover: RP0 held high when Timer 1 is all 1s<br>001: Timer 2 rollover: RP0 held high when Timer 2 is all 1s<br>010: Timer 3 rollover: RP0 held high when Timer 3 is all 1s<br>011: Timer 4 rollover: RP0 held high when Timer 4 is all 1s<br>100: Internal Test Point 0:<br>101: Internal Test Point 1:<br>110: lead held low<br>111: lead held high |
| 1/9/0:1 | 7 | ENT4I | **Enable Timer 4 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 4 is all ones. |
| 1/9/0:1 | 6 | ENT3I | **Enable Timer 3 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 3 is all ones. |
| 1/9/0:1 | 5 | ENT2I | **Enable Timer 2 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 2 is all ones. |
| 1/9/0:1 | 4 | ENT1I | **Enable Timer 1 Interrupt:** When set to 1, this bit enables coprocessor interrupt generation if the value of Timer 1 is all ones. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/9/0:1 | 3-2 | T4DIV(1-0) | **Timer 4 Division Mode:** These bits 3-2 contain a binary code that controls the clock division ratio for Timer 4, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:1 | 1 | ENT4 | **Enable Timer 4:** When set to 1, this bit enables Timer 4. |
| 1/9/0:1<br>1/9/0:0 | 0<br>7 | T3DIV1<br>T3DIV0 | **Timer 3 Division Mode:** These bits 0 and 7 contain a binary code that controls the clock division ratio for Timer 3, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 6 | ENT3 | **Enable Timer 3:** When set to 1, this bit enables Timer 2. |
| 1/9/0:0 | 5-4 | T2DIV(1-0) | **Timer 2 Division Mode:** These bits 5-4 contain a binary code that controls the clock division ratio for Timer 2, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 3 | ENT2 | **Enable Timer 4:** When set to 1, this bit enables Timer 2. |
| 1/9/0:0 | 2-1 | T1DIV(1-0) | **Timer 1 Division Mode:** These bits 2-1 contain a binary code that controls the clock division ratio for Timer 1, as follows:<br>00: no divide<br>01: clock rate ÷ 4<br>10: clock rate ÷ 16<br>11: clock rate ÷ 64 |
| 1/9/0:0 | 0 | ENT1 | **Enable Timer 1:** When set to 1, this bit enables Timer 1. |

**RP Register Map No. 2**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/8/0 | R/W | Timer 1 (32 bits) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/1 | R/W | Timer 2 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 1/8/2 | R/W | Timer 2 (32 bits) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/3 | R/W | Timer 3 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Timer 3 (16 bits) | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/4 | R/W | Timer 4 preload value | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Timer 4 (16 bits) | | | | | | | |
| | R/W | | | | | | | | |
| 1/8/5 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | Timer Status (3-0) | | | |



**RP Bit Descriptions No. 2**



| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 1/8/0:3-0 | 7-0 | Timer 1 | **Timer 1:** This is a 32-bit rollover timer. |
| 1/8/1:3-0 | 7-0 | Timer 2 Preload | **Timer 2 Preload Value:** The 32-bit Timer 2 will initially start with this value, and loads this value in after rollover. |
| 1/8/2:3-0 | 7-0 | Timer 2 | **Timer 2:** This is a 32-bit rollover timer. |
| 1/8/3:3-2 | 7-0 | Timer 3 Preload | **Timer 3 Preload Value:** The 16-bit Timer 3 will initially start with this value, and loads this value in after rollover. |
| 1/8/3:1-0 | 7-0 | Timer 3 | **Timer 3:** This is a 16-bit rollover timer. |
| 1/8/4:3-2 | 7-0 | Timer 4 Preload | **Timer 4 Preload Value:** The 16-bit Timer 4 will initially start with this value, and loads this value in after rollover. |
| 1/8/4:1-0 | 7-0 | Timer 4 | **Timer 4:** This is a 16-bit rollover timer. |
| 1/8/5:0 | 3-0 | Timer Status | **Timer Status:** These four bits (3-0) indicate the rollover events of the four Timers (4-1). A 1 indicates Timer rollover. These status bits do not clear automatically but must be reset to 0 by writing to the register. |

**RP Register Map No. 3**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/5/0 | R/W | RESERVED | CNRAMADDR(3-0) | | | | CNW | CNR | PORH |
| | R/W | CRCD | CCRC | QMMO | MIHMU | MILMU | MIHFLSH | MILFLSH | QMFLSH |
| | R/W | RESERVED | MIMDH(3-0) | | | | MIMDL(4-2) | | |
| | R/W | MIMDL(1-0) | | QMMD(3-0) | | | | ENCRC10 | QMOM |

**RP Bit Descriptions No. 3**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/5/0:3 | 6-3 | CNRAMADDR(3-0) | **Congestion/NACK RAM Address:** These four bits identify the RAM address for which the read or write operation will occur. |
| 0/5/0:3 | 2 | CNW | **Congestion/BACK Write:** Writing a 1 to this bit results in a write operation to the address pointed to by CNRAMADDR. This bit must be reset to 0 when the operation is completed. The data will be read from register 0/4/3, described in the next section. |
| 0/5/0:3 | 1 | CNR | **Congestion/NACK Read:** Writing a 1 to this bit results in a read operation from the address pointed to by CNRAMADDR. This bit must be reset to 0 when the operation is completed. The data will be written to register 0/4/3, described in the next section. |
| 0/5/0:3 | 0 | PORH | **Pass On-chip Routing Header:** Passes On-chip Routing Header (ORH) through to memory interface. Valid only when control bit ACIP is set to 0. This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 7 | CRCD | **CRC Done:** Indication from Queue Manager that one memory read has been completed and the CRC calculated. Residual available and valid in Queue Manager registers 0/4/5 and 0/4/6. This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 6 | CCRC | **Calculate CRC:** Indication that data received back from a memory read is cell data and should have CRC-32/-10 calculated on it. This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 5 | QMMO | **Queue Manager Mailbox Overflow:** Indication that the rate processor has attempted to write more words than are available in QM. Does not interrupt processor; intended for use in software debug. This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 4 | MIHMU | **High Priority Mailbox Memory Interface Underflow:** Indication that the rate processor has attempted to read more words than are available in Memory Interface (MI). Does not interrupt processor; intended for use in software debug. This bit is for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/5/0:2 | 3 | MILMU | **Low Priority Mailbox Memory Interface Underflow:** Indication that the rate processor has attempted to read more words than are available in Memory Interface (MI). Does not interrupt processor; intended for use in software debug. This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 2 | MIHFLSH | **Flush High Priority Memory Interface Mailbox:** This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 1 | MILFLSH | **Flush Low Priority Memory Interface Mailbox:** This bit is for internal TranSwitch use only. |
| 0/5/0:2 | 0 | QMFLSH | **Flush Queue Manager Mailbox:** This bit is for internal TranSwitch use only. |
| 0/5/0:1 | 6-3 | MIMDH(3-0) | **Memory Interface Mailbox Depth High Priority:** Code to indicate how many messages are in the MI high priority mailbox. Each message is of variable length, with length indicated by the first word. Queue Manager maintains the depth, popping a new word each time the Rate Processor reads from register 0/4/1. When a complete message is read out, the Queue Manager will decrement the message depth. These bits are for internal TranSwitch use only. |
| 0/5/0:1<br>0/5/0:0 | 2-0<br>7-6 | MIMDL(4-2)<br>MIMDL(1-0) | **Memory Interface Mailbox Depth Low Priority:** Code to indicate how many messages are in the MI low priority mailbox. Each message is of variable length, with length indicated by the first word. Queue Manager maintains the depth, popping a new word each time the Rate Processor reads from register 0/4/2. When a complete message is read out, the Queue Manager will decrement the message depth. These bits are for internal TranSwitch use only. |
| 0/5/0:0 | 5-2 | QMMD(3-0) | **Queue Manager Mailbox Depth:** Code to indicate how many messages are in the Queue Manager (QM) mailbox. Decremented as each message is read out. These bits are for internal TranSwitch use only. |
| 0/5/0:0 | 1 | ENCRC10 | **Enable CRC-10:** When set to 1, CRC-10 calculation mode is enabled. When set to 0, CRC-32 calculation mode is enabled. This bit is for internal TranSwitch use only. |
| 0/5/0:0 | 0 | QMOM | **Queue Manager Outgoing Mail:** Set by rate processor when there is a message or messages in the QM mailbox. Reset by QM after the MI is notified of the message presence. This bit is for internal TranSwitch use only. |

**RP Register Map No. 4**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/4/0 | R/W | QM_Mailbox(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/4/1 | R/W | MI_HI_Mailbox(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/4/2 | R/W | MI_LO_Mailbox(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/4/3 | R/W | CONG15 | NACK15 | CONG14 | NACK14 | CONG13 | NACK13 | CONG12 | NACK12 |
| | R/W | CONG11 | NACK11 | CONG10 | NACK10 | CONG9 | NACK9 | CONG8 | NACK8 |
| | R/W | CONG7 | NACK7 | CONG6 | NACK6 | CONG5 | NACK5 | CONG4 | NACK4 |
| | R/W | CONG3 | NACK3 | CONG2 | NACK2 | CONG1 | NACK1 | CONG0 | NACK0 |
| 0/4/4 | R/W | Tail_ORH(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/4/5 | R/W | CRC32_Residual(31-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/4/6 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | CRC-10(1-0) | |
| | R/W | CRC-10 Residual (7-0) | | | | | | | |

**RP Bit Descriptions No. 4**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/4/0:3<br>0/4/0:2<br>0/4/0:1<br>0/4/0:0 | 7-0<br>7-0<br>7-0<br>7-0 | QM_Mailbox(31-24)<br>QM_Mailbox(23-16)<br>QM_Mailbox(15-8)<br>QM_Mailbox(7-0) | **Queue Manager Mailbox:** For deposit of mail to memory interface. The depth of the mailbox is 8 words. The mailbox is managed as a FIFO. These bits are for internal TranSwitch use only. |
| 0/4/1:3<br>0/4/1:2<br>0/4/1:1<br>0/4/1:0 | 7-0<br>7-0<br>7-0<br>7-0 | MI_HI_Mailbox(31-24)<br>MI_HI_Mailbox(23-16)<br>MI_HI_Mailbox(15-8)<br>MI_HI_Mailbox(7-0) | **Memory Interface Mailbox For High Priority Messages:** For receipt of mail from memory interface. The depth of the mailbox is 16 words. These bits are for internal TranSwitch use only. |
| 0/4/2:3<br>0/4/2:2<br>0/4/2:1<br>0/4/2:0 | 7-0<br>7-0<br>7-0<br>7-0 | MI_LO_Mailbox(31-24)<br>MI_LO_Mailbox(23-16)<br>MI_LO_Mailbox(15-8)<br>MI_LO_Mailbox(7-0) | **Memory Interface Mailbox For Low Priority Messages:** For receipt of mail from memory interface. The depth of the mailbox is 32 words. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/4/3:3<br>0/4/3:2<br>0/4/3:1<br>0/4/3:0 | 7,5,3,1<br>7,5,3,1<br>7,5,3,1<br>7,5,3,1 | NACK(15-12)<br>NACK(11-8)<br>NACK(7-4)<br>NACK(3-0) | **Congestion/NACK Status Indications:** These 16 bit-pairs are used in conjunction with the control registers CNR, CNW, and CNRAMADDR described above. The CONG/ NACK bits will contain the data bits to be written to the Congestion/NACK RAM at the address specified by CNRAMADDR when a write operation is performed (CNW set to 1), and will contain the data bits read from the RAM at CNRAMADDR when a read operation is performed (CNR set to 1). |
| 0/4/3:3<br>0/4/3:2<br>0/4/3:1<br>0/4/3:0 | 6,4,2,0<br>6,4,2,0<br>6,4,2,0<br>6,4,2,0 | CONG(15-12)<br>CONG(11-8)<br>CONG(7-4)<br>CONG(3-0) | |
| 0/4/4:3<br>0/4/4:2<br>0/4/4:1<br>0/4/4:0 | 7-0<br>7-0<br>7-0<br>7-0 | Tail_ORH(31-24)<br>Tail_ORH(23-16)<br>Tail_ORH(15-8)<br>Tail_ORH(7-0) | **Tail_ORH:** On-chip Routing Header at tail of Traffic Outbound Header FIFO, if ACIP=0 this value can be modified. These bits are for internal TranSwitch use only. |
| 0/4/5:3<br>0/4/5:2<br>0/4/5:1<br>0/4/5:0 | 7-0<br>7-0<br>7-0<br>7-0 | CRC32_Residual(31-24)<br>CRC32_Residual(23-16)<br>CRC32_Residual(15-8)<br>CRC32_Residual(7-0) | **CRC32 Residual:** Residual from last CRC-32 calculation. These bits are for internal TranSwitch use only. |
| 0/4/6:1 | 1-0 | CRC-10(1-0) | **CRC-10:** These bits are for internal TranSwitch use only. |
| 0/4/6:0 | 7-0 | CRC-10 Residual (7-0) | **CRC-10 Residual:** Residual from last CRC-10 calculation. These bits are for internal TranSwitch use only. |



**RP Register Map No. 5**



| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/7/1D | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | | | WDTIMER(19-16) | | | |
| | R/W | WDTIMER(15-8) | | | | | | | |
| | R/W | WDTIMER(7-0) | | | | | | | |
| 0/7/1E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | WDCLR | WDEXP | WDENT |
| 0/7/1F | R/W | S/C | Update Mask (14-8) | | | | | | |
| | R/W | Update Mask (7-0) | | | | | | | |
| | R/W | RESERVED | Event (14-8) | | | | | | |
| | R/W | Event (7-0) | | | | | | | |
| 0/7/20 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | RPMSD |

**RP Bit Descriptions No. 5**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/7/1D:2<br>0/7/1D:1<br>0/7/1D:0 | 3-0<br>7-0<br>7-0 | WDTIMER(19-16)<br>WDTIMER(15-8)<br>WDTIMER(7-0) | **Watchdog Timer:** This field is a 20-bit timer. When enabled (by control bit WDENT = 1, see below), the watchdog timer will count up at the PCLK clock rate. If the timer is not reset by WDCLR, the timer will expire (all 1s). When the timer expires, the ASPEN device will be forced into a restart state, and will reload boot firmware. **Note**: When debug mode is active, and the Rate Processor is in a frozen state, the watchdog timer is also in a frozen state. |
| 0/7/1E:0 | 2 | WDCLR | **Watchdog Clear:** When this bit is set to 1, the watchdog timer is cleared, and then the bit is automatically reset to 0. This bit is initialized to 0 at reset. |
| 0/7/1E:0 | 1 | WDEXP | **Watchdog Expired:** This bit becomes set to 1 when the watchdog timer expires (all 1s). It is reset to 0 only when a hardware reset is performed (lead $\overline{\text{RESET}}$ low). |
| 0/7/1E:0 | 0 | WDENT | **Watchdog Timer Enable:** When this bit is set to 1, the watchdog timer is enabled. Once set to 1, the watchdog timer cannot be disabled except by a hardware or firmware reset (leads $\overline{\text{RESET}}$ or $\overline{\text{FWRST}}$ low). |
| 0/7/1F:3 | 7 | S/C | **Set/Clear:** When this bit is set to 1, all Update Maskn bits (n=14-0) which are set to 0 will cause the corresponding Eventn bit to be set to 1. When this bit is set to 0, all Update Maskn bits (n=14-0) which are set to 0 will cause the corresponding Eventn bit to be set to 0. This bit is for internal TranSwitch use only. |
| 0/7/1F:3<br>0/7/1F:2 | 6-0<br>7-0 | Update Mask (14-8)<br>Update Mask (7-0) | **Update Mask:** When an individual Update Mask bit is set to 1, the corresponding Event bit is not modified. These bits are for internal TranSwitch use only. |
| 0/7/1F:1<br>0/7/1F:0 | 6-0<br>7-0 | Event (14-8)<br>Event (7-0) | **Event:** Latched Event status. These bits are for internal TranSwitch use only. |
| 0/7/20:0 | 0 | RPMSD | **Rate Processor Multicast Session Done:** When set to 1, the OP multicast RAM is available. When set to 0, the OP multicast RAM is busy. RP must clear the bit when beginning a dequeue of a multicast cell to the OP multicast RAM. This bit is for internal TranSwitch use only. |

**RP Register Map No. 6**

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/0 | R/W | RESET | | | | | | | |
| | R | PN(15-8) | | | | | | | |
| | R | PN(7-0) | | | | | | | |
| | R | VER(3-0) | | | | ML(3-0) | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/1 | R | GROWTH(3-0) | | | | MID(11-8) | | | |
| | R | MID(7-0) | | | | | | | |
| | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/2 | R/W | UA(4-0) | | | | | 0 | CRC4I | RESERVED |
| | R/W | U16/$\overline{32}$A | U16/$\overline{32}$B | RESERVED | ONLINE | MASTERA | MASTERB | CBDIR(1-0) | |
| | R/W | NGTIMER(7-0) | | | | | | | |
| | R/W | 0 | FRNACK | $\overline{\text{TRHCRCG}}$ | $\overline{\text{TRHCRCC}}$ | ARBRST | 0 | EMPFLB | FRCCNG |
| 0/6/3 | R/W | IHSHMASK3(15-8) | | | | | | | |
| | R/W | IHSHMASK3(7-0) | | | | | | | |
| | R/W | IHSHMASK2(15-8) | | | | | | | |
| | R/W | IHSHMASK2(7-0) | | | | | | | |
| 0/6/4 | R/W | IHSHMASK1(15-8) | | | | | | | |
| | R/W | IHSHMASK1(7-0) | | | | | | | |
| | R/W | EHSHMASK3(15-8) | | | | | | | |
| | R/W | EHSHMASK3(7-0) | | | | | | | |
| 0/6/5 | R/W | EHSHMASK2(15-8) | | | | | | | |
| | R/W | EHSHMASK2(7-0) | | | | | | | |
| | R/W | EHSHMASK1(15-8) | | | | | | | |
| | R/W | EHSHMASK1(7-0) | | | | | | | |
| 0/6/6 | R/W | IFPT3 | EFPT3 | CBPOB | CBRPB1 | CBRPB0 | CBPOA | CBRPA1 | CBRPA0 |
| | R/W | RESERVED | | | | EQCBRH | 1 | 1 | 0 |
| | R/W | EHSHFT(3-0) | | | | IHSHSFT(3-0) | | | |
| | R/W | EDIRECT | IDIRECT | SBZ(1-0) | | SDW | HSTSZ | $\overline{\text{HST16K}}$ | HSTDW |
| 0/6/7 | R | CBNACKB | CBCONGB | CBIDB(4-0) | | | | | CBBIP8B |
| | R | CBCRC4 TRHB | CBCRC4 CRHB | CBNO GRTB | CBLOFB | CBLORCB | CBLOWCB | CBOFLWB | CBOQEB |
| | R | CBNACKA | CBCONGA | CBIDA(4-0) | | | | | CBBIP8A |
| | R | CBCRC4 TRHA | CBCRC4 CRHA | CBNO GRTA | CBLOFA | CBLORCA | CBLOWCA | CBOFLWA | CBOQEA |
| 0/6/8 | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | | | CBBURSTLEN1B(4-1) | | | |
| | R/W | CBBURST LEN1B0 | CBBURSTID1B(4-0) | | | | | CBBURSTLEN0B(4-3) | |
| | R/W | CBBURSTLEN0B(2-0) | | | CBBURSTID0B(4-0) | | | | |
| 0/6/9 | R/W | RESERVED | | | | | | | |
| | R/W | RESERVED | | | | CBBURSTLEN1A(4-1) | | | |
| | R/W | CBBURST LEN1A0 | CBBURSTID1A(4-0) | | | | | CBBURSTLEN0A(4-3) | |
| | R/W | CBBURSTLEN0A(2-0) | | | CBBURSTID0A(4-0) | | | | |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/A | R/W | RESERVED | | | | | | | |
| | R/W | C/NTAGB | | | | C/NTAGA | | | |
| | R/W | | | BURSTARRESTTH(4-0) | | | | | BRSTAA |
| | R/W | BURST_BACKOFF | | | RESERVED | | | | |
| 0/6/B | R | RESERVED | | TE0FILL(11-6) | | | | | |
| | R | TE0FILL(5-0) | | | | | | TE2FILL(17-16) | |
| | R | TE2FILL(15-0) | | | | | | | |
| | R | | | | | | | | |
| 0/6/C | R | RESERVED | | TE1FILL(11-6) | | | | | |
| | R | TE1FILL(5-0) | | | | | | TE3FILL(17-16) | |
| | R | TE3FILL(15-0) | | | | | | | |
| | R | | | | | | | | |
| 0/6/D | R | RESERVED | | CE0FILL(11-6) | | | | | |
| | R | CE0FILL(5-0) | | | | | | CE2FILL(17-16) | |
| | R | CE2FILL(15-0) | | | | | | | |
| | R | | | | | | | | |
| 0/6/E | R | RESERVED | | CE1FILL(11-6) | | | | | |
| | R | CE1FILL(5-0) | | | | | | CE3FILL(17-16) | |
| | R | CE3FILL(15-0) | | | | | | | |
| | R | | | | | | | | |
| 0/6/F | R/W | RESERVED | | | | | | | |
| | R/W | IHOFL(28-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/10 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/11 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/12 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | AVAIL |

| PP/ Page No./ Reg Addr | Mode | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0/6/13 | R/W | RESERVED | | | | | | | |
| | R/W | CHOFL(28-0) | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1C | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1D | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | OP-to-RP mailbox register (7-0) | | | | | | | |
| 0/6/1E | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| 0/6/1F | R/W | Port 15 UTOPIA Sent | | Port 14 UTOPIA Sent | | Port 13 UTOPIA Sent | | Port 12 UTOPIA Sent | |
| | R/W | Port 11 UTOPIA Sent | | Port 10 UTOPIA Sent | | Port 9 UTOPIA Sent | | Port 8 UTOPIA Sent | |
| | R/W | Port 7 UTOPIA Sent | | Port 6 UTOPIA Sent | | Port 5 UTOPIA Sent | | Port 4 UTOPIA Sent | |
| | R/W | Port 3 UTOPIA Sent | | Port 2 UTOPIA Sent | | Port 1 UTOPIA Sent | | Port 0 UTOPIA Sent | |
| 0/6/20 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | Max QID from *CellBus* (15-8) | | | | | | | |
| | R/W | Max QID from *CellBus* (7-0) | | | | | | | |
| 0/6/21 | R/W | RESERVED | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | | | | | | | | |
| | R/W | RESERVED | | | | | | | 30BLU |
| 0/6/22 | R/W | TE0MCE | TE2MCE | TE0Max (11-6) | | | | | |
| | R/W | TE0Max (5-0) | | | | | | TE2Max (17-16) | |
| | R/W | TE2Max (15-8) | | | | | | | |
| | R/W | TE2Max (7-0) | | | | | | | |
| 0/6/23 | R/W | TE1MCE | TE3MCE | TE1Max (11-6) | | | | | |
| | R/W | TE1Max (5-0) | | | | | | TE3Max (17-16) | |
| | R/W | TE3Max (15-8) | | | | | | | |
| | R/W | TE3Max (7-0) | | | | | | | |

**RP Bit Descriptions No. 6**

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/0:3 | 7-0 | RESET | **Software Initiated RP Reset:** Writing a 91 Hex into this location will generate a software reset to the RP subsystem. Writing other than 91 Hex to this location will remove the RP subsystem from the reset state. |
| 0/6/0:2<br>0/6/0:1 | 7-0<br>7-0 | PN(15-8)<br>PN(7-0) | **Part Number:** Read-only register containing the 16-bit binary equivalent of the 5-digit TranSwitch part identification number of the ASPEN device (05810) 16B2 hex. |
| 0/6/0:0 | 7-4 | VER(3-0) | **Version Number:** Read-only register containing the 4-bit binary equivalent of the version number of the ASPEN device (1). |
| 0/6/0:0 | 3-0 | ML(3-0) | **Mask Level:** Read-only register containing the 4-bit binary equivalent of the mask level of the ASPEN device (0). |
| 0/6/1:3 | 7-4 | GROWTH(3-0) | **Growth Field:** Read-only register containing the 4-bit binary equivalent of the growth field value of the ASPEN device (0). |
| 0/6/1:3<br>0/6/1:2 | 3-0<br>7-0 | MID(11-8)<br>MID(7-0) | **Manufacturer Identity:** This is a read-only 12-bit register containing the 11-bit binary equivalent of the component manufacturer's identity of TranSwitch (6B Hex) followed by a 1 in the LSB, MID0. |
| 0/6/2:3 | 7-3 | UA(4-0) | **User-number Assignment:** This is the 5-bit binary equivalent of the number assigned to identify the ASPEN device as an addressable user of the *CellBus*. It represents the inverted value of control straps $\overline{\text{UA(4-0)}}$. These bits are writable by the user. Once these bits are written, to reread the original strap settings, a software reset must be performed. |
| 0/6/2:3 | 1 | CRC4I | **Inverted CRC4:** When set to 1, the CRC-4 calculation is inverted to produce an incorrect CRC-4 value for the *CellBus* Routing Header. This bit is intended for test purposes. |
| 0/6/2:2 | 7 | U16/$\overline{32}$A | **Maximum number of *CellBus* devices on *CellBus* A:** This bit controls the maximum number of *CellBus* devices that can be connected to the *CellBus* A. When set to 1 there can be 16 devices, or 32 when set to 0. This bit is effective only if the lead $\overline{\text{ENARBA}}$ is low. |
| 0/6/2:2 | 6 | U16/$\overline{32}$B | **Maximum number of *CellBus* devices on *CellBus* B:** This bit controls the maximum number of *CellBus* devices that can be connected to the *CellBus* B. When set to 1 there can be 16 devices, or 32 when set to 0. This bit is effective only if the lead $\overline{\text{ENARBB}}$ is low. |
| 0/6/2:2 | 4 | ONLINE | **Online Select:** When this bit is set to 1, it enables reception of cells from both *CellBus* buses. |
| 0/6/2:2 | 3 | MASTERA | **Bus Master for *CellBus* A:** This bit reflects the state of lead $\overline{\text{ENARBA}}$. This bit is read only. |
| 0/6/2:2 | 2 | MASTERB | **Bus Master for *CellBus* B:** This bit reflects the state of lead $\overline{\text{ENARBB}}$. This bit is read only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/2:2 | 1-0 | CBDIR(1-0) | ***CellBus* Director Control:** These bits are used to determine on which *CellBus* an incoming cell is transferred, according to the following values of bits 1, 0:<br>00: Firmware controlled<br>01: *CellBus* A<br>10: *CellBus* B<br>11: Reserved |
| 0/6/2:1 | 7-0 | NGTIMER(7-0) | **No Grant Timer:** This is an 8-bit preset value for the time-out counter used for the bus access timer. If the timer expires after a request is made, and before a grant is received, alarm bit NOGRT for the corresponding *CellBus* is set. The count units are bus frame cycles. |
| 0/6/2:0 | 6 | FRNACK | **Force No Acknowledge:** When this bit is set to 1 it forces transmission of a No Acknowledge indication (NACK) on the *CellBus* (for all cells on both A and B buses). |
| 0/6/2:0 | 5 | $\overline{\text{TRHCRCG}}$ | **Tandem Routing Header CRC-4 Generate:** When this bit is set to 0, it enables generation of a CRC-4 across bits 15-4 of the outgoing Tandem Routing Header and placement of this CRC-4 in bits 3-0 of this Header. |
| 0/6/2:0 | 4 | $\overline{\text{TRHCRCC}}$ | **Tandem Routing Header CRC-4 Check:** When this bit is set to 0, it enables checking of a CRC-4 across bits 15-4 of the incoming Tandem Routing Header for comparison with the CRC-4 in bits 3-0 of this Header. |
| 0/6/2:0 | 3 | ARBRST | **Arbiter Reset:** When this bit is set to 1, it synchronously resets both *CellBus* arbiters to their home state. All other logic of the device is unaffected. This bit must be set to 0 for normal operation of the device. |
| 0/6/2:0 | 2 | EMPFLB | **Empty/Full Bar:** When this bit is set to 1, the CBOQSVC interrupt will occur on Outbound FIFO Empty. When set to 0, this interrupt occurs on Outbound FIFO Full. |
| 0/6/2:0 | 0 | FRCCNG | **Force Congestion indication:** When this bit is set to 1 it forces transmission of a Congestion indication (CONG) on the *CellBus* (for all cells on both A and B buses). |
| 0/6/3:3<br>0/6/3:2 | 7-0<br>7-0 | IHSHMASK3(15-8)<br>IHSHMASK3(7-0) | **Ingress Hashing Mask 3:** This is a 16-bit hashing index mask used to control the number of significant bits in the generated ingress hash index, which is used when the 28-bit hashing method for ingress header lookup is selected. |
| 0/6/3:1<br>0/6/3:0 | 7-0<br>7-0 | IHSHMASK2(15-8)<br>IHSHMASK2(7-0) | **Ingress Hashing Mask 2:** This is a 16-bit VPI mask used when the 28-bit hashing method for ingress header lookup is selected. |
| 0/6/4:3<br>0/6/4:2 | 7-0<br>7-0 | IHSHMASK1(15-8)<br>IHSHMASK1(7-0) | **Ingress Hashing Mask 1:** This is a 16-bit VCI mask used when the 28-bit hashing method for ingress header lookup is selected. |
| 0/6/4:1<br>0/6/4:0 | 7-0<br>7-0 | EHSHMASK3(15-8)<br>EHSHMASK3(7-0) | **Egress Hashing Mask 3:** This is a 16-bit hashing index mask used to control the number of significant bits in the generated egress hash index, which is used when the 28-bit hashing method for egress header lookup is selected. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/5:3<br>0/6/5:2 | 7-0<br>7-0 | EHSHMASK2(15-8)<br>EHSHMASK2(7-0) | **Egress Hashing Mask 2:** This is a 16-bit VPI mask used when the 28-bit hashing method for egress header lookup is selected. |
| 0/6/5:1<br>0/6/5:0 | 7-0<br>7-0 | EHSHMASK1(15-8)<br>EHSHMASK1(7-0) | **Egress Hashing Mask 1:** This is a 16-bit VCI mask used when the 28-bit hashing method for egress header lookup is selected. |
| 0/6/6:3 | 7 | IFPT3 | **Ingress FPT3 Enable:** When this bit is set to 1, it configures DMAC to generate a low priority message that include FPT3 word as part of ingress queue WQNE state change. This bit is for internal TranSwitch use only. |
| 0/6/6:3 | 6 | EFPT3 | **Egress FPT3 Enable:** When this bit is set to 1, it configures DMAC to generate a low priority message that include FPT3 word as part of egress queue WQNE state change. This bit is for internal TranSwitch use only. |
| 0/6/6:3 | 5 | CBPOB | ***CellBus* Request Priority Override for Bus B:** When this bit is set to 1, the *CellBus* B request priority is based on the value of control bits CBRPB(1-0) below. When it is 0, the value in the *CellBus* Routing Header CRC-4 field used. |
| 0/6/6:3 | 4-3 | CBRPB(1-0) | ***CellBus* Request Priority for Bus B:** This is a 2-bit value used to determine the request priority for a cell in the *CellBus* egress queue for *CellBus* B when control bit CBPOB is set to 1. The priority is set by the value of bits 4,3 as shown below:<br>00: No request<br>01: Low Priority<br>10: Medium Priority<br>11: High Priority |
| 0/6/6:3 | 2 | CBPOA | ***CellBus* Request Priority Override for Bus A:** When this bit is set to 1, the *CellBus* A request priority is based on the value of control bits CBRPA(1-0) below. When it is 0, the value in the *CellBus* Routing Header CRC-4 field used. |
| 0/6/6:3 | 1-0 | CBRPA(1-0) | ***CellBus* Request Priority for Bus A:** This is a 2-bit value used to determine the request priority for a cell in the *CellBus* egress queue for *CellBus* A when control bit CBPOA is set to 1. The priority is set by the value of bits 1,0 as shown below:<br>00: No request<br>01: Low Priority<br>10: Medium Priority<br>11: High Priority |
| 0/6/6:2 | 3 | EQCBRH | **Enable QID/CBRH Overwrite:** When this bit is set to 1, the QID overwrites the CBRH field in an incoming cell. When set to 0, the CBRH field of in incoming cell remains unchanged. This bit is for internal TranSwitch use only. |
| 0/6/6:1 | 7-4 | EHSHSFT(3-0) | **Egress Hash Shift:** This is a 4-bit field that is used in conjunction with EHSHMASK1 and EHSHMASK2 to control hash index generation. It is used when the 28-bit hashing method for egress header lookup is selected. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/6:1 | 3-0 | IHSHSFT(3-0) | **Ingress Hash Shift:** This is a 4-bit field that is used in conjunction with IHSHMASK1 and IHSHMASK2 to control hash index generation. It is used when the 28-bit hashing method for ingress header lookup is selected. |
| 0/6/6:0 | 7 | EDIRECT | **Egress Direct Lookup:** When this bit is set to 1, a direct lookup mechanism is used for egress header lookup. When it is set to 0, a 28-bit hash-based lookup method is used. |
| 0/6/6:0 | 6 | IDIRECT | **Ingress Direct Lookup:** When this bit is set to 1, a direct lookup mechanism is used for ingress header lookup. When it is set to 0, a 28-bit hash-based lookup method is used. |
| 0/6/6:0 | 5-4 | SBZ(1-0) | **Bank Size:** This is a 2-bit field that is used to specify the bank size of the memory used. These control bits also specify the function of the SCE2 and $\overline{\text{SCE2}}$ output leads. See the Block Diagram Description - SSRAM Memory Interface section. |
| 0/6/6:0 | 3 | SDW | **SSRAM Interface Data Bus Width:** This bit controls the width of the SSRAM interface memory. A value of 0 selects 32-bit, 1 selects 64-bit. This bit must be set to 1. |
| 0/6/6:0 | 2 | HSTSZ | **Host Interface Mailbox Size:** This bit controls the depth of a host mailbox. A value of 0 selects 64 words, 1 selects 256 words. This bit must be set to 0. |
| 0/6/6:0 | 1 | $\overline{\text{HST16K}}$ | **Host Interface Dual Port Memory Size:** This bit controls the depth of the Host Interface memory. A value of 0 selects 16k bits, 1 selects 64k bits. This bit must be set to 0. |
| 0/6/6:0 | 0 | HSTDW | **Host Interface Data Bus Width:** This bit controls the width of the Host Interface memory. A value of 0 selects 8 bits, 1 selects 16 bits. This bit must be set to 0. |
| 0/6/7:3 | 7 | CBNACKB | ***CellBus* No Acknowledge on Bus B:** This bit is set to 1 when a No Acknowledge is reported after a transfer in the *CellBus* B receiver (i.e., wait for acknowledgment times out). |
| 0/6/7:3 | 6 | CBCONGB | ***CellBus* Congestion on Bus B:** This bit is set to 1 when congestion is reported after a transfer in the *CellBus* B receiver. |
| 0/6/7:3 | 5-1 | CBIDB(4-0) | ***CellBus* ID of Congested or NACK'ed queue on bus B:** This 5-bit field contains the *CellBus* ID (user number) for *CellBus* B of the *CellBus* device reporting congestion or no acknowledge on *CellBus* B. |
| 0/6/7:3 | 0 | CBBIP8B | ***CellBus* BIP-8 Error on Bus B:** This bit is set to 1 when a BIP-8 error occurs in the *CellBus* B receiver |
| 0/6/7:2 | 7 | CBCRC4TRHB | ***CellBus* Tandem Routing Header CRC-4 Error on Bus B:** This bit is set to 1 when a Tandem Routing Header CRC-4 error occurs in the *CellBus* B receiver. |
| 0/6/7:2 | 6 | CBCRC4CRHB | ***CellBus* Routing Header CRC-4 Error on Bus B:** This bit is set to 1 when a *CellBus* Routing Header CRC-4 error occurs in the *CellBus* B receiver. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/7:2 | 5 | CBNOGRTB | ***CellBus* Grant Timeout on Bus B:** When set to 1 this bit indicates that no bus access grant has been received by the inlet side, after a bus access request, within a time established by register NGTIMER. |
| 0/6/7:2 | 4 | CBLOFB | ***CellBus* Loss of Frame on Bus B:** This bit is set to 1 if there are two consecutive missing *CellBus* B frame pulses in 32-user mode (U16/$\overline{32}$B set to 0), and four consecutive missing *CellBus* frame pulses in 16-user mode (U16/$\overline{32}$B set to 1). |
| 0/6/7:2 | 3 | CBLORCB | ***CellBus* Loss of Read Clock on Bus B:** This bit is set to 1 if the *CellBus* B read clock is not present for more than the equivalent of 32 clock cycles. |
| 0/6/7:2 | 2 | CBLOWCB | *CellBus* **Loss of Write Clock on Bus B:** This bit is set to 1 if the *CellBus* B write clock is not present for more than the equivalent of 32 clock cycles. |
| 0/6/7:2 | 1 | CBOFLWB | *CellBus* **Inlet FIFO Overflow for Bus B:** This bit is set to 1 if the *CellBus* inlet FIFO for bus B overflows. |
| 0/6/7:2 | 0 | CBOQEB | ***CellBus* Outbound Queue Empty/Full for Bus B:** - *CellBus* B egress requires servicing, status indicates either empty or full according to value of control bit EMPFLB. |
| 0/6/7:1 | 7 | CBNACKA | ***CellBus* No Acknowledge on Bus A:** This bit is set to 1 when a No Acknowledge is reported after a transfer in the *CellBus* A receiver (i.e., wait for acknowledgment times out). |
| 0/6/7:1 | 6 | CBCONGA | ***CellBus* Congestion on Bus A:** This bit is set to 1 when congestion is reported after a transfer in the *CellBus* A receiver. |
| 0/6/7:1 | 5-1 | CBIDA(4-0) | ***CellBus* ID of Congested or NACK'ed queue on bus A:** This 5-bit field contains the *CellBus* ID (user number) for *CellBus* A of the *CellBus* device reporting congestion or no acknowledge on *CellBus* A. |
| 0/6/7:1 | 0 | CBBIP8A | ***CellBus* BIP-8 Error on Bus A:** This bit is set to 1 when a BIP-8 error occurs in the *CellBus* A receiver |
| 0/6/7:0 | 7 | CBCRC4TRHA | ***CellBus* Tandem Routing Header CRC-4 Error on Bus A:** This bit is set to 1 when a Tandem Routing Header CRC-4 error occurs in the *CellBus* A receiver. |
| 0/6/7:0 | 6 | CBCRC4CRHA | ***CellBus* Routing Header CRC-4 Error on Bus A:** This bit is set to 1 when a *CellBus* Routing Header CRC-4 error occurs in the *CellBus* A receiver. |
| 0/6/7:0 | 5 | CBNOGRTA | ***CellBus* Grant Timeout on Bus A:** When set to 1 this bit indicates that no bus access grant has been received by the inlet side, after a bus access request, within a time established by NGTIMER(7-0) in register 0/6/2. |
| 0/6/7:0 | 4 | CBLOFA | ***CellBus* Loss of Frame on Bus A:** This bit is set to 1 if there are two consecutive missing *CellBus* A frame pulses in 32-user mode (U16/$\overline{32}$A set to 0), and four consecutive missing *CellBus* frame pulses in 16-user mode (U16/$\overline{32}$A set to 1). |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/7:0 | 3 | CBLORCA | ***CellBus* Loss of Read Clock on Bus A:** This bit is set to 1 if the *CellBus* A read clock is not present for more than the equivalent of 32 clock cycles. |
| 0/6/7:0 | 2 | CBLOWCA | ***CellBus* Loss of Write Clock on Bus A:** This bit is set to 1 if the *CellBus* A write clock is not present for more than the equivalent of 32 clock cycles. |
| 0/6/7:0 | 1 | CBOFLWA | ***CellBus* Inlet FIFO Overflow for Bus A:** This bit is set to 1 if the *CellBus* inlet FIFO for bus A overflows. |
| 0/6/7:0 | 0 | CBOQEA | ***CellBus* Outbound Queue Empty/Full for Bus A:** - *CellBus* A egress requires servicing, status indicates either empty or full according to value of control bit EMPFLB. |
| 0/6/8:2<br>0/6/8:1 | 3-0<br>7 | CBBURSTLEN1B(4-1)<br>CBBURSTLEN1B0 | ***CellBus* Burst Length for No. 1 Burst-Monitored device on Bus B:** This 5-bit field defines a number that is approximately equivalent to the congestion level experienced at the No. 1 burst-monitored ASPEN device on *CellBus* B that is identified by CBBURSTID1B(4-0). This field is a counter that is incremented for every consecutive cell directed to this device from *CellBus* B, and is decremented twice for every frame in which no cells arrive at this ASPEN device from *CellBus* B. The counter saturates at values of 31 and 0. |
| 0/6/8:1 | 6-2 | CBBURSTID1B(4-0) | ***CellBus* ID (user number) of No. 1 Burst-Monitored Device for Bus B:** This 5-bit field is the bus B ID (user number) of No. 1 of two ASPEN devices that are currently being traced by the Burst Monitor to quantify congestion levels for use in access grant decisions by the local arbiter block on *CellBus* B. |
| 0/6/8:1<br>0/6/8:0 | 1-0<br>7-5 | CBBURSTLEN0B(4-3)<br>CBBURSTLEN0B(2-0) | ***CellBus* Burst Length for No. 0 Burst-Monitored device on Bus B:** This 5-bit field defines a number that is approximately equivalent to the congestion level experienced at the No. 0 burst-monitored ASPEN device on *CellBus* B that is identified by CBBURSTID0B(4-0). This field is a counter that is incremented for every consecutive cell directed to this device from *CellBus* B, and is decremented twice for every frame in which no cells arrive at this ASPEN device from *CellBus* B. The counter saturates at values of 31 and 0. |
| 0/6/8:0 | 4-0 | CBBURSTID0B(4-0) | ***CellBus* ID (user number) of No. 0 Burst-Monitored Device for Bus B:** This 5-bit field is the bus B ID (user number) of No. 0 of two ASPEN devices that are currently being traced by the Burst Monitor to quantify congestion levels for use in access grant decisions by the local arbiter block on *CellBus* B. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/9:2<br>0/6/9:1 | 4-0<br>7 | CBBURSTLEN1A(4-1)<br>CBBURSTLEN1A0 | ***CellBus* Burst Length for No. 1 Burst-Monitored device on Bus A:** This 5-bit field defines a number that is approximately equivalent to the congestion level experienced at the No. 1 burst-monitored ASPEN device on *CellBus* A that is identified by CBBURSTID1A(4-0). This field is a counter that is incremented for every consecutive cell directed to this device from *CellBus* A, and is decremented twice for every frame in which no cells arrive at this ASPEN device from *CellBus* A. The counter saturates at values of 31 and 0. |
| 0/6/9:1 | 6-2 | CBBURSTID1A(4-0) | ***CellBus* ID (user number) of No. 1 Burst-Monitored Device for Bus A:** This 5-bit field is the bus A ID (user number) of No. 1 of two ASPEN devices that are currently being traced by the Burst Monitor to quantify congestion levels for use in access grant decisions by the local arbiter block on *CellBus* A. |
| 0/6/9:1<br>0/6/9:0 | 1-0<br>7-5 | CBBURSTLEN0A(4-3)<br>CBBURSTLEN0A(2-0) | ***CellBus* Burst Length for No. 0 Burst-Monitored device on Bus A:** This 5-bit field defines a number that is approximately equivalent to the congestion level experienced at the No. 0 burst-monitored ASPEN device on *CellBus* A that is identified by CBBURSTID0A(4-0). This field is a counter that is incremented for every consecutive cell directed to this device from *CellBus* A, and is decremented twice for every frame in which no cells arrive at this ASPEN device from *CellBus* A. The counter saturates at values of 31 and 0. |
| 0/6/9:0 | 4-0 | CBBURSTID0A(4-0) | ***CellBus* ID (user number) of No. 0 Burst-Monitored Device for Bus A:** This 5-bit field is the bus A ID (user number) of No. 0 of two ASPEN devices that are currently being traced by the Burst Monitor to quantify congestion levels for use in access grant decisions by the local arbiter block on *CellBus* A. |
| 0/6/A:2 | 7-4 | C/NTAGB(3-0) | **CONG/NACK Tag for *CellBus* B:** This 4-bit field contains the lower nibble of a firmware-assigned tag for the cell which experienced either congestion or No Acknowledge during transfer across *CellBus* B. |
| 0/6/A:2 | 3-0 | C/NTAGA(3-0) | **CONG/NACK Tag for *CellBus* A:** This 4-bit field contains the lower nibble of a firmware-assigned tag for the cell which experienced either congestion or No Acknowledge during transfer across *CellBus* A. |
| 0/6/A:1 | 5-1 | BURSTARRESTTH(4-0) | **Burst Arrest Threshold of Arbiter-Enabled Device:** This 5-bit field defines the threshold for engagement of burst arrest in the ASPEN device that has its arbiter enabled for a *CellBus* bus. The default value to be used is 1FH. |
| 0/6/A:1 | 0 | BRSTAA | **Burst Arrest Arbiter Enable:** When set to 1, this bit enables burst arrest. |
| 0/6/A:0 | 7-5 | BURST_BACKOFF(2-0) | **Burst Backoff:** This three-bit field defines the number of *CellBus* frames for the arbiter to skip when the burst arrest is engaged. The default value to be used is 2H. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/B:3<br>0/6/B:2 | 5-0<br>7-2 | TE0FILL(11-6)<br>TE0FILL(5-0) | **Terminal Egress Class 0 Fill of Queue Space:** This 12-bit field is the count of the number of cell buffer spaces occupied by terminal (UTOPIA) egress queues of class 0. |
| 0/6/B:2<br>0/6/B:1<br>0/6/B:0 | 1-0<br>7-0<br>7-0 | TE2FILL(17-16)<br>TE2FILL(15-8)<br>TE2FILL(7-0) | **Terminal Egress Class 2 Fill of Queue Space:** This 18-bit field is the count of the number of cell buffer spaces occupied by terminal (UTOPIA) egress queues of class 2. |
| 0/6/C:3<br>0/6/C:2 | 5-0<br>7-2 | TE1FILL(11-6)<br>TE1FILL(5-0) | **Terminal Egress Class 1 Fill of Queue Space:** This 12-bit field is the count of the number of cell buffer spaces occupied by terminal (UTOPIA) egress queues of class 1. |
| 0/6/C:2<br>0/6/C:1<br>0/6/C:0 | 1-0<br>7-0<br>7-0 | TE3FILL(17-16)<br>TE3FILL(15-8)<br>TE3FILL(7-0) | **Terminal Egress Class 3 Fill of Queue Space:** This 18-bit field is the count of the number of cell buffer spaces occupied by terminal (UTOPIA) egress queues of class 3. |
| 0/6/D:3<br>0/6/D:2 | 5-0<br>7-2 | CE0FILL(11-6)<br>CE0FILL(5-0) | ***CellBus* Egress Class 0 Fill of Queue Space:** This 12-bit field is the count of the number of cell buffer spaces occupied by *CellBus* egress queues of class 0. |
| 0/6/D:2<br>0/6/D:1<br>0/6/D:0 | 1-0<br>7-0<br>7-0 | CE2FILL(17-16)<br>CE2FILL(15-8)<br>CE2FILL(7-0) | ***CellBus* Egress Class 2 Fill of Queue Space:** This 18-bit field is the count of the number of cell buffer spaces occupied by *CellBus* egress queues of class 0. |
| 0/6/E:3<br>0/6/E:2 | 5-0<br>7-2 | CE1FILL(11-6)<br>CE1FILL(5-0) | ***CellBus* Egress Class 1 Fill of Queue Space:** This 12-bit field is the count of the number of cell buffer spaces occupied by *CellBus* egress queues of class 1. |
| 0/6/E:2<br>0/6/E:1<br>0/6/E:0 | 1-0<br>7-0<br>7-0 | CE3FILL(17-16)<br>CE3FILL(15-8)<br>CE3FILL(7-0) | ***CellBus* Egress Class 3 Fill of Queue Space:** This 18-bit field is the count of the number of cell buffer spaces occupied by *CellBus* egress queues of class 3. |
| 0/6/F:3<br>0/6/F:2<br>0/6/F:1<br>0/6/F:0 | 4-0<br>7-0<br>7-0<br>7-0 | IHOFL(28-24)<br>IHOFL(23-16)<br>IHOFL(15-8)<br>IHOFL(7-0) | **Initial Head OF Free List:** This 29-bit field contains the value of the physical memory address of the first element to be taken off of the free list at start-up. |
| 0/6/12:0 | 0 | AVAIL | **Host Mailbox Available:** When this bit is set to 1, it indicates that the RP-to-host mailbox is free for the ASPEN device to send the host a message. This bit is for internal TranSwitch use only. |
| 0/6/13:3<br>0/6/13:2<br>0/6/13:1<br>0/6/13:0 | 4-0<br>7-0<br>7-0<br>7-0 | CHOFL(28-24)<br>CHOFL(23-16)<br>CHOFL(15-8)<br>CHOFL(7-0) | **Current Head Of Free List:** This 29-bit field points to the next free buffer in the linked list of free buffers. This value is constantly changing as queuing and dequeuing operations occur. This field is provided for maintenance and free list auditing purposes. |
| 0/6/1D:0 | 7-0 | OP-to-RP mailbox register (7-0) | **OP-to-RP Mailbox Register:** This is an 8-bit mailbox shadow register from OP to RP used to return tokens controlling dequeues toward the egress UTOPIA. Read-only register for RP. Reflects the current value in OP registers 0/6/1F, bits 7-0. These bits are for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/1F:3<br><br>0/6/1F:2<br><br>0/6/1F:1<br><br>0/6/1F:0 | 7-0<br><br>7-0<br><br>7-0<br><br>7-0 | Port 15 UTOPIA Sent - Port 12 UTOPIA Sent<br>Port 11 UTOPIA Sent - Port 8 UTOPIA Sent<br>Port 7 UTOPIA Sent - Port 4 UTOPIA Sent<br>Port 3 UTOPIA Sent - Port 0 UTOPIA Sent | **Cell Sent For UTOPIA Port n (n=15-0):** Sixteen 2-bit rollover counters, one for each UTOPIA port, indicating a cell has been transferred across the egress UTOPIA interface. Used by the RP scheduler to throttle cells to a given port. The odd-numbered bits are the most significant bits. These counters are not incremented if a cell is dequed toward an inactive port as configured in ETE15-ETE0 bits in the OP. These bits are for internal TranSwitch use only. |
| 0/6/20:1<br><br>0/6/20:0 | 7-0<br><br>7-0 | Max QID from *CellBus* (15-8)<br>Max QID from *CellBus* (7-0) | 16-bit value used to compare against the outlet queue index of a received cell which is derived from the R1, R0, Q1, Q0, and TRH of the received cell. Cells exceeding the max are discarded. Avoids indexing beyond outlet FPT table bounds. Initial value=FFFFH. |
| 0/6/21:0 | 0 | 30BLU | **30-Bit Lookup:** When this bit is set to 1, it enables the inlet header lookup table to address 64 port UNI, 4 port NNI address space. This bit is for internal TranSwitch use only. |
| 0/6/22:3 | 7 | TE0MCE | **Terminal Egress Max Cells Exceeded for category 0 (CBR):** Latched state capturing a service class overflow of the TE0Max value. Can be reset by firmware back to zero after the event has been reported to the host. This bit is for internal TranSwitch use only. |
| 0/6/22:3 | 6 | TE2MCE | **Terminal Egress Max Cells Exceeded for category 2 (VBR-nrt):** Latched state capturing a service class overflow of the TE2Max value. Can be reset by firmware back to zero after the event has been reported to the host. This bit is for internal TranSwitch use only. |
| 0/6/22:3<br>0/6/22:2 | 5-0<br>7-2 | TE0Max (11-6)<br>TE0Max (5-0) | **Terminal Egress SC0 Max Cell Count:** Cell count limit for class 0 (CBR) service category in the outlet queue space. Once TE0FILL reaches TE0Max, all CBR cells entering the outlet queue space will be discarded until TE0FILL falls below TE0Max. These bits are for internal TranSwitch use only. |
| 0/6/22:2<br>0/6/22:1<br>0/6/22:0 | 1-0<br>7-0<br>7-0 | TE2Max (17-16)<br>TE2Max (15-8)<br>TE2Max (7-0) | **Terminal Egress SC2 Max Cell Count:** Cell count limit for class 2 (VBR-nrt) service category in the outlet queue space. Once TE2FILL reaches TE2Max, all VBR-nrt cells entering the outlet queue space will be discarded until TE2FILL falls below TE2Max. These bits are for internal TranSwitch use only. |
| 0/6/23:3 | 7 | TE1MCE | **Terminal Egress Max Cells Exceeded for category 1 (VBR-rt):** Latched state capturing a service class overflow of the TE1Max value. Can be reset by firmware back to zero after the event has been reported to the host. This bit is for internal TranSwitch use only. |
| 0/6/23:3 | 6 | TE3MCE | **Terminal Egress Max Cells Exceeded for category 3 (UBR):** Latched state capturing a service class overflow of the TE3Max value. Can be reset by firmware back to zero after the event has been reported to the host. This bit is for internal TranSwitch use only. |

| Address:Byte | Bit | Symbol | Description |
|---|---|---|---|
| 0/6/23:3<br>0/6/23:2 | 5-0<br>7-2 | TE1Max (11-6)<br>TE1Max (5-0) | **Terminal Egress SC1 Max Cell Count:** Cell count limit for class 1 (VBR-rt) service category in the outlet queue space. Once TE1FILL reaches TE1Max, all VBR-rt cells entering the outlet queue space will be discarded until TE1FILL falls below TE1Max. These bits are for internal TranSwitch use only. |
| 0/6/23:2<br>0/6/23:1<br>0/6/23:0 | 1-0<br>7-0<br>7-0 | TE3Max (17-16)<br>TE3Max (15-8)<br>TE3Max (7-0) | **Terminal Egress SC3 Max Cell Count:** Cell count limit for class 3 (UBR) service category in the outlet queue space. Once TE3FILL reaches TE3Max, all UBR cells entering the outlet queue space will be discarded until TE3FILL falls below TE3Max. These bits are for internal TranSwitch use only. |

**BASE POINTER RAM ACCESS:**

ASPEN contains a Base Pointer RAM (BPRAM) which is used to perform indexed-based reads and writes to the control tables in SSRAM. There are 32 entries in the table and each entry defines the physical base address of a given SSRAM control table. The BPRAM is initialized at startup by the device driver when the control tables are dimensioned. Thereafter, the values are used to find the base physical address for a given control table.

**Base Pointer RAM**

| Table # | Table Base Address |
|---|---|
| 0 | SSRAM base address for Control Table 0 |
| 1 | SSRAM base address for Control Table 1 |
| 2 | SSRAM base address for Control Table 2 |
| :<br>:<br>: | :<br>:<br>: |
| 31 | SSRAM base address for Control Table 31 |

**Figure 71. Base Pointer RAM Write Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00011 | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 1H | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=110 (BPRAM) | | |
| | 0 | DEST=00 (BPRAM) | | 0 | IRH=Offset into Base Pointer RAM | | | | |
| 1 | 3 | 00H (not used) | | | | | | | |
| | 2 | 00H (not used) | | | | | | | |
| | 1 | 00H (not used) | | | | | | | |
| | 0 | 00H (not used) | | | | | | | |
| 2 | 3 | Base Pointer RAM value (31-24) | | | | | | | |
| | 2 | Base Pointer RAM value (23-16) | | | | | | | |
| | 1 | Base Pointer RAM value (15-8) | | | | | | | |
| | 0 | Base Pointer RAM value (7-0) | | | | | | | |

**Figure 72. Base Pointer RAM Read Request Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00011 | | | | | 1=Read | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 1H | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=110 (BPRAM) | | |
| | 0 | DEST=00 (BPRAM) | | 0 | IRH=Offset into Base Pointer RAM | | | | |
| 1 | 3 | 00H (not used) | | | | | | | |
| | 2 | 00H (not used) | | | | | | | |
| | 1 | 00H (not used) | | | | | | | |
| | 0 | 00H (not used) | | | | | | | |

**SSRAM ACCESS:**

The following access mechanisms are provided for the SSRAM interface.

1. SSRAM Table Access
2. SSRAM Maskable Table Write,
3. SSRAM Physical Address Access,
4. Management Cell Insertion to Inlet or Outlet Queue space,
5. OAM Cell Transfer from Control Table to Traffic Queue.

**Figure 73. SSRAM Table Access Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=10000 | | | | | 0=Write 1=Read | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 1 up to Eh | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=100 (SSRAM) | | |
| | 0 | DEST=00 (SSRAM) | | 0 | IRH=Base Pointer RAM Table Number(0-31) | | | | |
| 1 | 3 | 00H (not used) | | | | | | | |
| | 2 | 00H (not used) | | | | | | | |
| | 1 | 00H (not used) | | | | | | | |
| | 0 | 00H (not used) | | | | | | | |
| 2 | 3 | Table Record Number(15-8) | | | | | | | |
| | 2 | Table Record Number(7-0) | | | | | | | |
| | 1 | Record Offset | | | | | | | |
| | 0 | Record Length | | | | | | | |
| 3 | 3 | Table Entry Data(31-24) | | | | | | | |
| | 2 | Table Entry Data(23-16) | | | | | | | |
| | 1 | Table Entry Data(15-8) | | | | | | | |
| | 0 | Table Entry Data(7-0) | | | | | | | |
| 4 | 3 | : | | | | | | | |
| | 2 | : | | | | | | | |
| | 1 | : | | | | | | | |
| | 0 | : | | | | | | | |
| max length | 3 | Table Entry Data(31-24) | | | | | | | |
| | 2 | Table Entry Data(23-16) | | | | | | | |
| | 1 | Table Entry Data(15-8) | | | | | | | |
| | 0 | Table Entry Data(7-0) | | | | | | | |

Table Record Number: Table index to be accessed
Record Offset: Number of 32-bit words from the start of the table record to begin transfer
Record Length: Size of each table record in this table
Table Entry Data: Message payload

**Figure 74. SSRAM Maskable Table Write Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00010 (Maskable write) | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 1 | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=100 (SSRAM) | | |
| | 0 | DEST=00 (SSRAM) | | 0 | IRH=Base Pointer RAM Table Number(0-31) | | | | |
| 1 | 3 | 00H (not used) | | | | | | | |
| | 2 | 00H (not used) | | | | | | | |
| | 1 | 00H (not used) | | | | | | | |
| | 0 | 00H (not used) | | | | | | | |
| 2 | 3 | Table Record Number(15-8) | | | | | | | |
| | 2 | Table Record Number(7-0) | | | | | | | |
| | 1 | Record Offset | | | | | | | |
| | 0 | Record Length | | | | | | | |
| 3 | 3 | Mask value(31-24) | | | | | | | |
| | 2 | Mask value(23-16) | | | | | | | |
| | 1 | Mask value(15-8) | | | | | | | |
| | 0 | Mask value(7-0) | | | | | | | |
| 4 | 3 | Data value(31-24) | | | | | | | |
| | 2 | Data value(23-16) | | | | | | | |
| | 1 | Data value(15-8) | | | | | | | |
| | 0 | Data value(7-0) | | | | | | | |



Table Record Number: Table index to be written
Record Offset: Number of 32-bit words from the start of the table record
Record Length: Size of a table record in this table
Mask value: A ’1’ indicates to change the corresponding SSRAM data bit to the state in "Data value".
Data value: Data to be written to SSRAM.

**Figure 75. SSRAM Physical Address Access Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00100 | | | | | 0=Write 1=Read | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 1 up to Eh | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=100 (SSRAM) | | |
| | 0 | DEST=00 (SSRAM) | | 0 | IRH=0 (not used) | | | | |
| 1 | 3 | 00H (not used) | | | | | | | |
| | 2 | 00H (not used) | | | | | | | |
| | 1 | 00H (not used) | | | | | | | |
| | 0 | 00H (not used) | | | | | | | |
| 2 | 3 | Physical Address(31-24) | | | | | | | |
| | 2 | Physical Address(23-16) | | | | | | | |
| | 1 | Physical Address(15-8) | | | | | | | |
| | 0 | Physical Address(7-0) | | | | | | | |
| 3 | 3 | Data value(31-24) | | | | | | | |
| | 2 | Data value(23-16) | | | | | | | |
| | 1 | Data value(15-8) | | | | | | | |
| | 0 | Data value(7-0) | | | | | | | |
| 4 | 3 | : | | | | | | | |
| | 2 | : | | | | | | | |
| | 1 | : | | | | | | | |
| | 0 | : | | | | | | | |
| max length | 3 | Data value(31-24) | | | | | | | |
| | 2 | Data value(23-16) | | | | | | | |
| | 1 | Data value(15-8) | | | | | | | |
| | 0 | Data value(7-0) | | | | | | | |

**Figure 76. Management Cell Insertion Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00100 (RP managed transfer) | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 0Eh | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=001 (OP) | | |
| | 0 | DEST=01 (OP) | | 0 | IRH=1 (quick insertion) | | | | |
| 1 | 3 | 0 | DIS=0 | EOP=0 | SC | | M/C=0 | MSN (8-7)=00 | |
| | 2 | MSN (6-0)=0000000 | | | | | | | C/T |
| | 1 | QID - MSB | | | | | | | |
| | 0 | QID - LSB | | | | | | | |
| 2 | 3 | CBRH - MSB | | | | | | | |
| | 2 | CBRH - LSB | | | | | | | |
| | 1 | TRH - MSB | | | | | | | |
| | 0 | TRH - LSB | | | | | | | |
| 3 | 3 | ATM cell header | | | | | | | |
| | 2 | ATM cell header | | | | | | | |
| | 1 | ATM cell header | | | | | | | |
| | 0 | ATM cell header | | | | | | | |
| 4 | 3 | cell payload - byte 0 | | | | | | | |
| | 2 | cell payload | | | | | | | |
| | 1 | cell payload | | | | | | | |
| | 0 | cell payload | | | | | | | |
| 5 - 14 | 3 | : | | | | | | | |
| | 2 | : | | | | | | | |
| | 1 | : | | | | | | | |
| | 0 | : | | | | | | | |
| 15 | 3 | cell payload | | | | | | | |
| | 2 | cell payload | | | | | | | |
| | 1 | cell payload | | | | | | | |
| | 0 | cell payload - byte 47 | | | | | | | |

SC: Service Category assignment, ’00’=CBR, ’01’=VBR-rt, ’10’=VBR-nrt, ’11’=UBR/GFR.

C/$\overline{T}$: Defines the queue space, ’0’ is inlet queue space, ’1’ is outlet queue space.

QID: Defines traffic queue for cell.

**Figure 77. OAM Cell Transfer from Control Table to Traffic Queue Message Format**

| Word No. | Byte No. | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 3 | OPCODE=00100 (RP managed transfer) | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 3 | | | | |
| | 1 | SRC = 01100 (host) | | | | | DEST=01001 (RP) | | |
| | 0 | DEST=01 (RP) | | 1 | IRH=0 (with envelope) | | | | |
| 1 | 3 | 00h (GP bus control) | | | | | | | |
| | 2 | 00h (GP bus control) | | | | | | | |
| | 1 | 00h (GP bus control) | | | | | | | |
| | 0 | 00h (GP bus control) | | | | | | | |
| 2 | 3 | OPCODE=00101 | | | | | 0=Write | 1 | 1 |
| | 2 | 0 | 0 | 0 | LENGTH = 1 | | | | |
| | 1 | SRC = 01001 (RP) | | | | | DEST=100 (SSRAM) | | |
| | 0 | DEST=00 (SSRAM) | | 1 | IRH=01101 (host insertion table) | | | | |
| 3 | 3 | Record Number - MSB | | | | | | | |
| | 2 | Record Number - LSB | | | | | | | |
| | 1 | Record Offset | | | | | | | |
| | 0 | Record Length | | | | | | | |
| 4 | 3 | 0 | DIS=0 | EOP=0 | SC | | M/C=0 | MSN (8-7)=00 | |
| | 2 | MSN (6-0)=0000000 | | | | | | | C/T |
| | 1 | QID - MSB | | | | | | | |
| | 0 | QID - LSB | | | | | | | |

Header (words 2 and 3 of message):
Opcode: SSRAM control space to SSRAM queue space - 00101 or 00110 for CRC-10 calculation
Table Record Number: Table index to read cell from.
Record Offset: Number of 32-bit words from the start of the table record
Record Length: Size of a table record in this table
SC: Service Category assignment, ’00’=CBR, ’01’=VBR-rt, ’10’=VBR-nrt, ’11’=UBR/GFR.
C/$\overline{T}$: Defines the queue space, ’0’ is inlet queue space, ’1’ is outlet queue space.
QID: Defines traffic queue for cell.

## OPERATION

The ASPEN device functions are determined by the operational firmware used for each particular application, and details are provided in the AccessEDGE Firmware User's Guide for that application.

For example, detailed information on ASPEN device functions when it is operating with ATM AccessEDGE firmware can be found in the ATM AccessEDGE Firmware User's Guide (document number TXC-05812-IM1). With the ATM AccessEDGE firmware loaded, the ASPEN device implements the ATM Layer processing functions of the ATM UNI/NNI, performing cell discrimination for up to 16k connections, payload type discrimination, loss priority indication, and cell/packet discard. The device also performs ATM Layer Management functions (invalid PHY/VPI/VCI, UPC, statistics, queuing, scheduling, and congestion control) and provides full support for OAM Fault Management (AIS/RDI, Continuity Check, and Loopback).

### RECOMMENDATIONS FOR ON-CHIP PLL

A resistor-capacitor filter between $V_{DD2.5}$ and ground is recommended for generating the analog PLLVDD power supply required by the phase-locked loop circuit (PLL) in the ASPEN device, as shown in Figure 78. PLLVSS is a separate ground associated with this derived power supply. Note: When performing PCB layout, place the resistor-capacitor filter as close as possible to the PLLVDD and PLLVSS leads.

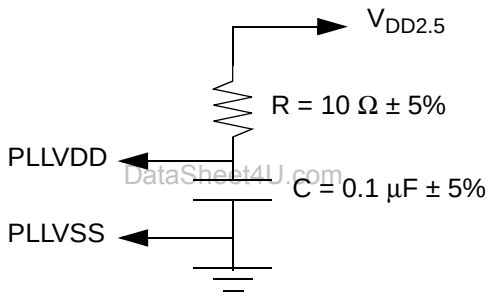
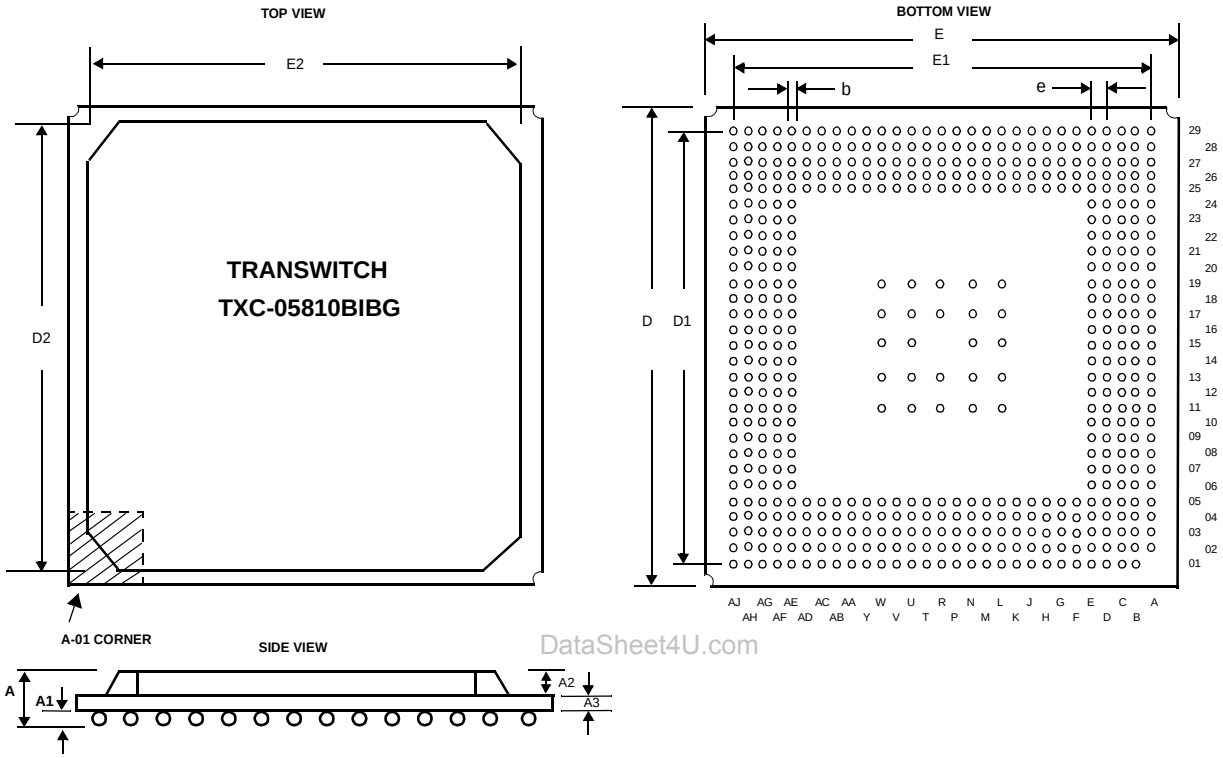



**Figure 78. RC Filter for PLLVDD**

## PACKAGE INFORMATION

The ASPEN device is packaged in a 503-lead plastic ball grid array (PBGA) suitable for surface mounting, as illustrated in Figure 79.






| Dimension (Note 1) | Min | Nominal | Max |
|---|---|---|---|
| A | 2.11 | 2.33 | 2.56 |
| A1 | 0.50 | 0.60 | 0.70 |
| A2 | 1.10 | 1.17 | 1.25 |
| A3 | | 0.56 REF | |
| b | 0.60 | 0.75 | 0.90 |
| D | 39.80 | 40.00 | 40.20 |
| D1 | | 35.56 BSC | |
| D2 | 37.50 | 38.50 | 39.50 |
| E | 39.80 | 40.00 | 40.20 |
| E1 | | 35.56 BSC | |
| E2 | 37.50 | 38.50 | 39.50 |
| e | | 1.27 BSC | |

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Diagram is stylized and not to scale.
3. Size of array: 29 x 29, JEDEC code MO-151.

**Figure 79. ASPEN Device (TXC-05810B) 503-Lead Plastic Ball Grid Array Package**

## ORDERING INFORMATION

Part Number: TXC-05810BIBG 503-Lead Plastic Ball Grid Array Package

## RELATED PRODUCTS

TXC-05802B, CUBIT-*Pro* VLSI Device (ATM *CellBus* switch fabric). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* architecture. A single-chip solution, the CUBIT-*Pro* has the ability to send and also receive cells for control purposes over the same *CellBus*. The *CellBus* technology works at aggregate rates of up to 1 Gbit/s and provides header translation, multiplexing, concentration, and switching functions for a wide variety of small-to-medium size ATM systems.

TXC-05804, CUBIT-3 VLSI Device (Multi-PHY *CellBus* Switch Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

TXC-05805, CUBIT-622 VLSI Device (Multi-PHY *CellBus* Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements are a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO has been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface.

TXC-05810, first product variant of ASPEN Device. ASPEN supports *CellBus* operation in both Cell and Packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation. Line interface is via UTOPIA 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables, is stored in an external synchronous SRAM.

TXC-05811, ASPEN-PX VLSI Device (ASPEN Port Expander). A single chip solution for increasing the UTOPIA port density of ASPEN based systems. The ASPEN-PX device acts as a port expander enabling the ASPEN (TXC-05810B) to address up to 64 ports on the UTOPIA Level 2 interface.

TXC-06203, PHAST-3P VLSI Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA 2P Interface). The PHAST-3P uses an 8/16-bit UTOPIA 2P Single-PHY or Multi-PHY interface for downstream access.

## STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

**ANSI (U.S.A.):**

**American National Standards Institute**
*25 West 43rd Street*
*New York, New York 10036*
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

**The ATM Forum (U.S.A., Europe, Asia):**

*404 Balboa Street*
*San Francisco, CA 94118*
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

**ATM Forum Europe Office**

*Kingsland House - 5th Floor*
*361-373 City Road*
*London EC1 1PQ, England*
Tel: 20 7837 7882
Fax: 20 7417 7500



**ATM Forum Asia-Pacific Office**

*Hamamatsucho Suzuki Building 3F*
*1-2-11, Hamamatsucho, Minato-ku*
*Tokyo 105-0013, Japan*
Tel: 3 3438 3694
Fax: 3 3438 3698



**Bellcore** (See Telcordia)

**CCITT (**See ITU-T)

**EIA (U.S.A.):**

**Electronic Industries Association**
**Global Engineering Documents**
*15 Inverness Way East*
*Englewood, CO 80112*
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

**ETSI (Europe):**

**European Telecommunications Standards Institute**
*650 route des Lucioles*
*06921 Sophia-Antipolis Cedex, France*
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

**GO-MVIP (U.S.A.):**

**The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)**
*3220 N Street NW, Suite 360*
*Washington, DC 20007*

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

**ITU-T (International):**

**Publication Services of International Telecommunication Union**
**Telecommunication Standardization Sector**
*Place des Nations, CH 1211*
*Geneve 20, Switzerland*

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

**MIL-STD (U.S.A.):**

**DODSSP Standardization Documents Ordering Desk**
*Building 4 / Section D*
*700 Robbins Avenue*
*Philadelphia, PA 19111-5094*

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil



**PCI SIG (U.S.A.):**

**PCI Special Interest Group**
*5440 SW Westgate Dr., #217*
*Portland, OR 97221*



Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

**Telcordia (U.S.A.):**

**Telcordia Technologies, Inc.**
**Attention - Customer Service**
*8 Corporate Place Rm 3A184*
*Piscataway, NJ 08854-4157*

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

**TTC (Japan):**

**TTC Standard Publishing Group of the Telecommunication Technology Committee**
*Hamamatsu-cho Suzuki Building*
*1-2-11, Hamamatsu-cho, Minato-ku*
*Tokyo 105-0013, Japan*

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

## LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated ASPEN TXC-05810B Data Sheet that have significant differences relative to the previous and now superseded ASPEN TXC-05810B Data Sheet.

Updated ASPEN TXC-05810B Data Sheet:*PRELIMINARY* Edition 3, June 2002

Previous ASPEN TXC-05810B Data Sheet:*PRELIMINARY* Edition 2, April 2002

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet.

| Page Number of Updated Data Sheet | Summary of the Change |
|---|---|
| All | Changed edition number and date. |
| 1 | Changed fifth bullet of Features section. |
| 2 - 4 | Updated Table of Contents and List of Figures. |
| 14 | Changed Note for UTOPIA Level 2P section. |
| 16, 20 | Added Note to Packet Interface Mode section. |
| 24 | Changed Note for Serial Control Interface section. Added Note to Host Interface section and changed first paragraph. |
| 27 | Changed first paragraph of Serial EEPROM Interface section. Moved Note to top of paragraph. Changed paragraph for SSRAM Memory Interface section. |
| 164 | Added last sentence to Description for Symbols SDW, HSTSZ, $\overline{\text{TST16K}}$ and HASTDW. |
| 182 | Changed List of Data Sheet Changes section. |

## - NOTES -



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