

PRODUCT INFORMATION

FEATURES

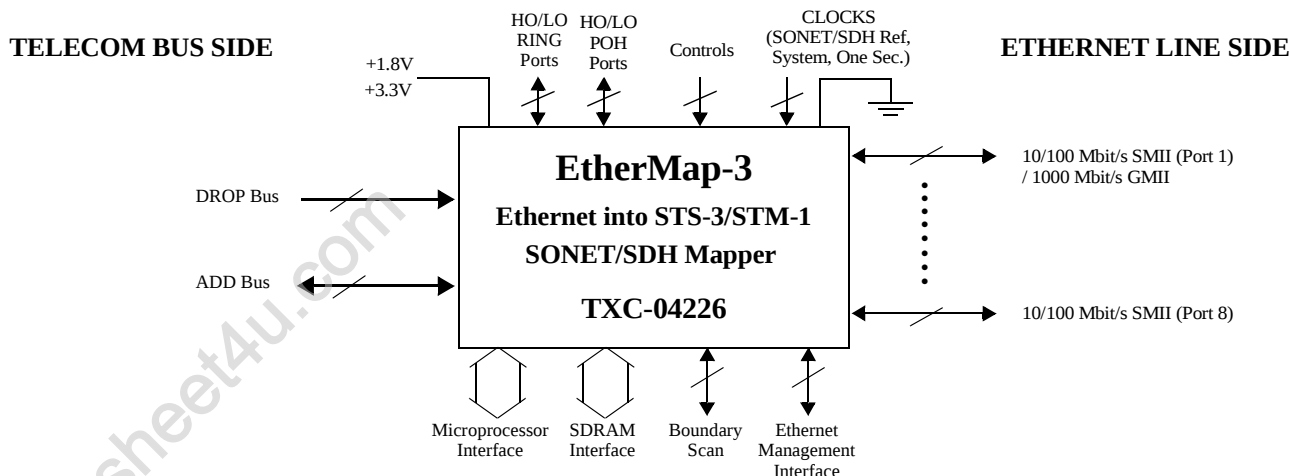
- Supports up to eight 10/100 Mbit/s Ethernet ports, each using a SMII interface
- Supports a single 1000 Mbit/s Ethernet port, using a parallel GMII interface (pin shared with SMII interfaces)
- Supports Ethernet Management interface for control and configuration of externally connected PHYs.
- Supports IEEE 802.3 flow control and management statistics (RMON) on 10/100/1000 Mbit/s Ethernet ports
- Supports Ethernet frame encapsulation/decapsulation protocols:
 - ITU-T G.7041, Generic Framing Procedure (GFP)
 - ITU-T X.86/X.85, Link Access Procedure SDH (LAPS)
 - ITU-T Q.922, Link Access Procedure Frame Mode (LAPF)
- Performs mapping/demapping of encapsulated Ethernet frames into/from low order (VT1.5 SPE/VC-12) and high order (STS-1 SPE/VC-3) virtual concatenated payloads
- Performs mapping/demapping of encapsulated Ethernet frames into/from a single contiguous concatenated (STS-3c-SPE/VC-4) payload
- Supports optional LCAS processing (per ITU-T G.7042) for low and high order virtual concatenated payloads
- Glueless memory interface to external 64/128Mb SDRAMs
- Supports 84/63 VT/TU Low Order POH and Pointer processing
- Supports High Order POH processing for STS-1/VC-3/STS-3c/VC-4
- Byte-wide parallel Add and Drop Telecom Bus interfaces
- Supports per-port Ethernet side and SONET/SDH system side loopback for system level diagnostics
- 16-bit wide microprocessor interface, selectable between Motorola or Intel
- Boundary scan (IEEE 1149.1 standard)
- + 3.3V and +1.8V power supplies, 5V tolerant I/O leads
- 256-lead plastic ball grid array package (27 mm x 27 mm)

DESCRIPTION

The EtherMap[™]-3 is a highly integrated device that provides for mapping of 10/100/1000 Mbit/s Ethernet into SONET/SDH STS-3/STM-1 Transport payloads. The device supports connection for up to eight 10/100 Mbit/s Ethernet ports, using SMII interfaces, or a single 1000 Mbit/s Ethernet port, using a GMII interface. In the transmit direction, for each port, received Ethernet frames are encapsulated using either GFP, LAPS or LAPF protocol. The encapsulated Ethernet frames are then mapped into a configurable number of virtual concatenated low and high order payloads, such as VT1.5 SPE/VC-12/STS-1 SPE/VC-3, or a contiguous concatenated payload such as STS-3c SPE/VC-4. For both low and high order payloads, the required SONET/SDH POH bytes are generated and output using a byte-wide parallel interface in the TranSwitch Telecom Bus format. The EtherMap-3 supports Drop bus and Add bus timing modes. In the receive direction, for each Ethernet port, a configurable number of low and high order payloads are terminated, with complete POH byte processing for virtual or contiguous concatenated payloads. Using an external SDRAM, alignment and differential delay compensation for the received low and high order virtual concatenated payloads is performed. The Ethernet frames are then decapsulated using GFP, LAPS or LAPF protocol and forwarded to each Ethernet port. For both low and high order virtual concatenated payloads, optional standards based LCAS processing is provided to allow hitless dynamic bandwidth adjustments. In addition to support for full-rate Ethernet transfer, over-subscribed Ethernet transfers are also supported using back pressure mechanisms in order to prevent frame loss.

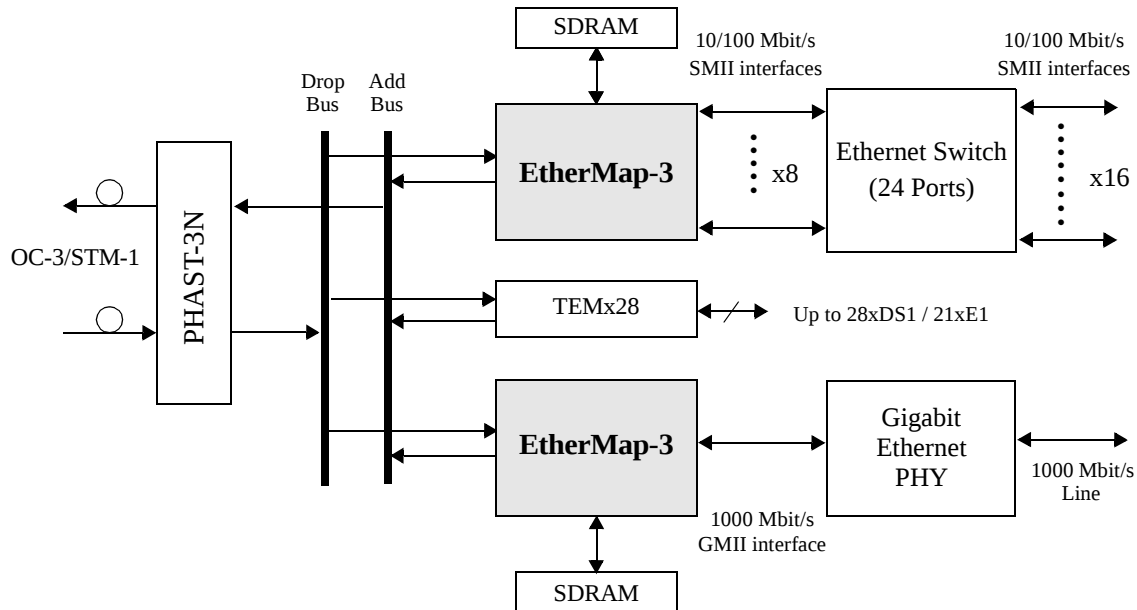
APPLICATIONS

- SONET/SDH add/drop and terminal multiplexers
- Multi-service access platforms
- Next generation Ethernet switches
- IP DSLAMS
- Integrated access devices



APPLICATION DIAGRAM

Multi-service Ethernet Aggregation with OC-3/STM-1 Uplink



RELATED PRODUCTS

- TXC-03453 Triple Level 3 Mapper VLSI Device (TL3M)
- TXC-04222 21/28 Channel Dual Bus High Density Mapper (TEMx28)
- TXC-06103 STM-1/STS-3/STS-3c SDH/SONET Overhead Terminator (PHAST-3N)
- TXC-06212 Programmable, High Performance ATM/PPP/TDM SONET/SDH Terminator for Level 12 with Enhanced Features VLSI Device (PHAST-12E)

FURTHER INFORMATION

Contact TranSwitch for technical and ordering information on these products.

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