TW8816 - LCD Flat Panel Processor with built-in MCU, NTSC/PAL/SECAM Decoder, T-CON and Analog RGB Support

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General Description

The TW8816 is a highly integrated multi-purpose LCD display solution for both analog and digital panels. To reduce BOM cost, TW8816 integrates an 8-bit MCU and a CCFL controller. Through multiple input ports, TW8816 can directly display video and graphic content from a variety of devices including TV Tuners, DVD players, back-up cameras, DTV/DMB receivers and navigation/GPS receivers.

Key Features

- Supports analog inputs including CVBS, S-Video, YPbPr & RGB signals and digital inputs including 24 bit RGB & 8/16/24 bit YCbCr. Interlaced and progressive ITU 656 inputs are supported.
- Supports both digital & analog panels up to WXGA resolutions
- Integrates cost saving features including a CCFL controller, charge pump booster, programmable panel offset control and on-chip 8 bit 8051 MCU with SPI interface
- Embedded Image Enhancement
    - Programmable CTI, hue, brightness, saturation, contrast & sharpness control
    - Black/White Stretch
    - Programmable favorite color enhancement- up to three colors
    - Programmable Gamma Correction tables

Features List

Analog Video Decoder

- NTSC (M, 4.34) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection
- Advanced synchronization processing for VCR trick play signal
- Three 10-bit ADCs and analog clamping circuit.
- Built-in analog anti-aliasing filter
- Fully programmable static gain or automatic gain control for the Y or CVBS channel
- Programmable white peak control for the Y or CVBS channel
- Software selectable analog inputs allows any of the following
    - Up to 4 composite video
    - UP to 3 S-Video
    - Up to 2 analog YPbPr and RGB
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Digital PLL for both color and horizontal locking
- Programmable hue, brightness, saturation, contrast, sharpness, Gamma control, and noise suppression
- Automatic color control and color killer
- Detection of level of copy protection according to Macrovision standard

Analog RGB / YPbPr input

- Built-in sync processor for SOG support
- Built-in Line-locked PLL
- Built-in input measurement function
- Support directly sampling up to SVGA(50MHz).

Digital interface

- Allows connection to 8/16/24-bit RGB/YCbCr
- Support both interlaced and progressive ITU 656.

TFT Panel Support

- Supports a variety of Digital single pixel TFT panels and Analog active matrix TFT panels
- Supports digital TTL panel up to WXGA(1280 x 768), 100MHz and analog panel up to WQVGA (480 x 234), 20 MHz
- Supports 3, 4, 6 or 8 bits per pixel format

Built-in Microcontroller

- Supports external SPI Interface and I2C Master interface with GPIO
- Supports 8 MCU GPIO
- Supports UART interface with GPIO
- Support IR or interrupt with GPIO

CCFL Controller

- Single channel CCFL controller based on push-pull architecture
- Lamp fault monitoring- Lamp Open, Lamp Over-current, Failure to Strike and Over-voltage
- Programmable Lamp Frequency to move EMI spurs out of band
- Analog or digital brightness control. 300:1 dimming range with the digital brightness control.
- Low power stand-by mode

OSD

- Built-in OSD controller with integrated character 202 ROM and programmable 227 RAM fonts.
- Multi-window (4) OSD support with color pallet
- 16 font & window colors available
- Support OSD overlay with alpha blending

Image Enhancement

- Programmable hue, brightness, saturation, and contrast controls.
- Sharpness control with vertical peaking
- Programmable CTI control
- Built-in de-interlacing engine
- Independent RGB gain and offset controls
- Panorama / Water-glass scaling
- YCbCr hue adjustment
- Programmable Gamma correction tables
- Programmable favorite color enhancement

Power Management

- Supports Panel power sequencing.
- Supports DPMS for monitor power management.
- 1.8 / 3.3 V operation

Timing Controller (TCON)

- Support programmable interface signals for control
- Column (source) driver / row (gate) driver

Miscellaneous

- Supports 2-wire serial bus interface
- Spread spectrum PLL
- Low-speed ADC for KEY scan
- Programmable panel VCOM offset control
- 5V tolerant I/O
- Power-down mode
- Typical power consumption < 500mW
- Single 27MHz crystal

Order Information

Package Description

Part #	Name	Description	Pin Count	Body Size
TW8816	LQFP 128	Low Profile Quad Flat Package	128	14 x 20 mm^2
	TFBGA 144	Thin & fine-pitch Ball Grid Array	144	7 x 7 mm^2

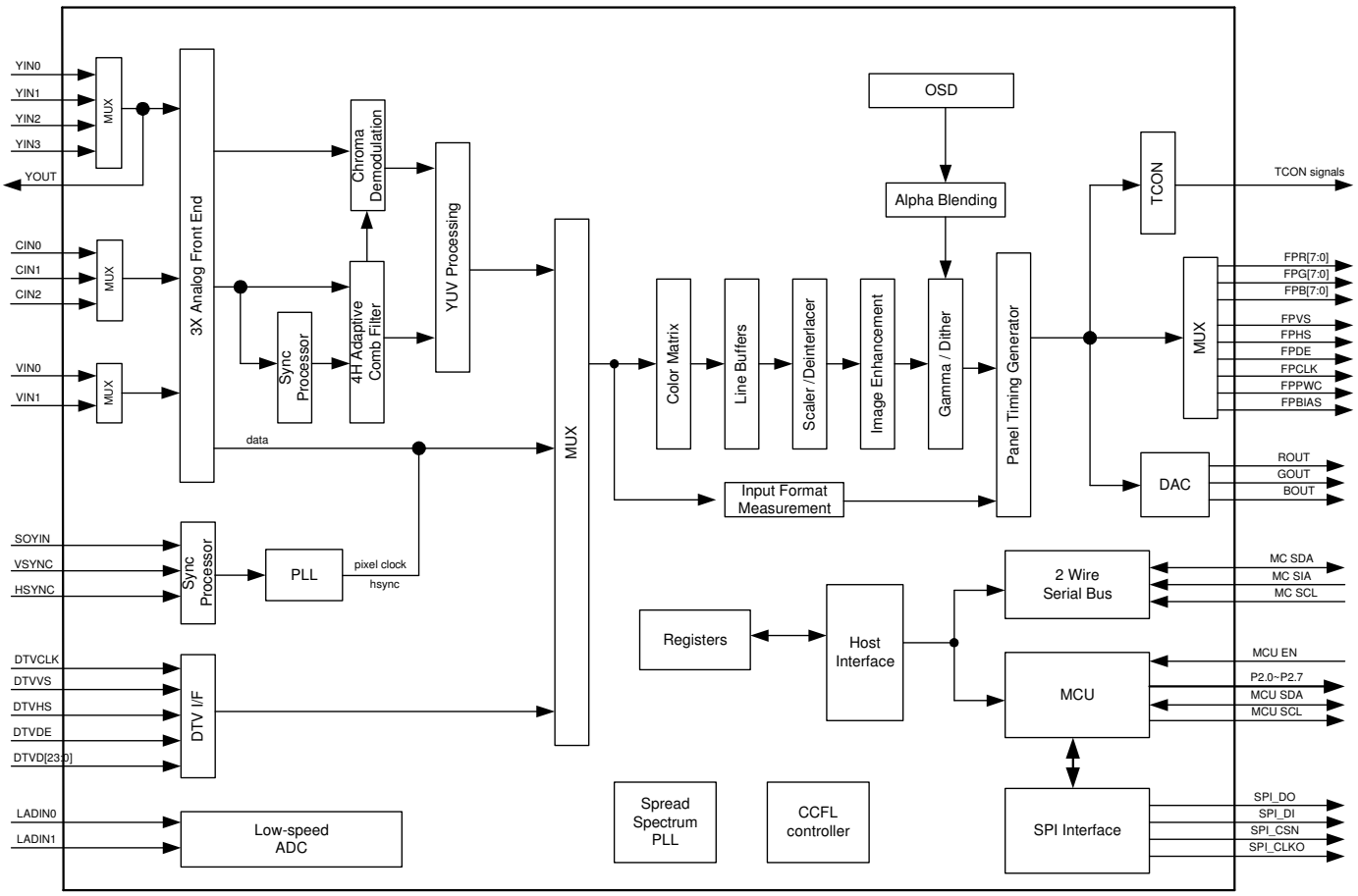


Figure 1 TW8816 Flat Panel TV/Monitor controller functional block diagram

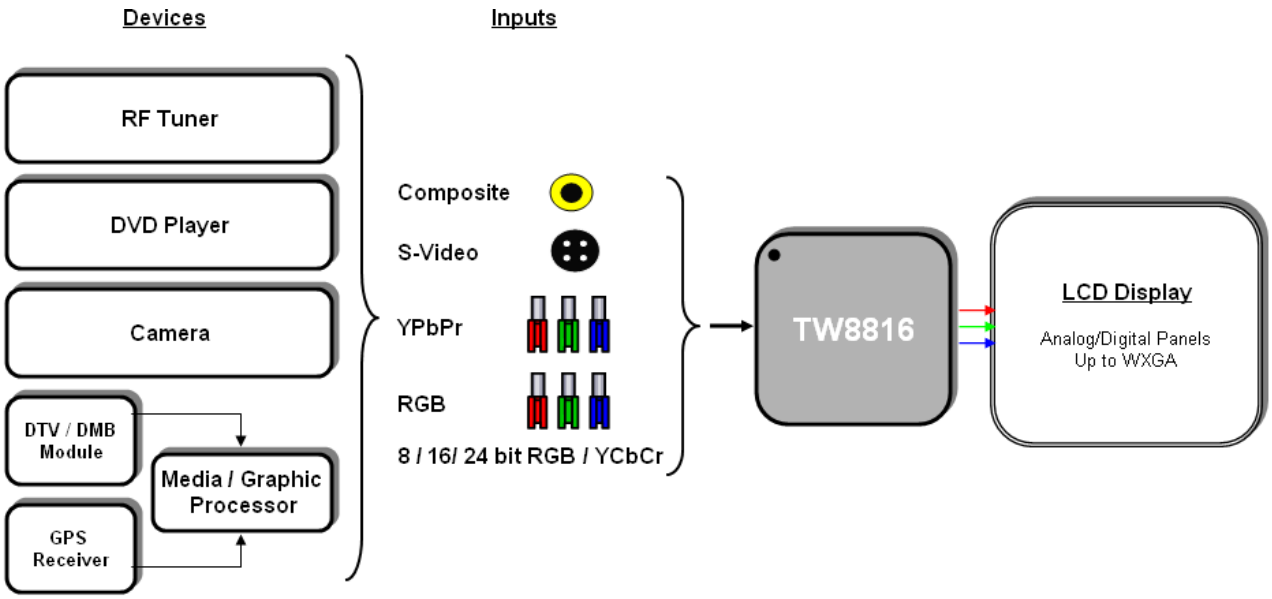


Figure 2 TW8816 Flat Panel TV/Monitor controller system block diagram

Functional Description

Overview

Techwell's TW8816 Flat Panel TV/Monitor controller is a low cost high quality TFT panel controller with embedded NTSC/PAL/SECAM TV decoder. This unique level of mixed signal integration enables the panel to be used as a stand-alone analog TV. An integrated YPbPr component input allows direct connection to DVD sources. Separated digital inputs allow it to be used as a high quality computer monitor. It incorporates easy-to-operate and powerful features in a single package for multi-purpose PC display and LCD/TV entertainment systems.

The TW8816 contains all the logic required to convert standard TV, DTV, and PC monitor signals to the digital control and data signals required to drive various TFT panel types. It supports TFT panel resolutions up to WXGA.

The chip accepts CVBS (composite) analog input or S-video analog input or YPbPr input for use as a video monitor. Up to four physical CVBS inputs or three S-video input or two component input or two RGB input can be connected synchronously.

The integrated analog front-end contains 3 ADCs with clamping circuits and Automatic Gain Control (AGC) circuit to minimize external component count. It employs a 4H, 5-line adaptive comb filter and proprietary Y/C processing technologies to produce exceptionally high quality pictures.

The chip's internal logic synchronizes the panel frame rate to the incoming input frame rate. A high quality image-scaling engine is used to convert the lower resolution formats or high resolution DTV formats to the output panel resolution. An internal de-interlacing engine also allows interlaced video to be supported.

On Screen Display is supported through on-chip OSD ROM/RAM combination for maximum flexibility. A Closed Caption decoder is built in. The TW8816 also accepts a 24 bit digital RGB input from external digital sources for use as Navigation monitor. In addition, it accepts 8/16/24 bits digital YCbCr input for direct connection with other digital source like MPEG decoder.

The TW8816 also supports TFT panel power sequencing, DPMS (VESATM Display Power Management Signaling) signaling and power management. The control interface is a 2-wire serial bus interface. The TW8816 core operates at 1.8 V, the IO at 3.3 V and packaged in a 128-pin LQFP package.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are three analog channels. Each channel contains clamping circuit, AGC circuit, Anti-aliasing filter and high performance ADCs to minimize the external component used. There are total 9 analog inputs for maximum flexibility. Software selectable analog inputs allow many possible input combinations between composite video, S-video, component video and RGB video inputs. In the case of component or RGB video mode, the built-in SOG processing circuit and PLL provides synchronization as well as format detection for various HD and RGB formats.

Video Decoder

The video decoder of TW8816 consists of synchronization, Y/C separation, color decoding and component processing circuits. The sync processor contains digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in non-standard signals such as those from VCR playback. It also provides exceptional weak signal performance.

Y/C separation

The Y/C separation block provides the luma / chroma separation for the composite video. For NTSC and PAL standard signals, this is achieved through high quality 5-line adaptive comb filter. For SECAM standard signals, adaptive notch/band-pass filter is employed. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen. If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Color demodulation

The color demodulation for NTSC and PAL standard is done by quadrature mixing the chroma signal to the base band. The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily. For the PAL system, the PAL ID is identified to aid the PAL color demodulation. The SECAM demodulation process is done through FM demodulation and de-emphasis filter. The chroma carrier frequency is identified and used to control the SECAM color demodulation.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC control is –6db to +24db. For low color amplitude signals, black and white video, or very noisy signals, the color output will be “killed”. The threshold has programmed hysteresis to prevent oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

Automatic standard detection

The TW8816 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW8816 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by the TW8816

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.58 MHz	Japan
PAL-B, G	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	3.58 MHz	Brazil
PAL-CN	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43 MHz	China
NTSC (4.43)	525	60	4.43 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

The TW8816 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW8816 also provides a sharpness control function through control registers. It provides the control in 16 steps up to +12db. The center frequency of the enhancement curve is selectable by software control. It also provides a high frequency coring function to minimize the amplification of high frequency noise. To further enhance the image, a programmable vertical peaking function is provided for up to +6db of enhancement.

The TW8816 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any hue distortion.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Digital Input Support

In addition to analog inputs, the TW8816 has a 24-bit digital input for YCbCr or RGB data. External ADCs can be used to make the conversion from analog component inputs to digital YCbCr or RGB to support of DTV 480p, 720p, and 1080i, or PC VGA inputs from QVGA to WXGA. The input includes VSYNC, HSYNC, pixel clock and the optional data qualifier. For interlaced video, the timing relationship between VSYNC and HSYNC determine the field flag. The optional data qualifier is needed when input video data is not continuously valid within a line.

TFT Panel Support

The TW8816 supports varieties of Digital active matrix TFT panels with one pixel per clock mode. It supports panel with resolution up to WXGA resolution.

The TW8816 supports varieties of Analog active matrix TFT panels with one pixel per clock mode. It supports panel with source driver frequency up to 40MHz.

Dithering

If the color depth of the input data is larger than the LCD panel color depth, the TW8816 can be set to dither the image. Up to four bits of apparent color depth can be added with the internal dithering ability of the TW8816. This allows LCD panels with 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel to can display up to 2.1 million colors.

The TW8816 uses both spatial and frame modulation dithering. When dithering with the least significant 4-bits of input data the TW8816 uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, the TW8816 uses both spatial modulation with 2x2 pixel blocks, and frame modulation.

Image Control

Input Image Control

The input cropping control provides a way for programming the active display window region for the selected input video or graphic. In the normal operation, the first active line starts with the VSYNC signal. This and vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in one pixel increments for single pixel input mode or two pixels increments for double pixels input mode. If data qualifier is used, then only qualified pixels will be counted in the window size.

Image Scaling

The TW8816 internal image-scaling engine operates in several modes. The first is the bypass mode. No image scaling is done in this mode. The number of active output lines per frame and the number of active output pixels per line are identical to the input active lines and pixels, respectively. This mode is best used for displaying computer graphic at panel's native resolution.

By default, the input active window is zoomed up to the full screen for display. This is used for non-interlaced data like PC graphics or progressive scan video. The vertical and horizontal magnification ratio can be adjusted independently. Since the TW8816 has no frame buffer, the zoom ratio and output clock rate should be coordinated appropriately to avoid internal buffer over-run.

The TW8816 has a de-interlacing mode to process interlaced video inputs. In this mode, every input field is zoomed to the full output frame resolution. A proprietary low angle compensation circuitry adaptively corrects the interpolation process to result in smooth video rendering. The de-interlaced fields can also be properly compensated to have fields aligned correctly to avoid any artifacts. The offset can be programmed to provide maximum flexibility.

The horizontal scaler can be programmed to perform panoramic or water-glass scaling for displaying 4:3 input on a 16:9 display.

Image Enhancement Processing

Adaptive Black/White Stretch
This feature is to expand dynamic range of the input image, which creates more vivid image impression.

Favorite Color enhancement
This feature allows enhancement of color that is not primary color. Up to three user programmable colors can be selected for enhancement. The gain for each color selected is adjustable for maximum flexibility. It yields rich and colorful video images.

Display Timing

The TW8816 is operated in Frame Sync mode only with no external memory required. In this mode, the output frame rate is synchronized with the input frame rate. Since there is no frame buffer, the display clock frequency and zoom ratio have to be properly selected to match the panel resolution. The internal scaling engine absorbs the difference between the input line rate and output line rate as well as the difference between the input pixel rate and output pixel rate.

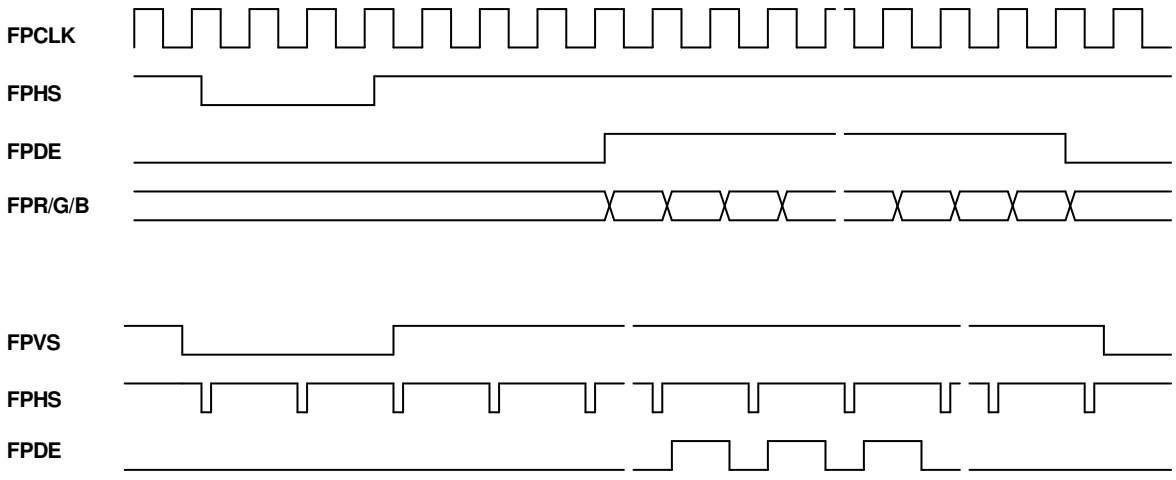


Figure 3 Flat Panel Output Signals

The frequency of the Flat Panel Clock Output pin can be controlled by an internal Spread Spectrum PLL or by an external oscillator connected to the PLLCKI pin. When the internal frequency multiplier is being used, the frequency of the Flat Panel Clock Output signal is determined by FPLL value and the post divider.

$$\text{Frequency FPCLK} = \frac{108\text{MHz} \times \text{FPLL}}{2^{17} \times 2^{\text{POST}}}$$

Color Space Conversion

The TW8816 has built-in YCbCr to RGB color space converter for the internal decoder output and the digital YCbCr input. The internal circuit will clamp the Y data value to the range of 16 to 235 for an 8-bit input. It also clamps the CbCr data value to the range of 16 to 240 in compliance with the CCIR601 standard.

On Screen Display

The TW8816 supports built-in OSD controller with integrated character ROM and programmable RAM font. The OSD display is independent of the input active window setting or the scaling ratio.

The on-chip OSD controller is a character-based controller. The pre-defined character or graphic bit map is stored in the internal ROM. There are a total of 202 built-in fonts. Each character is 12 pixels wide by 18 pixels high. The characters can be displayed on the screen in four user defined window locations of any size from 1 to 256 characters. The spaces between characters are also programmable. There is a limit of 256 characters that may be displayed on screen at one time in all windows combined. The attributes of each window can also be set to give it a shadow effect or 3-D effect. In addition, the characters can be expanded by a factor of 2,3 or 4 in vertical or horizontal directions and have the italic effect, under line effect on a character by character basis.

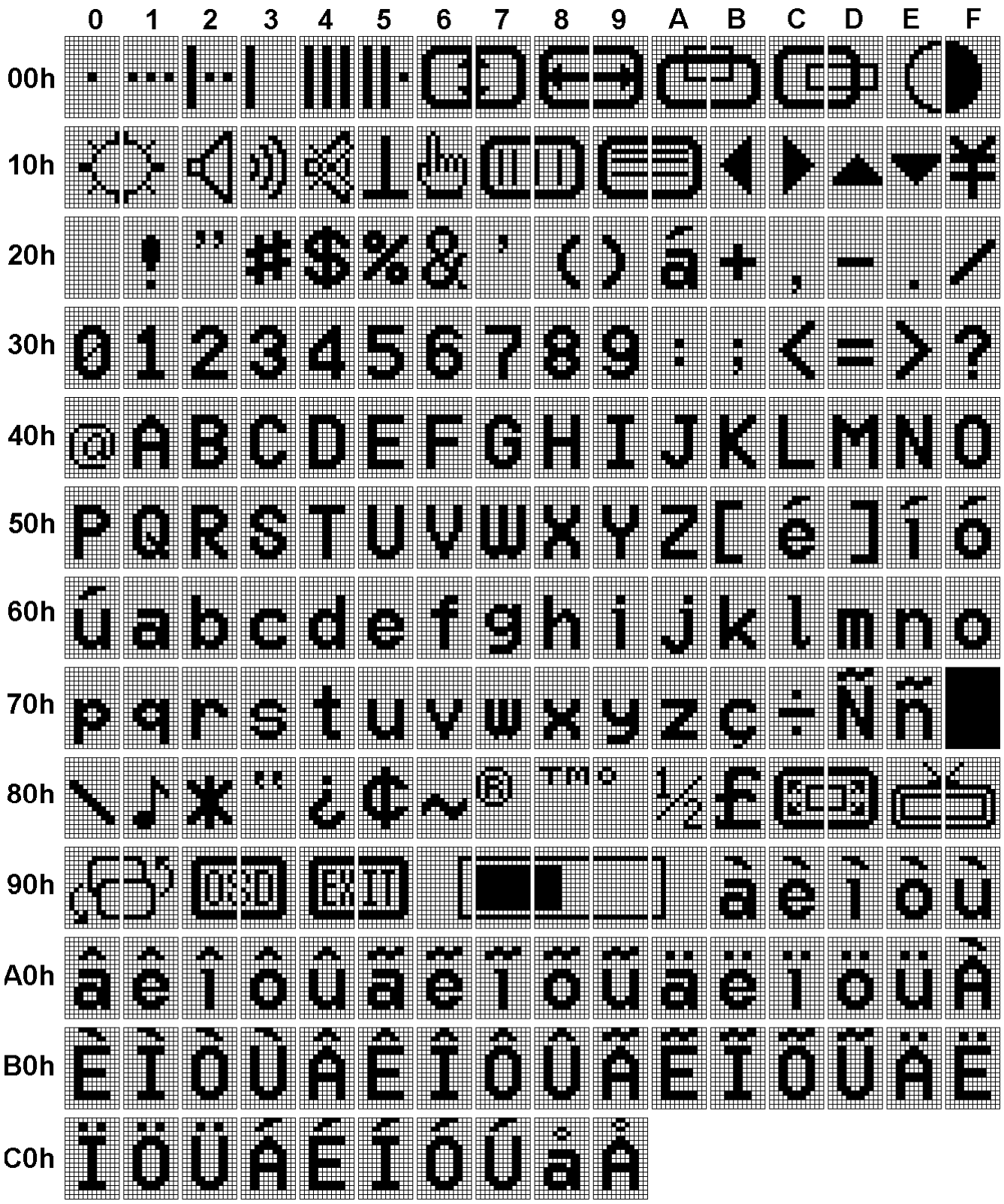


Figure 4 Font ROM Characters and Addresses

On chip OSD functions

% Font ROM : 202 Characters
- Capitalized English Alphabet, Numbers, Monitor Common Control Image, Special Alphabet Characters

% Font SRAM : Max 227 User Programmable Single Color Font or
Max 75 User Programmable Multi-Color Font Supports (6144x8 SRAM)
Single Color / Multi-Color Fonts Combine Number : defined by user.
(Multi-Color start address can change.)

% Character Register SRAM : 256 Location (8-bit Font Address + 11-bit Character Attribute, 256x20 SRAM)

% Characters
Character Color : 16 colors
Character Background Color : 16 colors
Character Blinking : Enable/Disable, 1 Hz Blinking frequency
Character Italic Effect : Enable/Disable
Character Under Line Effect : Enable/Disable
Character Space : Both H and V programmable by number of pixels
Quick Character Change in Window : Programmable Start Address and Buffer Size
Programmable OSD Color Palette Support
Re-designed OSD Font Supporting Standard Alpha-Numerical Character Set

% Windows
Number of Windows : 4 Independent Windows
Window Color : 16 colors
Window Zoom : 2, 3, 4 times zoom by dot number, H/V separate zooming control
Window Position : Programmable
H Direction : 1-pixel per step, V Direction : 1-Line per step
Window Size : Both H and V programmable by number of characters
Window Bordering/Shadowing Effect : 4 Independent Windows Enable/Disable Control
Window Alpha Blending Control : 4 Independent Windows Control
→ 16 Different Color for Alpha Blending support(4-bit control)
Window 3-D Effect : 4 Independent Windows Enable/Disable Control
Window Border Color : 16 Colors
Window Border Width : programmable

TW8816 Basic register setting flow for Built-in OSD controller

Step_1: OSD_WINDOW_CONFIGURATION setting

1. OSD Window Select	0x09E, bit1-0
2. OSD Window Disable	0x09F, bit0
3. OSD Window Zoom multiplier	0x0A9, bit7-6: V, bit5-4:H
4. OSD Window Background B Color	0x09F, bit6-4
5. OSD Window Background G Color	0x09F, bit6-4
6. OSD Window Background R Color	0x09F, bit6-4
7. OSD Window Background Color Extension	0x09F, bit7
8. OSD Window 3-D Effect Top/Bottom Mode Select	0x09F, bit3
9. OSD Window 3-D Effect Level Select	0x09F, bit1
10. OSD Window 3-D Effect Enable/Disable	0x09F, bit2
11. OSD Window H-Start Location (see details in next page)	0x0A1, bit0-7 0x0A0, bit2-0
12. OSD Window V-Start Location (see details in next page)	0x0A2, bit0-7 0x0A0, bit5-4
13. OSD Window Width	0x0A3, bit0-5
14. OSD Window Height	0x0A4, bit0-5
15. OSD Window Border_Line Width	0x0A5, bit0-3
16. OSD Window Border_Line B color	0x0A5, bit4-6
17. OSD Window Border_Line G color	0x0A5, bit4-6
18. OSD Window Border_Line R color	0x0A5, bit4-6
19. OSD Window Border_Line Enable	0x0A5, bit7
20. OSD Window Border Color Extension	0x0A6, bit7
21. OSD Window Shadow Width	0x0AB, bit0-3
22. OSD Window Shadow B color	0x0AB, bit4-6
23. OSD Window Shadow G color	0x0AB, bit4-6
24. OSD Window Shadow R color	0x0AB, bit4-6
25. OSD Window Shadow Enable	0x0AB, bit7
26. OSD Window Shadow Color Extension	0x0AD, bit7
27. OSD Window H-Space Width (Between Border_line and Characters)	0x0A6, bit0-6
28. OSD Window V-Space Width (Between Border_line and Characters)	0x0A7, bit0-6
29. Character H-Space Width (Between Character and Character)	0x0A8, bit0-3 0x0AE, bit2
30. Character V-Space Width (Between Character and Character)	0x0A8, bit4-7 0x0AE, bit3
31. OSD Window Alpha Blending Color Select	0x09E, bit4-7
32. OSD Window Alpha Blending Value Control	0x0AC, bit0-3
33. Window content start address	0x096
34. Repeat 1 – 32	

Step_2: OSD_COLOR_ATTRIBUTE / FONT setting (OSD RAM)

1. Enable OSD RAM Access - 0x094 (bit0 = 0)
2. OSD RAM Address - 0x095, 0x096
   - The first address is Step_1_33 Window content start address.
3. OSD RAM Data Port High (Font Address)
   - 0x097 Data is written to above address automatically.
   - 0x094_[7] = 0 or 0x097=8'hff : FONT_ROM h00 to hC9 (202 characters)
   - 0x094_[7] = 1 or 0x097=8'hfe : FONT_RAM h00 to hE2 (Max 227 characters)

4. OSD RAM Data Port Bit17(Italic Effect), Bit18(Under Line Effect)
   - 0x094 Bit6, Bit5, Bit4 Data is written to above address automatically.
5. OSD RAM Data Port Low (Color Attribute)
   - 0x098 Data is written to above address automatically.
6.Repeat 2), 3), 4), 5)
- The address should be increased by one each.

Step_3: COLOR LOOK-UP TABLE setting

1. Select Color Look-Up Table Write Address - 0x09C (bit[3:0])
- BIT[3:0] : These 4 bits specify one of the 16 entries in the look-up table. Each entry is indexed to a different color by its content.
- There are 256 colors available; but only sixteen of them are accessible by OSD controller at a given time.

BIT[3:0]	Default Value
0000	00h (000,000,00)
0001	03h (000,000,11)
0010	1Ch (000,111,00)
0011	1Fh (000,111,11)
0100	E0h (111,000,00)
0101	E3h (111,000,11)
0110	FCh (111,111,00)
0111	FFh (111,111,11)
1000	49h (010,010,01)
1001	02h (000,000,10)
1010	10h (000,100,00)
1011	12h (000,100,10)
1100	80h (100,000,00)
1101	82h (100,000,10)
1110	90h (100,100,00)
1111	92h (100,100,10)

2. Color Look-Up Table control bits setting - 0x09D
- The data of the Look-Up Table is accessed through 0x09D.
- An index 0x09D register write strobes the data into the corresponding entry pointed by 0x09C[3:0].
- Control BIT[7:5] → These bits assigned for R color(select one of 8 R color intensities).
- Control BIT[4:2] → These bits assigned for G color(select one of 8 G color intensities).
- Control BIT[1:0] → These bits assigned for B color(select one of 4 B color intensities).

R Color Table → BIT[7:5]	Table Setting Value	G Color Table → BIT[4:2]	Table Setting Value	B Color Table → BIT[1:0]	Table Setting Value
000	8'd0	000	8'd0	00	8'd0
001	8'd32	001	8'd32	01	8'd64
010	8'd64	010	8'd64	10	8'd128
011	8'd96	011	8'd96	11	8'd255
100	8'd128	100	8'd128		
101	8'd160	101	8'd160		
110	8'd192	110	8'd192		
111	8'd255	111	8'd255		

3. Repeat 1),2) to program each entry of the Look-Up Table.

Step_4: FONT_RAM_DATA setting (FONT RAM)

1. Enable FONT RAM Access - 0x094 (bit0 = 1)
2. Programmable SRAM Address Start Position Setting for Multi-Color Font.
   - 0x09B
3. FONT RAM Address Setting - 8 bits(h00 – hE2) - 0x099
   - h00~hE2 : Single Font RAM(227 Programmable Characters)
   - h00~hE2 : Multi-Color Font RAM(75 Programmable Characters)
     ex) 0x09B == h32 Setting Case
     → h00 ~ h31 : Single Font RAM(50 Programmable Characters)
     → h32 ~ hE2 : Multi-Color Font RAM(59 Programmable Characters)
     h32(R-color), h33(G-color), h34(B-color) are one set for 1 multi-color font.
4. FONT RAM Data Port
   - 0x09A Data is written to above address automatically.
5. Repeat (4) at 27 times for one FONT RAM Data
   - the internal address automatically increases by one each.
6. New FONT RAM Address Setting – 8 bits
7. Repeat 3),4),5)
   - The FONT RAM Address should be increased by one each.

Note) As for the FONT RAM configuration and font bit mapping, see the detailed description

Step_5: End of OSD setting and Enable OSD

1. Disable OSD RAM / FONT RAM Access - 0x094 (bit0 = 0)
2. OSD Window Enable - 0x09E bit[1:0] window select
   → 000: Window1, 001: Window2, 010: Window3, 011: Window4
   - bit0 = 1 of 0x09F

OSD Window Start Location : Built-in OSD controller

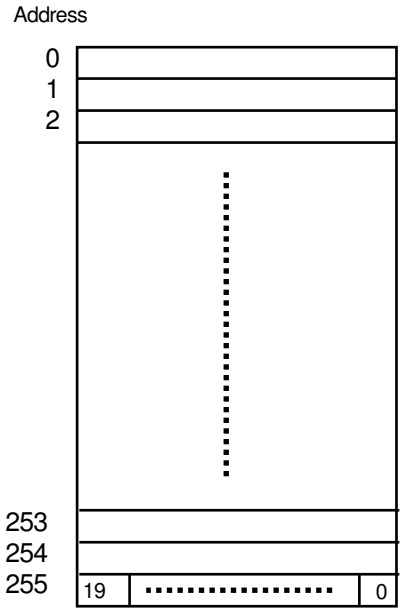
OSD window H_start location (N): 0x09E bit[1:0] window select, 0x0A2,0A0 increment by 1 at a time
N = 0, 1, 2, 3… Pixel 1 when N = 0,1

N	OSD_Window Start_Pixel
1	pixel 1 (begin with pixel 1)
2	pixel 2
3	pixel 3
N	pixel N

OSD window V_start location (M) : 0x09E bit[1:0] window select, 0x0A2,0A1 increment by 1 at a time
M = 0, 1, 2, 3.... Line 1 when M = 0,1

M	OSD_Window Start_Line
1	line 1 (begin with line 1)
2	line 2
3	line 3
M	line M

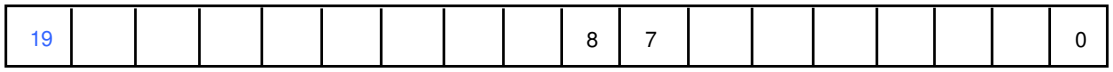
OSD_RAM Configuration



The characters can be displayed on the screen in four user defined window locations of any size from 1 to 256 characters. There is a limit of 256 characters that may be displayed on screen at one time in all windows combined.

Example

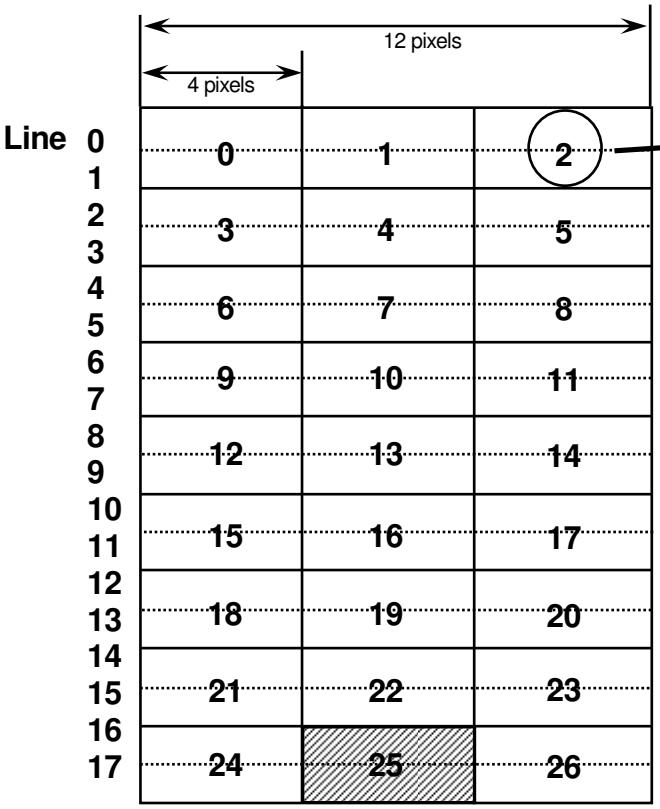
Window #1: Address 0 – 2 (3 characters)
Window #2: Address 3 – 100 (98 characters)
Window #3: Address 101– 254 (154 characters)
Window #4: Address 255 (1 character)

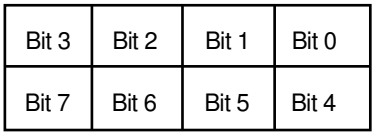


FONT_ADDRESS (12-bits)
Bit 19: Reserved
Bit 18: Under Line Effect ON
Bit 17: Italic Effect ON
Bit 16: FONT_RAM ON
Bit 15 - 8: FONT Address

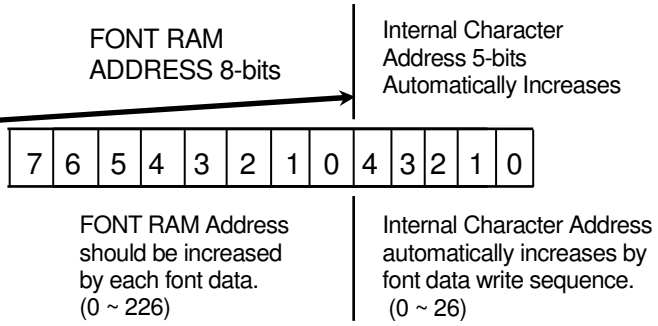
ATTRIBUTE (8-bits)
Bit 7: Character's Color Extension
Bit 6: Character's background R
Bit 5: Character's background G
Bit 4: Character's background B
Bit 3: Blink ON
Bit 2: Character R
Bit 1: Character G
Bit 0: Character B

FONT BIT MAP 12 x 18 dots = 1 character

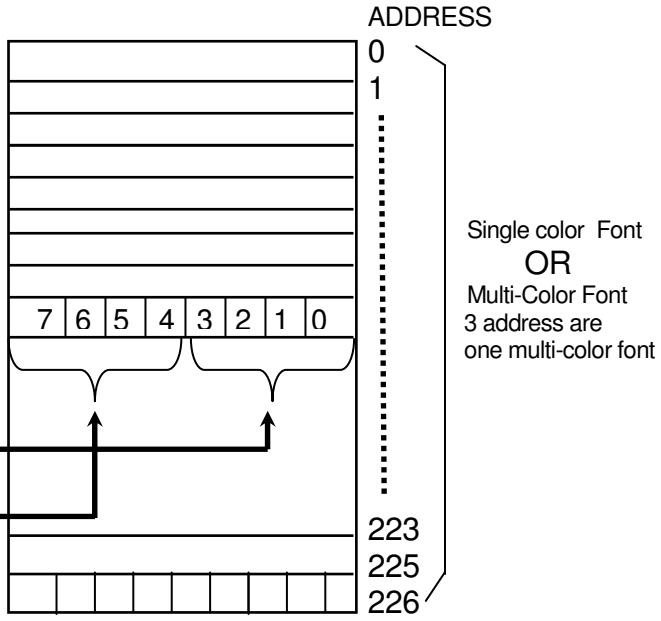




FONT RAM ADDRESS 7-bits



FONT RAM (6144 x 8 bits)



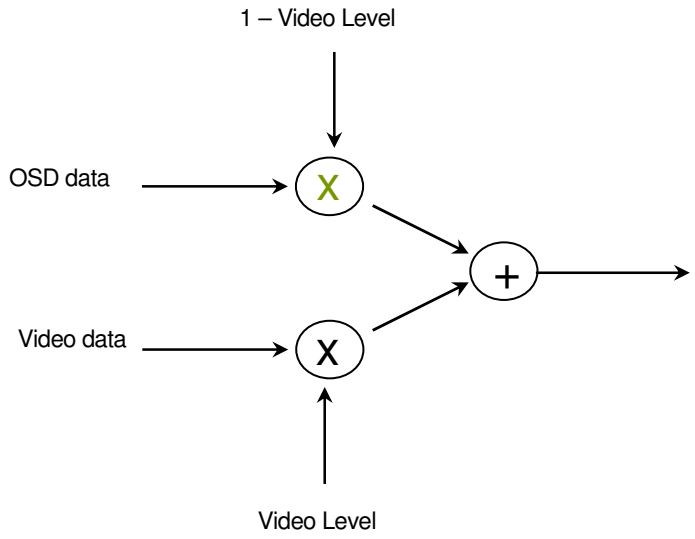
TW8816 Alpha Blending for OSD Window

The TW8816 uses "Alpha Blending" in OSD 4 separation windows & 16 separation colors. Alpha blending mixes (adds) the video signal and OSD signal at the following specified levels. In other words, alpha blending determines the transparency of the OSD window each color to in relation to video signal. When alpha blending is disabled, only OSD data is displayed in OSD window.
The alpha blending level selection are 4-bit assigned, it can support 8 different level control.

The alpha blending level bits and alpha blending color selection bits are in register 0x09E, 0x0AC for each windows(Window Control by register 0X9E bit[1:0]).

alpha[3:0]	Video Level
0000	0.00 %
0001	12.5
0010	25.0
0011	37.5
0100	50.0
0101	62.5
0110	75.0
0111	87.5
1000	100

Alpha Blending Concept :



Microcontroller Interface

The TW8816 registers are accessed via 2-wire serial bus interface. It operates as a slave device. Serial clock and data lines transfer data from the bus master at a rate up to 400 Kb/s.

Built-in Microcontroller

TW8816 has built-in microcontroller which supports several interface.

- Support external SPI Interface.
- Support I2C Master interface with GPIO { Port 1.0 SCL, Port 1.1 SDA}.
- Support 2 LED signal interface with GPIO { Port 1.6 LED0, Port 1.7 LED1}.
- Support extra 8 MCU GPIO { Port 2.0 GP0 ~ Port 2.7 GP7}.
- Support UART interface with GPIO { Port 3.0 RXD, Port 3.1 TXD}.
- Support IR or interrupt with GPIO { Port3.2 IR}.

Power Management

The TW8816 supports panel power sequencing. Typical TFT panels require different parts of the panel power to be applied in the right sequence to avoid premature damage to the panel. Pins are provided to control the panel backlight generator, digital circuitry and panel driver, separately. The TW8816 controls the power up and power down sequence for the LCD panels. The time lapses between different stages of the sequence are independently programmable to meet various power sequencing requirements.

The TW8816 also supports VESA™ DPMS for monitor power management. It can detect the DPMS status from input sync signals and automatically change into On/Off mode. To support the power management, the TW8816 has three operating modes: Power On mode, Power Off mode, and Panel Off mode. All the DPMS power saving mode will be covered by the Power Off mode.

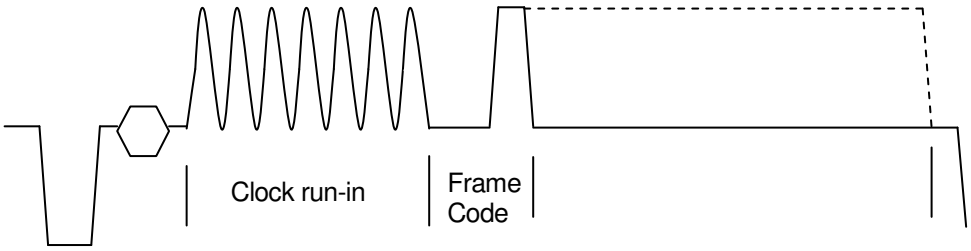


Figure 5 Typical CC/EDS scan line waveform

Closed Captioning and Extended Data Services

Closed Caption (CC) vertical blanking interval scan lines are on the odd field NTSC line 21. Extended Data Services (EDS) scan lines are on the even field NTSC line. A Closed Caption (CC) scan line on an NTSC-based system is made of 25 bit periods at a 0.503MHz rate. The data is an analog signal beginning with a packet header. It contains a Clock Synchronization Code consisting of 14 bits of double-frequency run-in clock at 1.006 MHz, a 2-bit framing code. The data of 16 bits/2 bytes follows the packet header. Each of these 2 bytes is a 7 bit + odd parity ASCII character which represents text or control characters for positioning or display control. For the purposes of CC or EDS, only the Y component of the video signal is used. Therefore, the input composite video has to go through the Y/C separation to extract Y component for further decoding. The TW8816 can be programmed to decode CC or EDS data by setting register 0x1B. Since the CC and EDS are independent, there could be one or both in a particular frame. A typical waveform is shown in Figure 5.

In the CC/EDS decode mode, the decoder monitors the appropriate scan lines looking for the clock run-in and start bits pattern. It found, it locks to the clock run-in, the caption data is sampled and loaded into shift registers, and the data is then transferred to the caption data FIFO. The TW8816 provides a 16 x 10 location FIFO for storing CC/EDS data. Once the video decoder detects the start signal in the CC/EDS signal, it captures the low byte of CC/EDS data first and checks to see if the FIFO is full. If the FIFO is not full, then the data is stored in the FIFO, and is available to the user through the CC_DATA register (0x1A). The high byte of CC/EDS data is captured next and placed in the FIFO. Upon being placed in the 10-bit FIFO, two additional bits are attached to the CC/EDS data byte by TW8816's CC/EDS decoder. These two bits indicate whether the given byte stored in the FIFO corresponds to CC or EDS data and whether it is the high or low byte of CC/EDS. These two bits are available to the user through the CC_STATUS register bits CC_EDS and LO_HI, respectively. As stored in the FIFO, LO_HI is bit 8 and CC_EDS is bit 9. Additionally, the TW8816 stores the results of the parity check in the PARITY_ERR bit in the CC_STATUS register.

The 16-location FIFO can hold eight lines worth of CC/EDS data, at two bytes per line. Initially when the FIFO is empty, bit Empty in the CC_STATUS register (0x1A) is set low and indicates that no data is available in the FIFO. Subsequently, when data has been stored in the FIFO, the Empty bit is set to logical high. Once the FIFO is half full, the CC_VALID interrupt pin signals to the system that the FIFO contents should be read in the near future. The CCVALID bit is enabled via a bit in the CC_STATUS register (0x1A). The system controller can then poll the CCVALID bit in the STATUS register (0x00) to ensure that it was the TW8816 that initiated the CCVALID interrupt.

When the first byte of CC/EDS data is decoded and stored in the FIFO, the data is immediately placed in the CC_DATA and CC_STATUS registers and is available to be read. Once the data is read from the CC_DATA register, the information in the next location of the FIFO is placed in the CC_DATA and CC_STATUS registers. If the controller in the system ignores TW8816's CCVALID bit for a sufficiently long period of time, then the CC/EDS FIFO will become full and the TW8816 will not be able to write additional data to the FIFO. Any incoming bytes of data will be lost and an overflow condition will occur; bit Overflow in the CC_STATUS register will be set to a logical one. The system may clear the overflow condition by reading the CC/EDS data and creating space in the FIFO for new information. As a result, the overflow bit is reset to a logical zero.

There will routinely be asynchronous reads and writes to the CC/EDS FIFO. The writes will be from the CC/EDS circuitry and the reads will occur as the system controller reads the CC/EDS data from TW8816. These reads and writes will sometimes occur simultaneously, and the TW8816 is designed to give priority to the read operations. In the case where the CC_DATA register data is specifically being read to clear an overflow condition, the simultaneous occurrence of a read and a write will not cause the overflow bit to be reset, even though the read has priority. An additional read must be made to the CC_DATA register in order to clear the overflow condition. As always, the write data will be lost while the FIFO is in overflow condition.

Two Wire Serial Bus Interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW8816 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For

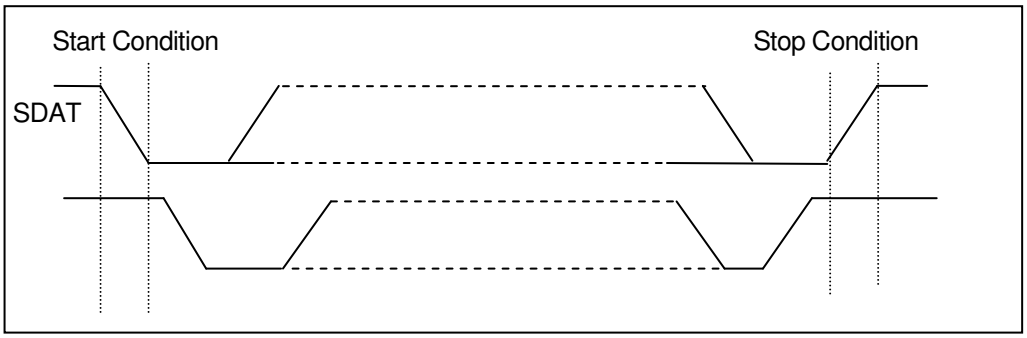


Figure 6 Definition of two-wire serial bus interface bus start and stop

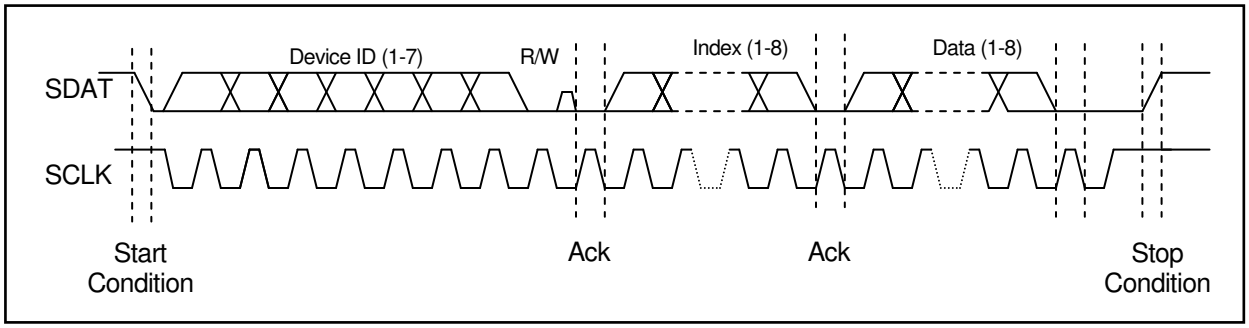


Figure 7 One complete serial bus interface register write sequence

both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW8816 is operated as a bus slave device. The most significant 7-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDAT from high to low, while SCLK is high, this is defined to be a start condition (See Figure 6.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 7. (For the TW8816, the next byte is normally the index to the TW8816 registers and is a write to the TW8816 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theTW8816, the master sends another 8-bits of data, the TW8816 loads this to the register pointed by the internal index register. The TW8816 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW8816 if they are in ascending sequential order. After each 8-bit transfer the TW8816 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW8816 the host will issue a stop condition.

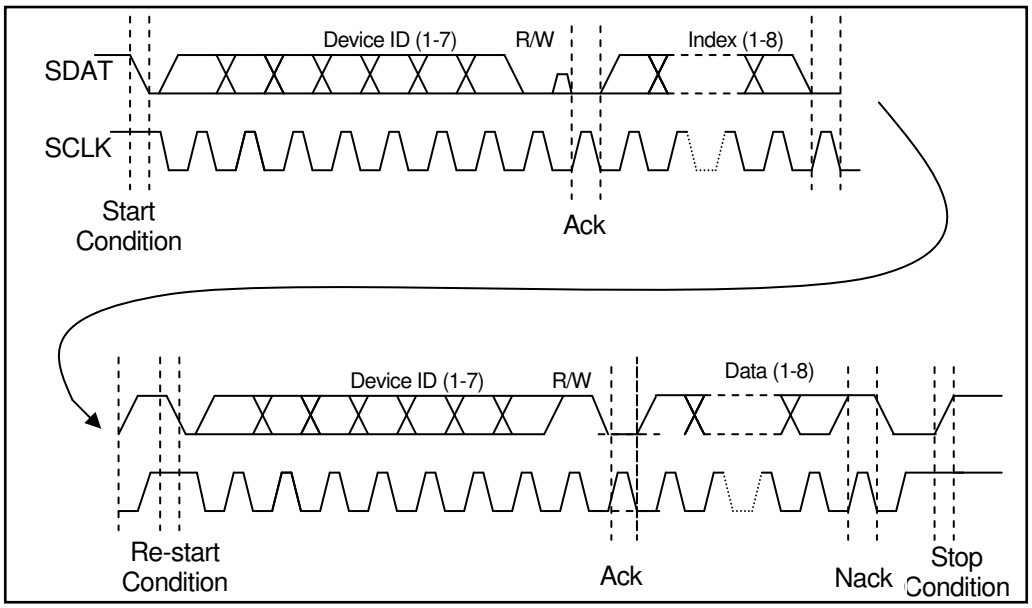


Figure 8 One complete serial bus interface register read sequence

Table 2 TW8816 serial bus interface 7-bit slave address and read write bit

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	1	1= Read 0=Write

A TW8816 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 8). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

The TW8816 contains more than 256 index registers. Since the index data for serial bus access is only eight bits wide, a page mechanism is used to access these registers. The bit 0 of index 0xFF is used to select either the first page of 255 registers or the second page of 255 registers. In the register map, the index consists of 9 bits. The MSB denotes the content of bit 0 of index 0xFF, and the rest 8 bits correspond to the serial bus index data. Hence 0x000 denotes the index 0 of page 0, while 0x100 denotes the index 0 of page 1. Index 0xFF is shared between page 0 and page 1.

Test Modes

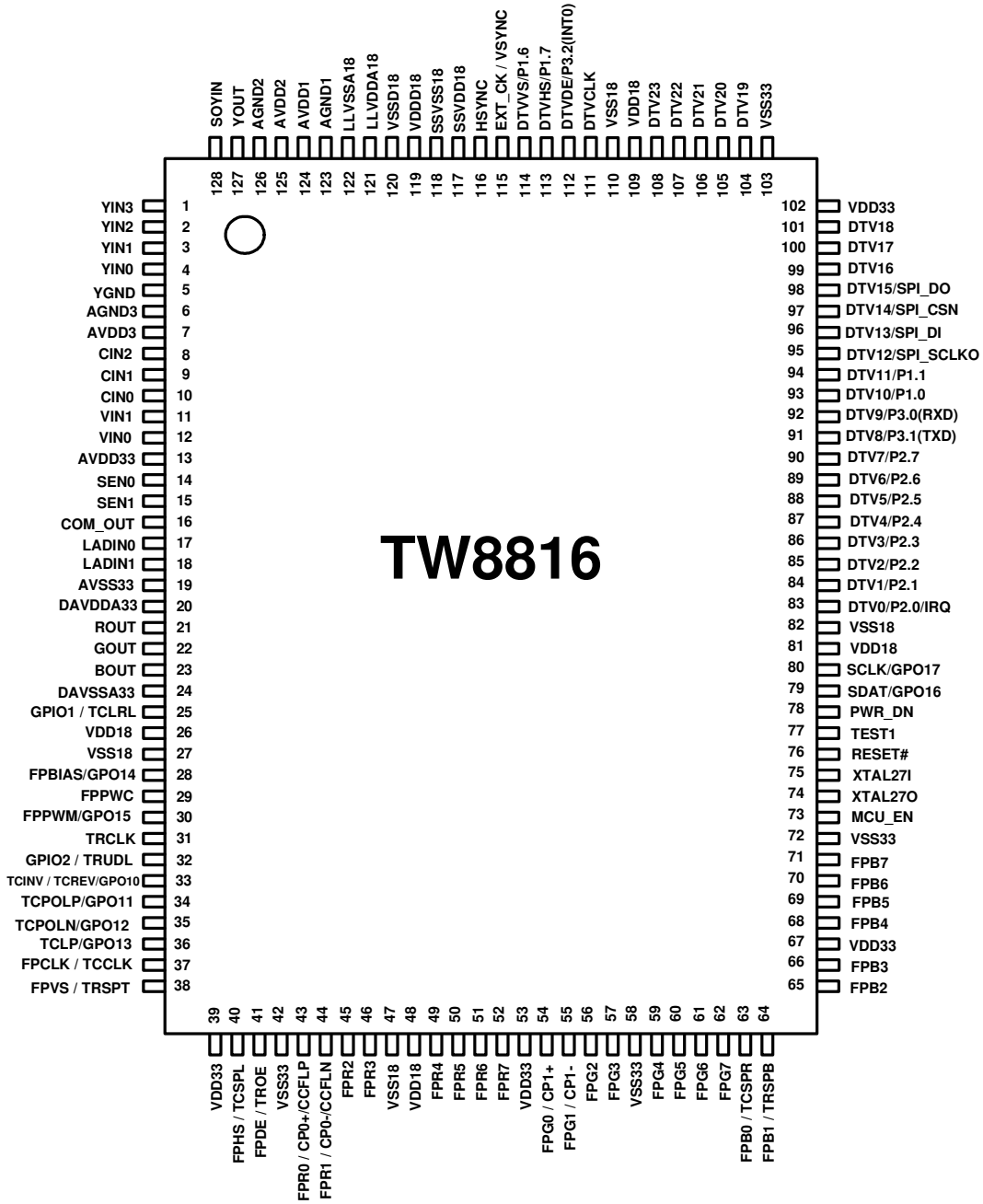
The TEST1 input pin provides test mode selection. If this pin is low at the rising edge of the RESET# pin and remains low, the TW8816 is in its normal operating mode. Table 3 shows the other test modes made available with this pin.

Table 3 Test modes

Test mode	TEST1 Before RESET# rising edge	TEST1 After RESET# rising edge	Description
Normal	0	0	Normal operation
Output tri-state	0	1	In this mode, all pin output drivers are tri-stated. Pin leakage current parameters can be measured.
Outputs high	1	0	In this mode, all pin output drivers are forced to the high output state. V_{OH} and I_{OH} can be measured.
Outputs low	1	1	In this mode, all pin output drivers are forced to the low output state. V_{OL} and I_{OL} can be measured.

TW8816 Package Pin Diagram

TW8816 128 pins LQFP



TW8816 144 pins TFBGA (Top-View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	AVDD2	AVDD1	LLVDDA18	VDDD18	VDDD18	SSVDD18	SSVDD18	VDD18	VDD33	DTV15 / SPI_DO	DTV13 / SPI_DI	DTV12 / SPI_SCLKO
B	AVDD3	CIN2	YIN1	YIN3	SOYIN	DTVVS / P1.6	DTVCLK	DTV21	DTV18	DTV16	DTV14 / SPI_CSN	DTV11 / P1.1
C	CIN1	CIN0	YIN0	YIN2	YOUT	EXT_CK / VSYNC	DTVDE / P3.2 (INT0)	DTV22	DTV19	DTV17	DTV10 / P1.0	DTV9 / P3.0(RXD)
D	VIN1	VIN0	YGND	AGND2	LLVSSA18	HSYNC	DTVHS / P1.7	DTV23	DTV20	DTV8 / P3.1(TXD)	DTV7 / P2.7	DTV6 / P2.6
E	AVDD33	SEN0	SEN1	AGND3	AGND1	SSVSS18	SSVSS18	VSS18	VSS33	DTV5 / P2.5	DTV4 / P2,4	DTV3 / P2.3
F	AVDD33	ROUT	COM_OUT	AVSS33	AVSS33	VSSD18	VSSD18	VSS18	DTV2	DTV1 / P2.1	DTV0 / P2.0	VDD18
G	DAVDDA33	GOUT	LADIN1	LADIN0	DAVSSA33	DAVSSA33	VSS18	VSS33	SDA / GPO16	SCLK / GPO17	PWR_DN	XTAL27I
H	DAVDDA33	BOUT	FPBIAS / GPO14	GPIO1/ TCLRL	VSS18	VSS18	VSS33	VSS33	TEST1	RESET#	MCU_EN	XTAL27O
J	VDD18	TRCLK	FPPWC	GPIO2 / TRUDL	VSS33	VSS33	VSS33	FPG2	FPG5	FPB7	FPB6	VDD33
K	TCPOLP/ GPO11	TCINV / TCREV / GPO10	FPPWM / GPO15	FPR0 / CP0+ / CCFLN	FPR3	FPR5	FPR7	FPG1 / CP1-	FPG4	FPB5	FPB4	VDD33
L	TCPOLN / GPO12	TRSPT	FPHS / TCSPL	FPDE / TROE	FPR2	FPR4	FPR6	FPG0 / CP1+	FPG3	FPG7	FPB1 / TRSPB	FPB3
M	TCLP / GPO13	FPCLK / TCCLK	VDD33	VDD33	FPR1 / CP0- / CCFLN	VDD18	VDD18	VDD33	VDD33	FPG6	FPB0 / TCSPR	FPB2

Pin Description

This section provides a detailed description of each pin for the TW8816. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

The pin description also includes the buffer direction and type used for that pin.

PIN #		I/O	Name	Description	Recommended Connection of Unused Pins
LQFP	TFBGA				
Analog I/F signals **ADC I/F signals and PLL Power**					
1	B4	AI	YIN3	Analog composite or luma input 3	Connect to Analog Ground
2	C4	AI	YIN2	Analog composite or luma input 2	Connect to Analog Ground
3	B3	AI	YIN1	Analog composite or luma input 1	Connect to Analog Ground
4	C3	AI	YIN0	Analog composite or luma input 0	Connect to Analog Ground
5	D3	P	YGND	Y input ground	
6	E4	P	AGND3	Analog ground	
7	B1	P	AVDD3	Analog VDD +1.8V	
8	B2	AI	CIN2	Analog component C input 2	Connect to Analog Ground
9	C1	AI	CIN1	Analog component C input 1	Connect to Analog Ground
10	C2	AI	CIN0	Analog component C input 0	Connect to Analog Ground
11	D1	AI	VIN1	Analog component V input 1	Connect to Analog Ground
12	D2	AI	VIN0	Analog component V input 0	Connect to Analog Ground
117	A7, A6	P	SSVDD18	Analog SS-PLL VDD +1.8V	
118	E7, E6	P	SSVSS18	Analog SS-PLL Ground	
119	A5, A4	P	VDDD18	Analog VDD + 1.8V	
120	F7, F6	P	VSSD18	Analog Ground	
121	A3	P	LLVDDA18	Analog LL-PLL VDD +1.8V	
122	D5	P	LLVSSA18	Analog LL-PLL Ground	
123	E5	P	AGND1	Analog Ground	
124	A2	P	AVDD1	Analog VDD +1.8V	
125	A1	P	AVDD2	Analog VDD +1.8V	
126	D4	P	AGND2	Analog Ground	
127	C5	AO	YOUT	Y output (Y out or Y + C out)	Open / Unconnected
128	B5	AI	SOYIN	Sync On Y(or Green) input	Connect to Analog Ground

DAC I/F signals					
20	G1,H1	P	DAVDDA33	DAC Analog +3.3V	
21	F2	AO	ROUT	DAC Analog Red data output	Open/ Unconnected
22	G2	AO	GOUT	DAC Analog Green data output	
23	H2	AO	BOUT	DAC Analog Blue data output	
24	G5,G6	P	DAVSSA33	DAC Analog ground	
Charge Pump, VCOM I/F and Low-speed ADC signals					
13	E1,F1	P	AVDD33	Analog Power 3.3V	
14	E2	AI	SEN0	Analog sensing 0 Input	Connect to Analog Ground
15	E3	AI	SEN1	Analog sensing 1 Input	
16	F3	AO	COM_OUT	Analog VCOM Output	Open/ Unconnected
17	G4	AI	LADIN0	Low speed ADC input 0	Connect to Analog Ground
18	G3	AI	LADIN1	Low speed ADC input 1	Connect to Analog Ground
19	F4,F5	P	AVSS33	Analog Ground	
*** Other charge pump output signals sharing digital panel data output.					
LCD Panel I/F signals					
43, 44, 45, 46, 49, 50, 51,52	K4,M5, L5,K5, L6,K6, L7, K7	O	FPR[0:7]	Red Flat Panel Output bits Pin 43 = CP0+ : Charge Pump 0 + CCFLP : CCFL Driver Polarity (Positive) Pin 44 = CP0- : Charge Pump 0 - CCFLN : CCFL Driver Polarity (Negative)	Open/ Unconnected
54, 55, 56, 57, 59, 60, 61, 62	L8, K8, J8, L9, K9, J9, M10, L10	O	FPG[0:7]	Green Flat Panel Outputs bits Pin 54 = CP1+ : Charge Pump 1 + Pin 55 = CP1- : Charge Pump 1 -	
63, 64, 65, 66, 68, 69, 70, 71	M11, L11, M12, L12, K11, K10, J11, J10	O	FPB[0:7]	Blue Flat Panel Output bits Pin 63 = TCSPR : TCON Column Driver Start Pulse (right to left scan) Pin 64 = TRSPB : Row Driver Starting Pulse (Bottom start)	
28	H3	O	FPBIAS / GPO14	Power on/off control for panel backlight bias General Purpose Output	
29	J3	O	FPPWC	Power on/off control for flat panel display	
30	K3	O	FPPWM / GPO15	PWM control for panel backlight General Purpose Output	
TCON I/F Signals **Column (Source) Driver signals**					
37	M2	O	TCCLK / FPCLK	TCON Column Driver Clock Flat Panel Clock Output	Open/ Unconnected
25	H4	O	TCLRL / GPIO1	Left Right selection (Left: high, Right: low) GPIO1	
40	L3	O	TCSPL / FPHS	TCON Column Driver Start Pulse (Left to right scan) Horizontal sync output for flat panel	
36	M1	O	TCLP / GPO13	Column Driver Load Pulse General Purpose Output	
34	K1	O	TCPOLP /	Column Driver Polarity (Positive)	

			GPO11	General Purpose Output	
35	L1	O	TCPOLN / GPO12	Column Driver Polarity (Negative) General Purpose Output	
33	K2	O	TCINV / TCREV / GPO10	TCON Column Driver Inversion TCON Column Driver Reverse General Purpose Output 10	
Row (Gate) Driver signals					
31	J2	O	TRCLK	Row Driver Shift Clock	Open/ Unconnected
32	J4	I/O	TRUDL / GPIO2	Up Down selection (Up : high, Down : low) GPIO2	
38	L2	O	TRSPT / FPVS	Row Driver Starting Pulse (Top Start) Vertical sync output for flat panel	
41	L4	O	TROE / FPDE	Row Driver Output Enable Data valid for flat panel	
DTV I/F Signals					
83 ~ 101, 104~ 108	F11, F10, F9, E12, E11, E10, D12, D11, D10, C12, C11, B12, A12, A11, B11, A10, B10, C10, B9, C9, D9, B8, C8, D9	I/O	DTVD[0:23]	Digital input Pin 83 = MCU Port 2.0 Pin 84 = MCU Port 2.1 Pin 85 = MCU Port 2.2 Pin 86 = MCU Port 2.3 Pin 87 = MCU Port 2.4 Pin 88 = MCU Port 2.5 Pin 89 = MCU Port 2.6 Pin 90 = MCU Port 2.7 Pin 91* = MCU Port 3.1(MCU TXD) Pin 92* = MCU Port 3.0 (MCU RXD) Pin 93* = MCU Port 1.0 Pin 94* = MCU Port 1.1 Pin 95 = SPI Clock Out Pin 96 = SPI Data In Pin 97 = SPI CS (Low enable) Pin 98 = SPI Data Out	Connect to VSS33. *When use internal MCU enable mode, pin 91, 92, 93, 94, 112, 113, and 114 are open drain.
111	B7	I	DTVCLK	Clock input for DTV interface	
112	C7	I/O	DTVDE/ P3.2(INT0)	Data valid for DTV interface MCU Port 3.2 (MCU Int 0) *	
113	D7	I/O	DTVHS / P1.7	Horizontal sync for DTV interface MCU Port 1.7 *	
114	B6	I/O	DTVVS / P1.6	Vertical sync for DTV interface MCU Port 1.6 *	
Other I/F Signals					
73	H11	I	MCU_EN	MCU Enable	Connect to VSS33
78	G11	I	PWR_DN	Power Down pin	Connect to VSS33
74	H12	O	XTAL27O	Crystal terminal (if crystal is used)	
75	G12	I	XTAL27I	Crystal terminal (if crystal is used) or oscillator input	
76	H10	I	RESET#	Reset pin	Connect to VSS33
77	H9	I	TEST1	Production test pin	Connect to VSS33

79	G9	I/O	SDAT / GPO16	2-wire microprocessor interface data pin General Purpose Output 16	
80	G10	I	SCLK / GPO17	2-wire microprocessor interface clock pin General Purpose Output 17	
115	C6	I	EXT_CK / VSYNC	External Clock Digital VSYNC Input	Connect to VSS33
116	D6	I	HSYNC	Digital HSYNC input	Connect to VSS33
Power					
39, 53, 67, 102	M3, M4, M8, M9, K12, J12, A9	P	VDD33	3.3V Digital I/O Power	
42, 58, 72, 103	J5, J6, H7, J7, H8, G8, E9	P	VSS33	3.3V Digital I/O Return	
26, 48, 81, 109	J1, M6, M7, F12, A8	P	VDD18	1.8V Digital core Power	
27, 47, 82, 110	H5, H6, G7, F8, E8	P	VSS18	1.8V Digital core Return	

Parametric Information

AC/DC Electrical Parameters

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD1, AVDD2, AVDD3, LLVDDA18, VDDD18, SSVDD18(measured to AGND1, AGND2, AGND3, LLVSSA18, VSSD18, SSVDD18)	V_{DDAM}	-	-	1.92	V
AVDD33, DAVDDA33, (measured to AVSS33, DAVSSA33)	V_{DDA33M}	-	-	3.6	V
VDD18 (measured to VSS18)	V_{DDM}	-	-	1.98	V
VDD33 (measured to VSS33)	V_{DDEM}	-	-	3.6	V
Voltage on any digital signal pin (See the note below)	-	VSS33 – 0.5	-	5.5	V
Analog Input Voltage (supplied by 1.8V)	-	AVSS – 0.5	-	1.92	V
Analog Input Voltage (supplied by 3.3V)	-	AVSS33 – 0.5	-	3.6	V
Storage Temperature	T_S	–65	-	+150	℃
Junction Temperature	T_J	-	-	+125	℃
Vapor Phase Soldering(15 Seconds)	T_{VSOL}	-	-	+220	℃

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 4 can induce destructive latch-up.

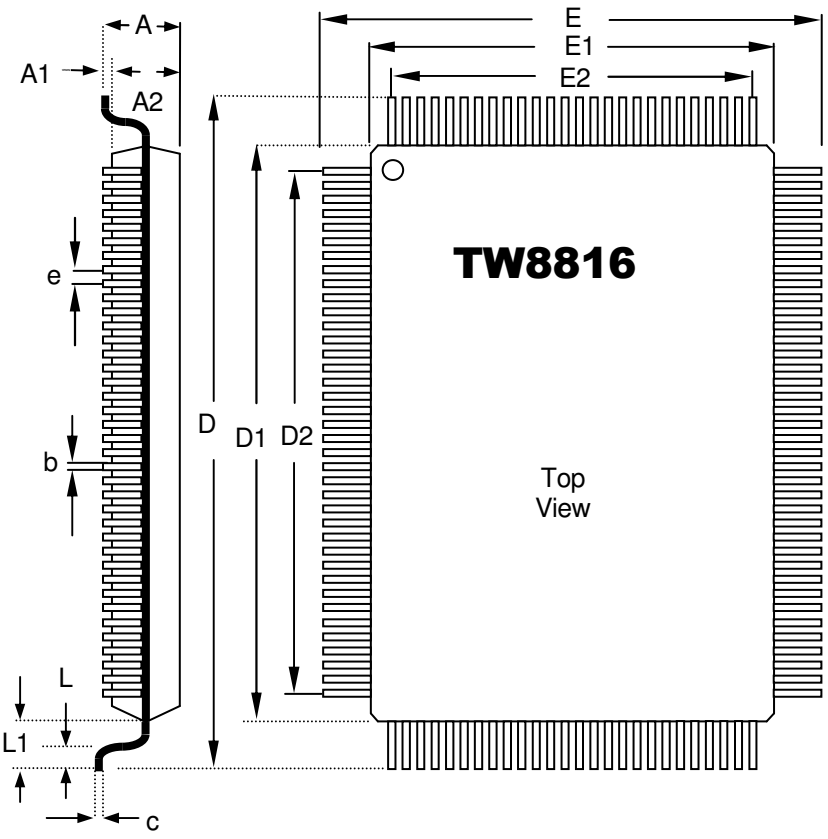
Table 5. Characteristics

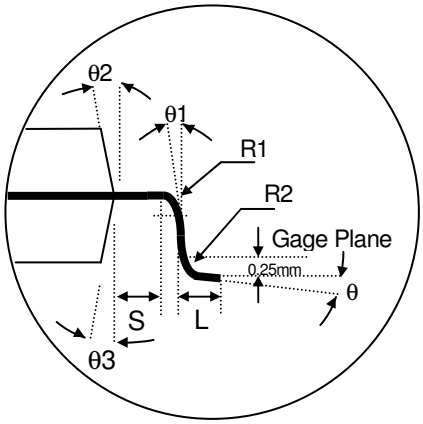
Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO	V_{DDE}	3.15	3.3	3.6	V
Power Supply — Analog 3.3V	V_{DDA33}	3.15	3.3	3.6	V
Power Supply — Analog 1.8V	V_{DDA}	1.62	1.8	1.92	V
Power Supply — Digital	V_{DD}	1.62	1.8	1.98	V
Ambient Operating Temperature	T_A	-40		+85	℃
Analog Supply current 3.3V	Iaae	-	24.3	-	mA
Analog Supply current 1.8V(CVBS only)	Iaa	-	21.1	-	mA
Digital I/O Supply current *	Idde	-	23.1	-	mA
Digital Core Supply Current *	Idd	-	79.7	-	mA
* Note: Digital I/O and core supply current measurement is base on WVGA input(40MHz clock rate) with SMPTE pattern.					

Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD33} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Digital Outputs					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	V_{DD33}	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
YIN0, YIN1 , YIN2 and YIN3 Input Range (AC coupling required)		0.5	1.0	2.0	Vpp
CIN0, CIN1, CIN2 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
VIN0,VIN1 Amplitude Range (AC coupling required)		0.5	1.0	2.0	Vpp
SEN0, SEN1 DC Input Range		0.65	1.65	2.65	V
Analog Pin Input Capacitance	C_A	-	7	-	pF
Analog Output					
COM_OUT(I = 200uA max) DC output		0.65	-	2.65	V
ADCs					
ADC resolution	ADCR	-	9	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	27	60	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz

Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
Deviation *		-	-	±50	ppm
load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
*Note : Crystal Deviation crossover normal operation temperature range					

128-pin LQFP Package Mechanical Drawing





Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	---	0.20	0.004	---	0.008
e	0.50 Basic			0.020 Basic		
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039REF		
R1	0.08	---	---	0.003	---	---
R2	0.08	---	0.20	0.003	---	0.008
S	0.20	---	---	0.008	---	---
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	4° TYP			4° TYP		
θ2	12° TYP			12° TYP		
θ3	12° TYP			12° TYP		

Note:

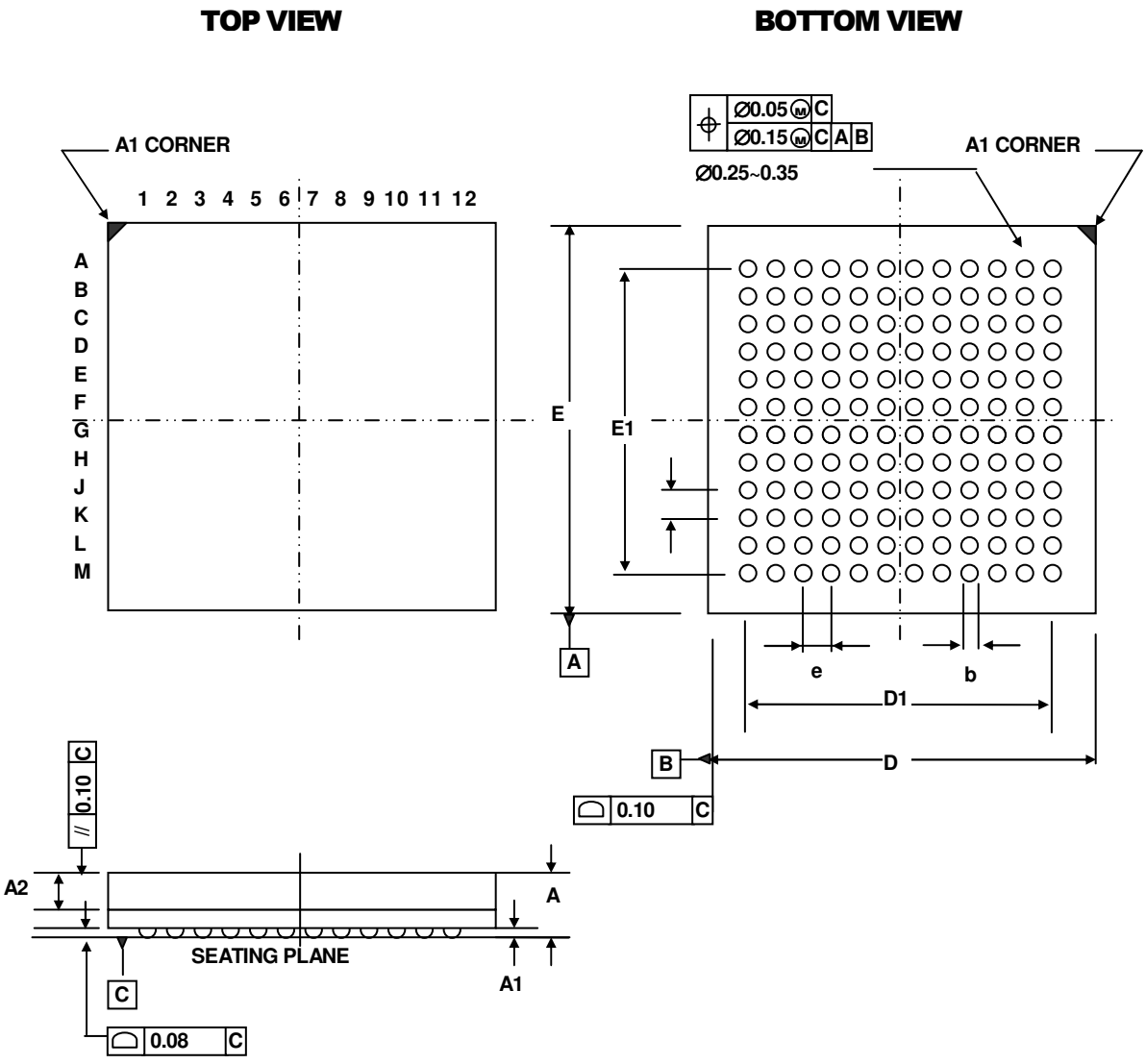
1. Dimension of D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 are maximum plastic body size dimensions including mold mismatch.

2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed. Dambar cannot be located on the lower radius or the lead root.

3. Controlling dimension : Millimeter.

4. A1 is defined as the distance from the seating plane to the lowest point of the package body.

144-pin TFBGA Package Mechanical Drawing



Symbol	Millimeter			Inch		
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	---	---	1.60	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.22	0.26	0.30	0.009	0.010	0.012
e	0.50 Basic			0.020 Basic		
D	6.90	7.00	7.10	0.272	0.276	0.280
D1	---	5.50	---	---	0.217	---
E	6.90	7.00	7.10	0.272	0.276	0.280
E1	---	5.50	---	---	0.217	---

Note:

1. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
2. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Controlling dimension : Millimeter.
4. There shall be A minimum clearance of 0.25mm between the edge of the solder ball and the body edge.

TW8816 Register Summary

The registers are organized in functional groups in this Register Summary. A register containing different functional bits may appear more than once in different functional groups. If a particular bit of a register is not related to that functional group, it is printed in smaller font than those related. For example, bit 7 of index 006 is classified as "General" and is printed in normal size; the other bits in this register are printed in smaller size for their functionality is not classified as "General".

General

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
000	ID					REV			21h
XFF	*	*	*	*	*	*	*	PAGE_1	00h

Decoder

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
001	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	CCVALID	MONO	DET50	00h
002	CSEL1	FC27	IFSEL		YSEL		CSEL0	VSEL	40h
003	-								-
004	-	CKHY		-					00h
005	-								-
006	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	V_PDN	-
007	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		12h
008	VDELAY_LO								12h
009	VACTIVE_LO								20h
00A	HDELAY_LO								10h
00B	HACTIVE_LO								D0h
00C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CCh
00D	SAVE	MIX	WSSEN	CCODDLINE					15h
00E	CRCERR	WSSFLD	WSS1						-
00F	WSS2								-
010	BRIGHTNESS								00h
011	CONTRAST								5Ch
012	SCURVE	VSF	CTI		SHARPNESS				11h
013	SAT_U								80h
014	SAT_V								80h
015	HUE								00h
016	-								-
017	SHCOR				-	VSHP			30h
018	CTCOR		CCOR		VCOR		CIF		44h
019	-								-
01A	-	EDS_EN	CC_EN	PARITY	FF_OVF	FF_EMP	CC_EDS	LO_HI	00h
01B	CC_DATA								-
01C	DTSTUS	STDNOW			ATREG	STANDARD			17h
01D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSCM	7Fh
01E	-	CVSTD			CVFMT				08h
01F	TEST								00h

Decoder (Cont.)

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
020	CLPEND				CLPST				**50h**
021	NMGAIN				WPGAIN			AGCGAIN8	**42h**
022	AGCGAIN								**F0h**
023	PEAKWT								**D8h**
024	CLMPLD	CLMPL							**BCh**
025	SYNCTD	SYNCT							**B8h**
026	MISSCNT				HSWIN				**44h**
027	PCLAMP								**2Ah**
028	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	**00h**
029	BSHT			VSHT					**00h**
02A	CKILLMAX		CKILLMIN						**78h**
02B	HTL				VTL				**44h**
02C	CKLM	YDLY			HFLT				**30h**
02D	HPLC	EVCNT	PALC	SDET	TBC_EN	BYPASS	SYOUT	HADV	**14h**
02E	HPM		ACCT		SPM		CBW		**A5h**
02F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	**E0h**
030	SID_FAIL	PID_FAIL	FSC_FAIL	SLOCK_FAIL	CSBAD	MVCSN	CSTRIPE	CTYPE	**-**
031	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	**-**
032	HFREF/GVAL/PHERRDO/CGAINO/BAMPO/MINAVG/SYTHRD/SYAMP								**-**
033	FRM		YNR		CLMD		PSP		**05h**
034	INDEX		NSEN/SSEN/PSEN/WKTH						**1Ah**
035	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	**00h**
036-37	-								
038	DEC_SEL	-	-	-	FBPY	FBPC	FBPV	-	**80h**

LCDC – Input Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
040	OFDM	RVODDP	SLVSFLD	ECSYNC	DE_POL	HS_POL	VS_POL	CK_POL	00h
041	*	*	EXT_HA	SELDE	PCLK_POL	DTVCK_DELAY			20h
042	VGAFLD	SELFVS	VSDL_656	SELFTHS	CR601	INPUT_DATA_BUS_ROUTING			04h
043	*	*	PCKCAP		*	*	DECPOL		22h
044	COAST_RANGE		DUAL_656	B8601	IP_COLOR_FMT		IP_SEL		08h
045	OFD_DET_END				OFD_DET_ST				54h
046	CSYNC_VS_OFFSET								20h
047	IP_HA_ST_LO								00h
048	IP_HA_END_LO								CFh
049	IP_HA_END_HI				*	IP_HA_ST_HI			20h
04A	IP_VA_ST_ODD_LO								13h
04B	IP_VA_ST_EVN_LO								13h
04C	IP_VA_LENGTH_LO								00h
04D	*	IP_VA_LENGTH_HI			IP_VA_ST_EVN_HI		IP_VA_ST_ODD_LO		30h
04E	*	GPIOEN2	GPIOEN1	GPIOEN0	IRQ_AL	SEL_GPIO_OUT2	SEL_GPIO_OUT1	*	00h
04F	GPIO1_P	GPIO1_SRC		GPIO1_D	GPIO0_P	GPIO0_SRC		GPIO0_D	00h

LCDC – Input Measurement

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
050	*								00h
051	MEA_WIN_H_ST_LO								20h
052	MEA_WIN_H_END_LO								FFh
053	MEA_WIN_H_END_HI				*	MEA_WIN_H_ST_HI			10h
054	MEA_WIN_V_ST_LO								20h
055	MEA_WIN_V_END_LO								FAh
056	*	MEA_WIN_V_END_HI			*	MEA_WIN_V_ST_HI			00h
057	RESULT_0								-
058	RESULT_1								-
059	RESULT_2								-
05A	RESULT_3								-
05B	RESULT_SEL				FIELD_SEL		RD_LOCK	STARTM	00h
05C	U_27M	NOISE_MASK			ERR_TOLER			ENDET	00h
05D	THRESHOLD_FOR_ACT_DET				ENALU	NOFSEL		*	30h

LCDC - Scaling

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
060	X_SCALE_UP_MID								B4h
061	X_SCALE_DOWN_LO								80h
062	Y_SCALE_UP/DOWN_MID								50h
063	PANORA_MA	*	*	ZOOMBP	Y_SCALE_UP/DOWN_HI	Y_SCALE_UP/DOWN_MI	X_SCALE_DOWN_HI	X_SCALE_UP_HI	00h
064	X_OFFSET								00h
065	Y_OFFSET_EVEN								80h
066	H_NON_DISPLAY_PIXEL / H_PANORAMA_PIXEL								00h
067	LB_CE	*	*	*	*	*	H_NON_DISPLAY / H_PANORMAN_PIXEL		00h
068	X_SCALE_UP_LO (AT_THE_SIDE_FOR_PANORAMA)								00h
069	X_SCALE_UP_LO								00h
06A	Y_SCALE_UP/DOWN_LO								00h
06B	Y_OFFSET_ODD								00h

LCDC – Image Adjustment

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
070	*	INDX_CB	HUE						20h
071	CONTRAST_R / CONTRAST_Y								80h
072	CONTRAST_G / CONTRAST_Cb								80h
073	CONTRAST_B / CONTRAST_Cr								80h
074	BRIGHTNESS_R / BRIGHTNESS_Y								80h
075	BRIGHTNESS_G								80h
076	BRIGHTNESS_B								80h
077	H_SHARP_COR				H_SHARPNESS				3Fh
078	H_SHARP_FREQ	*	DYNR		HFLT				0Ah
079	*		*		*	*			-
07A	*								-
07B	*		*		*				-
07C	T_BW	*	PEDLVL	WHTLVL	UBTILT	UWTILT	BPBW	*	1Ch
07D	BW_LINE_ST_LO								08h
07E	BW_LINE_END_LO								F6h
07F					BW_LINE_END_HI		BW_LINE_ST_HI		08h
080	BW_H_DELAY								10h
081	*		BW_H_FILTER_GAIN						0Dh
082	*		BW_V_FILTER_GAIN						03h
083	BW_LDIFF								00h
084	BW_BLACK_TILT								67h
085	BW_WHITE_TILT								94h
086	BW_BLACK_LIMIT								18h
087	BW_WHITE_LIMIT								E8h
088	BW_MODE		*						CAh
089	*	BW_GAIN							02h
08A	*	*	*	*					0Ah
08B	*	*	*	*					04h

LCDC – OSD

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
090	*	*	*	*	*	*	*	*	-
091	*	*	*	*	*	*	*	*	-
092	*	*	*	*	E_VDLY				06h
093	*	*	*	*	*	*	*	*	-
094	F_RAM	ITALIC	UNDER_LINE	CBS_EN	FR_ADD[1:0]		FRAM_CL	FR_RAC_SEL	00h
095	W1END	VBEND	CH_EXT	RD978_SEL	*	*	*	*	00h
096	SERIAL_BUS_OSD_RAM_ADDR[7:0]								00h
097	SERIAL_BUS_OSD_RAM_DATA_HI (Font Data)								-
098	SERIAL_BUS_OSD_RAM_DATA_LO (Font Attribute)								-
099	SERIAL_BUS_FONT_RAM_ADDR								00h
09A	SERIAL_BUS_FONT_RAM_DATA								-
09B	START_SRAM_ADDRESS								31h
09C	RAM_D16	*	*	OSD_OFF	CH_COLOR_LOOKUP_ADDR				00h
09D	CH_COLOR_LOOKUP_DATA								00h
09E	WIN_ALPHA_COLOR_SEL				*	*	WIN_CON_SEL		00h
09F	WIN_C	WIN_R	WIN_G	WIN_B	WIN_3D	WIN_E3D	WIN_E3L	WIN_EN	00h
0A0	*	*	WIN_V_ST[9:8]		*	WIN_H_ST[10:8]			00h
0A1	WIN_H_ST[7:0]								00h
0A2	WIN_V_ST[7:0]								00h
0A3	*	*	WIN_WIDTH						00h
0A4	*	*	WIN_HEIGHT						00h
0A5	WINBC_EN	WINBC_R	WINBC_G	WINBC_B	WINBC_WIDTH				00h
0A6	WINBC	WIN_BORDER_H_WIDTH							00h
0A7	*	WIN_BORDER_V_WIDTH							00h
0A8	WIN_CHARACTER_V_SPACE				WIN_CHARACTER_H_SPACE				00h
0A9	WIN_V_ZOOM		WIN_H_ZOOM		*	*	*	*	00h
0AA	WIN_CNT_ST_ADDR[7:0]								00h
0AB	WINS_E	WINS_R	WINS_G	WINS_B	WIN_SHADOW_WIDTH				00h
0AC	*	*	*	*	WIN_ALPHA_BLENDING				00h
0AD	WINSC	WINMC_EN	CV_EXT	WINC_BSE_SE	WINC_SHAD_C	WINC_SHAD_R	WINC_SHAD_G	WINC_SHAD_B	00h
0AE	*	*	*	*	WIN_C_V_SPACE[4]	WIN_C_H_SPACE[4]	WIN_SHA_WIDTH[4]	WINBC_WIDTH[4]	00h

LCDC – Display Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0B0	*	FPDEAH	FPHSAH	FPVSAH	RVFPCK	DELTA_N	RVBIT	FPCLKC	40h
0B1	TCONS	*	DEMODE	OP6B	TRIFP	FPCLK_DELAY			00h
0B2	FPHS_PERIOD_LO								3Ah
0B3	FPHS_ACTIVE_PW								10h
0B4	FP_H_BACK_PORCH								1Bh
0B5	FPDE_ACTIVE_LO								00h
0B6	USEREG	FPDE_ACTIVE_HI			FPHS_PERIOD_HI				42h
0B7	FPVS_PERIOD_LO								26h
0B8	FPVS_ACTIVE_PW								06h
0B9	FP_V_BACK_PORCH								1Fh
0BA	FP_V_ACTIVE_LO								00h
0BB	EARLY_ST	FP_V_ACTIVE_HI			*	FPVS_PERIOD_HI			33h
0BC	*	DITHER_OPTION			*	DITHER_FORMAT			00h
0BD	VSYNC_DELAY								08h
0BE	FRCLONG	FRCSHRT	EPWMX	PWM_AL	VH_DISHA	FRERUN	AUTOC	SDELVS	00h
0BF	DISP_SNGFLD		RVF_AC	TVVSF4	NOEVNI	EVNDLY			00h
0C0	INI_CNT_EVN_LO								00h
0C1	INI_CNT_ODD_LO								00h
0C2	INI_CNT_EVN_HI				INI_CNT_ODD_HI				00h
0C3	EVNPM	NUMBER_OF_LINES_TO_BLACK_OUT							00h
0C4	PWMC_D2	PWM_COUNTER							40h
0C5	-								00h
0C6	-								00h
0C8	-		MCUDBG	LADC_PD_CMP	LADC_PD	LADC_DIV[2 :0]			00h
0C9	LADC0[7:0]								00h
0CA	LADC1[7:0]								00h

LCDC – Status & Interrupt

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0D0	LB_OVF	LB_UNF	V_LOS_C	H_LOS_C	VDLOS_C	V_LOSS	H_LOSS	SYNCS	-
0D1	M_RDY	PWS_C	V_PRD_C	H_PRD_C	LBOUNF	VDC_C	VH_LOS_C	SYNCS_C	-
0D2	IRQ_MSK_7	IRQ_MSK_6	IRQ_MSK_5	IRQ_MSK_4	IRQ_MSK_3	IRQ_MSK_2	IRQ_MSK_1	IRQ_MSK_0	FFh
0D3	IRQ_OUT_EN	*				*	*	*	07h

LCDC – Power Management

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0D4	DIVDE_DOWN_COUNTER_MSB								00h
0D5	PCLK_PDN	EN_PIN5	PWR_STATE		MANPWR	EDPMS	PWR_STATE_WT		00h
0D6	SUSPEND_STDBY_CNT				ON_SUSPEND_CNT				00h
0D7	OFF_STDBY_CNT				STDBY_OFF_CNT				00h
0D8	STDBY_SUSPEND_CNT				SUSPEND_ON_CNT				00h

LCDC – Color Enhancement

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0DA	CE_CENTER0								3Dh
0DB	CE_CENTER1								C3h
0DC	CE_CENTER2								FCh
0DD	CE_EN	CE_SPREAD0		CE_GAIN0					00h
0DE	*	CE_SPREAD1		CE_GAIN1					00h
0DF	*	CE_SPREAD2		CE_GAIN2					00h

LCDC – ETC

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0E0	LLBF	SELFCNT	*	SACNT	*	*	*	wr_sqnc_en	40h

LCDC – Gamma

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F0	GAMAE_R	GAMAE_G	GAMAE_B	*	AUTO_INC		GAMMA_RGB_INDX		00h
0F1	GAMMA_RAM_STARTING_ADDR								00h
0F2	GAMMA_RAM_DATA								-

DAC

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F6				DA_Rgain[4:0]					00h
0F7				DA_Ggain[4:0]					00h
0F8	DAC PD		daciref_new	DA_Bgain[4:0]					00h

SSPLL

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0F9	CLK_SEL		-	-	FPLL[19:16]				00h
0FA	FPLL[15:8]								40h
0FB	FPLL[7:0]								00h
0FC	FSS[7:0]								40h
0FD	PD_SSPLL	SSD			SSG				30h
0FE	POST		VCO		-	IPMP			11h

CCFL Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
130	OVEN	OIEN	UIEN	FBEN	LOCKV	LOCKH	CCFLENB	CCFLDEN	F2h
131	LVT		LILT		LIT				ADh
132			CCFL_ST		LSTP				04h
133	FPWM								80h
134	FDIM								84h
135				DDIM					00h
136	PWMTOP								20h

Test Control and GPO

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
01F	TEST_MODE								00h
140	GPO17_EN	GPO16_EN	GPO15_EN	GPO14_EN	GPO13_EN	GPO12_EN	GPO11_EN	GPO10_EN	00h
141	GPO17_O	GPO16_O	GPO15_O	GPO14_O	GPO13_O	GPO12_O	GPO11_O	GPO10_O	00h
142									0h
143									0h
157	COUNTER_READ_BYTE_0								-
158	COUNTER_READ_BYTE_1								-
159	COUNTER_READ_BYTE_2								-
15A	COUNTER_READ_BYTE_3								-

TCON

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
176	*				GPIO_PIX_H[3:0]				00h
177	GPIO_PIX_L[7:0]								5Ah
178	*				GPIO_LINE_H[3:0]				00h
179	GPIO_LINE_L[7:0]								7Fh
17A	*					GPIO_FRAME[2:0]			01h
17B	GPIO_CON	LINE_CON	SYNC_CON[1:0]		CLPSEL[1:0]		CSPSEL[1:0]		00h
180	GPIO_0	TCCK_PH	ROE_EN	*				DIV_CK	20h
181	*	POL_CON	DELTA_LINE_CON	DELTA_LINE_EN	REV_EN	*	INV		00h
182	*				TOP_BTM		LFT_RHT		05h
183	*			RCK_P	ROE_P	RSP_P	CLP_P	CSP_P	1Fh
184	*		PGM_RCK	PGM_ROE	PGM_RSP	PGM_CP	PGM_CLP	PGM_CSP	00h
185	*							INV_SW	00h
18A	*		RSP_WIDTH		*		COMPANY		02h
18B	REVV_REVC								4Dh
18C	*				V_ST[11:8]				00h
18D	V_ST[7:0]								06h
18E	*				V_ED[11:8]				01h
18F	V_ED[7:0]								E2h
190	CP_SW[11:8]								02h
191	CP_SW[7:0]								D0h
192	*				LP_ST[11:8]				02h
193	LP_ST[7:0]								D0h
194	*				LP_ED[11:8]				00h
195	LP_ED[7:0]								06h
19A	*				SP_ST[11:8]				00h
19B	SP_ST[7:0]								C8h
19C	*				SP_ED[11:8]				00h
19D	SP_ED[7:0]								01h

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1A0	*				CSP_ST[11:8]				00h
1A1	CSP_ST[7:0]								00h
1A2	*				CSP_ED[11:8]				02h
1A3	CSP_ED[7:0]								30h
1A4	*				RSP_ST[11:8]				00h
1A5									06h
1A6	*				RSP_ED[11:8]				00h
1A7									01h
1AC	*				ROE_ST[11:8]				00h
1AD									0Ah
1AE	*				ROE_ED[11:8]				00h
1AF	ROE_ED[7:0]								36h
1B0	*						REV_INV	LINE_INV	02h

LCDC – Sense

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1B1	*		SEN_SEL	BIAS_CTL	SEN_FREQ				03h
1B2	CP0_LVL				CP1_LVL				88h
1B3	CP0_FREQ				CP1_FREQ				00h
1B4	VCOM DC								00h

ADC/LLPLL

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1C0	*		CS_INV	CS_SEL	SOG_SEL	HS_POL	*	CK_SEL	00h
1C1	VS_POL	HS_POL	VS_DET	HS_DET	CS_DET	DET_FMT			-
1C2	LLC_POST		LLC_VCO		-	LLC_PIMP			00h
1C3	-	-	-	-	LLC_ACKN[11:8]				03h
1C4	LLC_ACKN[7:0]								5Ah
1C5	*		LLC_PHA						00h
1C6	LLC_ACPL	LLC_APG			-	LLC_APZ			20h
1C7	-				LLC_ACKI[11:8]				04h
1C8	LLC_ACKI[7:0]								00h
1C9	PRE_COAST								06h
1CA	POST_COAST								06h
1CB	PUSOG	PUPLL	COAST_EN	SOG_TH					30h
1CC	-	-	-	VSY_SEL	HSY_SEL		VSY_POLC	HSY_POLC	00h
1CD	-	-	-	-	-	-	-	INIT	00h

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1D0						GAINY[8]	GAINC[8]	GAINV[8]	00h
1D1	GAINY[7:0]								F0h
1D2	GAINC[7:0]								F0h
1D3	GAINV[7:0]								F0h
1D4	RGB_MODE		CL_EDGE	CLKY	CLKC	CL_Y_EN	CL_C_EN	CL_V_EN	00h
1D5	CL_START								00h
1D6	CL_END								10h
1D7	CL_LOC								70h
1D8		LLC_DBG_SEL				ADC_TEST	CL_Y_TEST	CL_C_TEST	00h
1D9	CL_Y_VAL								10h
1DA	CL_C_VAL								80h

Test Control

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
1F0	PCCINIA_INDEX		FRC_2F	FRC_1F	PCCINIA_SUB_INDX				**00h**
1F1	PCCINID								**00h**
1F2	-								
1F3	SEL_C	GRAYD	DATA_0	*	*	*	ROMSFT	RAMSFT	**00h**

MCU SFR Register

Index (HEX)	7	6	5	4	3	2	1	0	Reset value
0x9A	*		BANK_SEL[5:0]						**00h**
0x9B	*		SCLK_SEL[1:0]		LOWSPD	HOST_S1	HOST_S0	DUAL	**00h**
0x9C	T0_DIV_H[7:0]								**00h**
0x9D	T0_DIV_L[7:0]								**90h**
0x9E	T1_DIV_H[7:0]								**00h**
0x9F	T1_DIV_L[7:0]								**90h**
0x93	T2_DIV_H[7:0]								**00h**
0x94	T2_DIV_L[7:0]								**90h**

0x000 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	The TW8816 Product ID code is 00100.	00100b
2-0	Revision	R	Revision number	001b

0x001 – Chip Status Register (CSTATUS)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	*Reserved*	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x002 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	CSEL[1]	R/W	CSEL[1:0] (It's include in CSEL[0]) 00 : CIN0, 01 : CIN1, 10 : CIN2, 11 : N/A	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	11 = Component video decoding (Progressive input) 10 = Component video decoding (Interlace input) 01 = S-video decoding 00 = Composite video decoding	00
3-2	YSEL[1:0]	R/W	These two bits control the input video selection. It selects the composite video source or luma source. 00 : YOUT = YIN0 01 : YOUT = YIN1 10 : YOUT = YIN2 11 : YOUT = YIN3	00
1	CSEL[0]	R/W	CSEL[1:0] 00 : CIN0, 01 : CIN1, 10 : CIN2, 11 : Not exist	0
0	VSEL	R/W	This bit select the V channel input 0 : VIN0, 1 : VIN1	0

0x003 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x004 – HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	0
6-5	CKHY	R/W	Color killer time constant 0: fast 3: slow	0
4-0	Reserved	R/W	Reserved	0

0x005 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x006 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	A 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	1
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = 27 MHz clock in power down mode.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	0
0	V_PDN	R/W	0 = V channel ADC in normal operation. 1 = V channel ADC in power down mode.	0

0x007 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	00
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	01
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	00
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	10

0x008 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12h

0x009 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20h

0x00A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	10h

0x00B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0h

0x00C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	Combined with VTL[3], there are four different chroma bandwidth can be selected. 1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Color killer sensitivity. 1= low 0 = high	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC/PAL 0 = Notch filter	1
2	HCOMP	R/W	1 = Operation mode 1. (recommended) 0 = Operation mode 0.	1
1	YCOMB	R/W	This bit controls the comb operation when there is no color burst. 1 = No comb. 0 = comb.	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0x00D – CC Control

Bit	Function	R/W	Description	Reset
7	SAVE	R/W	Reference current save mode control. 0 = normal mode. 1 = 2/3 of normal current	0
6	MIX	R/W	Analog YOUT control 0 = Y output. 1 = Y + C output.	0
5	WSSEN	R/W	1 = Enable WSS decoding. 0 = Disabled.	
4-0	CCODDLINE	R/W	These bits control the Closed Caption decoding line number in case of odd field	15h

0x00E – WSS1

Bit	Function	R/W	Description	Reset
7	CRCERR	R	This is the CRC error indicator for 525-line WSS. 1:CRC error.0:no error	-
6	WSSFLD	R	These bit indicates the detected WSS field information, 0=odd and 1=even.	-
5-0	WSS1	R	These bits represent the sliced WSS data bit 13 to 8.	-

0x00F – WSS2

Bit	Function	R/W	Description	Reset
7-0	WSS2	R	These bits represent the sliced WSS bit 7 to 0.	-

0x010 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	Brightness	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00h

0x011 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	Contrast	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 1 (`100_0000`) has no effect on the video data.	5Ch

0x012 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	Color transient improvement level control. There are 4 enhancement levels with 0 being the lowest and 3 being the highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image and '15' being the strongest.	1

0x013 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x014 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80h

0x015 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue. It is in 2's complement form with 0 being the center value. Positive value results in red hue and negative value gives green hue.	00h

0x016 – Reserved

Bit	Function	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x017 – Vertical Peaking Control I

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	3h
3	Reserved	R/W	Reserved	0
2-0	VSHP	R/W	Vertical peaking gain control	0

0x018 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring function for the CTI. It has internal step size of 2.	1h
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0h
3-2	VCOR	R/W	These bits control the coring function of the vertical peaking logic. It has an internal step size of 2.	1h
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5 dB 2 = 3 dB 3 = 6 dB	0h

0x019 – Reserved

Bit	Name	R/W	Description	Reset
7-0	Reserved	R/W	Reserved	-

0x01A – CC/EDS Status Register (CC_STATUS)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W	Reserved	0
6	EDS_EN	R/W	0 = EDS data is not transferred to the CC_DATA FIFO. 1 = EDS data is transferred to the CC_DATA FIFO.	0
5	CC_EN	R/W	0 = CC data is not transferred to the CC_DATA FIFO. 1 = CC data is transferred to the CC_DATA FIFO.	0
4	PARITY	R	0 = Data in CC_DATA has no error. 1 = Data in CC_DATA has odd parity error.	-
3	FF_OVF	R	0 = An overflow has not occurred. 1 = An overflow has occurred in the CC_DATA FIFO.	-
2	FF_EMP	R	0 = CC_DATA FIFO is empty. 1 = CC_DATA FIFO has data available.	-
1	CC_EDS	R	0 = Closed caption data is in CC_DATA register. 1 = Extended data service data is in CC_DATA register.	-
0	LO_HI	R	0 = Low byte of the 16-bit word is in the CC_DATA register. 1 = High byte of the 16-bit word is in the CC_DATA register.	-

0x01B – CC/EDS Data Register (CC_DATA)

Bit	Function	R/W	Description	Reset
7-0	CC Data	R	These bits store the incoming closed caption or even field closed caption data.	-

0x01C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	1
2-0	Standard	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7h

0x01D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x01E – Component Video Format (CVFMT)

Bit	Name	R/W	Description	Reset
7	RSV	R	Reserved	0
6-4	CVSTD	R	Component video input format detection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p	0h
3-0	CVFMT	R/W	Component video format selection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p, 8 = Auto	8h

0x01F – Test Control Register (TEST)

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 03h = Digital video decoder & RGB mix direct input test This test mode allows digital data to be input from DTVD[23:0] pins to the input of the digital logic of the video decoder (replaces YCADC output) as the case when the contents of this register is 04h. Besides this, the FPG1/FPB1/FPR1 pins become inputs and provide data in place of RGBADC data output. 04h = Digital video decoder direct input test This test mode allows digital data to be input from DTVD pins to the input of the digital logic of the video decoder. (Replaces ADC output) DTVD(23-16) > "Y" decoder input data, DTVD(15-8) > "U" decoder input data DTVD(7-0) > "V" decoder input data 05h = Closed caption test mode. 06h = YCADC test mode (DTVD pins become outputs) YCADC digital output is made available externally. "Y" ADC output data > DTVD(15-8), "C" & "FB" ADC output data > DTVD(7-0) Index-1F3-bit-7 = 1 > "C" data Index-1F3-bit-7 = 0 > "FB" data. 07h = Digital video decoder output test (DTVD pins become outputs) The output of the digital video decoder output is available externally. "R" decoder out data > DTVD(23-16), "G" decoder out data > DTVD(15-8) "B" decoder out data > DTVD(7-0) "Vsync" > CLAMP "Hsync" > GPIO[1] "Hactive" > GPIO[0] 08h = RGBADC test mode (DTVD pins become outputs) RGBADC digital output is made available externally. "G" ADC output data > DTVD(15-8), "B" & "R" ADC output data > DTVD(7-0) Index-1F3-bit-7 = 1 > "B" data Index-1F3-bit-7 = 0 > "R" data. 09h = DAC test mode. DTVD[7:0] inputs are routed to the DAC data input "DIN". 0Ah = Analog ADC Clamp test mode. DTVD[3:0] inputs are routed to ADC clamping control. 0Bh = DAC test mode. Internal generates incremental data for DAC data input. 11h = TW88 internal node to flat panel output	00h

0x020 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping time is determined by this together with CLPST.	5h
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0h

0x021 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	4h
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1h
0	AGCGAIN8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x022 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0h

0x023 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold.	D8h

0x024– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3Ch

0x025– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38h

0x026 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4h
3-0	HSWIN	R/W	These bits set the size for the horizontal sync detection window.	4h

0x027 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	2Ah

0x028 – Vertical Control I

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	00
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	00
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = normal 0 = short	0

0x029 – Vertical Control II

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control.	0h
4-0	VSHT	R/W	Vsync output delay control in the increment of half line length	00h

0x02A – Color Killer Level Control

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1h
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38h

0x02B – Comb Filter Control

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter combing strength control.	4h
3-0	VTL	R/W	Adaptive Comb filter combing strength control. Higher value provides stronger comb filtering.	4h

0x02C – Luma Delay and HFilter Control

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3h
3-0	HFLT	R/W	Peaking control 2. The peaking curve is controlled by SCURVE bit.	0h

0x02D – Miscellaneous Control Register I (MISC1)

Bit	Function	R/W	Description	Reset
7	HPLC	R/W	Reserved.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation.	0
5	PALC	R/W	Reserved.	0
4	SDET	R/W	ID detection sensitivity. A "1" is recommended.	1
3	TBC_EN	R/W	1 = Internal TBC enabled. (test purpose only) 0 = TBC off.	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = Hsync is disabled when video loss is detected. 0 = Hsync is always generated.	0
0	HADV	R/W	Reserved.	0

0x02E – Miscellaneous Control Register II (MISC2)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 0 = slow 1 = medium 2 = auto 3 = Fast	2h
5-4	ACCT	R/W	ACC time constant 00 = No ACC 01 = slow 10 = medium 11 = fast	2h
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1h
1-0	CBW	R/W	Chroma low pass filter bandwidth control. 0 = Low 1 = Medium 2 = High 3 = NA	1h

0x02F – Miscellaneous Control III (MISC3)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x030 – Macrovision Detection

Bit	Function	R/W	Description	Reset
7	SID_FAIL	R		-
6	PID_FAIL	R		-
5	FSC_FAIL	R		-
4	SLOCK_FAIL	R		-
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	-
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	-
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	-
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	-

0x031 – Chip STATUS II (CSTATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator	-
6	WKAIR	R	Weak signal indicator 2	-
5	WKAIR1	R	Weak signal indicator1	-
4	VSTD	R	Standard line per field indicator	-
3	NINTL	R	Non-interlaced signal indicator	-
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	-
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	-
0	CCDET	R	1 = CC data detected. 0 = Not detected.	-

0x032 – H Monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF, etc.	R	Horizontal line frequency indicator HREF[9:2] / GVAL[8:1] / PHERRDO / CGAINO / BAMPO / MINAVG / SYTHRD / SYAMP	-

0x033 – CLAMP MODE(CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode. 0X = Auto mode 10 = 60 Hz 11 = 50 Hz	0h
5-4	YNR	R/W	Y HF Noise Reduction. 0 = None 1 = smallest 2 = small 3 = medium	0h
3-2	CLMD	R/W	Clamping mode control. 00 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1h
1-0	PSP	R/W	Slice level. 0 = Low 1 = Medium 2 = High	1h

0x034 – ID Detection Control (NSEN/SSEN/PSEN/WKTH)

Bit	Function	R/W	Description	Reset
7-6	Index	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	00
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1E / 20 / 1C / 2A

0x035 – Clamp Control (CLCNTL)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debug use.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = C channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Sync filter bandwidth control	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x038 – Anti-Aliasing Filter and Decoder Control

Bit	Function	R/W	Description	Reset
7	DEC_SEL	R/W	Analog ADC input selection 0 : Input from RGB path 1 : Input from Decoder path	1
6-4	Reserved	R/W	Reserved	-
3	FBPY	R/W	Anti-Aliasing Filter control channel Y 0 : Filter 1 : Bypass	0
2	FBPV	R/W	Anti-Aliasing Filter control channel V 0 : Filter 1 : Bypass	0
1	FBPC	R/W	Anti-Aliasing Filter control channel C 0 : Filter 1 : Bypass	0
0	Reserved	R/W	Reserved	0

Flat Panel Display Registers

0x040 to 0x04F – Scaler Input Control Registers

Address	Bit	R/W	Description	Reset
0x040	7	R/W	This bit has dual function. It serves as odd field detection method selection or ITU656 progressive/interlaced selection. If bits 3:2 of Index 44h does not choose ITU656: Odd Field Detection Method for Digital input port 0: Use internal default method 1: Use Detection method defined by register 0x45 If bits 3:2 selects ITU656, this bit sets the input to interlaced (0) or progressive(1).	0
	6	R/W	Invert internal detected field signal	0
	5	R/W	Field is determined by the leading or trailing edge of input VSYNC when using 0x45 for field determination. 1: Trailing edge.	0
	4	R/W	Enable CSYNC (Composite SYNC); DTVHS is treated as a CSYNC input.	0
	3	R/W	DE polarity of the digital source. 0: Active High	0
	2	R/W	HSYNC polarity of the digital source. 0: Active High	0
	1	R/W	VSYNC polarity of the digital source. 0: Active High	0
	0	R/W	Invert Digital input port DTVCLK polarity, 0: Rising edge 1: Falling edge	0
Address	Bit	R/W	Description	Reset
0x041	7	R/W	Reserved.	0
	6	R/W	Reserved.	0
	5	R/W	Select Explicit DE (Data Enable also called HA for Horizontal Active); 0: HA is asserted in the input active region defined by registers 0x47 through 0x4D 1: HA is defined by individual video source	1
	4	R/W	0 = Pin DTVDE is used as the data enable (DE). 1 = Pin DTVDE is used as HSYNC input	0
	3	R/W	PCLK Polarity	0
	2 - 0	R/W	Input clock DTVCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	000

Address	Bit	R/W	Description	Reset
0x042	7	R/W	Enable field detection for Digital input port when index 44 bit 1 & 0 is 2'b01.	0
	6	R/W	Set this bit to "1" if the DTVVS input is not a pulse but a "field" signal.	0
	5	R/W	ITU656 even field VSYNC delay. 1: Delay the assertion to the falling edge of "ha". 0: No delay	0
	4	R/W	Use filtered HSYNC to maintain constant input HSYNC period.	0
	3	R/W	Set this bit to 1 in 8 bit 601 mode if the Cr data arrives before Cb data.	0
	2 –0	R/W	Data bus routing selection for Digital input port For 24 bit YpbPr or 24 bit RGB DTVD[23:16] DTVD[15:8] DTVD[7:0] 000: Pr/B Y/R Pb/G 001: Pr/B Pb/G Y/R 010: Pb/G Y/R Pr/B 011: Pb/G Pr/B Y/R 100: Y/R Pb/G Pr/B 101: Y/R Pr/B Pb/G For 16 bit Ypb/Pr: Follow the table above with Y and Pb. Example: If Y data is connected to DTVD[23:16] and Pb/Pr data is connected DTVD[7:0], the bus routing selection should be set to "101". If Explicit DE, Index 44 bit [4], is set, the very first DTVDE is assumed to have Pb data. On the other hand if Explicit DE is reset, Index 40 bit [3] is used to select the order of Pb /Pr. For 8 bit Y/Pb/Pr: Follow the table above with Pr. Example: If Y/Pb/Pr data is connected to DTVD[15:8], the bus routing selection can be set to "011" or "101". Use the table below for the correct data order. Index 41 bit 5 Index 40 bit 3 Index 42 bit 3 Data Order 1 X 0 Pb-Y-Pr-Y 1 X 1 Pr-Y-Pb-Y 0 0 0 Pb-Y-Pr-Y 0 0 1 Pr-Y-Pb-Y 0 1 0 Y-Pb-Y-Pr 0 1 1 Y-Pr-Y-Pb	100
Address	Bit	R/W	Description	Reset
0x043	7	R/W	Reserved.	0
	6	R/W	Reserved.	0
	5-4	R/W	FPCLK output driving capability control. 00 = reserved 01 = 4mA 10=8mA 11= disabled	10h
	3	R/W	When this bit is set to one, GPIO[2] output is used to output the PLLCK. For PLL operation monitoring.	0
	2	R/W	Reserved.	-
	1-0	R/W	DEC_VS, DEC_HS polarity control 00 = VS active hign, HS active low 01 = VS active high, HS active high 10 = VS active low, HS active low 11 = VS active low, HS active high	10h

<table>
<tr><th>Address</th><th>Bit</th><th>R/W</th><th>Description</th><th>Reset</th></tr>
<tr><td>0x044</td><td>7 - 6</td><td>R/W</td><td>Pin COAST is driven to “enabled” state in the window defined below
00: COAST enabled 1 HSYNC period before VSYNC and 7 HSYNC periods after VSYNC
01: COAST enabled 2 HSYNC periods before VSYNC and 8 HSYNC periods after VSYNC
10: COAST enabled 3 HSYNC periods before VSYNC and 9 HSYNC periods after VSYNC
11: COAST enabled 4 HSYNC periods before VSYNC and10 HSYNC periods after VSYNC</td><td>00</td></tr>
<tr><td></td><td>5</td><td>R/W</td><td>Dual 656 mode set
1: Dual 656 mode , pin_112 will be a clock for 2nd 656 input
0: Normal mode</td><td>0</td></tr>
<tr><td></td><td>4</td><td>R/W</td><td>1: 8 bit 601 input mode 0: 8bit 656 input mode</td><td>0</td></tr>
<tr><td></td><td>3 - 2</td><td>R/W</td><td>Input format selection;
00: 422 (16 bit ITU601),
01: ITU656 (8 bits) or ITU601 (8 bit) ; determined by bit 4.
10: 444,
11: RGB</td><td>10</td></tr>
<tr><td></td><td>1 - 0</td><td>R/W</td><td>Input Video/DTV Source Selection;
00: Internal analog video decoder,
01/10: DTV input port,
11: Line Lock ADC input port.</td><td>00</td></tr>
<tr><th>Address</th><th>Bit</th><th>R/W</th><th>Description</th><th>Reset</th></tr>
<tr><td>0x045</td><td>7 - 4</td><td>R/W</td><td>Horizontal Ending Locations of internal Odd Field Detection for Digital input port</td><td>0101</td></tr>
<tr><td></td><td>3 -0</td><td>R/W</td><td>Horizontal Starting Locations of internal Odd Field Detection for Digital input port
<table>
<tr><th></th><th>Start Pixel</th><th>End Pixel</th><th></th><th>Start Pixel</th><th>End Pixel</th></tr>
<tr><td>0000</td><td>32</td><td>64</td><td>1000</td><td>512</td><td>1024</td></tr>
<tr><td>0001</td><td>64</td><td>128</td><td>1001</td><td>576</td><td>1152</td></tr>
<tr><td>0010</td><td>128</td><td>256</td><td>1010</td><td>640</td><td>1280</td></tr>
<tr><td>0011</td><td>192</td><td>384</td><td>1011</td><td>704</td><td>1408</td></tr>
<tr><td>0100</td><td>256</td><td>512</td><td>1100</td><td>768</td><td>1536</td></tr>
<tr><td>0101</td><td>320</td><td>640</td><td>1101</td><td>832</td><td>1664</td></tr>
<tr><td>0110</td><td>384</td><td>768</td><td>1110</td><td>896</td><td>1792</td></tr>
<tr><td>0111</td><td>448</td><td>896</td><td>1111</td><td>960</td><td>1920</td></tr>
</table></td><td>0100</td></tr>
</table>

Address	Bit	R/W	Description	Reset
0x046	7 - 0	R/W	Offset amount to re-construct VSYNC from CSYNC input. The L to H transition of CSYNC input provides the L to H transition of HSYNC. This register defines the amount of offset from this transition edge for generating VSYNC.	0010 0000
Address	Bit	R/W	Description	Reset
0x047	7 - 0	R/W	Input Active Window definition: Horizontal Starting Pixel Position - Low Byte.	0000 0000
Address	Bit	R/W	Description	Reset
0x048	7 - 0	R/W	Input Active Window definition: Horizontal Ending Pixel Position - Low Byte	1100 1111
Address	Bit	R/W	Description	Reset
0x049	7 - 4	R/W	Input Active Window definition: Horizontal Ending Pixel Position – High (Total 12 bits). This position is referenced to the rising edge of input HSYNC.	0010
	3	R/W	Reserved.	-
	2 - 0	R/W	Input Active Window definition: Horizontal Starting Pixel Position - High (Total 11 bits) This position is referenced to the rising edge of input HSYNC.	000
*Note: The value written in this register does not come into effect until a register write to index 0x047 or 0x048 is followed.				
Address	Bit	R/W	Description	Reset
0x04A	7-0	R/W	Input Active Window definition: Odd Field Vertical Line Start Position - Low Byte	0001 0011
Address	Bit	R/W	Description	Reset
0x04B	7-0	R/W	Input Active Window definition: Even Field Vertical Line Start Position - Low Byte	0001 0011
Address	Bit	R/W	Description	Reset
0x04C	7-0	R/W	Input Active Window definition: Vertical Length - Low Byte	0000 0000
Address	Bit	R/W	Description	Reset
0x04D	7	R/W	Reserved.	0
	6 - 4	R/W	Input Active Window definition: Vertical Length - High (Total 11 bits)* The unit of this length is one input HSYNC.	011
	3 - 2	R/W	Input Active Window definition: Even Field Vertical Line Start Position - High (Total 10 bits)*. This position is referenced to the rising edge of input VSYNC.	00
	1 - 0	R/W	Input Active Window definition: Odd Field Vertical Line Start Position - High (Total 10 bits)*. This position is referenced to the rising edge of VSYNC.	00
*Note: When the Explicit-DE is not used (Register 0x041, bit 5), the input active window is defined by the above H-Active and V-Active registers.				

Address	Bit	R/W	Description	Reset
0x04E	7	R/W	Reserved.	0
	6	R/W	GPIO[2] input/output selection. 1: Output (see 0x43 and 0x50 for data source). 0: Input	0
	5	R/W	GPIO[1] input/output selection. 1: Output (see 0x4F for data source). 0: Input	0
	4	R/W	GPIO[0] input/output selection. 1: Output (see 0x4F for data source). 0: Input	0
	3	R/W	Reserved	0
	2	R/W	SEL_GPIO_OUT2 (Active Low) 1: select TCON RD_UD signal for pin output 0: select GPIO2 signal for pin output	0
	1	R/W	SEL_GPIO_OUT1(Active Low) 1: select TCON CD_LR signal for pin output 0: select GPIO1 signal for pin output	0
	0	R/W	Reserved.	0
Address	Bit	R/W	Description	Reset
0x04F	7	R/W	Invert pin GPIO[1] output.	0
	6 - 5	R/W	Output source selection for pin GPIO[1]. 00: Data written to bit 4, 01: VDLOSS, 10: HLOCK, 11: BW_ACTIVE	00
	4	R/W	Read: Shows the sampled input value of pin GPIO[1] Write: Holds the data that can be output to pin GPIO[1]	0
	3	R/W	Invert pin GPIO[0] output.	0
	2 - 1	R/W	Output source selection for pin GPIO[0]. 00: Data written to bit 0, 01: FIELD, 10: HZ50, 11: SLOCK	00
	0	R/W	Read: Shows the sampled input value from pin GPIO[0] Write: Holds the data that can be output to pin GPIO[0]	0
Address	Bit	R/W	Description	Reset
0x050	7 - 3	R/W	Reserved.	-
	2	R/W	Invert pin GPIO[2] output.	0
	1	R/W	Output source selection for pin GPIO[2]. 0 : Data written to bit 0 1 : SS-PLL Clock output if PLL test mode set(regFE[2]).	0
	0	R/W	Read: Shows the sampled input value from pin GPIO[2] Write: Holds the data that can be output to pin GPIO[2]	0

0x051 to 0x05C – Input Format Measurement Registers

Address	Bit	R/W	Description	Reset
0x051	7-0	R/W	Input Measurement Window definition: Horizontal Start - Low Byte	0010 0000
Address	Bit	R/W	Description	Reset
0x052	7-0	R/W	Input Measurement Window definition: Horizontal Stop - Low Byte	1111 1111
Address	Bit	R/W	Description	Reset
0x053	7-4	R/W	Input Measurement Window definition: Horizontal Stop - High three bits (Total 12 bits) This Horizontal Stop position if referenced to the rising edge of input HSYNC and the unit is one input pixel.	0001
	3	R/W	Reserved	0
	2-0	R/W	Input Measurement Window definition: Horizontal Start - High three bits (Total 11 bits) This Horizontal Start position if referenced to the rising edge of input HSYNC and the unit is one input pixel.	000
Address	Bit	R/W	Description	Reset
0x054	7-0	R/W	Input Measurement Window definition: Vertical Start - Low Byte	0010 0000
Address	Bit	R/W	Description	Reset
0x055	7-0	R/W	Input Measurement Window definition: Vertical Stop - Low Byte	1111 1010
Address	Bit	R/W	Description	Reset
0x056	7	R/W	Reserved	0
	6-4	R/W	Input Measurement Window definition: Vertical Stop - High three bits (Total 11 bits) This Vertical Stop position is referenced to the rising edge of input VSYNC and the unit is one input HSYNC.	000
	3		Reserved	0
	2-0	R/W	Input Measurement Window definition: Vertical Start - High three bits (Total 11 bits) This Vertical Start position is referenced to the rising edge of input VSYNC and the unit is one input HSYNC.	000
Address	Bit	R/W	Description	Reset
0x057	7-0	R	Result 0: Data byte 0 of 4 bytes Measurement Result (0x5B bits 7-4 specifies which result to read out)	-
Address	Bit	R/W	Description	Reset
0x058	7-0	R	Result 1: Data byte 1 of 4 bytes Measurement Result (0x5B bits 7-4 specifies which result to read out)	-
Address	Bit	R/W	Description	Reset
0x059	7-0	R	Result 2: Data byte 2 of 4 bytes Measurement Result (0x5B bits 7-4 specifies which result to read out)	-
Address	Bit	R/W	Description	Reset
0x05A	7-0	R	Result 3: Data byte 3 of 4 bytes Measurement Result (0x5B bits 7-4 specifies which result to read out)	-

Address	Bit	R/W	Description	Reset
0x05B	7 - 4	R/W	Select which measurement result to read out from 0x57 ~ 0x5A 0000: Phase Measurement Result - Blue (use Result 3-0 registers) 0001: Phase Measurement Result - Green (use Result 3-0 registers) 0010: Phase Measurement Result - Red (use Result 3-0 registers) 0011: Minimum Value (Result2: R, Result1: G, Result 0:B) 0100: Maximum Value (Result2: R, Result1: G, Result 0:B) 0101: VSYNC Period (Result3, 2) HSYNC Period (Result 1, 0) 0110: HSYNC Rise to HSYNC Fall Interval (Result 1, 0) and HSYNC Rise to HACTIVE Fall Interval (Result 3, 2). 0111: VSYNC pulse width (Result 1,0), Horizontal pixel counter value at the leading edge of VSYNC (Result 3, 2). 1000: Min Horizontal Active Starting Pixel (Results 1 & 0) Max Horizontal Active Starting Pixel (Results 3 & 2) 1001: Min Horizontal Active Ending Pixel (Results 1 & 0) Max Horizontal Active Ending Pixel (Results 3 & 2) 1010: Vertical Active Starting Line recorded with a. Min Vertical Active Starting Line (Results 1 & 0) b. Max Vertical Active Starting Line (Results 3 & 2) 1011: Vertical Active Ending Line recorded with a. Min Vertical Active Ending Line (Results 1 & 0) b. Max Vertical Active Ending Line (Results 3 & 2) 1100: Horizontal counter value when buffer read pointer starts to toggle. (Results 1 & 0) 1101: Luminance values. Minimum luminance (Result 0) Maximum luminance (Result 1) Average luminance (Result2) 1110: VSYNC Period measured with 27 MHz clock (Result 2, 1 & 0).	0000
	3 - 2	R/W	Field Selection for Input Measurement 00: Odd field only 01: Even field only 1x: Disregard field	00
	1	R/W	Reserved.	0
	0	R/W	STARTM Start Input Measurement. This bit is self-cleared after the measurement is done.	0
Address	Bit	R/W	Description	Reset
0x05C	7	R/W	0: Use FPCLK for input HSYNC period measurement. 1: Use 27MHz clock for input HSYNC period measurement.	0
	6 - 4	R/W	Noise mask bits for each of the 3 LSB input signals.	000
	3 - 1	R/W	Error Tolerance before asserting "Change Detected" status 000: Exact match 001: Up to 4 counts 0 10: Up to 8 counts 011: Up to 16 counts 100: Up to 32 counts 101: Up to 64 counts 110: Up to 128 counts 111: Up to 256 counts.	000
	0	R/W	ENDET Enable Input VSYNC, HSYNC Period Change/Loss Detection. When this bit is set, the internal circuitry will perform new measurements. The new results are compared against the results retained in the registers obtained by the most recent measurement.	0
Address	Bit	R/W	Description	Reset
0x05D	7 - 4	R/W	Threshold value for input active region detection. Each increment increases the threshold value by 16.	0011
	3	R/W	1:Enable luminance measurement.	0
	2 - 1	R/W	Noise filter selection for luminance measurement.	00
	0	R/W	Reserved.	0

0x060 to 0x06B – Zoom Control Registers

Address	Bit	R/W	Description	Reset
0x060	7 - 0	R/W	Horizontal (X-Direction) Scale Up Factor – Higher Fraction Byte (Coarse adjustment) 65536 * (Input Horizontal Active Pixel Number) / (Flat Panel Horizontal Active Pixel Number) Example: VGA 640x480 , Panel Resolution: 1024x768 65536 * 640 / 1024 = 40960 = 0A000h Example: Decoder 720x240, Panel Resolution: 1024x768 65536 * 720 / 1024 = 46080 = 0B400h	1011 0100
Address	Bit	R/W	Description	Reset
0x061	7 - 0	R/W	Horizontal (X-Direction) Scale Down Factor - Fraction Byte 128 * (Input Horizontal Active Pixel Number) / (Flat Panel Horizontal Active Pixel Number) Example: Decoder 720x240, Panel Resolution: 640x480 128 * 720 / 640 = 144 = 090h	1000 0000
Address	Bit	R/W	Description	Reset
0x062	7 - 0	R/W	Vertical (Y-Direction) Scale Up Factor – Higher Fraction Byte (Coarse adjustment) 65536 * (Input Vertical Active Pixel Number) / (Flat Panel Vertical Active Pixel Number) Example: VGA 640x480 , Panel Resolution: 1024x768 65536 * 480 / 768 = 40960 = 0A000h Example: Decoder 720x240, Panel Resolution: 1024x768 65536 * 240 / 768 = 20480 = 05000h	0101 0000
Address	Bit	R/W	Description	Reset
0x063	7	R/W	1: Enable Panorama / Water-glass scaling.	0
	6 - 5	R/W	Reserved.	00
	4	R/W	Set Zoom by-pass. When this bit is set, the Horizontal and Vertical scale up factors has no effects.	0
	3 - 2	R/W	Integer portion of Vertical (Y-Direction) Scale factor (Total 18 bits). For vertical scale up, maximum value is 0x10000. For vertical Y-direction scale down, the value should be larger than 0x100. Vertical Scale Factor < 0x10000 : Up scaling Vertical Scale Factor = 0x10000 : No scaling Vertical Scale Factor > 0x10000 : Down scaling The max vertical down scaling factor that the scaler can handle is 0x20000.	00
	1	R/W	Horizontal (X-Direction) Scale Down Factor – Integer portion bit (Total of 9 bits)	0
	0	R/W	Horizontal (X-Direction) Scale Up Factor – Integer portion bit (Total 17 bits)	0
Address	Bit	R/W	Description	Reset
0x064	7 - 0	R/W	Horizontal (X-Direction) Scale Up Offset This offset is used to adjust the initial value for the X-Direction scale up operation.	0000 0000
Address	Bit	R/W	Description	Reset
0x065	7 - 0	R/W	Vertical (Y-Direction) Scale Up Offset for Odd field This offset is used to adjust the initial value for the Y-Direction scale up operation.	1000 0000
Address	Bit	R/W	Description	Reset
0x066	7 - 0	R/W	Horizontal non-display pixel number applied to both left and right sides. This is useful when displaying 4:3 image on wide screen 16:9 panel. Example: A wide screen panel with 1024 horizontal pixels. If this register has a value of 100, the active horizontal display will be 824 pixels. Each side is "blacked" out by 100 pixels. This register also serves as the panorama horizontal width definition.	0000 0000
Address	Bit	R/W	Description	Reset
0x067	7	R/W	1: Non-display left/right independent control.. Use 0x66,67[1:0] only for left and use 0x6C,67[5:4] for right, 0:Use 0x66,67[1:0] for both left and right.	0
	5 - 4	R/W	Thnd2[9:8] Non display width for right side (MSB)	00
	3 - 2	R/W	Reserved	-
	1 - 0	R/W	High 2 bits of 0x066 register.	00

Address	Bit	R/W	Description	Reset
0x068	7 - 0	R/W	Horizontal scale at the side of display in panorama scaling mode.	0000 0000
Address	Bit	R/W	Description	Reset
0x069	7 - 0	R/W	Horizontal (X-Direction) Scale Up Factor – Lower Fraction Byte (Fine adjustment)	0000 0000
Address	Bit	R/W	Description	Reset
0x06A	7 - 0	R/W	Vertical (Y-Direction) Scale Up Factor – Lower Fraction Byte (Fine adjustment)	0000 0000
Address	Bit	R/W	Description	Reset
0x06B	7 - 0	R/W	Vertical (Y-Direction) Scale Up Offset for Even field	0000 0000
Address	Bit	R/W	Description	Reset
0x06C	7 - 0	R/W	Thnd2[7:0] Non display width for right side (LSB)	0000 0000
Address	Bit	R/W	Description	Reset
0x06D	7 - 6	R/W	Reserved	-
	5 - 0	R/W	Top (or both Top and Bottom) line number to be masked	00 0000
Address	Bit	R/W	Description	Reset
0x06E	7	R/W	1: Top/Bottom masking independent control enable. (0x6E[5:0] is active and 0x6D only controls top), 0: 0x6D controls both top and bottom [Default]	0
	6	R/W	Reserved	-
	5 - 0	R/W	Bottom line number to be masked.	00 0000

0x070 to 0x07B – Image Adjustment Registers

Address	Bit	R/W	Description	Reset
0x070	7	R/W	Reserved.	0
	6	R/W	There are 2 sets of registers for index 71 ~ 76. 0: Select the 1st set, R/G/B Contrast and R Brightness 1: Select the 2nd set, Y/Cb/Cr Contrast and Y Brightness	0
	5 - 0	R/W	Hue Adjustment for Digital Input Port. These bits control the color hue. The range is +45 degrees to –45 degrees in 1.4 degree increments. 0 degrees is the default (xx10 0000)	10 0000
Address	Bit	R/W	Description	Reset
0x071	7 - 0	R/W	Red (or Y) Contrast Adjustment for all input sources 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x072	7 - 0	R/W	Green (or Cb) Contrast Adjustment for all input sources 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x073	7 - 0	R/W	Blue (or Cr) Contrast Adjustment for all input sources 80h+ : Higher contrast, 80h: Neutral, 80h-: Lower contrast	1000 0000
Address	Bit	R/W	Description	Reset
0x074	7 - 0	R/W	Red (or Y) Brightness Adjustment for all input sources 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x075	7 - 0	R/W	Green Brightness Adjustment for all input sources 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x076	7 - 0	R/W	Blue Brightness Adjustment for all input sources 80h+ : Higher brightness, 80h: Neutral, 80h-: Lower brightness	1000 0000
Address	Bit	R/W	Description	Reset
0x077	7 - 4	R/W	Coring function for peaking control.	0011
	3 - 0	R/W	Peaking adjustment	1111
Address	Bit	R/W	Description	Reset
0x078	7	R/W	Sharpness frequency select. 0 = Low freq. 1 = High freq.	0
	6	R/W	Reserved.	-
	5 - 4	R/W	YNR.	00
	3 - 0	R/W	Sharpness adjustment.	1010
Address	Bit	R/W	Description	Reset
0x079	7 - 4	R/W	Reserved.	-
	3	R/W	Reserved.	-
	2 - 0	R/W	Reserved.	-
Address	Bit	R/W	Description	Reset
0x07A	7 - 0	R/W	Reserved.	-
Address	Bit	R/W	Description	Reset
0x07B	7 - 4	R/W	Reserved.	-
	3 - 0	R/W	Reserved	0100

0x07C to 0x08B – Black/White Stretch Adjustment Registers

Address	Bit	R/W	Description	Reset
0x07C	7	R/W	1: BW stretch test.	0
	6	R/W	1: Use histogram information.	0
	5	R/W	Black level selection. 0: 0 1: 16	0
	4	R/W	White level selection. 0: 235 1: 255	1
	3	R/W	Black stretch limit. 1: Stretch regardless of black level, 0: Limit stretch up to black level	1
	2	R/W	White stretch limit. 1: Stretch regardless of white level, 0: Limit stretch up to white level	1
	1	R/W	1: Bypass BW stretch and peaking 0: Normal	0
	0	R/W	1: BW stretch enable, 0: Disable.	0
Address	Bit	R/W	Description	Reset
0x07D	7 - 0	R/W	Y Min/Max detection window start line, lower 8 bits (total 10 bits).	0000 1000
Address	Bit	R/W	Description	Reset
0x07E	7 - 0	R/W	Y Min/Max detection window line end, lower 8 bits (total 10 bits).	1111 0110
Address	Bit	R/W	Description	Reset
0x07F	7 - 4	R/W	Reserved.	0000
	3 - 2	R/W	Y Min/Max detection window line end, upper 2 bits.	10
	1 - 0	R/W	Y Min/Max detection window start line, upper 2 bits.	00
Address	Bit	R/W	Description	Reset
0x080	7 - 0	R/W	BWHDLY, Y Min/Max detection window H margin from Start/End pixel of HACTIVE.	0001 0000
Address	Bit	R/W	Description	Reset
0x081	7 - 6	R/W	Reserved	00
	5 - 0	R/W	Y Min/Max Horizontal filter gain.	00 1101
Address	Bit	R/W	Description	Reset
0x082	7 - 6	R/W	Reserved	00
	5 - 0	R/W	Y Min/Max Vertical filter gain.	00 0011
Address	Bit	R/W	Description	Reset
0x083	7 - 0	R/W	Minimum required Y difference for BW stretch. If Ymax – Ymin is smaller than this value, BW stretch will turned off.	0000 0000
Address	Bit	R/W	Description	Reset
0x084	7 - 0	R/W	Tilt point for black stretch.	0110 0111
Address	Bit	R/W	Description	Reset
0x085	7 - 0	R/W	Tilt point for white stretch.	1001 0100
Address	Bit	R/W	Description	Reset
0x086	7 - 0	R/W	Maximum Ymin for Black stretch. If Ymin is bigger than this value, Black stretch will turned off.	0001 1000
Address	Bit	R/W	Description	Reset
0x087	7 - 0	R/W	Minimum Ymax for White stretch. If Ymax is smaller than this value, White stretch will turned off.	1110 1000
Address	Bit	R/W	Description	Reset
0x088	7	R/W	1: Adjust White stretch gain for smoother transient. 0: No adjustment.	1
	6	R/W	1: Adjust Black stretch gain for smoother transient. 0: No adjustment.	1
	5	R/W	Reserved.	0
	4 - 0	R/W	Reserved.	0 1010
Address	Bit	R/W	Description	Reset
0x089	7	R/W	Reserved.	0
	6 - 0	R/W	Black/White Stretch Field recursive filter gain.	000 0010
Address	Bit	R/W	Description	Reset
0x08A	7 - 5	R/W	Reserved.	000
	4 - 0	R/W	Reserved.	0 1010

Address	Bit	R/W	Description	Reset
0x08B	7 - 5	R/W	Reserved.	000
	4 - 0	R/W	Reserved.	0 0100

0x092 to 0x09D – OSD Control Registers

Address	Bit	R/W	Description	Reset
0x092	3 - 0	R/W	Reserved for test.	0110
Address	Bit	R/W	Description	Reset
0x094	7	R/W	Font RAM select 0 : Font ROM 1: Font RAM	0
	6	R/W	1: Character Italic effect enable.	0
	5	R/W	1: Character Underline effect enable.	0
	4	R/W	Reserved for Character Bordering/Shadowing effect enable.	0
	3 - 2	R/W	OSD RAM Auto Increase of Write Address Mode Selection. 00: Normal mode 01: Font Data or Attribute Address auto mode 11: Font Data auto mode(Previous Attribute data automatic write)	00
	1	R/W	OSD RAM Auto Clear Mode	0
	0	R/W	Font/OSD RAM Serial Bus Access 0: OSD RAM 1: Font RAM access	0
Address	Bit	R/W	Description	Reset
0x095	7	R	For every end of window 1 active, this signal is toggled.	-
	6	R	For every end of active window, this signal is toggled.	-
	5	R/W	1: Enable character horizontal extension.	0
	4	R/W	Register 097h, 098h Read mode selection. 0 : Normal display 1: QVGA display	0
	3 - 0	R/W	Reserved.	0000
Address	Bit	R/W	Description	Reset
0x096	7 - 0	R/W	OSD RAM Address (word address for single byte access).	0000 0000
Address	Bit	R/W	Description	Reset
0x097	7 - 0	R/W	OSD RAM Data Port Hi (Font Data).	-
Address	Bit	R/W	Description	Reset
0x098	7 - 0	R/W	OSD RAM Data Port Lo (Font Attribute).	-
Address	Bit	R/W	Description	Reset
0x099	7 - 0	R/W	Serial Bus Font RAM Address.	0000 0000
Address	Bit	R/W	Description	Reset
0x09A	7 - 0	R/W	Serial Bus Font RAM Data Port.	-
Address	Bit	R/W	Description	Reset
0x09B	7 - 0	R/W	Programmable SRAM address start position for Multi-Color fonts.	0011 0001
Address	Bit	R/W	Description	Reset
0x09C	7	R/W	When set, the content of OSD RAM bit16 is read out from bit 7 of index 094.	0
	6 - 5	R/W	Reserved.	000
	4	R/W	OSD ON/OFF Enable Control 0: OSD ON, 1: OSD OFF	0
	3 - 0	R/W	Character color look up table write address select.	0000
Address	Bit	R/W	Description	Reset
0x09D	7 - 0	R/W	Character color look up table data port.	00h

0x09E to 0x0AE – OSD Window Control Registers

Address	Bit	R/W	Description	Reset
0x09E	7 - 4	R/W	Window alpha blending color selection.	0000
	3 - 2	R/W	Reserved.	00
	1 - 0	R/W	Window selection (Window #n).	00
Address	Bit	R/W	Description	Reset
0x09F	7	R/W	OSD Window #n Background Color Look-up Table selection.	0
	6 - 4	R/W	OSD Window #n Background Color control (Register setting flow for OSD : step_3). 000 : Black 001 : Blue 010 : Green 011 : Cyan 100 : Red 101 : Magenta 110 : Yellow 111 : White	000
	3	R/W	OSD Window #n 3-D effect top/bottom toggle.	0
	2	R/W	OSD Window #n 3-D effect enable.	0
	1	R/W	OSD Window #n 3-D effect Level Control.	0
	0	R/W	OSD Window #n Enable.	0
Address	Bit	R/W	Description	Reset
0x0A0	7 - 6	R/W	Reserved.	00
	5 - 4	R/W	OSD Window #n V-Start Location High 2 bits (total 10 bits).	00
	3	R/W	Reserved.	0
	2 - 0	R/W	OSD Window #n H-Start Location High 3 bits (total 11 bits).	000
Address	Bit	R/W	Description	Reset
0x0A1	7 - 0	R/W	OSD Window #n H-Start Location Low 8-bit (1 pixels per step).	0000 0000
Address	Bit	R/W	Description	Reset
0x0A2	7 - 0	R/W	OSD Window #n V-Start Location Low 8-bit (1 scan lines per step).	0000 0000
Address	Bit	R/W	Description	Reset
0x0A3	7 - 6	R/W	Reserved.	00
	5 - 0	R/W	OSD Window #n H-Width (1 Character width per step).	00 0000
Address	Bit	R/W	Description	Reset
0x0A4	7 - 6	R/W	Reserved.	00
	5 - 0	R/W	OSD Window #n V-Height (1 Character height per step).	00 0000
Address	Bit	R/W	Description	Reset
0x0A5	7	R/W	OSD Window #n Border Color Enable.	0
	6 - 4	R/W	OSD Window #n Border Color control.	000
	3 - 0	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step).	0000
Address	Bit	R/W	Description	Reset
0x0A6	7	R/W	OSD Window #n Border Color Look-up Table Selection Bit.	0
	6 - 0	R/W	OSD Window #n H-Border Width (1 pixel per step).	000 0000
Address	Bit	R/W	Description	Reset
0x0A7	7	R/W	Reserved	0
	6 - 0	R/W	OSD Window #n V-Border Width (1 scan line per step).	000 0000
Address	Bit	R/W	Description	Reset
0x0A8	7 - 4	R/W	Character V-Space inside Window #n (1 scan line per step).	0000
	3 - 0	R/W	Character H-Space inside Window #n (1 pixel per step)	0000
Address	Bit	R/W	Description	Reset
0x0A9	7 - 6	R/W	OSD Window #n Vertical Zoom. 00: no zoom, 01: x2, 10: x3, 11: x4	00
	5 - 4	R/W	OSD Window #n Horizontal Zoom. 00: no zoom, 01: x2, 10: x3, 11: x4	00
	3 - 0	R/W	Reserved.	0000
Address	Bit	R/W	Description	Reset
0x0AA	7 - 0	R/W	OSD Display RAM starting address (low byte) of OSD Window #n.	0000 0000

Address	Bit	R/W	Description	Reset
0x0AB	7	R/W	OSD Window #n shadow enable.	0
	6 - 4	R/W	OSD Window #n shadow color control.	000
	3 - 0	R/W	OSD Window #n shadow width.	0000
Address	Bit	R/W	Description	Reset
0x0AC	7 - 4	R/W	Reserved.	0000
	3 - 0	R/W	OSD Window #n alpha blending amount.	0000
Address	Bit	R/W	Description	Reset
0x0AD	7	R/W	OSD Window #n shadow Color Look-up Table Selection.	0
	6	R/W	1: OSD Window #n multicolor font enable.	0
	5	R/W	1: Character vertical extension enable.	0
	4	R/W	Character Border/Shadow selection. 1: Shadow 0: Border	0
	3	R/W	OSD Window #n character border/shadow color Look-up Table Selection	0
	2 - 0	R/W	OSD Window #n character border/shadow color Control	000
Address	Bit	R/W	Description	Reset
0x0AE	7 - 4	R/W	Reserved.	0000
	3	R/W	Character V-Space inside Window #n (1 scan line per step) MSB bit.	0
	2	R/W	Character H-Space inside Window #n (1 pixel per step) MSB bit.	0
	1	R/W	OSD Window #n shadow width MSB bit.	0
	0	R/W	OSD Window #n Border Color Width (1 pixel or scan line per step) MSB bit.	0

0x0B0 to 0x0C6 – PANEL CONTROL

Address	Bit	R/W	Description	Reset
0x0B0	7	R/W	Reserved	0
	6	R/W	Set pin FPDE Active High 0: Active Low	1
	5	R/W	Set pin FPHS Active High 0: Active Low	0
	4	R/W	Set pin FPVS Active High 0: Active High	0
	3	R/W	Invert pin FPCLK polarity 0: Output signals to flat panel (FPVS, FPHS, … etc.) are referenced to the falling edge of FPCLK.	0
	2	R/W	Delta_n	0
	1	R/W	Reverse the bit order on panel data bus. 0: MSB is on FPR[7], FPG[7], FPB[7]. 1: MSB is on FPR[0], FPG[0], FPB[0].	0
	0	R/W	Swapping Red and Blue data bus 0 : No swapping 1 : Data bus swapping red and blue	0
Address	Bit	R/W	Description	Reset
0x0B1	7	R/W	TCON Mode select 1: All of the panel output pins assign to TCON interface signals. ** Refer Timing Controller shared pin description after pin description	00
	6	R/W	Set this bit to 1 making FPCLK become inactive during vertical blanking time.	0
	5	R/W	DE mode selection. 1: FPVS and FPHS are forced to inactive state.	0
	4	R/W	FP data outputs shift down 2 bits. When set, FPR0, FPR1, FPG0, FPG1, FPB0, FPB1 bus signals are shifted down by 2 bits.	0
	3	R/W	Tri-state all the output signals to flat panel.	0
	2 - 0	R/W	Panel clock FPCLK delay time selection. 000: No delay time inserted. Each increment increases the delay by 1 ns.	000
Address	Bit	R/W	Description	Reset
0x0B2	7 - 0	R/W	FPHS Period - Low Byte	0011 1010
Address	Bit	R/W	Description	Reset
0x0B3	7 - 0	R/W	FPHS Active Pulse Width This register is usually filled in with the minimum FPHS pulse width requirement from the flat panel specification	0001 0000
Address	Bit	R/W	Description	Reset
0x0B4	7 - 0	R/W	Flat Panel Horizontal Back Porch Width --- The duration from the trailing edge of FPHS to the leading edge of FPDE. This register is usually filled in with the minimum horizontal back porch requirement from the flat panel specification.	0001 1011
Address	Bit	R/W	Description	Reset
0x0B5	7 - 0	R/W	FPDE Horizontal Active Length	0000 0000

Address	Bit	R/W	Description	Reset
0x0B6	7	R/W	When this bit is set, the internal circuitry uses the programmed value of index B6[3:0] and index B2[7:0] as the FPHS period disregarding the setting of "Auto Calculation", bit 1 of index BE.	0
	6 - 4	R/W	FPDE Horizontal Active Length – High three bits (Total 11 bits) This horizontal active length is equivalent to the panel horizontal resolution. For example, the horizontal resolution of an XGA panel is 1024.	100
	3 - 0	R/W	FPHS Period – High three bits (Total 12 bits) The following formula gives the correct number to fill in for FPHS period. FPHS_Period = *F*_pllcki / (*F*_ihsync * VSUR) Where *F*_pllcki is the frequency of EXTCLK, *F*_ihsync is the frequency of input HSYNC, and VSUR is the vertical scale up ratio. VSUR = (Panel Vertical Resolution) / (Input Vertical Resolution) Example: Input is VGA with HSYNC frequency 31.5KHz with 60 Hz refresh rate to be displayed on an XGA panel. VSUR = 768/480 = 1.6 Choose *F*_pllcki = 69 MHz FPHS_Period = 69000000 / (31500 * 1.6) = 1369.05 → 1369 = 559h	0010
Note: The unit for Index B2 through B6 is one panel pixel clock, which is either the output of internal PLL or EXTCLK. The FPHS Period should be larger than the sum of 1) FPHS Active Pulse Width, 2) FPHS Back Porch Width, and 3) FPDE Horizontal Active Length.				
Address	Bit	R/W	Description	Reset
0x0B7	7 - 0	R/W	FPVS Period - Low Byte	0010 0110
Address	Bit	R/W	Description	Reset
0x0B8	7 - 0	R/W	FPVS Active Pulse Width The unit of this pulse width is one FPHS. This register is usually filled in with the minimum FPVS pulse width requirement from the flat panel specification.	0000 0110
Address	Bit	R/W	Description	Reset
0x0B9	7 - 0	R/W	Flat Panel Vertical Back Porch Width The unit of this pulse width is one FPHS. The following formula gives the correct number to fill in for FPVS back porch. FPVS_Back_Porch = (VAS–VSYNC_pw+2)* VSUR–FPVS_Pulse_Width Where VAS is the input Vertical active starting line number, VSYNC_pw is the input VSYNC pulse width, VSUR is the Vertical Scale Up ratio. VSUR = (Panel Vertical Resolution) / (Input Vertical Resolution)	0001 1111
Address	Bit	R/W	Description	Reset
0x0BA	7 - 0	R/W	Flat Panel Vertical Active Length - Low Byte	0000 0000
Address	Bit	R/W	Description	Reset
0x0BB	7	R/W	Early start. Start to output data earlier in non auto calculation mode.	0
	6 - 4	R/W	Flat Panel Vertical Active Length - High three bits (Total 11 bits) The unit of this active length is one FPHS This vertical active length is equivalent to the panel vertical resolution. For example, the vertical resolution of an XGA panel is 768.	011
	3	R/W	This bit is for internal used.	0
	2 - 0	R/W	FPVS Period – High three bits (Total 11 bits) The unit of this period is one FPHS.	011
Note: The unit for Index B7 through BB is one FPHS, i.e. whenever there is an active FPHS, the count is incremented by 1. The FPVS Period should be larger than the sum of 1) FPVS Active Pulse Width, 2) FPVS Back Porch Width, and 3) Flat Panel Vertical Active Length.				
Note: The value written in this register does not come into effect until it is followed by a register write to index 0x0B7 or 0x0BA.				

Address	Bit	R/W	Description	Reset
0x0BC	7	R/W	This is pixel double function for vertical scaling. Enable this bit, the horizontal scaling ratio register value must set exactly two times. 0 : Disable, 1 : Enable	0
	6 - 4	R/W	Dither Option Code "010" is recommended for 6:6:6 output	000
	3	R/W	This is line double function for vertical scaling. Enable this bit, the vertical scaling ratio register value must set exactly two times. 0 : Disable, 1 : Enable	0
	2 - 0	R/W	Dither Output Format Selection "001" is recommended for 6:6:6 output	000

Table 6 Dither Output Selection and Calculations

Dither Output Format Selection	Flat Panel RGB Bit Format Output	Dither Option Code	Input LSBs Used in Dither Calculation	Dither Method
000	8:8:8	xxx	n/a	none
001	6:6:6	001	(1) (1) (1)	2x2
		010	(1,0) (1,0)	2x2
010	5:6:5	001	(2) (1) (2)	2x2
		010	(2,1) (1,0) (2,1)	2x2
		011	(2,1,0) (1,0) (2,1,0)	2x2
011	5:5:5	001	(2) (2) (2)	2x2
		010	(2,1) (2,1) (2,1)	2x2
		011	(2,1,0) (2,1,0) (2,1,0)	2x2
100	4:4:4	001	(3) (3) (3)	2x2
		010	(3,2) (3,2) (3,2)	2x2
		011	(3,2,1) (3,2,1) (3,2,1)	2x2
		100	(3,2,1,0) (3,2,1,0) (3,2,1,0)	4x4
101	3:3:3	001	(4) (4) (4)	2x2
		010	(4,3) (4,3) (4,3)	2x2
		011	(4,3,2) (4,3,2) (4,3,2)	2x2
		100	(4,3,2,1) (4,3,2,1) (4,3,2,1)	4x4
110	3:3:2	001	(4) (4) (5)	2x2
		010	(4,3) (4,3) (5,4)	2x2
		011	(4,3,2) (4,3,2) (5,4,3)	2x2
		100	(4,3,2,1) (4,3,2,1) (5,4,3,2)	4x4

Address	Bit	R/W	Description	Reset
0x0BD	7 - 0	R/W	Output Vsync delay from Input Vsync	0000 1000
Address	Bit	R/W	Description	Reset
0x0BE	7	R/W	Force long. In auto calculation with this bit set, the FPHS period assumes the next higher integer value if the calculated FPHS contains fractional part.	0
	6	R/W	Force short. In auto calculation with is bit set, the FPHS period assumes the integer part; i.e. the fractional part of the calculated FPHS period is discarded.	0
	5	R/W	Tri-State PWM pin.	0
	4	R/W	PWM polarity. 1: Active low	0
	3	R/W	When set, the input “HACTIVE” or “DE” is forced to inactive if either VSYNC or HSYNC is active.	0
	2	R/W	Force into free run mode.	0
	1	R/W	Enable auto calculation. When this bit is set, an internal circuitry calculates the optimum FPHS period, and then adjusts the FPHS period dynamically so that for one vsync (FPVS) period it has integer multiples of FPHS. The internal circuitry also adjust the FPHS active position to minimize the line buffer overflow/underflow.	0
	0	R/W	When this bit is set, the input VSYNC is delayed by the amount specified by index 0xBD in the unit of input HSYNC. The regular meaning of index 0xBD -- “Output VSYNC delay from Input VSYNC” is fixed at 2.	0

Address	Bit	R/W	Description	Reset
0x0BF	7 - 6	R/W	Display single field on flat panel. 0x : Function disabled. 10 : Display odd field. 11 : Display even field.	00
	5	R/W	When set the field signal is reversed in the auto calculation circuitry.	0
	4	R/W	Select different vertical sync source in single field input.	0
	3	R/W	No even field initialization	0
	2 - 0	R/W	Even field delay. 001= +1, 010= +2, … 101= +5, 110= -1, 111= -2	000
Address	Bit	R/W	Description	Reset
0x0C0	7 - 0	R/W	Bits 8 to 1 of 13 bit counter – C2(3-0), C0(7-0)	0000 0000
Address	Bit	R/W	Description	Reset
0x0C1	7 - 0	R/W	Bits 8 to 1 of 13 bit counter – C2(7-4), C1(7-0)	0000 0000
Address	Bit	R/W	Description	Reset
0x0C2	7 - 4	R/W	Upper 4 bits (bits 13 to 9) of 13 bit counter – C2(7-4), C1(7-0) For non-Free-Run mode, this specifies the upper 12-bits of the initial value of a 13-bit counter for the even field. For Free-Run with Calibrate bit set, this specifies the value for the vertical line counter to load at the falling edge of input VSYNC.	0000
	3 - 0	R/W	Upper 4 bits (bits 13 to 9) of 13 bit counter – C2(3-0), C0(7-0) For non-Free-Run mode, this specifies the upper 12-bits of the initial value of a 13-bit counter for the odd field. For Free-Run with Calibrate bit set, this specifies the value for pixel counter to load at the falling edge of input VSYNC.	0000
Address	Bit	R/W	Description	Reset
0x0C3	7 - 6	R/W	Even field vertical start point adjustment. 00 : Even field start with the same line count specified in 0x as odd field. 01 : Even field start with one extra line count specified in 0xC1. 10 : Even field start with one less line count specified in 0xC1.	00
	5 - 0	R/W	Reserved	00 0000
Address	Bit	R/W	Description	Reset
0x0C4	7	R/W	PWM clock selection 0: 27 MHz (XTAL27I input frequency) / 128 1:(27/2MHz) / 128	0
	6 - 0	R/W	Positive pulse width of the PWM. If this register has an “N” value, the positive pulse width duration is “N+1” PWM clocks.	100 0000
Address	Bit	R/W	Description	Reset
0x0C5	7-0	R/W	Reserved	00h
Address	Bit	R/W	Description	Reset
0x0C6	7-0	R/W	Reserved	00h

Low Speed ADC and MCU control Registers

0x0C8 to 0x0CA – LADC and MCU Control Registers

Address	Bit	R/W	Description	Reset
0x0C8	7 - 6	R/W	Reserved.	00
	5	R/W	MCU Debug Mode control bit	0
	4	R/W	LADC_PD_CMP control bit	0
	3	R/W	LADC_PD control bit	0
	2 - 0	R/W	Higher 3 bits of LADC Clock divide value. DIV Value = { 0X0C8[2:0], 1001}. Default LADC clock frequency = 27/ 9 = 3 MHZ	000
Address	Bit	R/W	Description	Reset
0x0C9	7 - 0	R/W	LADC Channel 0 Input Value	0
Address	Bit	R/W	Description	Reset
0x0CA	7 - 0	R/W	LADC Channel 1 Input Value	0

0x0D0 to 0x0D3 – Status and Interrupt Registers

Address	Bit	R/W	Name	Description	Reset
0x0D0	7	R	Line buffer over flow	This bit is set if the FP clock count exceeds the maximum number in between two consecutive FPHS pulses for the even field, cleared by writing back a "1".	-
	6	R	Line buffer under flow	This bit is set if the FP clock count exceeds the maximum number in between two consecutive FPHS pulses for the odd field, cleared by writing back a "1".	-
	5	R	Input VSYNC Loss status changed	This bit is set when the status bit of "Input VSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	-
	4	R	Input HSYNC Loss status changed	This bit is set when the status bit of "Input HSYNC Loss" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	-
	3	R/W	Video input status changed indication	Vdloss status bit change (register 1 bit 7) or det50 status bit change (register 1 bit 0) Write a one to this bit to reset.	0
	2	R	Input VSYNC Loss	This bit is set when the input VSYNC pulse is lost, reset by re-appearance of VSYNC. An 11-bit counter is used for VSYNC period measurement. If this counter overflows 4 times, the VSYNC is considered to be lost.	-
	1	R	Input HSYNC Loss	This bit is set when the input HSYNC pulse is lost, reset by re-appearance of HSYNC. An 11-bit counter is used for HSYNC period measurement. If this counter overflows 4 times, the HSYNC is considered to be lost.	-
	0	R	SYNC detect status	Logic function of: Inverted "bit 1" ANDing with inverted "bit 2"	-
Address	Bit	R/W	Name	Description	Reset
0x0D1	7	R	Input Measurement Data Ready	This bit is set when the measurement data is ready for readout, reset when a new "startm" is set.	-
	6	R	Power State Changed	This bit is set when the power management state has changed, reset by writing back a "1".	-
	5	R	Input VSYNC Period Change Detected	This bit is set when the input VSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the VSYNC period is measured for every frame. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the VSYNC period is considered to have changed.	-

Address	Bit	R/W	Name	Description	Reset
	4	R	Input HSYNC Period Change Detected	This bit is set when the input HSYNC period is changed, reset when "endet" is cleared. When "endet" bit is set, the HSYNC period is measured for every scan line. If the difference from the last measurement result stored in the registers, is larger than the error tolerance, the HSYNC period is considered to have changed.	-
	3	R	Line buffer Overflow or Underflow		-
	2	R	VDCCDET	High if there is a change in VDLOSS or DET50 or CCVALID	-
	1	R	VLOSS/ HLOSS status changed	This bit reflects the “OR” condition of status bit index B0 bit 5 (VLOSS status changed) and index 0x0D0 bit 4 (HLOSS status changed).	-
	0	R	"SYNC Detect Status" Changed	This bit is set when the status bit of "SYNC Detect Status" had changed, either 1 to 0 or 0 to 1. This bit is cleared by writing back a "1", or by resetting the "endet" bit.	-
Address	Bit	R/W	Description		Reset
0x0D2	7	R/W	Enable/Disable 0x0D1 bit 7 as an IRQ source 0: Enable 1: Disable		1
	6	R/W	Enable/Disable 0x0D1 bit 6 as an IRQ source 0: Enable 1: Disable		1
	5	R/W	Enable/Disable 0XD1 bit 5 as an IRQ source 0: Enable 1: Disable		1
	4	R/W	Enable/Disable 0XD1 bit 4 as an IRQ source 0: Enable 1: Disable		1
	3	R/W	Enable/Disable 0XD1 bit 3 as an IRQ source 0: Enable 1: Disable		1
	2	R/W	Enable/Disable 0XD1 bit 2 as an IRQ source 0: Enable 1: Disable		1
	1	R/W	Enable/Disable 0XD1 bit 1 as an IRQ source 0: Enable 1: Disable		1
	0	R/W	Enable/Disable 0XD1 bit 0 as an IRQ source 0: Enable 1: Disable		1
Address	Bit	R/W	Description		Reset
0x0D3	7	R/W	IRQ out enable 1: output enable, 0: output disable * In MCU Mode, This bit should be “1” to use pin #83 as a mcu output port.		0
	6-3	R/W	Reserved.		0
	2-0	R/W	Reserved.		1

0x0D4 to 0x0D8 – Power Management Registers

Address	Bit	R/W	Description	Reset
0x0D4	7-0	R/W	MSB of an internal 23 bit divide down counter. The 27 MHz clock from XTAL27I is divided by this counter to serve as the clock for the Power State Transition timer.	0000 0000
Address	Bit	R/W	Description	Reset
0x0D5	7	R/W	Force the internal PCLK to "0".	0
	6	R/W	Power sequence reference source selection. 0 : 27MHz 1 : VSYNC	0
	5-4	R	Show current power management state. These power states determine the states of pins FPPWC, FPBIAS & FP interface signals which includes FPVS, FPHS, FPDE, FPCLK and all data signals. FPPWC FPBIAS FP Interface Signals 00: Off "0" "0" "0" 01: Standby "1" "0" "0" 10: Suspend "1" "0" "1" or "0" 11: On "1" "1" "1" or "0" The transition between the power states does not occur right away. It takes place after the timer expiration by the corresponding timer counts defined in 0xD6-0xD8.	00
	3	R/W	Manual power sequencing control. When this bit is set, bits [2:0] control FPBIAS, FP Interface Signals, and FPPWC directly.	0
	2	R/W	If bit 3 is "0" and this bit is "1", this enable auto power sequencing. VSYNC loss & HSYNC loss ---> Off VSYNC loss & HSYNC active ---> Standby VSYNC active & HSYNC loss ---> Suspend VSYNC active & HSYNC active ---> On	0
	1-0	R/W	Power state steering. When these 2 bits are written, assuming both bit 3 and bit 2 are 0's, and the current power state is different from the value written, the power state will be sequencing to the state that matches the value written. For example, current power state is 11. A 01 value is written. The power state will be steered to "01" and stay in "01. 00: Off State, 01: Standby, 10: Suspend, 11: ON state	00
Address	Bit	R/W	Description	Reset
0x0D6	7-4	R/W	Timer Counts for Suspend State to Standby State Transition	0000
	3-0	R/W	Timer Counts for On State to Suspend State Transition	0000
Address	Bit	R/W	Description	Reset
0x0D7	7-4	R/W	Timer Counts for Power Off State to Standby State Transition	0000
	3-0	R/W	Timer Counts for Standby State to Power Off State Transition	0000
Address	Bit	R/W	Description	Reset
0x0D8	7-4	R/W	Timer Counts for Standby State to Suspend Sate Transition	0000
	3-0	R/W	Timer Counts for Suspend to On State Transition	0000

0x0DA to 0x0DF – Color Enhancement

Address	Bit	R/W	Description	Reset
0x0DA	7-0	R/W	Color Enhancement Center Color phase for color 1. The range for center color phase is –180° ~ + 180°, 2 degree per step.	3Dh
Address	Bit	R/W	Description	Reset
0xDB	7-0	R/W	Color Enhancement Center Color phase for color 2. The range for center color phase is –180° ~ + 180°, 2 degree per step.	C3h
Address	Bit	R/W	Description	Reset
0xDC	7-0	R/W	Color Enhancement Center Color phase for color 3. The range for center color phase is –180° ~ + 180°, 2 degree per step.	FCh
Address	Bit	R/W	Description	Reset
0x0DD	7	R/W	1: Color Enhancement Enable, 0: Disable	0
	6-5	R/W	Color Enhancement Gain Spread Range for color 1 00 : No enhance 01 : -8° ~ +8° of center color phase 10 : -16° ~ +16° of center color phase 11 : -32° ~ + 32° of center color phase	00
	4-0	R/W	Color Enhancement Gain for color 1. The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0000
Address	Bit	R/W	Description	Reset
0x0DE	7	R/W	Reserved	0
	6-5	R/W	Color Enhancement Gain Spread Range for color 2 00 : No enhance 01 : -8° ~ +8° of center color phase 10 : -16° ~ +16° of center color phase 11 : -32° ~ + 32° of center color phase	00
	4-0	R/W	Color Enhancement Gain for color 2 . The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0000
Address	Bit	R/W	Description	Reset
0x0DF	7	R/W	Reserved	0
	6-5	R/W	Color Enhancement Gain Spread Range for color 3 00 : No enhance 01 : -8° ~ +8° of center color phase 10 : -16° ~ +16° of center color phase 11 : -32° ~ + 32° of center color phase	00
	4-0	R/W	Color Enhancement Gain for color 3. The minimum Gain value is 00000 and maximum is 11111 from 0 to 0.484 with 31 step of 1/64.	0000

0x0E0 – Etc

ADDR	Bit	R/W	Description	Reset
0x0E0	7	R/W	Line buffer overflow/underflow status report method.	0
	6	R/W	Pixel clock counter selection for field selection for field detection circuitry.	0
	5	R/W	Reserved.	0
	4	R/W	Disable Serial Bus index address increment during multiple data write/read.	0
	3 -1	R/W	Reserved.	000
	0	R/W	Enable for write sequence register mode	0

0x0F0 – Gamma

Address	Bit	R/W	Description	Reset
0x0F0	7	R/W	Enable Red gamma correction.	0
	6	R/W	Enable Green gamma correction.	0
	5	R/W	Enable Blue gamma correction.	0
	4	R/W	Reserved.	0
	3-2	R/W	Enable Gamma table address auto increment for reading/writing Gamma data port. 00: Disable, 01: Read Only, 10: Write Only, 11: Read/Write	00
	1 - 0	R/W	Gamma tables access selection: Index address 0x0F1 to 0x0F2 are used for gamma table accesses. There are 3 sets of gamma table, one table for one color, sharing the same address port and data port. These 2 bits identifies which table is accessed. 00: RGB Gamma table 01: Red Gamma table 10: Green Gamma table 11: Blue Gamma table	00
Address	Bit	R/W	Description	Reset
0x0F1	7-0	R/W	Gamma table address port.	0000 0000
Address	Bit	R/W	Description	Reset
0x0F2	7-0	R/W	Gamma table data port.	-

0x0F6 – DAC Control

Address	Bit	R/W	Description	Reset
0x0F6	7:5	R/W	*	0000 0000
	4-0	R/W	Dac R Channel Gain	

0x0F7 – DAC Control

Address	Bit	R/W	Description	Reset
0x0F7	7:5	R/W	Reserved	0000 0000
	4-0	R/W	Dac G Channel Gain	

0x0F8 – DAC Control

Address	Bit	R/W	Description	Reset
0x0F8	7	R/W	DAC power down	0000 0000
	6	R/W	*	
	5	R/W	daciref_new	
	4-0	R/W	Dac B Channel Gain	

0x0F9 to 0x0FE – Spread Spectum Synthesizer Control Registers

Address	Bit	R/W	Description	Reset
0x0F9	7-6	R/W	Internal operating clock selection 2'h0 : SS-PLL output clock 2'h1 : 27MHz XTAL 2'h2 : EXT_CK 2'h3 : Reserved	00h
	3-0	R/W	FPLL[19:16] PLL Oscillation frequency = 108MHz * FPLL / 2 ^ 17 / 2^ POST	
Address	Bit	R/W	Description	Reset
0x0FA	7-0	R/W	FPLL[15:8]	40h
Address	Bit	R/W	Description	Reset
0x0FB	7-0	R/W	FPLL[7:0]	00h
Address	Bit	R/W	Description	Reset
0x0FC	7-0	R/W	FSS[7-0], Spread spectrum modulation frequency = 27MHz * FSS / 2^16	40h
Address	Bit	R/W	Description	Reset
0x0FD	7	R/W	PD_SSPLL, PLL power down control. 1 = Power Down	
	6-4	R/W	SSD, Spread spectrum gain divider.	30h
	3-0	R/W	SSG, Spread Spectrum gain control. The frequency deviation is controller by a center spreading sawtooth waveform. The controlling frequency is determined by FSS and its associated equation. The percentage of peak-to-peak spread or deviation of the center frequency is determined by the following equation. DEVpp = SSG * 2^8 / (FPLL * 2^SSD) * 100 %	
Address	Bit	R/W	Description	Reset
0x0FE	7-6	R/W	POST : PLL post divider 0 – 1 1 – ½ 2 – ¼ 3 – 1/8	11h
	5-4	R/W	VCO : VCO Range 00 : 13.5 ~ 27MHz, 01 : 27 ~ 54 MHz 10 : 54 ~ 108MHz, 11 : 108 ~ 216MHz	
	3	R/W		
	2-0	R/W	Charge pump currents (uA) 3'b000 : 1.5 3'b001 : 2.5 3'b010 : 5 3'b011 : 10 3'b100 : 20 3'b101 : 40 3'b110 : 80 3'b111 : 160	

0x0FF (or 0x1FF)

Address	Bit	R/W	Description	Reset
0x0FF/ 0x1FF	7-1	R/W	Reserved	00
	0	R/W	Index register page selection. 0: 0x000~0x0FE 1: 0x100 ~ 0x1FE	0

0x130 – CCFL Control I

Bit	Function	R/W	Description	Reset
7	OVEN	R/W	Over voltage feedback control 0 = disable 1 = enable	1
6	OIEN	R/W	Over current feedback control 0 = disable 1 = enable	1
5	UIEN	R/W	Under current feedback control 0 = disable 1 = enable	1
4	FBEN	R/W	CCFL feedback loop control 0 = open loop 1 = close loop	1
3	LOCKV	R/W	0 = Dimming frequency set by FDIM 1 = Dimming frequency locked to panel vertical sync.	0
2	LOCkH	R/W	0 = PWM frequency set by FPWM 1 = PWM frequency locked to panel horizontal frequency	0
1	CCFLENB	R/W	0 = CCFL analog core power down 1 = CCFL analog core power up.	1
0	CCFLDEN	R/W	0 = CCFL out disable. 1 = CCFL out enable.	0

0x131 – CCFL Threshold

Bit	Function	R/W	Description	Reset
7-6	LVT	R/W	Lamp voltage threshold	2h
5-4	LILT	R/W	Lamp low current threshold	2h
3-0	LIT	R/W	Lamp normal current threshold	Dh

0x132 – CCFL Control II

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W		00
5-4	CCFL_ST	R/W	CCFL status	-
3-0	LSTP	R/W	CCFL feedback gain control with 1 being the smallest gain.	4h

0x133 – CCFL PWM

Bit	Function	R/W	Description	Reset
7-0	FPWM	R/W	CCFL PWM control frequency	80h

0x134 – CCFL Dim Frequency

Bit	Function	R/W	Description	Reset
7-0	FDIM	R/W	CCFL dimming frequency control.	84h

0x135 – CCFL Dim Control

Bit	Function	R/W	Description	Reset
4-0	DDIM	R/W	CCFL dimming control. 0=full brightness, 1F=lowest brightness	00h

0x136 – PWMTOP

Bit	Function	R/W	Description	Reset
7-0	PWMTOP	R/W	Reserved	20h

0x140 to 0x141 – GPO

Address	Bit	R/W	Description	Reset
0x140	7	R/W	Enable for GP17	0
	6	R/W	Enable for GP16	0
	5	R/W	Enable for GP15	0
	4	R/W	Enable for GP14	0
	3	R/W	Enable for GP13	0
	2	R/W	Enable for GP12	0
	1	R/W	Enable for GP11	0
	0	R/W	Enable for GP10	0
Address	Bit	R/W	Description	Reset
0x141	7	R/W	Data for GP17	0
	6	R/W	Data for GP16	0
	5	R/W	Data for GP15	0
	4	R/W	Data for GP14	0
	3	R/W	Data for GP13	0
	2	R/W	Data for GP12	0
	1	R/W	Data for GP11	0
	0	R/W	Data for GP10	0

0X157 to 0x15A, 0x1F0 to 0x1F9 – Debug Registers

Address	Bit	R/W	Description	Reset
0x157 0x158 0x159 0x15A	7 - 0	R	These four index addresses provide real time data read out of some internal counters. The index of these counters is set by 0x05B[7:4]. Index 0x157 0x158 0x159 0x15A 0 LVPCNT_ODD[7:0] LVPCNT_ODD[15:8] LVPCNT_ODD[23:16] 1 LVPCNT_EVN[7:0] LVPCNT_EVN[15:8] LVPCNT_EVN[23:16] 2 LIVCNT_ODD[7:0] LIVCNT_ODD[11:8] 3 LIVCNT_EVN[7:0] LIVCNT_EVN[11:8] 4 LHPCNT[7:0] LHPCNT[13:8] LBOVFC[7:0] LBOVFC[10:8]	-
Address	**Bit**	**R/W**	**Description**	**Reset**
0x1F0	7 - 4	R/W	Index for simulation initialization of internal auto calculation counters. 0: VPCNT[23:0] Pixel counter for 1 VSYNC period 1: LVPCNT_ODD[23:0] Pixel counter for 1 Odd field VSYNC period 2: LVPCNT_EVN[23:0] Pixel counter for 1 Even field VSYNC period 3: IVCNT[11:0] Line counter for 1 VSYNC period 4: LIVCNT_ODD[11:0] Line counter for 1 Odd field VSYNC period 5: LIVCNT_EVN[11:0] Line counter for 1 Even field VSYNC period 6: GOCNT[23:0] Pixel counter from VSYNC to the beginning of output display 7: LGOOCNT[23:0] Pixel counter from VSYNC to the beginning of output display (odd) 8: LGOECNT[23:0] Pixel counter from VSYNC to the beginning of output display (even)	0000
	3	R/W	1: Force auto calculation to treat input as two fields.	0
	2	R/W	1: Force auto calculation to treat input as one field.	0
	1 - 0	R/W	Sub index for the above counters, providing byte wide data read/write from/to 0x1F1. 00: Bits [7:0] of the counter pointed by the index 01: Bits [15:8] of the counter pointed by the index 10: Bits [23:16] of the counter pointed by the index	00
Address	**Bit**	**R/W**	**Description**	**Reset**
0x1F1	7 - 0	R/W	Data port for those counters mentioned in index 0x1F0.	00h

Address	Bit	R/W	Description	Reset
0x1F3	7	R/W	Chip test usage only. Data output selection for analog circuit test. 0: V data 1: C data	0
	6	R/W	When set, gray scale data replace the normal data output to panel. The content of index 61 is used as the first pixel data.	0
	5	R/W	If this bit is set to "1", the scaler output is forced to all 0's.	0
	4	R/W	Reserved.	0
	3	R/W	Reserved.	0
	2	R/W	Reserved.	0
	1	R/W	Start OSD ROM self test.	0
	0	R/W	Start OSD RAM self test.	0
Address	Bit	R/W	Description	Reset
0x1F4	7 - 0	R	BWYMIN	-
Address	Bit	R/W	Description	Reset
0x1F5	7 - 0	R	BWYMAX	-
Address	Bit	R/W	Description	Reset
0x1F6	7 - 0	R	BWFMIN	-
Address	Bit	R/W	Description	Reset
0x1F7	7 - 0	R	BWFMAX	-
Address	Bit	R/W	Description	Reset
0x1F8	7 - 0	R	BWBTILT	-
Address	Bit	R/W	Description	Reset
0x1F9	7 - 0	R	BWWTILT	-

Timing Controller Configuration Registers

0x176 – GPIO Pixel Count High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	GPIX_H[11:8]	R/W	GPIX_H[11:8]	0

0x177 – GPIO Pixel Count Low Register

Bit	Function	R/W	Description	Reset
7-0	GPIX_L[7:0]	R/W	GPIX_L[7:0]	5A

0x178 – GPIO Line Count High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	GLINE_H[11:8]	R/W	GLINE_H[11:8]	0

0x179 – GPIO Line Count Low Register

Bit	Function	R/W	Description	Reset
7-0	GLINE_L[7:0]	R/W	GLINE_L[7:0]	7F

0x17A – GPIO Frame Count Register

Bit	Function	R/W	Description	Reset
7-3	Reserved	R/W	Reserved	-
2-0	GFRAME[2:0]	R/W	GFRAME[2:0]	1

0x17B – TCON and Delta RGB Misc. Control Register

Bit	Function	R/W	Description	Reset
7	GPIO_CON	R/W	TCON GPIO Control bit	0
6	LINE_CON	R/W	Delta RGB Line Control bit. Line control for Delta RGB mode. For example, odd line start with {R,G,B,...} and even line start with {G,B,R,...} or reversed.	0
5-4	SYNC_CON	R/W	Delta RGB Sync Control bit .To adjust the dot start point of Delta RGB mode. For example, {R,G,B,...} or {G,B,R,...} or {B,R,G,...}.	0
3-2	CLPSEL[1:0]	R/W	CLPSEL[1:0]	0
1-0	CSPSEL[1:0]	R/W	CSPSEL[1:0]	0

0x180 – Output Mode Control Register

Bit	Function	R/W	Description	Relative Pin	Reset
7	GPIO_0	R/W	LCD Panel signals control 0 : Normal (Same as before) 1 : All signals and data keep zero after GPIO[0] was zero. (Between Back light off and LCD power OFF)		0
6	TCCK_PH	R/W	TCCLK phase control if reg80[0] set is high. (Dual pixel mode) 0 : No clock phase shift 1 : Clock phase 90 degree shift *** It's set regb0[3] (invert clock polarity) high and this bit set high also then TCCLK is 270 degree shift.	TCCLK	0
5	ROE_EN	R/W	ROE (Row Driver) Output Enable 0 : Disable 1 : Enable	TROE	1
4-1	Reserved	R/W	Reserved		-
0	DIV_CK	R/W	Output mode selection 0 : One pixel data out per TCCLK 1 : Two pixel data out per TCCLK (Rising and Falling both)	TCCLK	Reset

0x181 – Display Control Register

Bit	Function	R/W	Description	Relative Pin	Reset
7	Reserved	R/W	Reserved		-
6	POL_CON	R/W	TCON Polarity Swap Control bit		0
5	DELTA_LINE_CON	R/W	Delta RGB Line Control bit 0 : To interpolate EVEN line. 1 : To interpolate ODD line.		0
4	DELTA_LINE_EN	R/W	Delta RGB Interpolation Enable bit 0 : Disable 1 : Enable pixel interpolation for Delta RGB mode.		0
3	REV_EN	R/W	Pixel data reverse control 0 : Data no reverse (Don't case TCREV signal) 1 : Data reverse if TCREV signal is high period	TCREV	0
2	Reserved	R/W	Reserved		-
1-0	INV	R/W	Inversion mode selection 2'b00 : Disable 2'b01 : Disable 2'b10 : Line Inversion 2'b11 : Frame Inversion * Need set reg0x1B0[1] to "0", TCINV output, in order to make inversion mode selection.	TCINV	00

0x182 – Display Direction Control Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-2	TOP_BTM	R/W	Top/Bottom display direction select 2'b00 : Top low active (Normal) 2'b01 : Top high active (Normal) 2'b10 : Bottom low active (Flip) 2'b11 : Bottom high active (Flip)	TRUDL TRSPT TRSPB	01
1-0	LFT_RHT	R/W	Left/Right display direction select 2'b00 : Left low active (Normal) 2'b01 : Left high active (Normal) 2'b10 : Right low active (Mirror) 2'b11 : Right high active (Mirror)	TCLRL TCSPL TCSPR	01

0x183 – Control Signal Polarity Selection Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-5	Reserved	R/W	Reserved		-
4	RCK_P	R/W	Row Clock Polarity Control signal	TRCLK	1
3	ROE_P	R/W	Row Driver Output Enable signal 0 : Active low 1 : Active high	TROE	1
2	RSP_P	R/W	Row Driver Start Pulse signal 0 : Active low 1 : Active high	TRSPT TRSPB	1
1	CLP_P	R/W	Column Driver Latch Pulse signal 0 : Active low 1 : Active high	TCLP	1
0	CSP_P	R/W	Column Driver Start Pulse signal 0 : Active low 1 : Active high	TCSPL TCSPR	1

0x184 – Control Signal Generation Method Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-6	Reserved	R/W	Reserved		-
5	PGM_RCK	R/W	Row Driver Clock signal 0 : This is generate during horizontal display enable. 1 : It's generated that set TCON register address 1A0 though 1A3.	TRCLK	0
4	PGM_ROE	R/W	Row Driver Output Enable signal 0 : This is generate during horizontal display enable. 1 : It's generated that set TCON register address 1AC though 1AF. Also, this is relative to vertical active register 18C though 18F.	TROE	0
3	PGM_RSP	R/W	Row Driver Start Pulse signal 0 : This signal immediately generate and then keep one horizontal period activation received from vertical active signal. 1 : It's generated that set TCON register address 1A4 though 1A7. Also, this is relative to vertical back porch register B9.	TRSPT TRSPB	0
2	PGM_CP	R/W	Column Driver Polarity signal 0 : This signal toggling when horizontal display enable started. 1 : It's generated that set TCON register address 190 though 191.	TCPOL	0
1	PGM_CLP	R/W	Column Driver Latch Pulse signal 0 : This signal generate after horizontal display enable done a every scan line. 1 : It's generated that set TCON register address 192 though 195.	TCLP	0
0	PGM_CSP	R/W	Column Driver Start Pulse signal 0 : This signal generate after horizontal display enable. 1 : It's generated that set TCON register address 19A though 19D. Also, this is relative to horizontal back porch register B4.	TCSPL TCSPR	0

0x185 – Inversion signal operating period register

Bit	Function	R/W	Description	Relative Pin	Reset
7-1	Reserved	R/W	Reserved		-
0	INV_SW	R/W	Inversion signal (Column Driver) working period selection 0 : Inversion signal working within display enable period 1 : Inversion signal working whole(display enable and blanking time) period	TCPOL	0

0x18A – Special Companies LCD Module Control Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-6	Reserved	R/W	Reserved		-
5-4	RSP_WIDTH	R/W	Row Driver Start Pulse width (period) selection 0 : One horizontal period 1 : Two horizontal period 2 : Three horizontal period 3 : Four horizontal period	TRSPT TRSPB	00
3-2	Reserved	R/W	Reserved		-
1-0	COMPANY	R/W	LCD module company selection 2'b00 : LG-Philips LCD module 2'b01 : Sharp LCD module 2'b10, 2'b11 : Other companies LCD module	TCPOLP TCPOLN	10

0x18B – TCPOLP / TCPOLN Control Registers

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	REVV_REVC	R/W	REVV_REVC[7 :0]; for use with Sharp panel	TCPOLP TCPOLN	4D

0x18C – Vertical Active Start High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	V_ST[11:8]	R/W	VER_ASH[11:8]	0

0x18D – Vertical Active Start Low Register

Bit	Function	R/W	Description	Reset
7-0	V_ST[7:0]	R/W	VER_ASL[7:0]	06

0x18E – Vertical Active End High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	V_ED[11:8]	R/W	VER_AEH[11:8]	1

0x18F – Vertical Active End Low Register

Bit	Function	R/W	Description	Reset
7-0	V_ED[7:0]	R/W	VER_AEL[7:0]	E2

Column Driver Chip Control Signals Relative Registers

0x190 – Polarity Control High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	CP_SW[11:8]	R/W	Programmable polarity period high[11:8] value.	TCPOLP TCPOLN	2

0x191 – Polarity Control Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	CP_SW[7:0]	R/W	Programmable polarity period low[7:0] value.	TCPOLP TCPOLN	D0

0x192 – Load/Latch Pulse Start High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	CLP_ST[11:8]	R/W	LP_HSH[11:8]	TCLP	2

0x193 – Load/Latch Pulse Start Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	CLP_ST[7:0]	R/W	LP_HSL[7 :0]	TCLP	D0

0x194 – Load/Latch Pulse Width High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	CLP_ED[11:8]	R/W	LP_HEH[11:8]	TCLP	0

0x195 – Load/Latch Pulse Width Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	CLP_ED[7:0]	R/W	LP_HEL[7:0]	TCLP	06

0x19A – Column Driver Start Pulse High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	CSP_ST[11:8]	R/W	SP_HSH[11:8]	TCSPL TCSPR	0

0x19B – Column Driver Start Pulse Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	CSP_ST[7:0]	R/W	SP_HSL[7 :0]	TCSPL TCSPR	C8

0x19C – Column Driver Start Pulse Width High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	CSP_ED[11:8]	R/W	SP_HEH[11 :8]	TCSPL TCSPR	0

0x19D – Column Driver Start Pulse Width Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	CSP_ED[7:0]	R/W	SP_HEL[7 :0]	TCSPL TCSPR	01

Row Driver Chip Control Signals Relative Registers

0x1A0 – Clock Start Pulse High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	RSP_ST[11:8]	R/W	SP_HSH[11:8]	TRCLK	0

0x1A1 – Clock Start Pulse Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	RSP_ST[7:0]	R/W	SP_HSL[7 :0]	TRCLK	0

0x1A2 – Clock Start Pulse Width High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	RSP_ED[11:8]	R/W	SP_HEH[11 :8]	TRCLK	2

0x1A3 – Clock Start Pulse Width Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	RSP_ED[7:0]	R/W	SP_HEL[7 :0]	TRCLK	30

0x1A4 – Row Start Pulse High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	RSP_ST[11:8]	R/W	RSP_VSH[11:8]	TRSPT TRSPB	0

0x1A5 – Row Start Pulse Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	RSP_ST[7:0]	R/W	RSP_VSL[7 :0]	TRSPT TRSPB	06

0x1A6 – Row Start Pulse Width High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	RSP_ED[11:8]	R/W	RSP_VEH[11 :8]	TRSPT TRSPB	0

0x1A7 – Row Start Pulse Width Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	RSP_ED[7:0]	R/W	RSP_VEL[7 :0]	TRSPT TRSPB	01

0x1AC – Row Output Enable High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	ROE_ST[11:8]	R/W	ROE_HSH[11:8]	TROE	0

0x1AD – Row Output Enable Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	ROE_ST[7:0]	R/W	ROE_HSL[7 :0]	TROE	0A

0x1AE – Row Output Enable Width High Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-4	Reserved	R/W	Reserved		-
3-0	ROE_ED[11:8]	R/W	ROE_HEH[11 :8]	TROE	0

0x1AF – Row Output Enable Width Low Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-0	ROE_ED[7:0]	R/W	ROE_HEL[7 :0]	TROE	36

0x1B0 – Panel type Select Register

Bit	Function	R/W	Description	Relative Pin	Reset
7-2	Reserved	R/W	Reserved		-
1	REV_INV	R/W	Signal output selection 0 : TCINV signal output select 1 : TCREV output select	TCINV TCREV	1
0	LINE_INV	R/W	Analog panel data swapping 0 : No data inversion 1 : Every line data inversion	ROUT GOUT BOUT TCPOLP TCPOLN	0

Analog Sense Block Register

0x1B1 – Analog Sense Block Clock generation register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5	SEN_SEL	R/W	Sense logic (Charge Pump) selection 0 : No Selection 1 : Selection	0
4	BIAS_CTL	R/W	Bias Control	0
3-0	SEN_FREQ	R/W	Sense block clock frequency 0 : 13.5MHz, 1 : 6.75MHz, 2 : 3.375MHz, 3 : 1.69MHz 4 : 844KHz, 5 : 422KHz, 6 : 211KHz, 7 : 105.5KHz 8 : 52.75KHz, 9 : 26.38KHz, 10 : 13.19KHz, 11 ~ 15 : Reserved	3

0x1B2 – Sensing Level Control register

Bit	Function	R/W	Description	Reset
7-4	CP0_LVL	R/W	Sensing level control for Charge Pump 0.	8
3-0	CP1_LVL	R/W	Sensing level control for Charge Pump 1.	8

0x1B3 – Charge Pump Output duration Control Register

Bit	Function	R/W	Description	Reset
7-4	CP0_FREQ	R/W	Charge Pump 0 0 : 13.5MHz, 1 : 6.75MHz, 2 : 3.375MHz, 3 : 1.69MHz 4 : 844KHz, 5 : 422KHz, 6 : 211KHz, 7 : 105.5KHz 8 : 52.75KHz, 9 : 26.38KHz, 10 : 13.19KHz, 11 ~ 15 : Reserved	0
3-0	CP1_FREQ	R/W	Charge Pump 1 0 : 13.5MHz, 1 : 6.75MHz, 2 : 3.375MHz, 3 : 1.69MHz 4 : 844KHz, 5 : 422KHz, 6 : 211KHz, 7 : 105.5KHz 8 : 52.75KHz, 9 : 26.38KHz, 10 : 13.19KHz, 11 ~ 15 : Reserved	0

0x1B4 – VCOM DC Level Control Register

Bit	Function	R/W	Description	Reset
7-0	VCOM DC	R/W	Control for VCOM DC level.	0

ADC/LLPLL Configuration Registers

0x1C0 – LLPLL Input Control Register

Bit	Function	R/W	Description	Reset
7-6	INP_SEL	R/W	Reserved	0
5	CS_INV	R/W	CSYNC Detection Input Polarity, active low needed. 0 : No Inversion 1 : Inversion	0
4	CS_SEL	R/W	PLL Input Selection 0 : Slicer or HSYNC 1 : CS_PAS	0
3	SOG_SEL	R/W	CSYNC Detection Selection 0 : SOG Slicer 1 : HSYNC	0
2	HS_POL	R/W	PLL Input Plarity 0 : Inversion 1 : Normal	0
1	Reserved	R/W		0
0	CK_SEL	R/W	Clock selection 0 : Select PLL clock 1 : Select oscillator clock	0

0x1C1 – LLPLL Input Detection Register

Bit	Function	R/W	Description	Reset
7	VS_POL	R	Detected VSYNC polarity, 0 = low active	-
6	HS_POL	R	Detected HSYNC polarity, 0 = low active	-
5	VS_DET	R	VSYNC detection	-
4	HS_DET	R	HSYNC detection	-
3	CS_DET	R	Composite Sync detection	-
2-0	DET_FMT	R	Input source detection 0 : 480i, 1 : 576i, 2 : 480p, 3 : 576p 4 : 1080i, 5 : 720p 6: 1080p 7: none of above	-

0x1C2 – LLPLL Control Register

Bit	Function	R/W	Description	Reset
7-6	LLC_POST	R/W	PLL post divider 0: 1 1: ½ 2: ¼ 3: 1/8	0
5-4	LLC_VCO	R/W	VCO range select (MHz) 2'b00 : 5 ~ 27 2'b01 : 10 ~ 54 2'b10 : 20 ~ 108 2'b11 : 40 ~ 216	0
3	Reserved			
2-0	LLC_IPMP	R/W	Charge pump currents (uA) 3'b000 : 1.5 3'b001 : 2.5 3'b010 : 5 3'b011 : 10 3'b100 : 20 3'b101 : 40 3'b110 : 80 3'b111 : 160	0

0x1C3 – LLPLL Divider High Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3-0	PLL_ACKN[11:8]	R/W	PLL feedback divider.	3h

0x1C4 – LLPLL Divider Low Register

Bit	Function	R/W	Description	Reset
7-0	PLL_ACKN[7:0]	R/W	PLL feedback divider	5Ah

0x1C5 – LLPLL Clock Phase Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	-
4-0	LLC_PHA	R/W	This 5bit value adjusts the sampling phase in 32 steps across on pixel time. Each step represents an 11.25 degree shift in sampling phase.	00h

0x1C6 – LLPLL Loop Control Register

Bit	Function	R/W	Description	Reset
7	LLC_ACPL	R/W	PLL loop control 0: Closed Loop 1: Open Loop	0
6-4	LLC_APG	R/W	PLL loop gain control	2h
3	Reserved	R/W	Reserved	0
2-0	LLC_APZ	R/W	PLL filter control	0h

0x1C7 – LLPLL VCO Control Register

Bit	Function	R/W	Description	Reset
3-0	LLC_ACKI[11-8]	R/W	PLL VCO nominal frequency. Reserved for internal use.	4h

0x1C8 – LLPLL VCO Control Register

Bit	Function	R/W	Description	Reset
7-0	LLC_ACKI[7-0]	R/W	PLL_VCO nominal frequency. Reserved for internal use.	00h

0x1C9 – LLPLL Pre Coast Register

Bit	Function	R/W	Description	Reset
7-0	PRE_COAST	R/W	Sets the number of HSYNC periods that coast is active before VSYNC edge.	06h

0x1CA – LLPLL Post Coast Register

Bit	Function	R/W	Description	Reset
7-0	POST_COAST	R/W	Sets the number of HSYNC periods that coast is active after VSYNC edge.	06h

0x1CB – SOG Threshold Register

Bit	Function	R/W	Description	Reset
7	PUSOG	R/W	SOG power down control, 0 – power down	0
6	PUPLL	R/W	PLL power down control, 0 - power down	0
5	COAST_EN	R/W	PLL Coast control, 1 - Enable	1
4-0	SOG_TH[4:0]	R/W	SOG slicer threshold This bits control the comparator threshold of the SOG slicer at 10mV per every step. The setting value of 5"b00000 equals 330mV and the maximum setting value is 5'11111 which equals 10mV.	10h

0x1CC – Scaler Sync Selection Register

Bit	Function	R/W	Description	Reset
7-5	Reserved	R/W	Reserved	0
4	VSY_SEL	R/W	Active VSYNC select 0 : Composite Sync Separation Output 1 : VSYNC input pin	0
3-2	HSY_SEL	R/W	Active HSYNC select 00 - HSYNC pin 01 – Sync separator output 10 – regenerated HSYNC 11 – Sync slicer output	0h
1	VSY_POLC	R/W	VSYNC polarity control 0 – No inversion 1 - Inversion	0
0	HSY_POLC	R/W	HSYNC polarity control 0 – No inversion 1 - Inversion	0

0x1CD – PLL Initialization Register

Bit	Function	R/W	Description	Reset
0	INIT	R/W	PLL initialization, self-resetting	0

0x1D0 – Clamp Gain Control Register

Bit	Function	R/W	Description	Reset
7-4	Reserved	R/W	Reserved	-
3	Reserved	R/W	Reserved	-
2	GAINY[8]	R/W	Y channel gain adjust bit[8]	0
1	GAINC[8]	R/W	C channel gain adjust bit[8]	0
0	GAINV[8]	R/W	V channel gain adjust bit[8]	0

0x1D1 – Y Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINY[7-0]	R/W	Y channel gain adjust bit[7-0]	F0h

0x1D2 – C Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINC[7-0]	R/W	C channel gain adjust bit[7-0]	F0h

0x1D3 – V Channel Gain Adjust Register

Bit	Function	R/W	Description	Reset
7-0	GAINV[7-0]	R/W	V channel gain adjust bit[7-0]	F0h

0x1D4 – Clamp Mode Control Register

Bit	Function	R/W	Description	Reset
7	RGB_SEL	R/W	RGB or YCV selection 0 : YCV Mode 1 : RGB Mode	0
6	Reserved	R/W	Reserved	-
5	CL_EDGE	R/W	Clamp reference edge	0
4	CLKY	R/W	Clamping current control 1	0
3	CLKC	R/W	Clamping current control 2	0
2	CL_Y_EN	R/W	Green / Y channel clamp 0 : enable, 1 : disable	0
1	CL_C_EN	R/W	Blue / C channel clamp 0 : enable, 1 : disable	0
0	CL_V_EN	R/W	Red / V channel clamp 0 : enable, 1 : disable	0

0x1D5 – Clamp Start Position Register

Bit	Function	R/W	Description	Reset
7-0	CL_ST	R/W	This register sets programmable clamping start position. It is start count value that after the trailing edge of the HSYNC signal.	00h

0x1D6 – Clamp Stop Position Register

Bit	Function	R/W	Description	Reset
7-0	CL_ED	R/W	This register sets programmable clamping stop position. Clamping duration set between start and stop position.	10h

0x1D7 – Clamp Master Location Register

Bit	Function	R/W	Description	Reset
7-0	CL_LOC	R/W	This bit sets the RGB(YCV) clamp position from the H sync edge.	70h

0x1D8 – ADC TEST Register

Bit	Function	R/W	Description	Reset
6-4	LLC_DBG_SEL	R/W	Debugging register for internal use	00h
3	Reserved			
2	RGB_ADC_TEST	R/W	Internal Test Only	0
1	CL_TEST_UV	R/W	Programmable Blue and Red / U and V select 0: Use default value (R/B:0x10, U/V:0x80) 1: Programmable value	0
0	CL_TEST_Y	R/W	Programmable Green / Y select 0: Use default value (G:0x10, U/V:0x3c) 1: Programmable value	0

0x1D9 – Y Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_Y_VAL	R/W	Green/ Y channel Clamping reference level in programmable mode.	10h

0x1DA – C Clamp Reference Register

Bit	Function	R/W	Description	Reset
7-0	CL_C_VAL	R/W	Blue and Red/ U and V channel Clamping reference level in programmable mode.	80h

MCU SFR Register

0x9A – MCU Bank Select Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	-
5-0	BANK_SEL[5:0]	R/W	Bank select for MCU External RAM	0

0x9B – MCU Misc. Control Register

Bit	Function	R/W	Description	Reset
7-6	Reserved	R/W	Reserved	00
5-4	SCLK_SEL[1:0]	R/W	SPI Interface Clock selection. 2'b00 DIV1, 2'b01 DIV2, 2'b10 DIV3, 2'b11 DIV4.	00
3	LOWSPD	R/W	SPI Interface Speed Control bit. 1'b1 low speed mode.	0
2	HOST_S1	R/W	Host Interface test mode. 1'b1 force external I2C.	0
1	HOST_S0	R/W	Host Interface parallel type selection. 1'b0 8051 parallel type.	0
0	DUAL	R/W	SPI Interface dual output mode. 1'b1 dual mode.	0

0x9C – MCU External Timer Clock 0 Divider High Register

Bit	Function	R/W	Description	Reset
7-0	T0_DIV_H[7:0]	R/W	T0_DIV_H[7:0]	0

0x9D – MCU External Timer Clock 0 Divider Low Register

Bit	Function	R/W	Description	Reset
7-0	T0_DIV_L[7:0]	R/W	T0_DIV_L[7:0]	90

0x9E – MCU External Timer Clock 1 Divider High Register

Bit	Function	R/W	Description	Reset
7-0	T1_DIV_H[7:0]	R/W	T1_DIV_H[7:0]	0

0x9F – MCU External Timer Clock 1 Divider Low Register

Bit	Function	R/W	Description	Reset
7-0	T1_DIV_L[7:0]	R/W	T1_DIV_L[7:0]	90

0x93 – MCU External Timer Clock 2 Divider High Register

Bit	Function	R/W	Description	Reset
7-0	T2_DIV_H[7:0]	R/W	T2_DIV_H[7:0]	0

0x94 – MCU External Timer Clock 2 Divider Low Register

Bit	Function	R/W	Description	Reset
7-0	T2_DIV_L[7:0]	R/W	T2_DIV_L[7:0]	90

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Datasheet revision history

Date	Revision Note
07/18/2007	Rev A. Initial Draft
08/01/2007	Correct Analog power pin description
08/02/2007	Correct DTV/MCU and TCON pin description(pin83~114, pin63~64).
08/20/2007	Correct pin17~18 pin diagram and description. Correct power supply pin 47, 48, 102, 103 description. Updated register 0x17B[6], 0x17B[5:4], 0x181[5], 0x181[4] description. Updated TW8816 Package Mechanical Drawing data.
08/31/2007	Add SPLL maximum percentage of frequency deviation at register 0x0FD. Updated register 0x1C0[4:2] description.
09/13/2007	Add Power Consumption information. Remove register 0x043[7] and 0x0D3[2:0] description. Updated register 0x0D3[7] description. Updated register 0x0F9 description for PLL frequency equation.
10/08/2007	Remove register 0x0C5, 0x0C6 description. Updated register 0x041[7][6][3], 0x04E[2:1],0x0B0[7][2], and 0x130[1:0] description. Add TCON register 0x175, 0x183[4] description.
10/15/2007	Correct register 0x002[3:2], 0x0B0[4], and 0x0D1[1]description. Updated register 0x181[1:0] description. Remove register 0x01A[7], 0x175.

11/02/2007	Correct and updated MCU pin direction
11/14/2007	0x0FD, Spread Spectrum control description updated.
11/19/2007	Remove OSD FONT_Address Character Border/Shadow Effect control.
11/30/2007	Ambient operation temperature range updated
12/20/2007	Add LADIN0, LADIN1, MCU_EN, and HSYNC unused connect recommendation.
01/14/2008	Add RoHS compliant Label at Page1. Change MCU Port Name and Port Description.
03/04/2008	Correct register 0x006[6], 0x00D[7:6] and 0x038[0] description.
03/19/2008	Updated register 0x088[4:0], 0x08A, 0x08B, 0x041[7:6] description. Add BGA package information. Remove GPIO18, GPIO19 from pin description.
5/15/2008	Correct pin#72 typo.