

P-Channel Power MOSFET

-20V, -6.4A, 40mΩ

Features

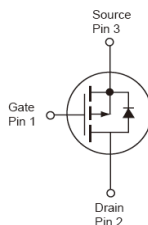
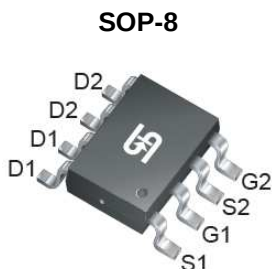
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

KEY PERFORMANCE PARAMETERS

PARAMETER		VALUE	UNIT
V_{DS}		-20	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	40	mΩ
	$V_{GS} = -4.5V$	60	
Q_g		19	nC


Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 8	V
Continuous Drain Current ^(Note 1)	$T_C = 25^\circ\text{C}$	I_D	-6.4	A
	$T_C = 100^\circ\text{C}$		-3.8	
Pulsed Drain Current ^(Note 2)		I_{DM}	-19.2	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$		P_{DTOT}	2.5	W
Single Pulsed Avalanche Energy ^(Note 3)		E_{AS}	13.94	mJ
Single Pulsed Avalanche Current ^(Note 3)		I_{AS}	16.7	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	30	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-20	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-0.4	--	-1.0	V
Gate Body Leakage	V _{GS} = ±8V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = -16V, V _{GS} = 0V	I _{DSS}	--	--	-1	μA
On-State Drain Current	V _{DS} ≤ -5V , V _{GS} = -4.5V	I _{D(ON)}	-10	--	--	A
Drain-Source On-State Resistance	V _{GS} = -4.5V, I _D = -6.4A	R _{DS(ON)}	--	31	40	mΩ
	V _{GS} = -2.5V, I _D = -5.1A		--	45	60	
Forward Transconductance	V _{DS} = -9V, I _D = -6.4A	g _{fs}	--	14	--	S
Dynamic ^(Note 5)						
Total Gate Charge	V _{DS} = -10V, I _D = -6.4A, V _{GS} = -4.5V	Q _g	--	12	19	nC
Gate-Source Charge		Q _{gs}	--	1.7	--	
Gate-Drain Charge		Q _{gd}	--	3.3	--	
Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	1020	--	pF
Output Capacitance		C _{oss}	--	191	--	
Reverse Transfer Capacitance		C _{rss}	--	140	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	3	--	Ω
Switching ^(Note 6)						
Turn-On Delay Time	V _{DD} = -10V, R _{GEN} = 6Ω, I _D = -1A, V _{GS} = -4.5V,	t _{d(on)}	--	25	40	ns
Turn-On Rise Time		t _r	--	43	65	
Turn-Off Delay Time		t _{d(off)}	--	71	110	
Turn-Off Fall Time		t _f	--	48	75	
Source-Drain Diode ^(Note 4)						
Forward On Voltage	I _S = -2.5A, V _{GS} = 0V	V _{SD}	--	-0.9	-1.2	V
Reverse Recovery Time	I _S = -4A	t _{rr}	--	12.6	--	ns
Reverse Recovery Charge	dI _F /dt = 100A/μs	Q _{rr}	--	2.84	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 0.1\text{mH}, I_{AS} = 16.7A, V_{DD} = 25V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM9434CS RLG	SOP-8	2,500pcs / 13" Reel

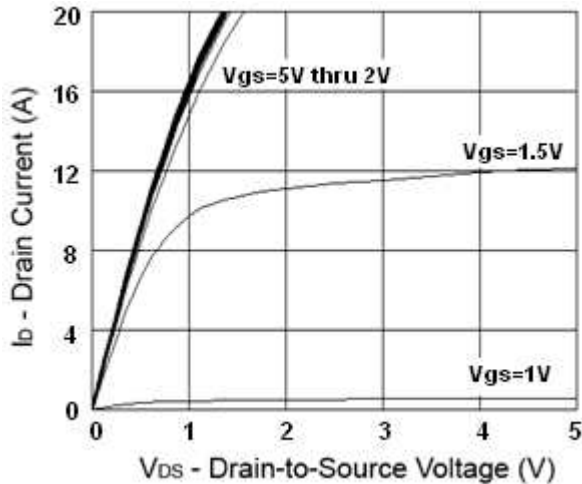
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

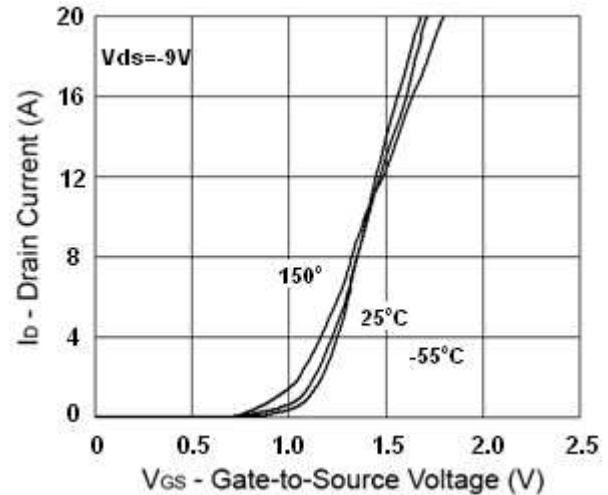
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

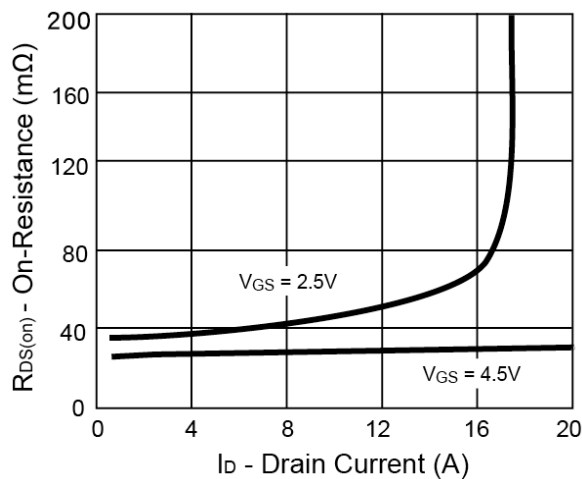
Output Characteristics



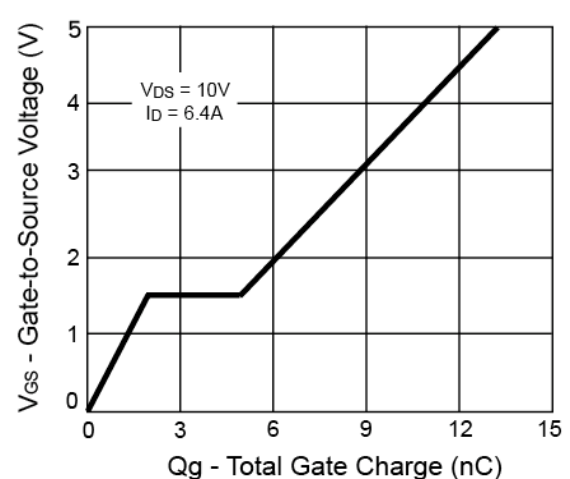
Transfer Characteristics



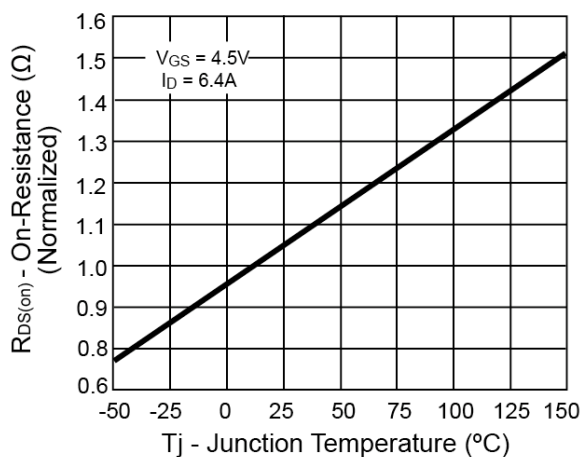
On-Resistance vs. Drain Current



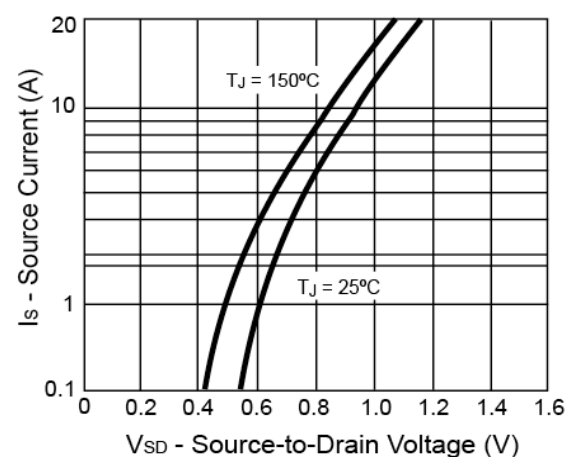
Gate Charge



On-Resistance vs. Junction Temperature



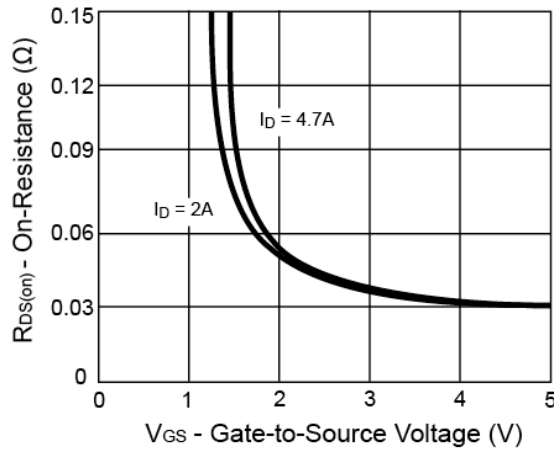
Source-Drain Diode Forward Voltage



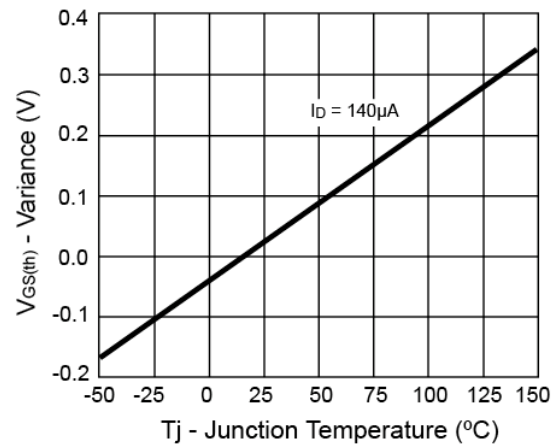
CHARACTERISTICS CURVES

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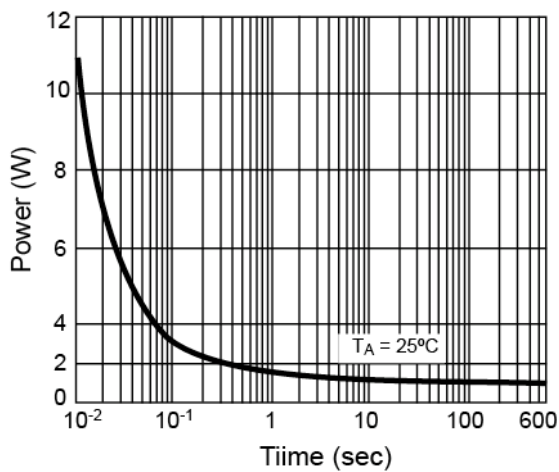
On-Resistance vs. Gate-Source Voltage



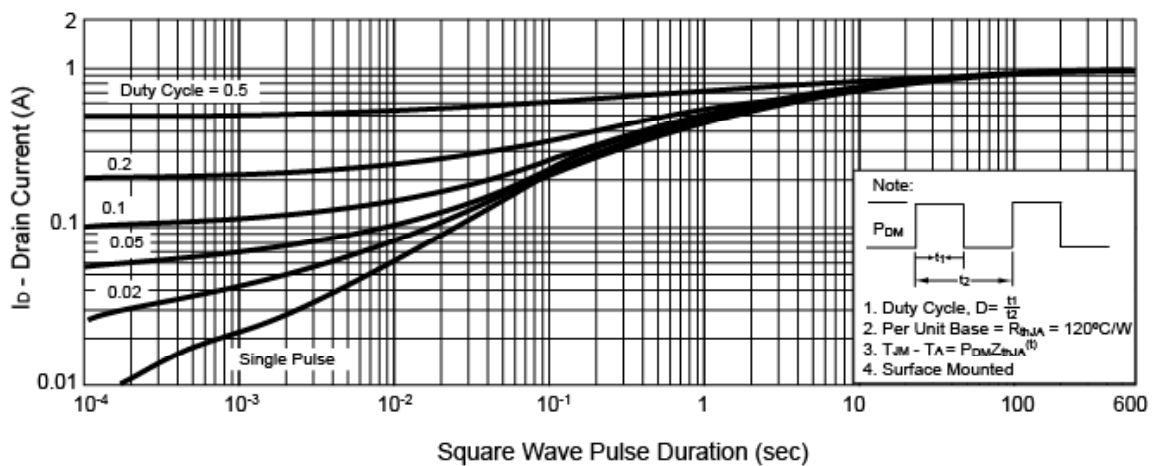
Threshold Voltage



Single Pulse Power

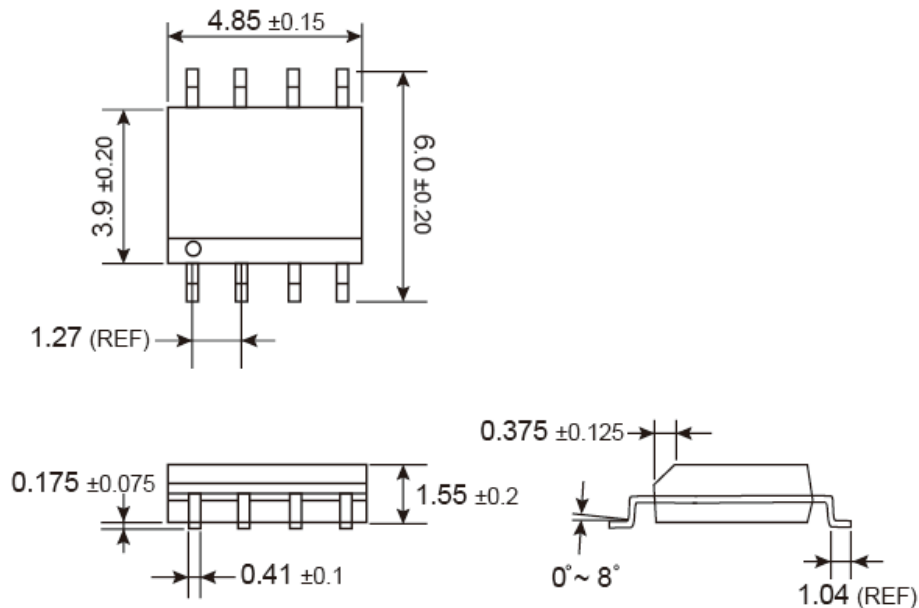


Normalized Thermal Transient Impedance, Junction-to-Ambient

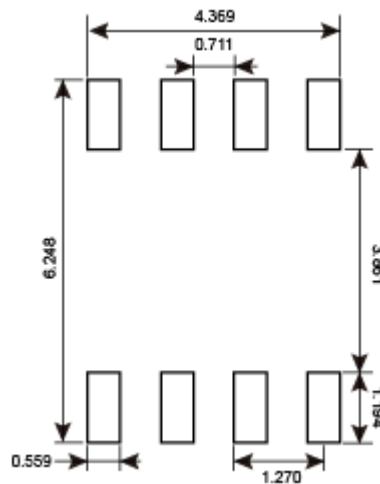


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

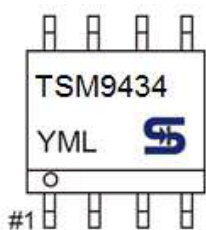
SOP-8



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan **P** =Feb **Q** =Mar **R** =Apr

S =May **T** =Jun **U** =Jul **V** =Aug

W =Sep **X** =Oct **Y** =Nov **Z** =Dec

L = Lot Code (1~9, A~Z)

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