TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM7N65

650V N-Channel Power MOSFET

ITO-220

TO-220

Pin Definition:
1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(Ω)	I_D (A)
650	1.2 @ V_{GS} =10V	3

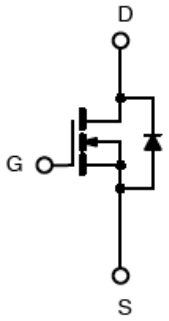
General Description

The TSM7N65 N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- Low $R_{DS(ON)}$ 1.2Ω (Max.)
- Low gate charge typical @ 32nC (Typ.)
- Low Crss typical @ 25pF (Typ.)
- Fast Switching

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM7N65CZ C0	TO-220	50pcs / Tube
TSM7N65CI C0	ITO-220	50pcs / Tube

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	Ta = 25ºC	I_D	6.4	A
	Ta = 100ºC		3.8	A
Pulsed Drain Current *		I_{DM}	22	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	216	mJ
Avalanche Current (Repetitive) (Note 1)		I_{AR}	6	A
Maximum Power Dissipation @ Tc = 25°C	TO-220	P_D	125	W
	ITO-220		30	
Operating Junction Temperature		T_J	150	ºC
Storage Temperature Range		T_{STG}	-55 to +150	°C

* Limited by maximum junction temperature

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Thermal Performance

Parameter		Symbol	Limit	Unit
Thermal Resistance - Junction to Case	TO-220	$R\Theta_{JC}$	1.0	°C/W
	ITO-220		4.2	
Thermal Resistance - Junction to Ambient		$R\Theta_{JA}$	62.5	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec

Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	650	--	--	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 3A	$R_{DS(ON)}$	--	1.0	1.2	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	2.0	--	4.0	V
Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V	I_{DSS}	--	--	1	uA
	V_{DS} = 650V, V_{GS} = 0V, T_C=125°C		--	--	50	
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±10	uA
Forward Transfer Conductance	V_{DS} = 8V, I_D = 1A	g_{fs}	--	3.7	--	S
Diode Forward Voltage	I_S = 6A, V_{GS} = 0V	V_{SD}	--	--	1.6	V
Dynamic [b]						
Total Gate Charge	V_{DS} = 300V, I_D = 6A, V_{GS} = 10V	Q_g	--	32	46	nC
Gate-Source Charge		Q_{gs}	--	6	--	
Gate-Drain Charge		Q_{gd}	--	11	--	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	905	--	pF
Output Capacitance		C_{oss}	--	115	--	
Reverse Transfer Capacitance		C_{rss}	--	25	--	
Switching [c]						
Turn-On Delay Time	V_{GS} = 10V, I_D = 6A, V_{DD} = 300V, R_G = 25Ω	$t_{d(on)}$	--	14	--	nS
Turn-On Rise Time		t_r	--	14	--	
Turn-Off Delay Time		$t_{d(off)}$	--	47	--	
Turn-Off Fall Time		t_f	--	19	--	
Reverse Recovery Time	V_{GS} = 0V, I_S = 6A, dI_F/dt = 100A/us	t_{fr}	--	638	--	nS
Reverse Recovery Charge		Q_{fr}	--	4.8	--	uC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. V_{DD} = 50V, I_{AS}=3.6A, L=30mH, V_{DS}=500V
3. Pulse test: pulse width ≤300uS, duty cycle ≤2%
4. Essentially Independent of Operating Temperature

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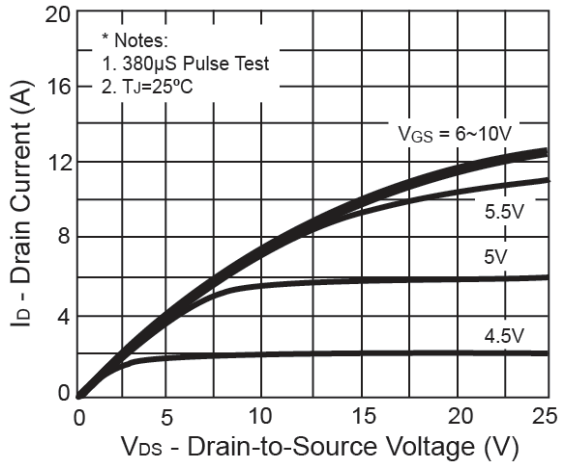
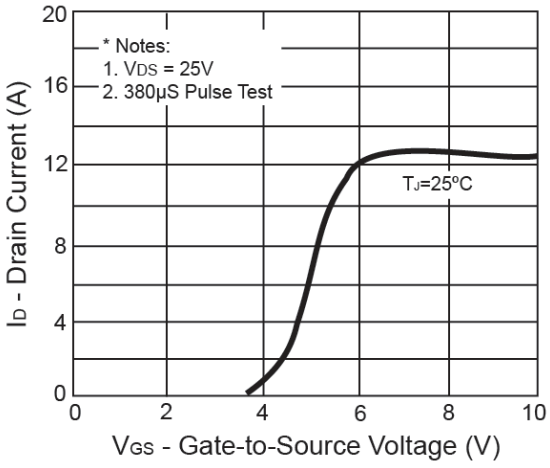
Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

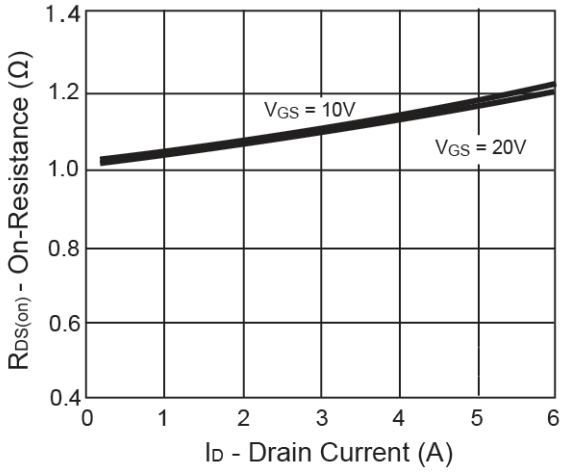
Output Characteristics



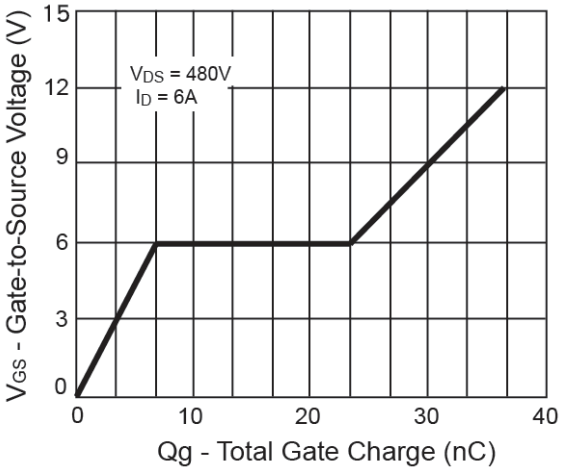
Transfer Characteristics



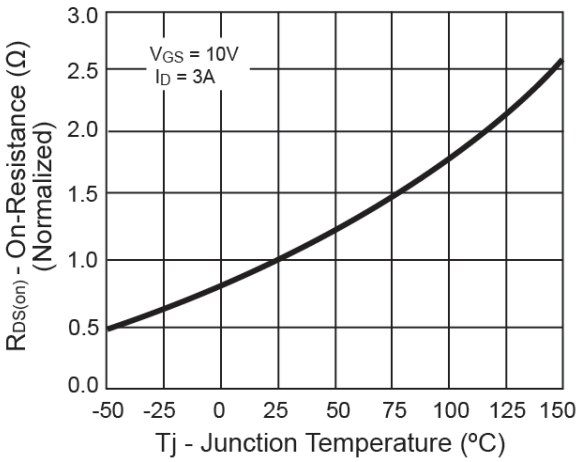
On-Resistance vs. Drain Current



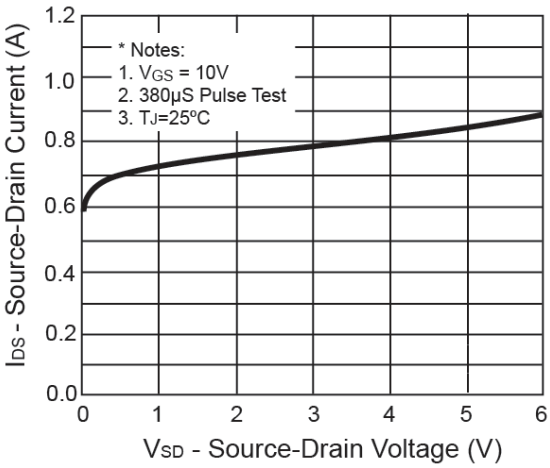
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



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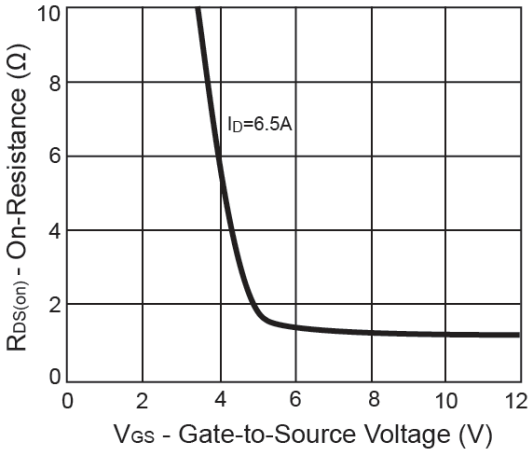
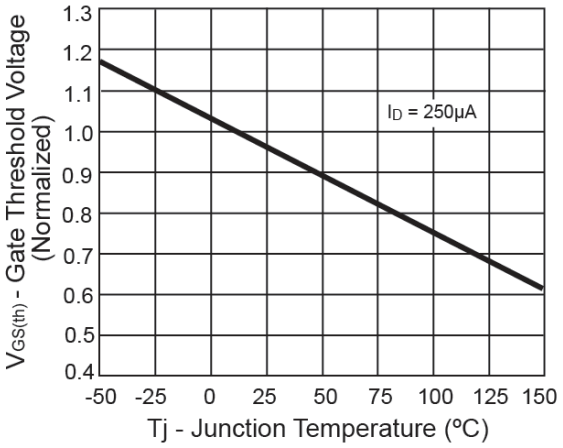
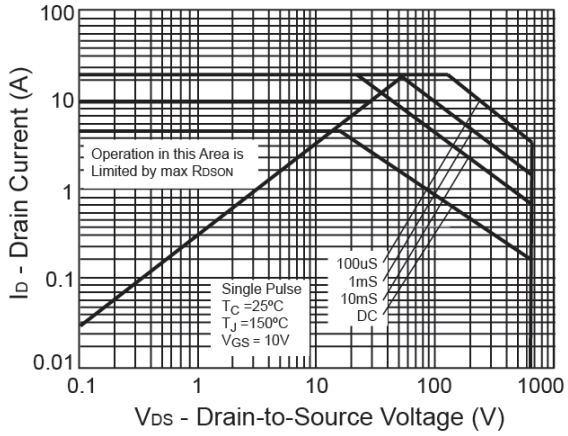
On-Resistance vs. Gate-Source Voltage



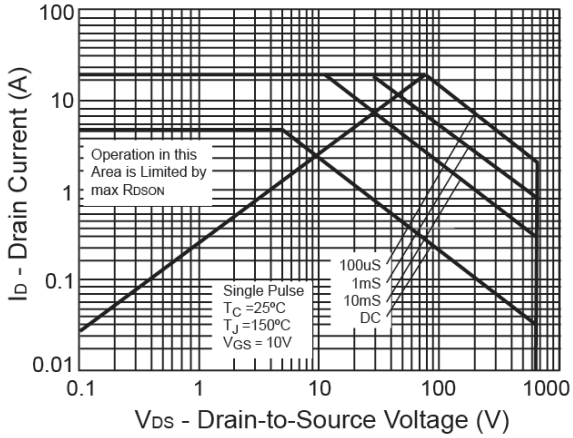
Threshold Voltage



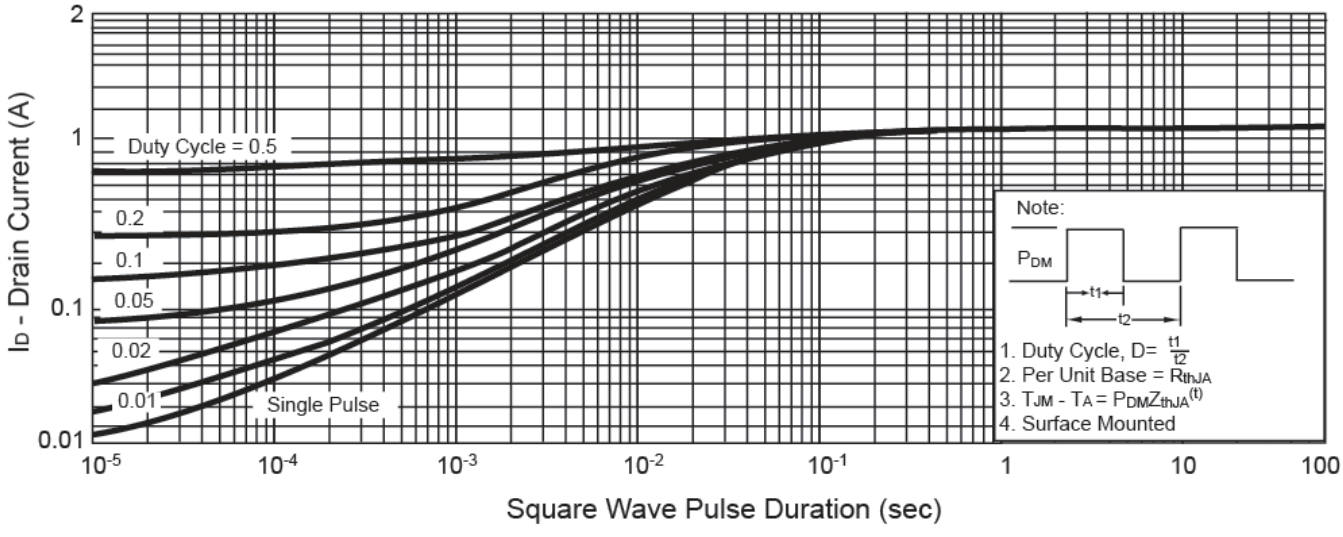
Maximum Safe Operating Area - TO-220



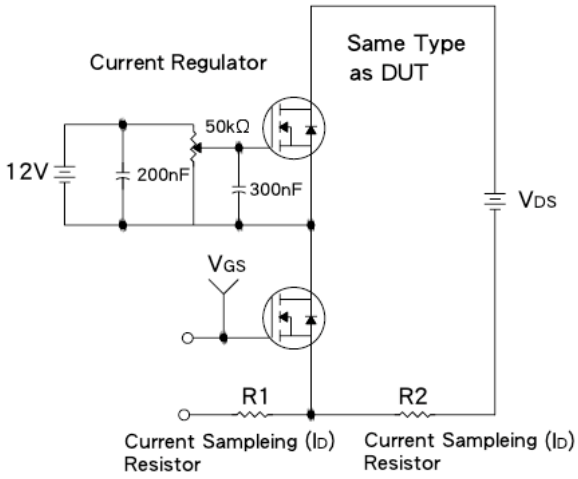
Maximum Safe Operating Area - ITO-220

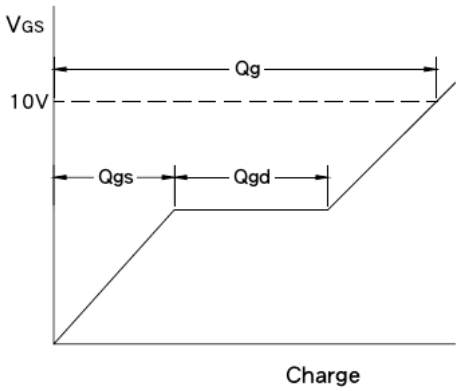


Normalized Thermal Transient Impedance, Junction-to-Ambient

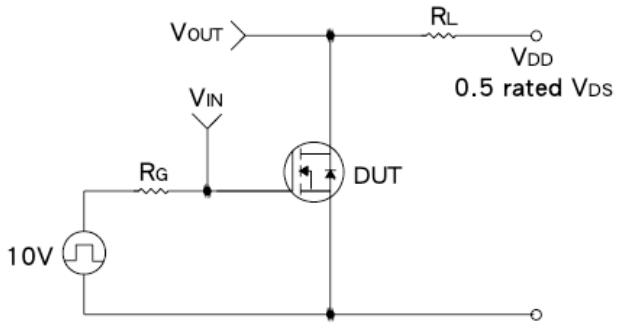


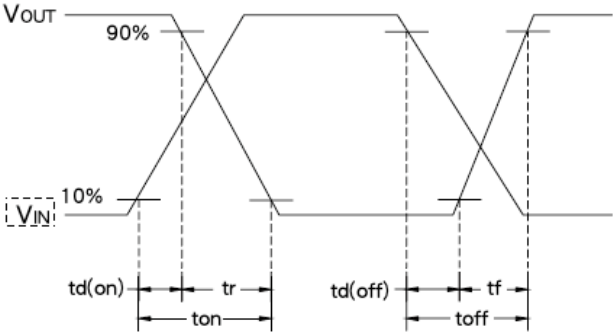
Gate Charge Test Circuit & Waveform



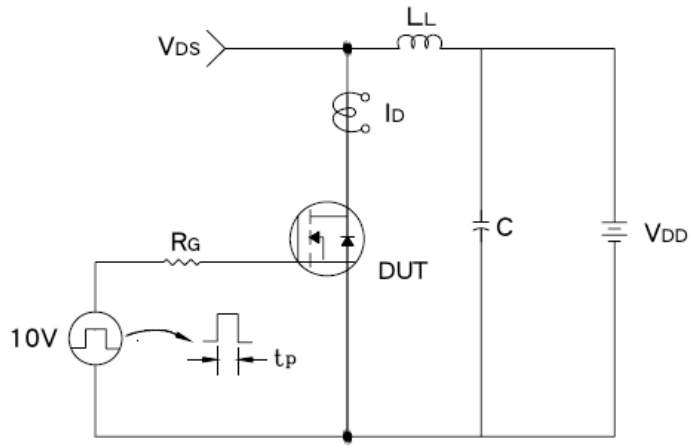


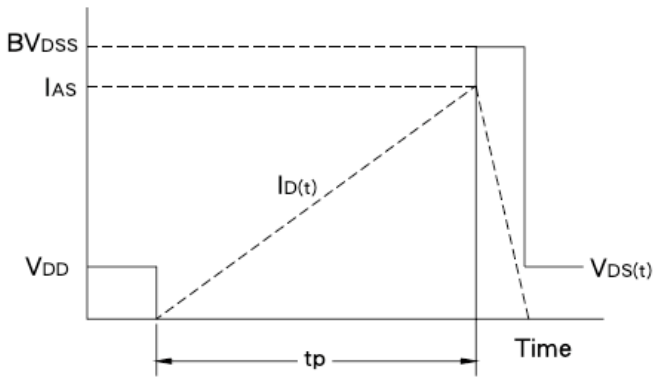
Resistive Switching Test Circuit & Waveform



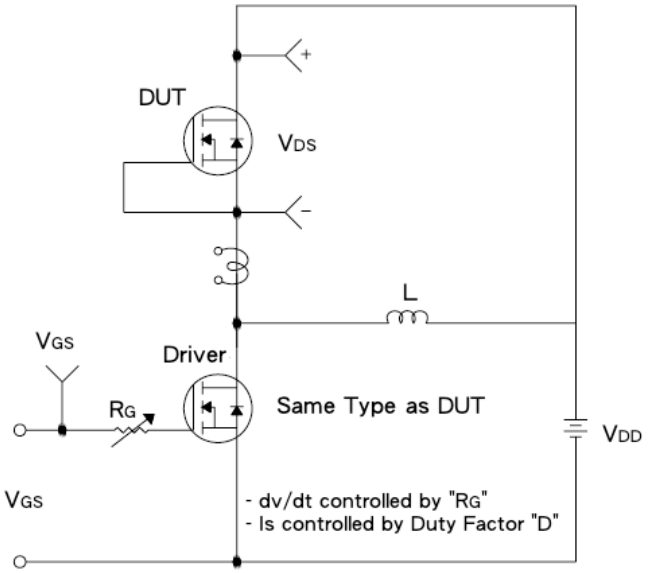


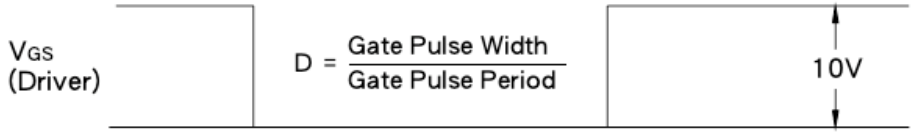
E_{AS} Test Circuit & Waveform

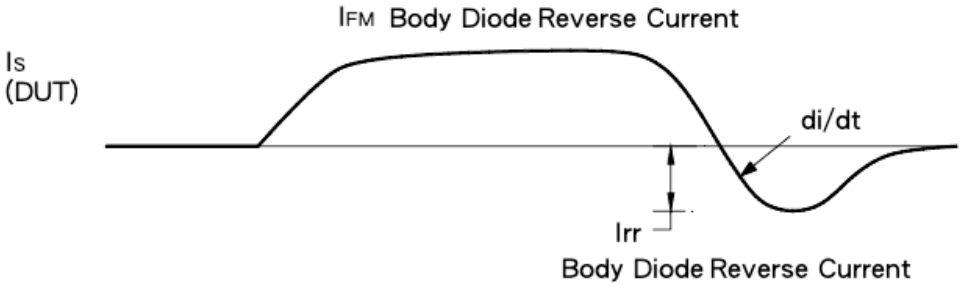


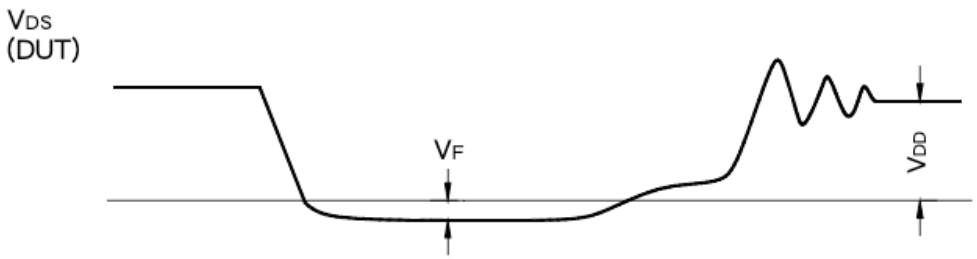


Diode Reverse Recovery Time Test Circuit & Waveform









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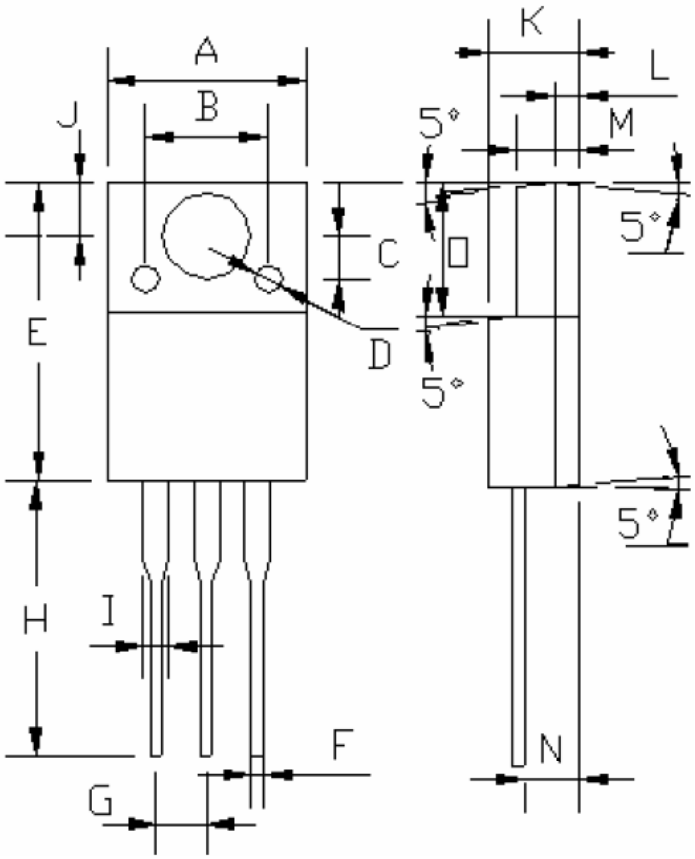
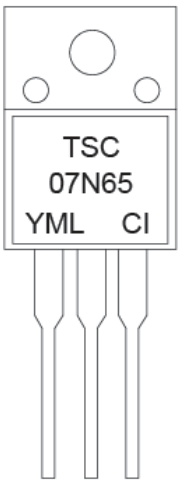
ITO-220 Mechanical Drawing



ITO-220 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.04	10.07	0.395	0.396
B	6.20 (typ.)		0.244 (typ.)	
C	2.20 (typ.)		0.087 (typ.)	
D	∮ 1.40 (typ.)		∮ 0.055 (typ.)	
E	15.0	15.20	0.591	0.598
F	0.52	0.54	0.020	0.021
G	2.35	2.73	0.093	0.107
H	13.50	13.55	0.531	0.533
I	1.11	1.49	0.044	0.058
J	2.60	2.80	0.102	0.110
K	4.49	4.50	0.176	0.177
L	1.15 (typ.)		0.045 (typ.)	
M	3.03	3.05	0.119	0.120
N	2.60	2.80	0.102	0.110
O	6.55	6.65	0.258	0.262

Marking Diagram



Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
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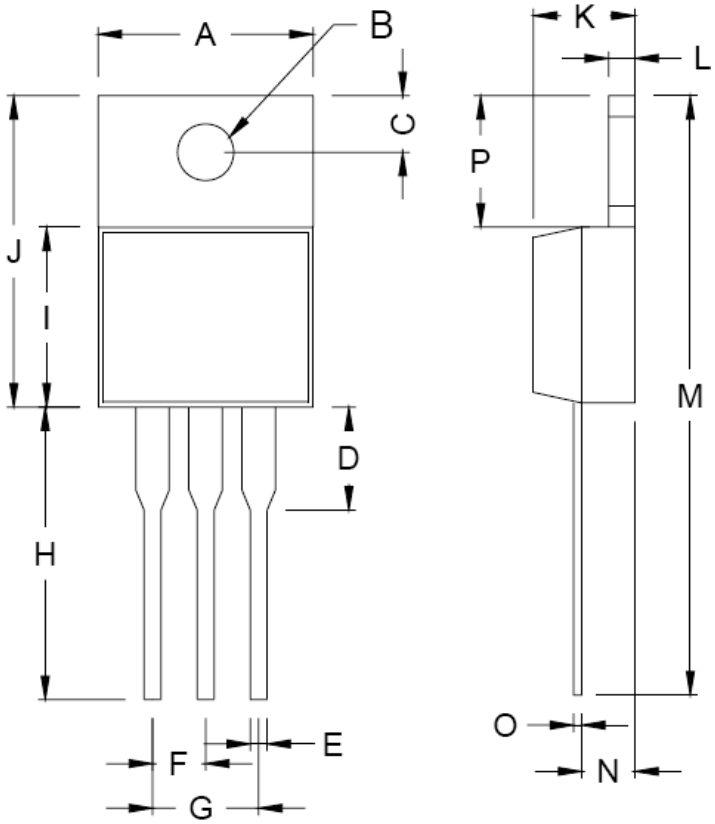
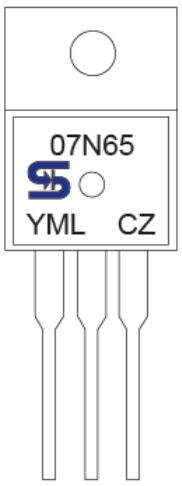
TO-220 Mechanical Drawing



TO-220 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.000	10.500	0.394	0.413
B	3.740	3.910	0.147	0.154
C	2.440	2.940	0.096	0.116
D	-	6.350	-	0.250
E	0.381	1.106	0.015	0.040
F	2.345	2.715	0.092	0.058
G	4.690	5.430	0.092	0.107
H	12.700	14.732	0.500	0.581
J	14.224	16.510	0.560	0.650
K	3.556	4.826	0.140	0.190
L	0.508	1.397	0.020	0.055
M	27.700	29.620	1.060	1.230
N	2.032	2.921	0.080	0.115
O	0.255	0.610	0.010	0.024
P	5.842	6.858	0.230	0.270

Marking Diagram



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