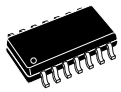
TSM006

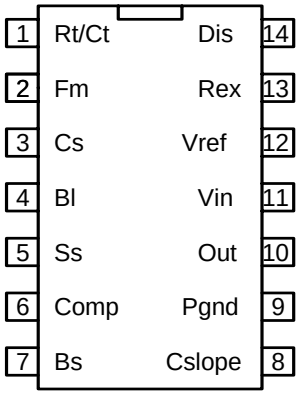
Primary PWM Controller

- **Current-mode PWM Controller**
- **High-current output drive suitable for Power MOSFET**
- **Automatic burst mode in zero-load condition**
- **Primary overcurrent protection (hiccup mode)**
- **Internal leading edge blanking on current sense**
- **External slope compensation capability**
- **Programmable soft start**
- **Frequency modulation for low emi**
- **Accurate oscillator frequency**
- **77% duty cycle limitation**
- **5V reference**
- **Under voltage protection**
- **Thermal shutdown at 130°C**
- **2kV ESD protection**



D
SO-14
(Plastic MicroPackage)

PIN CONNECTIONS (top view)



DESCRIPTION

The TSM006 integrated circuits incorporate all circuitry to implement off line or DC-DC power supply applications using a fixed frequency current mode control.

Based on a standard current mode PWM controller, these devices include additional features for higher integration.

APPLICATION

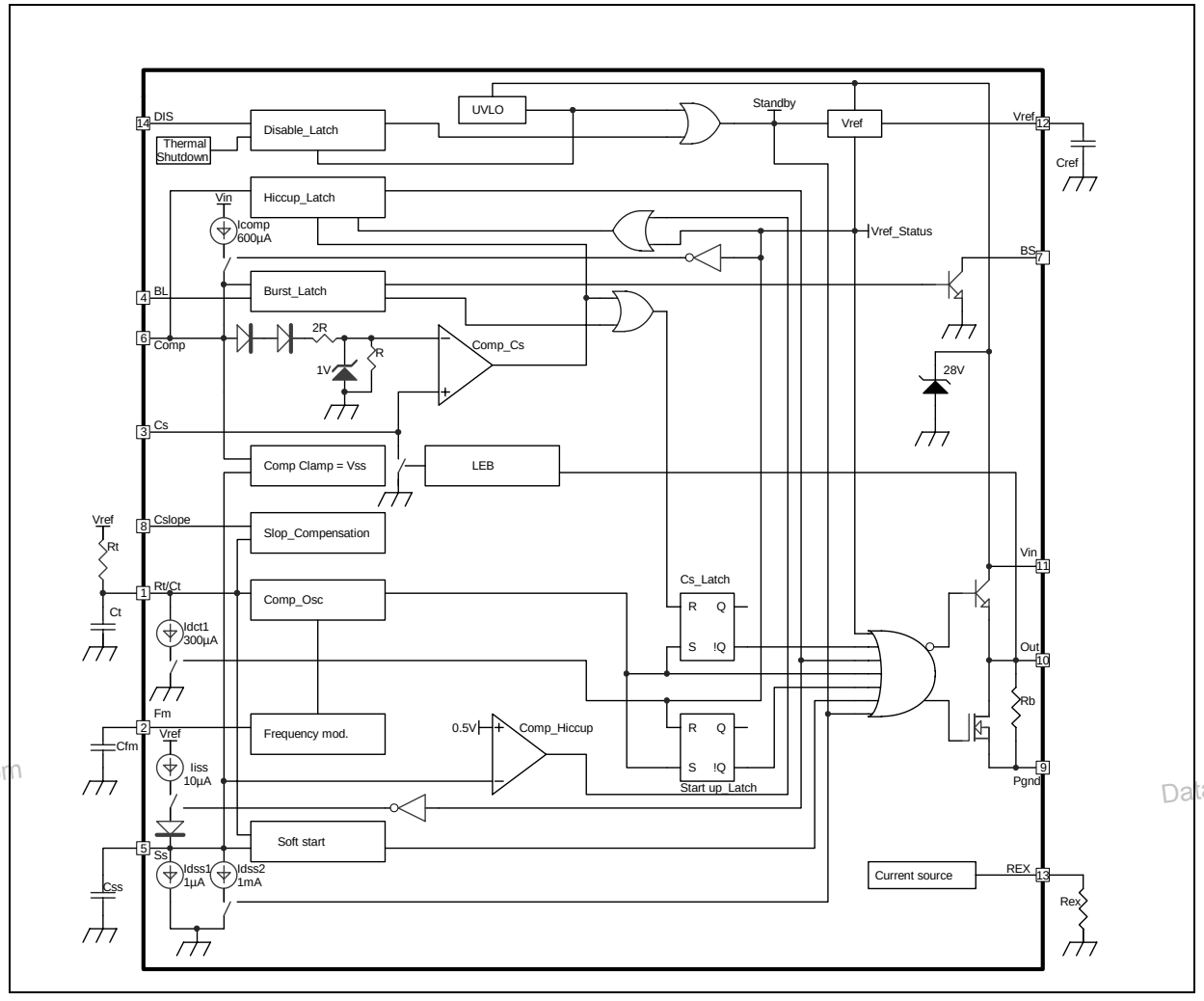
- **AC/DC adapter**

D = Small Outline Package (SO) - also available in Tape & Reel (DT)

ORDER CODES

Part Number	Temperature Range	Package	Packaging	Marking
TSM006ID	0, +105°C	SO	Tube	TSM006
TSM006IDT			Tape & Reel	TSM006

1 Block Diagram



PIN DESCRIPTION

Name	SO14	Type	Function
RT/CT	1	Timing capacitor	Sets the oscillator frequency and maximum duty cycle
FM	2	Analog input	Frequency modulation
CS	3	Analog input	Current sense.
BL	4	Analog output	Burst level
SS	5	Timing capacitor	Soft start and hiccup timing, latched disable input.
COMP	6	Analog input	Current comparator for current mode control.
BS	7	Output input	Burst mode status
CSLOPE	8	Analog output	Slope compensation
PGND	9	Power supply	Power ground
OUT	10	Analog output	Totem pole output to direct drive a power MOSFET.
VIN	11	Power supply	Supply input voltage.
VREF	12	Analog output	+5V Voltage reference
REX	13	Analog input	External resistor for internal constant current
DIS	14	Analog input	Latched disable

2 Absolute Maximum Ratings

Symbol	DC Supply Voltage	Value	Unit
Vin	DC Supply Voltage (Iin<50mA) [1]	-0.3 to self limit	V
Io	DC output current	0.1	A
Iopeak	Peak output current	1	A
Vcomp	COMP terminal voltage	-0.3 to 6.5	V
Isinkcomp	COMP terminal sink current	6	mA
Vss	SS terminal voltage	-0.3 to 8	V
Vout	OUT terminal voltage	-0.3 to Vin	V
Vter	Other terminal voltage (CT, VREF, BS, BL, CSLOPE REX, CS, FM, DIS)	-0.3 to Vref	V
Pt	Power dissipation at 25°C	500	mW
Tstg	Storage temperature	-40 to 150	°C
Tj	Junction temperature	150	°C
ESD	Electrostatic Discharge	2	kV

1) All voltage values, except differential voltage are with respect to network ground terminal (GND).

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
Vcc	DC Supply Conditions	8 to 20	V
Toper	Operating Free Air Temperature Range	0 to 105	°C

3 Electrical Characteristics

Tamb = 25°C, Vin=15V, Rt=39k, Ct=470pF, Rex=27k, Cfm=1nF unless otherwise specified

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Main oscillator						
Fosco	Lower oscillating frequency	8≤Vin≤20V, 0≤Ta≤105°C Vfm=GND	63	68	73	kHz
FoscL	Upper oscillating frequency	Vfm=Vref	57.6	62	66.4	kHz
Fjit	Frequency jitter	Fjit=Fosco - FoscL	6	7	8	kHz
Ffm	Frequency modulation			4.5		kHz
Vthct	Upper trip point	Vfm=GND		3.0		V
Vtlct	Lower trip point	Vfm=GND		1.4		V
ΔVct	Amplitude	Vfm=GND		1.6		V
Idct1	Discharge current	Vct=2V		300		µA
Idct2	Current at Ct in UVLO	Vct=1V	1	3		mA
Disable						
Vdis	Voltage threshold		2.5	2.65	2.8	V
Vref reference pin						
Vref	Voltage reference		4.91	5.00	5.09	V
ΔVline	Line regulation	12V ≤ Vin ≤ 20V		5	10	mV
ΔVload	Load regulation	1mA ≤ Iref ≤ 5mA		10	20	mV
ΔVtotal	Total variation	Line, load, temp	4.85	5.00	5.15	V
Ios	Short circuit current	Vref=0	10			mA
Slope Compensation						
IsinkCP	Sink current	Vct=2.2V, VCslope=1V		90		µA
IsrcCP	Source current	Vct=2.2V, VCslope=0V	2			mA
Comp						
Icomp	Source current	Vcomp=5V	0.5	0.6	0.7	mA
Current sense						
Avcs	Gain	0V ≤ Vcs ≤ 0.8V	2.85	3.00	3.15	
Vz1	Maximum sensing voltage	Vcomp=5V	0.9	1.0	1.1	V
PSRR	Power supply voltage rejection ratio	8V ≤ Vin ≤ 20V		70		dB
Leading edge blanking						
LEB	Delay to output	Vcs = 0 to 2 V Vcomp = 2 V		280		ns
Output						
VOL1	Output low voltage 1	Iosink=20mA			1.0	V
VOL2	Output low voltage 2	Iosink=200mA		0.8	2.2	V
VOH1	Output high voltage 1	Iosource=20mA	Vin-2.0			V
VOH2	Output high voltage 2	Iosource=200mA	Vin-3.0			V
tr	Rise time	CL=1nF, 10% to 90%		70	100	ns
tf	Fall time	CL=1nF, 90% to 10%		40	60	ns
VOL3	UVLO saturation	Vin=5V, Iosink=1mA			0.5	V
Fout	Output frequency	Option 1		Fosc		kHz
DCmax	Maximum Duty Cycle	Option 1		77.5		%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Soft start						
Iiss	Charge current	Vss=2V	8	10	12	µA
dIiss	Temperature stability	0°C ≤ Ta ≤ 105°C	7	10	13	µA
Idss1	Discharge current (hiccup)	Vss=2V, Vcs=2V		1	1.2	µA
Idss2	Sink current (uvlo)	Vss=2V, Vin=7V	3			mA
Iiss/Idss1	Charge/discharge ratio			10	11	
VHss	Clamp voltage		4			V
VLss	Low voltage (uvlo)	Vin=7V, Idss=1mA			0.5	V
Under Voltage Lockout (UVLO)						
VH	UVLO top threshold		11.5	12	12.5	V
VL	UVLO bottom threshold		8.0	8.4	8.8	V
Supply current						
Iin	Operating current	CL=1nF		4.5	5.0	mA
Iidle	Supply current in idle mode	Vcomp=1V		3.3	3.8	mA
Istby	Supply current in standby mode	Vin<VH		40	60	µA
Vclamp	Clamp voltage	Iin=50mA	22	25	30	V
Burst						
Vbsol	Output low voltage	Iobs=1mA		0.3		V
Iohbs	Leakage current	Vbs=5V		2		µA
Vbl1	Threshold level on Comp to enter Burst mode	BL pin left unconnected		1.25		V
Vbl1hyst	Vbl1 Hysteresis			0.3		V
Vbl2	Threshold level on Comp to exit burst mode			1.75		V
Hiccup						
Vz2	Threshold level on Cs to enter Hiccup mode		1.15	1.25	1.35	V
Vhicc	Threshold level on Ss to exit Hiccup mode			0.5		V

4 Functional Description

TSM006: PWM Controller IC.

UVLO function

The Under Voltage Lock Out function disables the whole device when supply voltage is lower than the threshold.

Vref block

The Vref block provides a 5V reference voltage. An internal Vref status signal is active when Vref is lower than 4.7V and is used to drive the output driver low when Vref is not valid.

Current sense input

A voltage proportional to the output inductor current is applied to the CS pin. The control IC uses this information to perform current mode control. The PWM function will be stopped if the CS pin voltage is greater than 1.0V.

Current leading edge blanking

An internal delay is built into the IC to mask the first 100ns of the current sense signal. This delay is made of a capacitor charged with a current source. The capacitor is discharged when CT reaches its maximum level.

COMP input

This pin is connected to the current comparator for current mode control. The pin should be connected to the collector (primary side) of an optocoupler which anode (secondary side) is driven by the output of error amplifier.
The COMP input is used to set the reference level for the current sense comparator. The current sense threshold is set to (Vcomp - 2 * Vbe) / 3.

During the soft start period, COMP voltage is clamped to the SS pin plus two Vbe voltage.

Startup latch

The startup latch is set when the IC exits from standby mode or UVLO state. It is reset when the CT capacitor is discharged for the first time.

Output driver

The OUT totem pole output is capable to sink and source more than 1.0A (peak) in order to direct drive a power MOSFET.

Oscillator

A capacitor from the RT/CT pin to GND and a resistor to the VREF set the oscillating frequency. The maximum duty cycle at the OUT pin is limited at 77%.

Frequency modulation

A FM generator adds a small amount of jitter on the oscillator frequency in a way that reduces the conducted and radiated EMI. The FM frequency is set by an external capacitor connected to the FM pin.

Slope compensation

A buffered Rt/Ct voltage is brought to the Cslope pin. This signal is used to provide the necessary slope compensation.

Soft start

A capacitor from the SS pin to GND provides the soft start function. The capacitor starts to charge when VIN reaches the UVLO threshold and Vref is good.

The soft start block enables the IC to start with a progressive PWM duty cycle. The soft start comparator drives the output driver low when the SS pin voltage is greater than the CT pin voltage minus one Vbe voltage.
During soft start, the COMP pin voltage is clamped to the SS pin voltage plus two Vbe voltage, limiting the maximum peak current.

External reference pin

An external resistor at REX pin sets the internal current reference.

Automatic burst mode

Burst mode is used during light load condition to reduce the number of MOS switching, and thus reducing overall power dissipation. Light load condition is detected when **COMP** voltage is low.
When **COMP** voltage is lower than a threshold V_{BL1} set by the external **BL** pin, the device output is forced to off state, providing minimum duty cycle and pulse skipping.
The burst status is available on the **BS** pin to put other devices in standby mode when in light load condition.

When **COMP** voltage (Vcomp) is higher than V_{BL2}, the device operates in normal mode. Current is limited to **(Vcomp-2*Vbe)/3 / Rshunt** (Rshunt is the shunt resistor used to measure the primary current, Vbe is the forward voltage of a diode, and 3 is the R/2R network attenuation). Maximum current is **1V/Rshunt**. When Vcomp becomes lower than V_{BL}, device enters burst mode, PWM is stopped while Comp voltage is lower than V_{BL}. As PWM is stopped, no more energy is transferred to the secondary side, output voltage is decreasing, and Vcomp (which is an image of the error comparator) tends to increase. As soon as Vcomp becomes just higher than V_{BL}, PWM operation can resume for some cycles, so current in burst mode is limited to **(V_{BL}-2*Vbe)/3 / Rshunt**.

OverCurrent detection and Hiccup mode

Overcurrent is detected when voltage at the CS pin is greater than Vz2=1.2V. To avoid false triggering, the overcurrent detection is delayed in the same way than the normal pulse by pulse current limitation.

When overcurrent is detected, the device enters the hiccup mode. Output is switched off immediately and the soft start capacitor is discharged slowly. When the SS pin voltage goes below 0.5V, normal soft start is started. If the overcurrent is no more present, device operation is resumed normally, otherwise, overcurrent is detected again and the cycle is repeated until the overcurrent situation disappears.

Duty cycle of the hiccup mode is set by the ratio of SS pin discharge and charge currents: 10% typ. With a typical capacitor Css=100nF, soft start delay is about 40ms and hiccup off-time is 400ms.

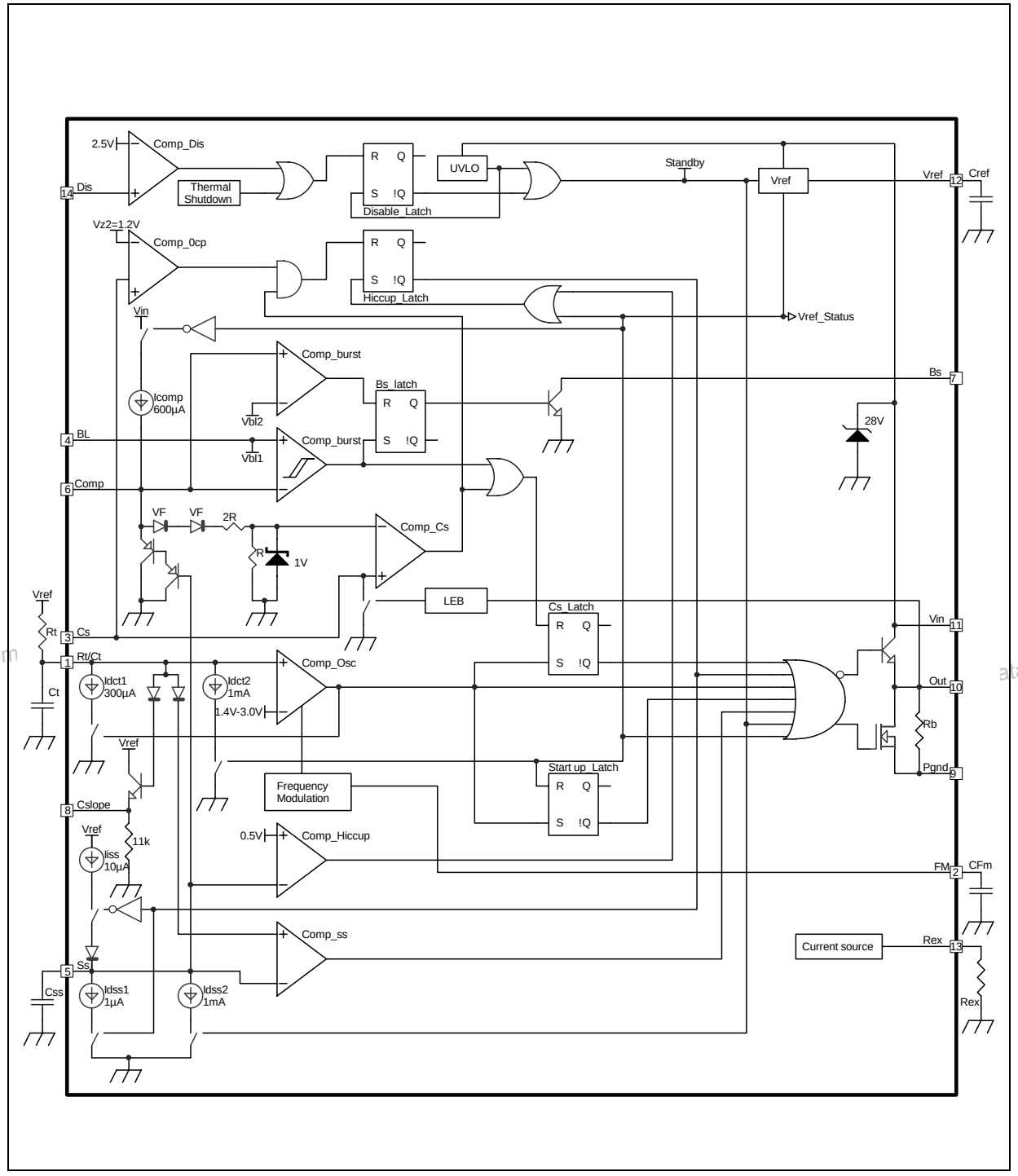
Latched disable function

Disable mode is entered when the DIS pin voltage is driven above 2.5V. Disable state is latched and can only be exit by driving the Vin power supply voltage under the UVLO level.

Thermal shutdown

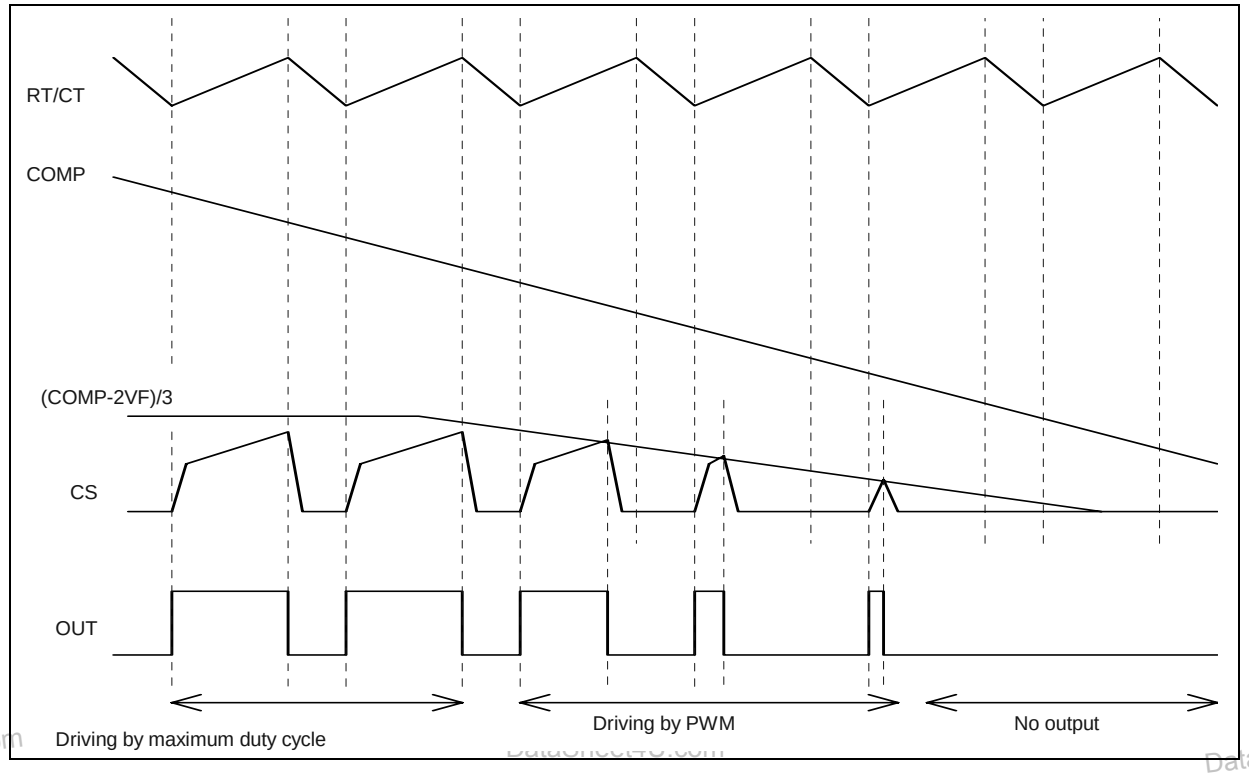
The device operation is shut down when the internal temperature exceed 130°C. Hysteresis provides stable working and shutdown states.

Fig. 1: Detailed Internal Schematic

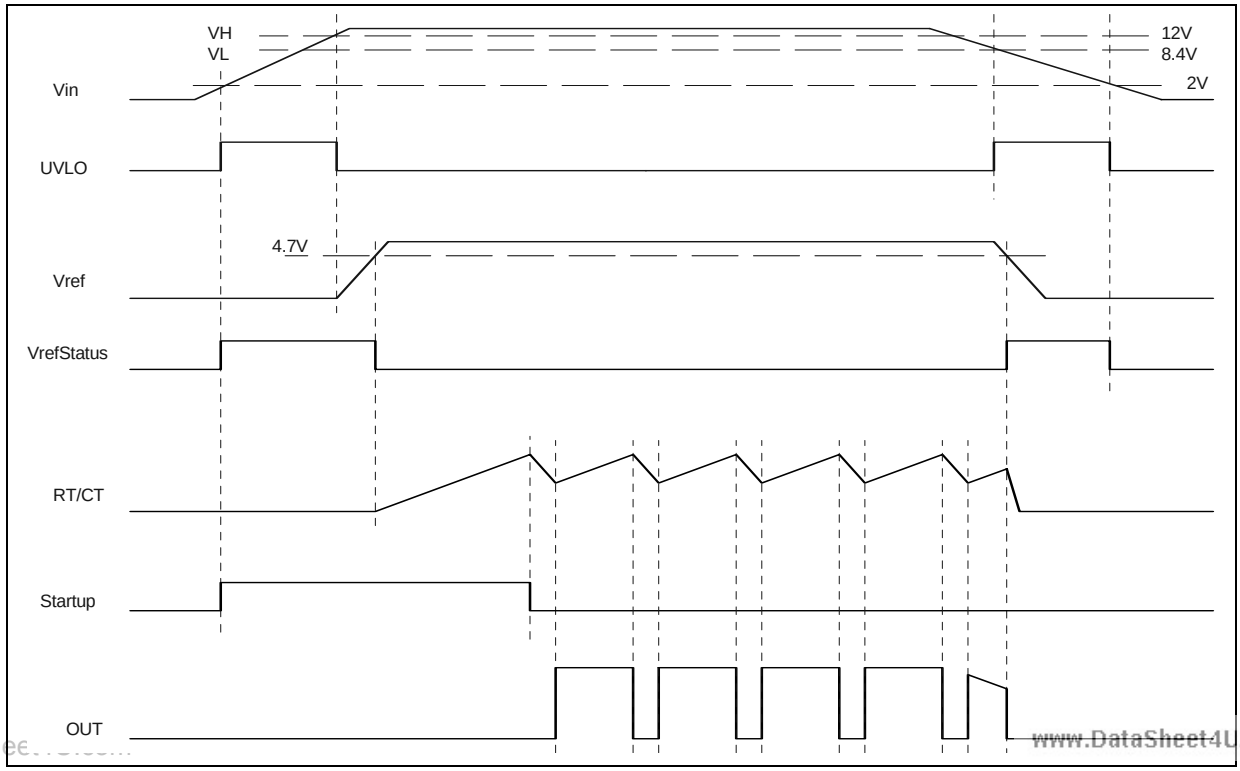


5 Timing Diagram

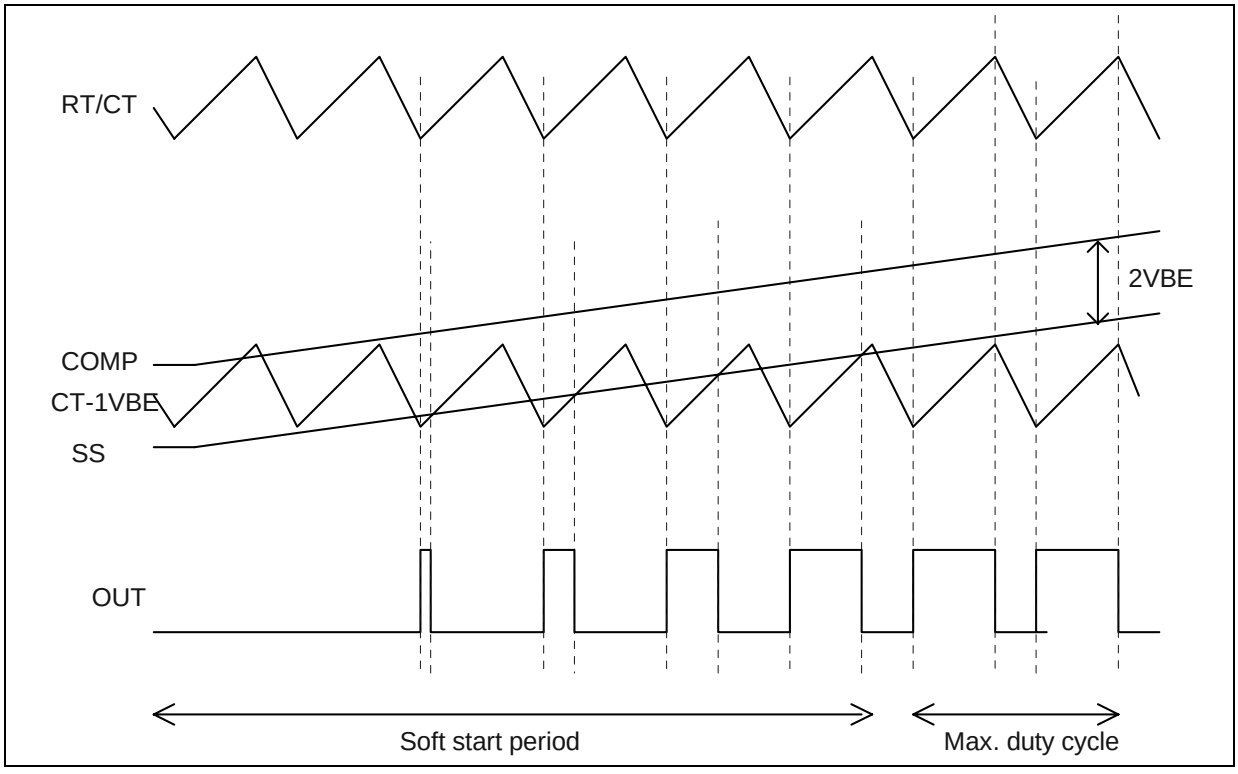
Timing for PWM function



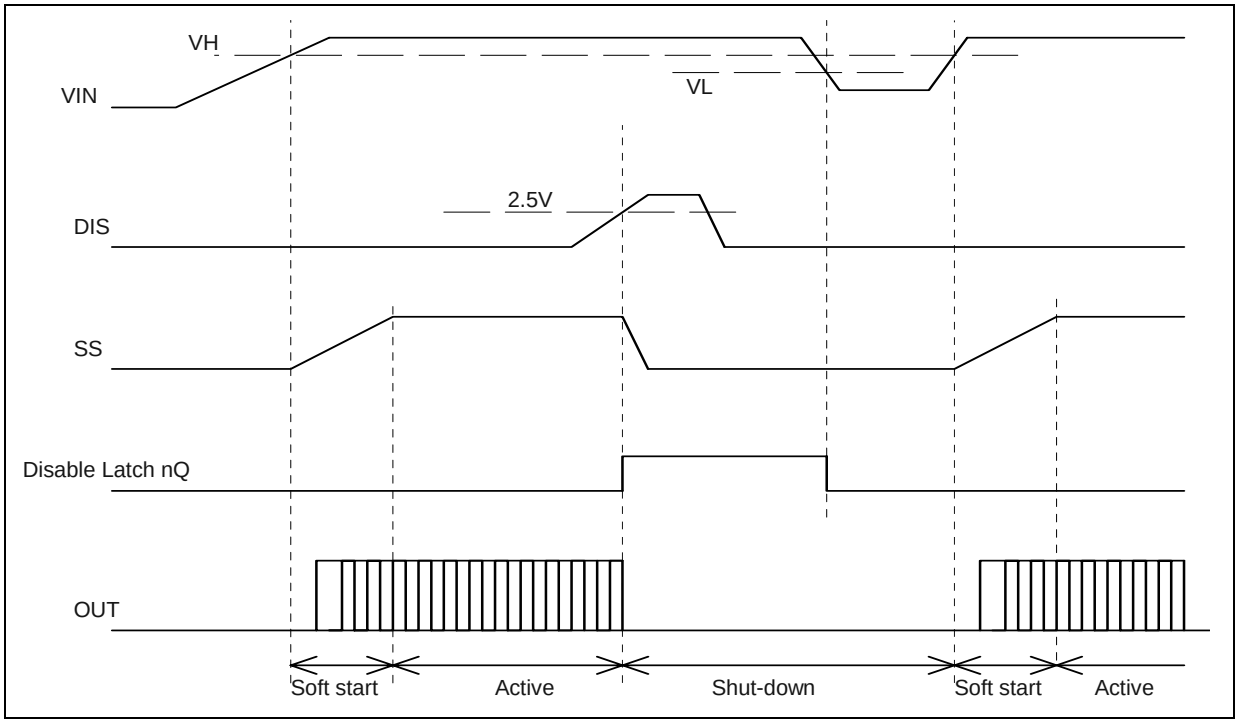
Timing at Vref rise up and shut down



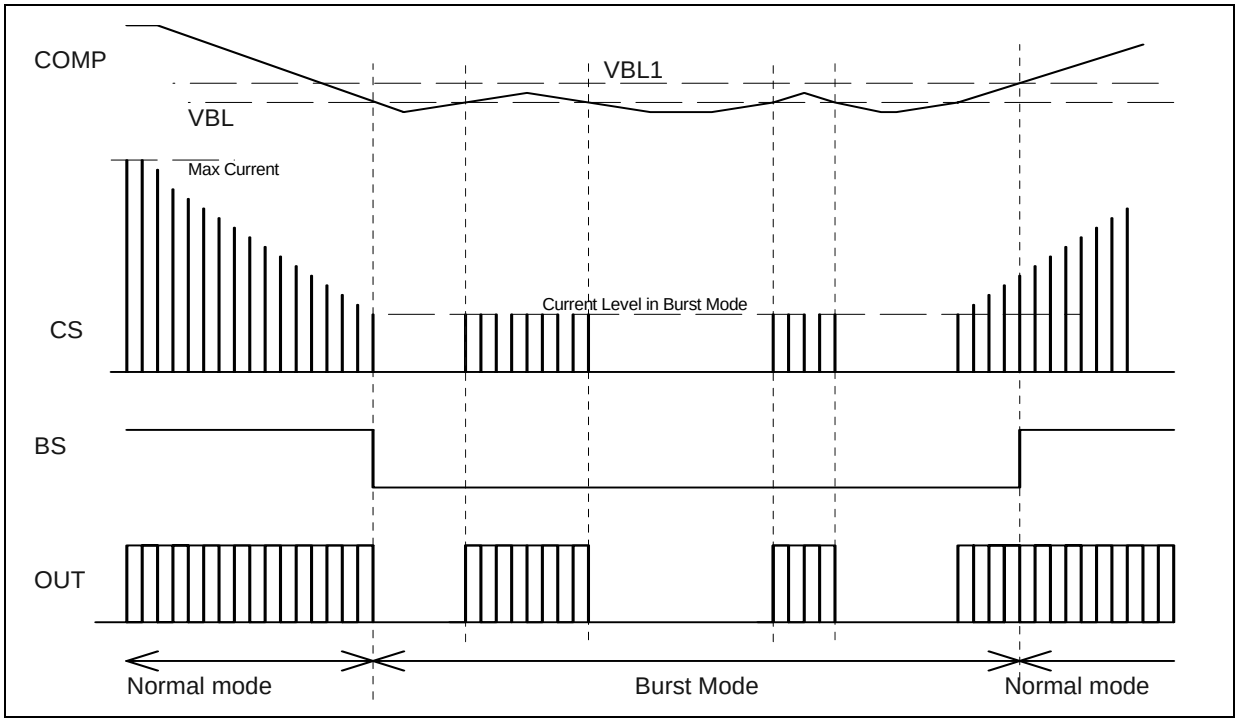
Timing for soft start function



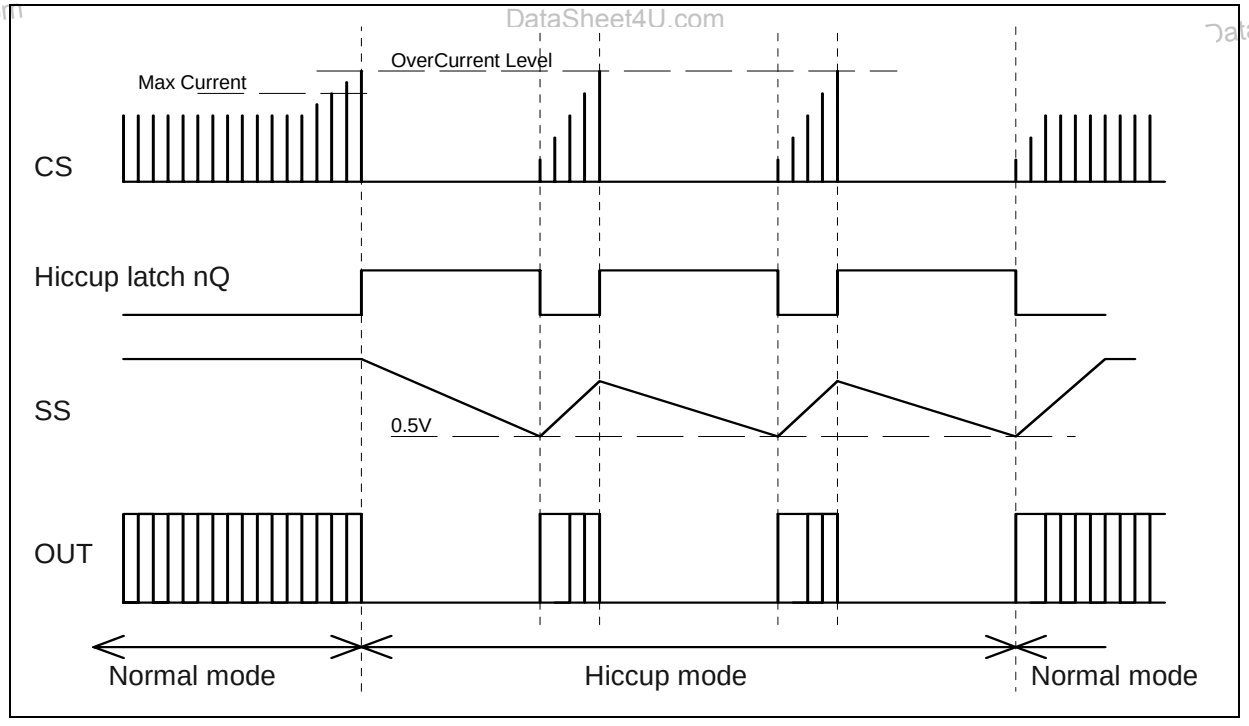
Timing for latched disable function



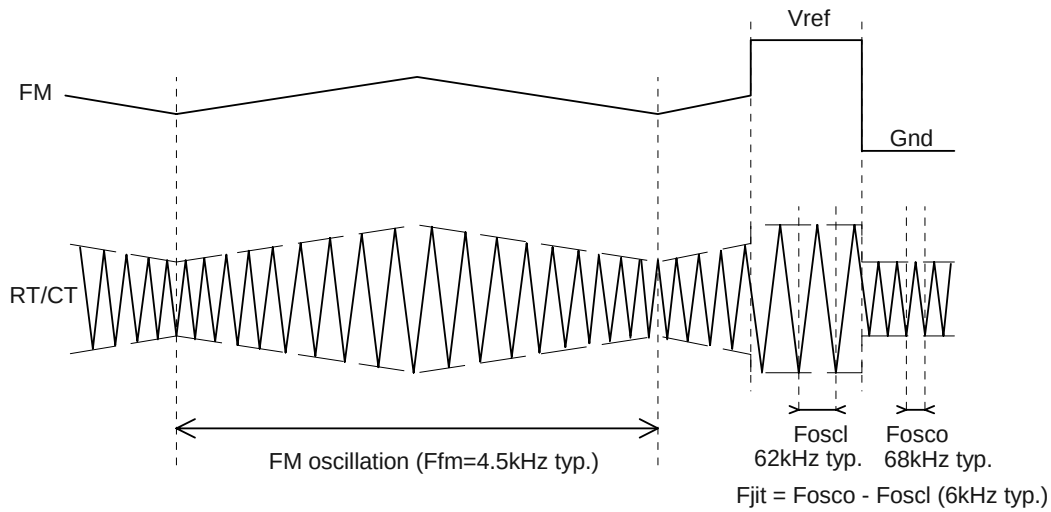
Timing for burst mode function



Timing for hiccup function



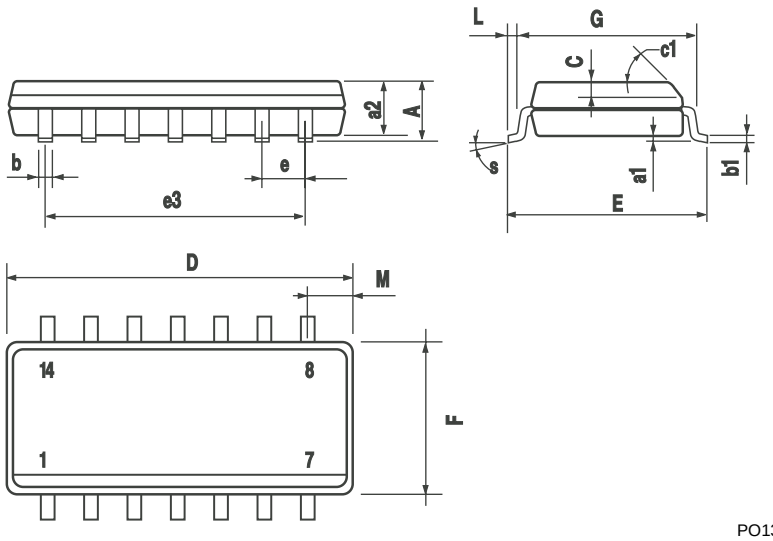
Timing for oscillator function



PACKAGE MECHANICAL DATA

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PO13G