

PRODUCT	:	LCD COG MODULE
MODEL NO.	:	TSE8024DWTDHW-P-G-H-LED
SUPPLIER	:	TRULY SEMICONDUCTORS LTD.
DATE	:	April 13, 2005



CERT. No. 946535

CERT. No. H002005

# SPECIFICATION

( Version :1.0)

1. 1. 1. Product Reversion History		
ver	Contents	date
1.0	Generation first version	2005/4/13

# PRODUCT SPECIFICATIONS

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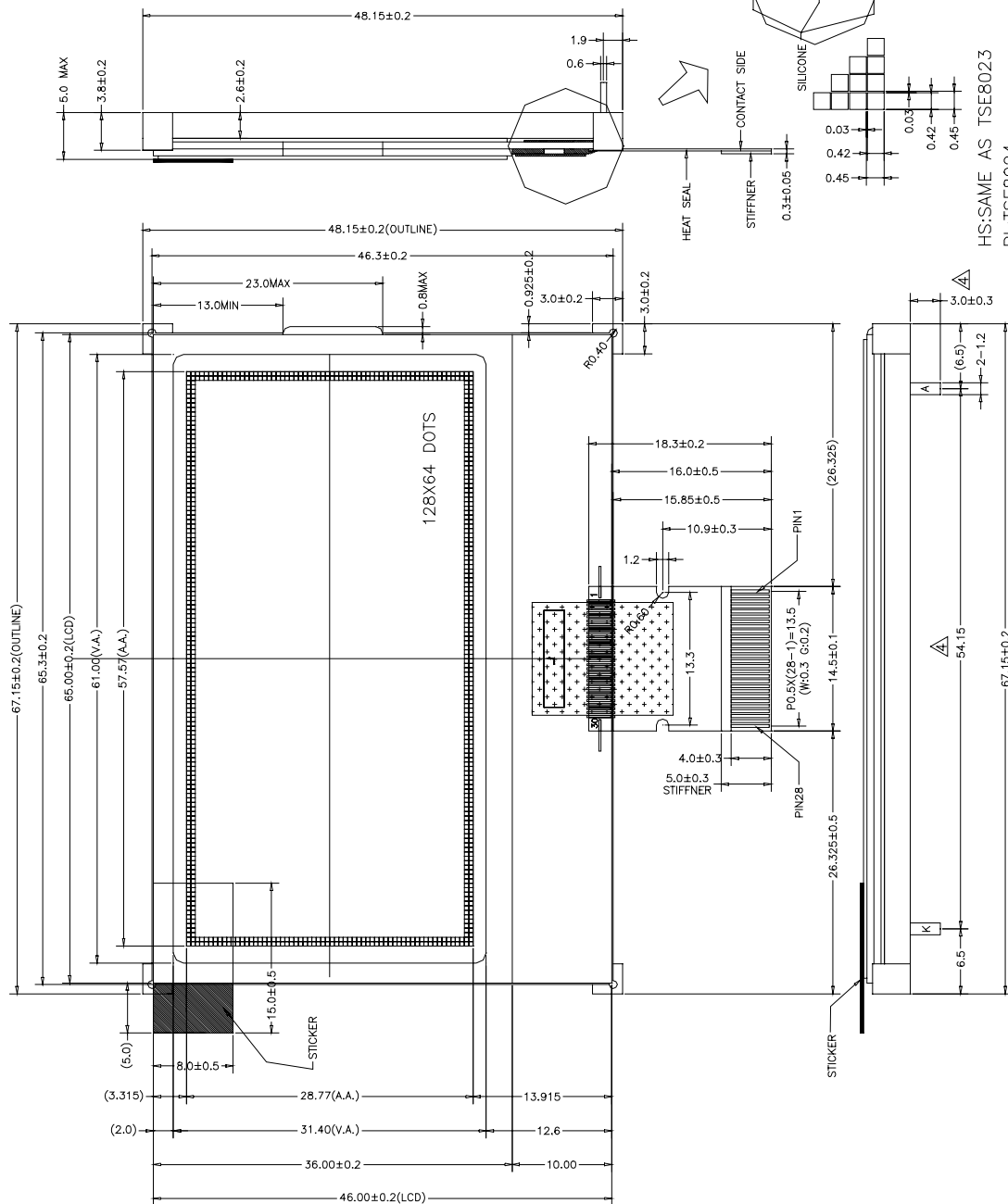
WRITTEN BY	APPROVED BY
Christy	K.K.HO

**■ PHYSICAL DATA**

Item	Contents	Unit
LCD type	FSTN	---
LCD duty	1/65	---
LCD bias	1/9	---
Viewing direction	6	O'Clock
Viewing area (W×H)	61.0 x31.4	mm
Number of dots	128x 64	---
Dot size (W×H)	0.42 × 0.42	mm
Dot pitch (W×H)	0.45 × 0.45	mm
External dimension (WXH)	65.0× 46.0	mm

**EXTERNAL DIMENSIONS**

PIN CONFIGURATION	
PIN1	CS1B
PIN2	RESETB
PIN3	RS
PIN4	RW_WRB
PIN5	E_RDB
PIN6	DB0
PIN7	DB1
PIN8	DB2
PIN9	DB3
PIN10	DB4
PIN11	DB5
PIN12	DB6-SCLK
PIN13	DB7-SID
PIN14	VDD
PIN15	VSS
PIN16	VOUT
PIN17	C4+
PIN18	C3+
PIN19	C1-
PIN20	C1+
PIN21	C2+
PIN22	C2-
PIN23	V1
PIN24	V2
PIN25	V3
PIN26	V4
PIN27	V0
PIN28	PS



TRULY SEMICONDUCTORS LTD.			
PRODUCT NO.	DRAW NO.	REV	
TSE8024	A190 (4-3)	D	
DWN 吕春添	DSN 20040928	20041125	
CHKD 孙伟	20041125	APPD 孙伟	20041125
NOT IN SCALE	UNIT: mm		

HS: SAME AS TSE8023  
BL: TSE8024  
GENERAL TOLERANCE ±0.3



■ BACK LIGHT



SHENZHEN DIGUANG ELECTRICAL CO.,LTD

TEL :86-755-26553580,26611730 FAX :86-755-26634369

Type : DGL-0301W-3AC

Release No. 00

TSE8024

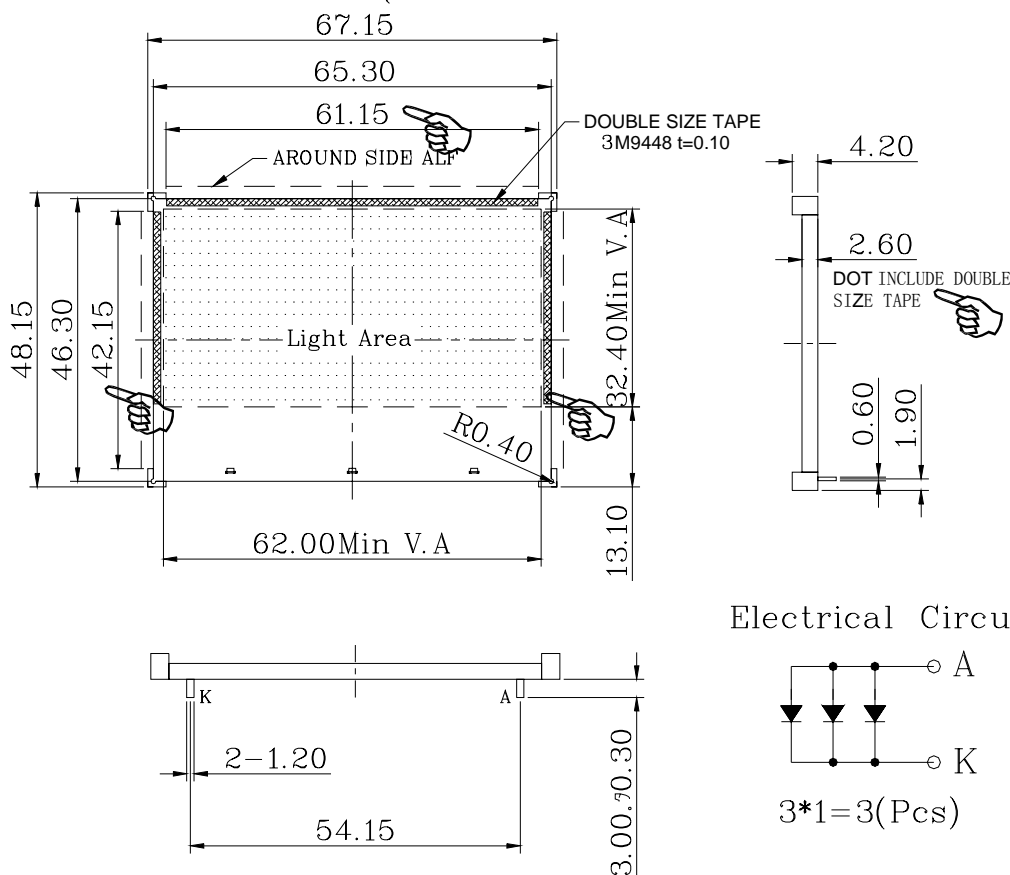
Electronics/Optical Specifications:

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	V <sub>f</sub>	2.9		3.5	V	If= 45.0 mA
Forward Current	I <sub>f</sub>		45.0		mA	
Power Dissipation	P <sub>d</sub>			0.16	W	If= 45.0 mA
Reverse Voltage	V <sub>R</sub>			5.0	V	
Reverse Current	I <sub>R</sub>			0.30	mA	
Luminous Intensity	I <sub>v</sub>	TBD			cd/m <sup>2</sup>	If= 45.0 mA
Luminous Uniformity		70			%	If= 45.0 mA
Emission Wavelength	X	0.283		0.330		If=15mA Ta=25°C Each chip
	Y	0.276		0.339		

	SYMBOL	RATINGS
Operating Temperature	Topr	-20°C to +70°C
	Tsty	-30°C to +75°C

NOTE: The parameters shown in the table are only for your reference. The actual parameters are subject to the specification stated in the sample.

PACKAGE DIMENSIONS (UNIT: mm UNMARKED TOLERANCE: .70.20)



Date	
RevNo	
Revision note	

Design 3 4

20041124

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Approved

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## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	TYP	Max	Unit
Supply voltage for logic	VDD	-0.3	---	7.0	V
Supply voltage for LCD	V0	0.3	---	17	V
Input voltage	V <sub>IN</sub>	-0.3	---	VDD+0.3	V
Operating temperature	TOP	-20	25	70	°C
Storage temperature	TST	-30	25	80	°C

## ■ ELECTRICAL CHARACTERISTICS

### ◇ DC CHARACTERISTICS

(VSS = 0V, VDD = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		VDD	Select by product code		2.4	-	3.6	V	VDD *1
					2.4	-	5.5		
Operating voltage (2)		V0			4.5	-	15.0	V	V0 *2
Input voltage	High	VIH			0.8VDD	-	VDD	V	*3
	Low	VIL			VSS	-	0.2VDD		
Output voltage	High	VOH	IOH = -0.5mA		0.8VDD	-	VDD	V	*4
	Low	VOL	IOL = 0.5mA		VSS	-	0.2VDD		
Input leakage current		IIL	VDD = 3.0V VIN = VDD or VSS		- 1.0	-	+ 1.0	μA	*5
Output leakage current		IOZ	VIN = VDD or VSS		- 3.0	-	+ 3.0	μA	*6
LCD driver ON resistance		RON	Ta = 25°C, V0 = 8V		-	2.0	3.0	kΩ	SEgN COMn *7
Oscillator frequency	Internal	fOSC	VDD = 3.0V Ta = 25°C Duty ratio = 1/65		32.7	43.6	54.5	kHz	CL *8
	External	fCL			4.09	5.45	6.81		
Voltage converter input voltage		VCI	× 2		2.4	-	5.5	V	VCI
			× 3		2.4	-	5.0		
			× 4		2.4	-	3.75		
			× 5		2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load )		95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT			6.0	-	16.0	V	VOUT
Voltage follower operating voltage		V0			4.5	-	15.0	V	V0 *9
Reference voltage		VREF	VDD = 3.0V Ta = 25°C	- 0.05%/°C	2.04	2.1	2.16	V	*10

**Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)**

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	IDD1	VDD = 3.0V V0 – VSS = 11.0V 1/65 duty ratio Display pattern OFF	-	15	23	μA	*11

**Dynamic Current Consumption (2) when the Built-in Power Circuit is ON (At Operate Mode)**

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	IDD2	VDD = 3.0V, (VCI = VDD, 4 times boosting) V0 – VSS = 11.0V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	40	60	μA	*12
		VDD = 3.0V, (VCI = VDD, 4 times boosting) V0 – VSS = 11.0V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	150	200	μA	*12

**Current Consumption during Power Save Mode**

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	IDDS1	VDD = 3.0V During sleep	-	-	2.0	μA	
Standby mode current	IDDS2	VDD = 3.0V During standby	-	-	10.0	μA	



# The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	fCL	fM
1/65	On-chip oscillator circuit is used	$\frac{f_{osc}}{8}$	$\frac{f_{osc}}{2 \times 8 \times 65}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{f_{CL}}{2 \times 65}$
1/55	On-chip oscillator circuit is used	$\frac{f_{osc}}{9}$	$\frac{f_{osc}}{2 \times 9 \times 55}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{f_{CL}}{2 \times 55}$
1/49	On-chip oscillator circuit is used	$\frac{f_{osc}}{10}$	$\frac{f_{osc}}{2 \times 10 \times 49}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{f_{CL}}{2 \times 49}$
1/33	On-chip oscillator circuit is used	$\frac{f_{osc}}{15}$	$\frac{f_{osc}}{2 \times 15 \times 33}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{f_{CL}}{2 \times 33}$

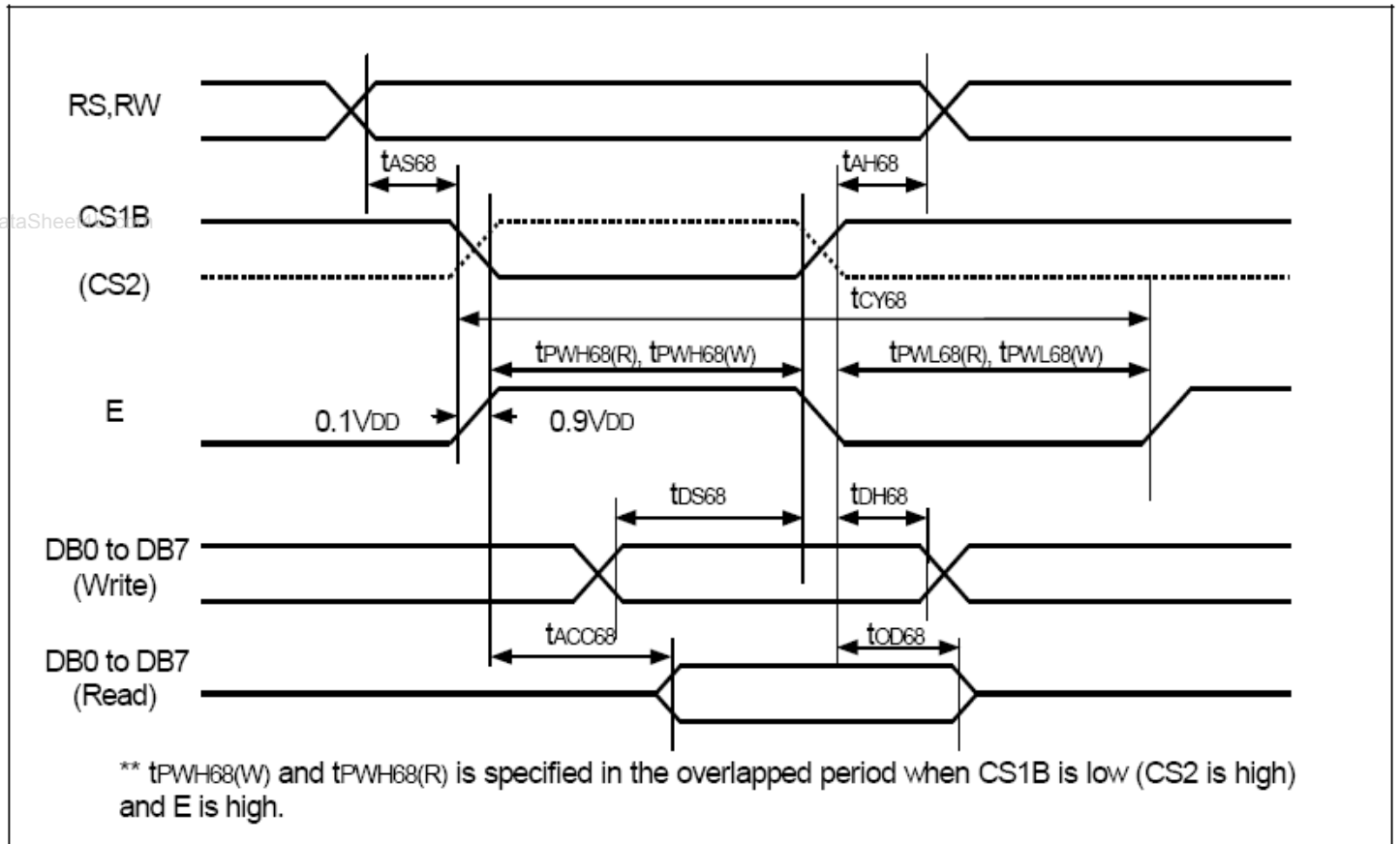
(fosc: oscillation frequency, fCL: display clock frequency, fFR: LCD AC signal frequency)

## [\* Remark Solves]

- \*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
- \*2. In case of external power supply is applied.
- \*3. CS1B, CS2, RS, DB0 to DB7, E\_RDB, RW\_WRB, RESETB, MS, C68, PS, INTR, HPMB, CLS, CL, M, FR, DISP pins.
- \*4. DB0 to DB7, M, FR, DISP, CL pins.
- \*5. CS1B, CS2, RS, DB[7:0], E\_RDB, RW\_WRB, RESETB, MS, C68, PS, INTR, HPMB, CLS, CL, M, FR, DISP pins.
- \*6. Applies when the DB[7:0], M, FR, DISP, and CL pins are in high impedance.
- \*7. Resistance value when  $\pm 0.1$ [mA] is applied during the ON status of the output pin SEGn or COMn.  
 $R_{ON} = \Delta V / 0.1$  [k $\Omega$ ] ( $\Delta V$ : voltage change when  $\pm 0.1$ [mA] is applied in the ON status.)
- \*8. See table 21 for the relationship between oscillation frequency and frame frequency.
- \*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
- \*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
- \*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.  
The current consumption, when the built-in power supply circuit is ON or OFF.  
The current flowing through voltage regulation resistors (Ra and Rb) is not included.  
It does not include the current of the LCD panel capacity, wiring capacity, etc.

# ◇ AC CHARACTERISTICS

## Read/Write Characteristics (6800-series Microprocessor)

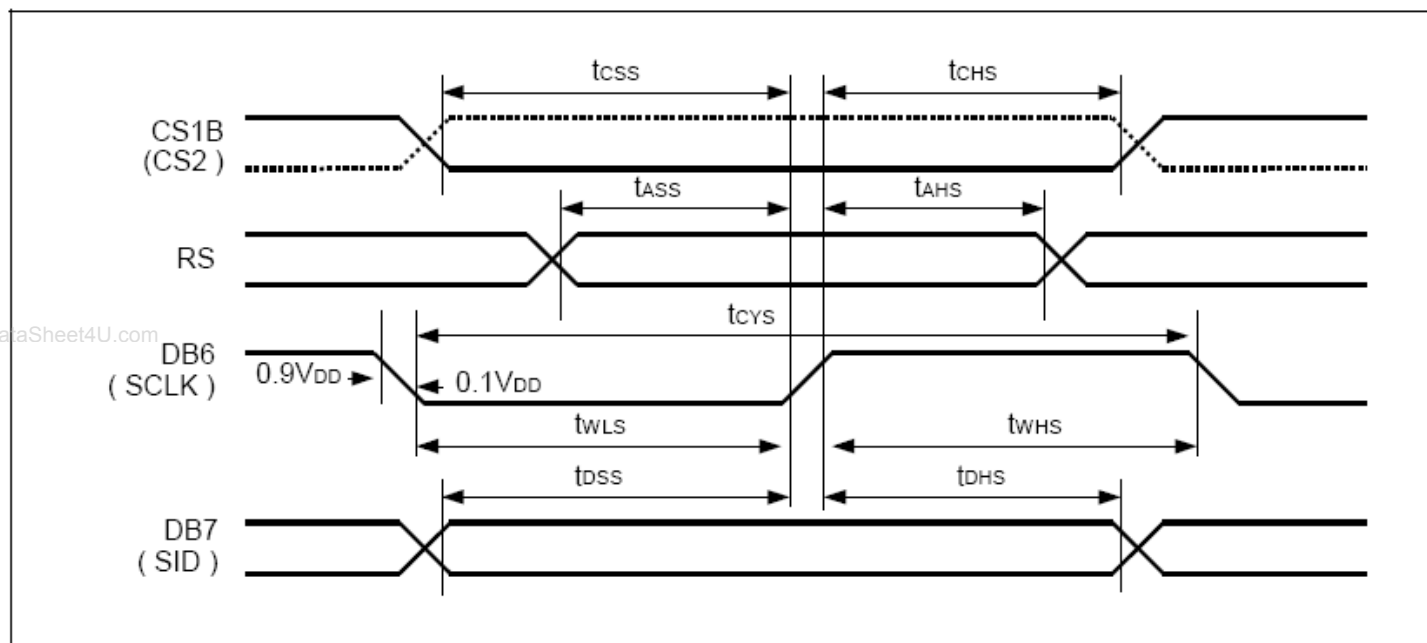


(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time	RS,RW	tAS68	0	-	-	ns	
Address hold time		tAH68	0	-	-	ns	
System cycle time	E	tCY68	300	-	-	ns	
Enable Pulse High Width	Read	E	tPWH68 (R)	120		ns	
	Write		tPWH68 (W)	60			
Enable Pulse Low Width	Read	E	tPWL68 (R)	60		ns	
	Write		tPWL68 (W)	60			
Data setup time	DB7 To DB0	tDS68	40	-	-	ns	
Data hold time		tDH68	15	-	-	ns	
Access time		tACC68	-	-	140	ns	CL = 100 pF
Output disable time		tOD68	10	-	100	ns	

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less.  
Or (tr + tf) < (tCY68 – tPWL68 (W) – tPWH68 (W) ) for write, (tr + tf) < (tCY68 – tPWL68 (R) – tPWH68 (R)) for read.

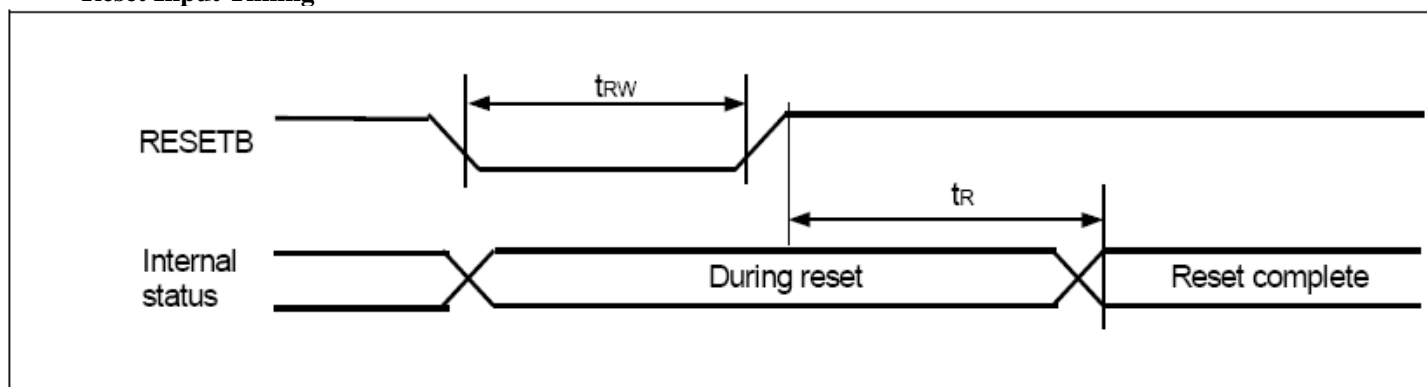
# Series interface Characteristics



(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	DB6 (SCLK)	$t_{CYS}$	250	-	-	ns	
SCLK high pulse width	DB6 (SCLK)	$t_{WHS}$	100	-	-	ns	
SCLK low pulse width	DB6 (SCLK)	$t_{WLS}$	100	-	-	ns	
Address setup time	RS	$t_{ASS}$	150	-	-	ns	
Address hold time	RS	$t_{AHS}$	150	-	-	ns	
Data setup time	DB7 (SID)	$t_{DSS}$	100	-	-	ns	
Data hold time	DB7 (SID)	$t_{DHS}$	100	-	-	ns	
CS1B setup time	CS1B	$t_{CSS}$	150	-	-	ns	
CS1B hold time	CS1B	$t_{CHS}$	150	-	-	ns	

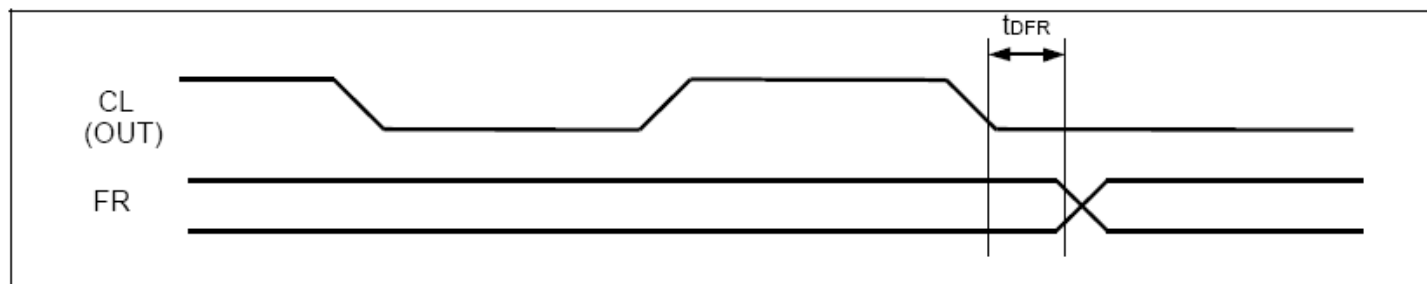
# Reset Input Timing



(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	$t_{RW}$	1.0	-	-	$\mu s$	
Reset time	-	$t_R$	-	-	1.0	$\mu s$	

## Display Control Output Timing



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(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	tDFR	-	20	80	ns	CL = 50 pF

## ■ OPERATING PRINCIPLES & METHODS

### ◇ Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0724 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E\_RDB, and RW\_WRB inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

### ◇ Parallel/ Serial Interface

S6B0724 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*x	Serial-mode

\*x: Don't care

### ◇ Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 9. The type of data transfer is determined by signals at RS, E\_RDB and RW\_WRB as shown in Table 10.

**Table 9. Microprocessor Selection for Parallel Interface**

C68	CS1B	CS2	RS	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RDB	/WRB	DB0 to DB7	8080-series

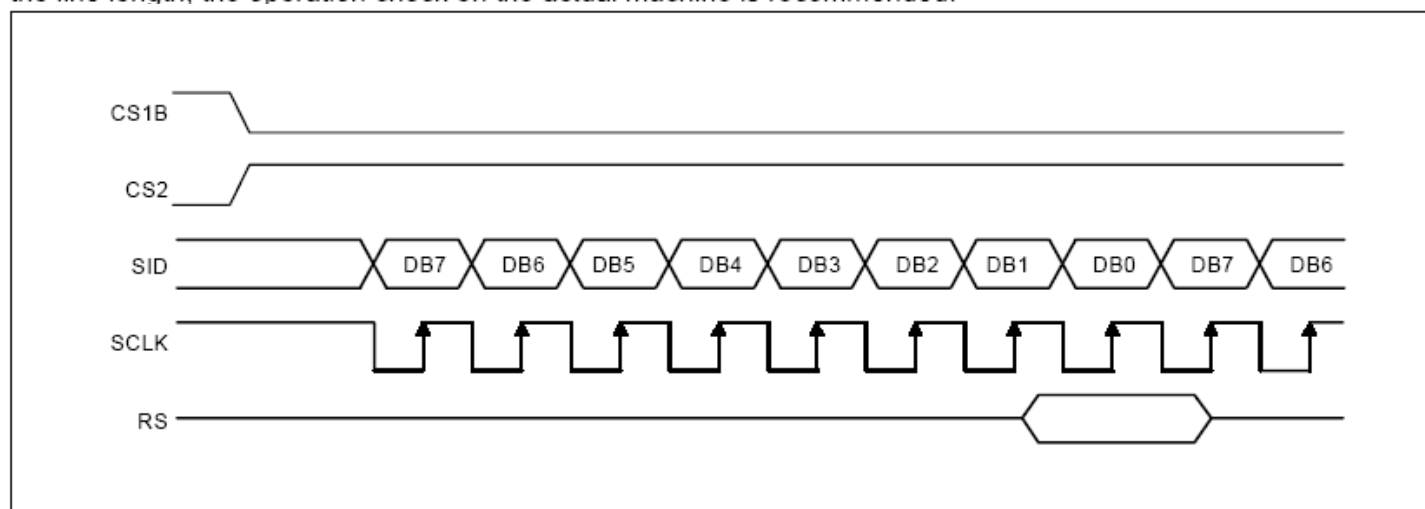
**Table 10. Parallel Data Transfer**

Common	6800-series		8080-series		Description
RS	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

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### ◇ Serial Interface (PS = "L")

When the S6B0724 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

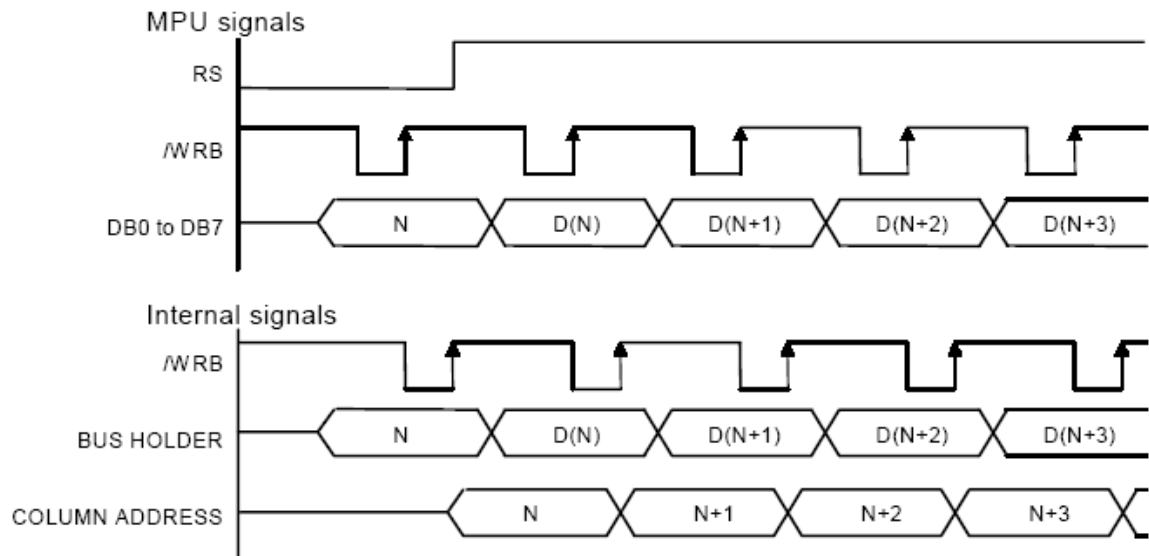

**Figure 5. Serial Interface Timing**

### ◇ Busy Flag

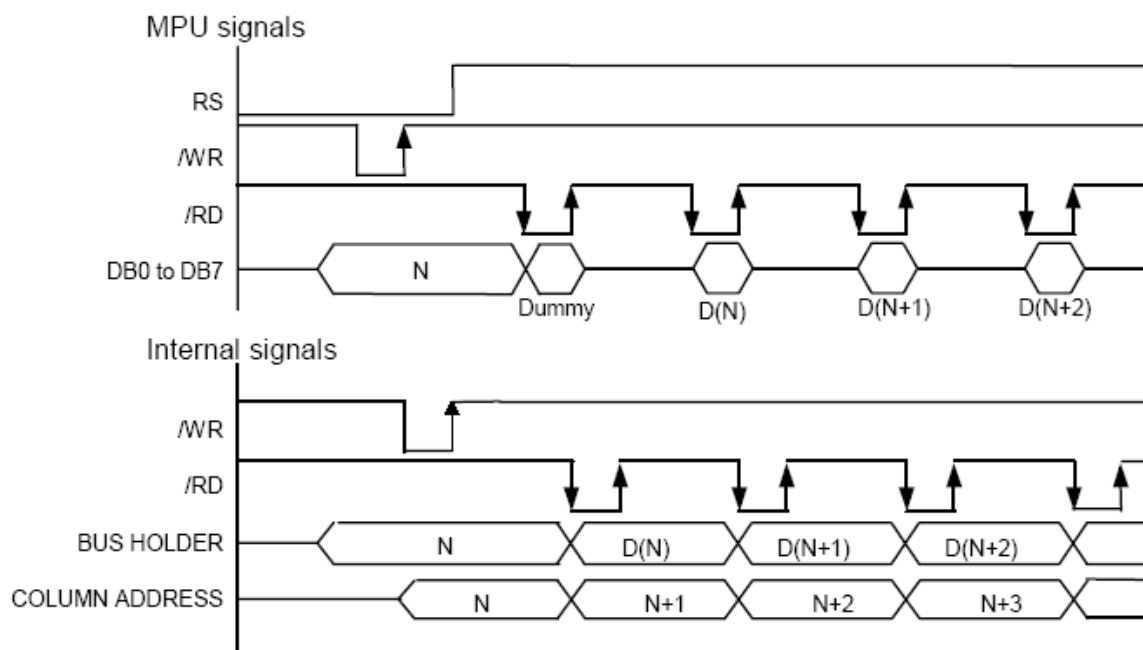
The Busy Flag indicates whether the S6B0724 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

### ◇ Data Transfer

The S6B0724 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.



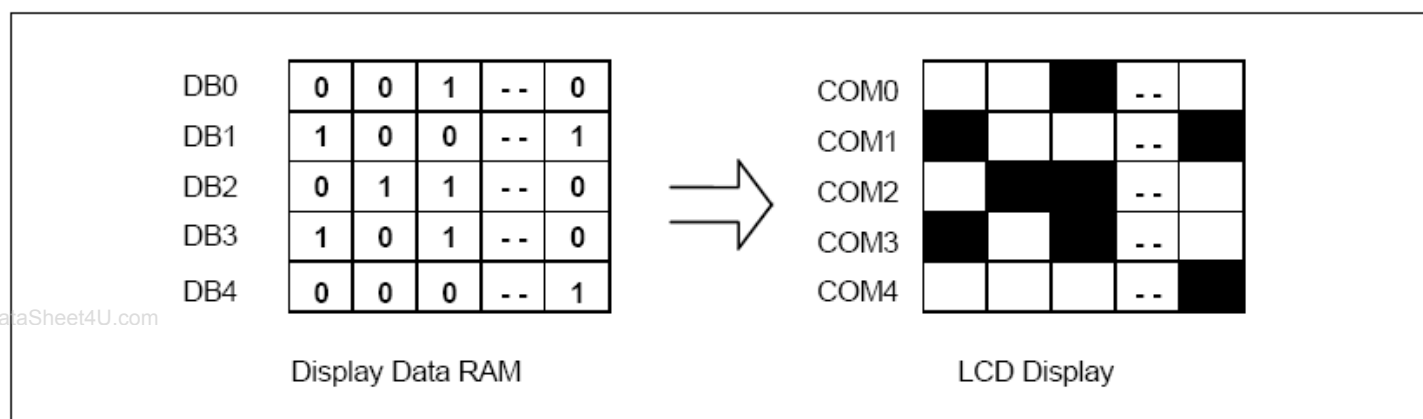
**Figure 6. Write Timing**



**Figure 7. Read Timing**

### ◇ DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.



**Figure 8. RAM-to-LCD Data Transfer**

### ◇ Page Address Circuit

This circuit is for providing a Page Address to DISPLAY-DATA-RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.


















### ◇ Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

### ◇ Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC Select instruction. Refer to the following figure 7.

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	... ..	SEG 128	SEG 129	SEG 130	SEG 131
Column address [Y7:Y0]	00H	01H	02H	03H	... ..	80H	81H	82H	83H
Display data	1	0	1	0		1	1	0	0
LCD panel display (ADC = 0)					... ..				
									
LCD panel display ( ADC = 1 )					... ..				

**Figure 9. The Relationship between the Column Address and the Segment Outputs**



# ◇ Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

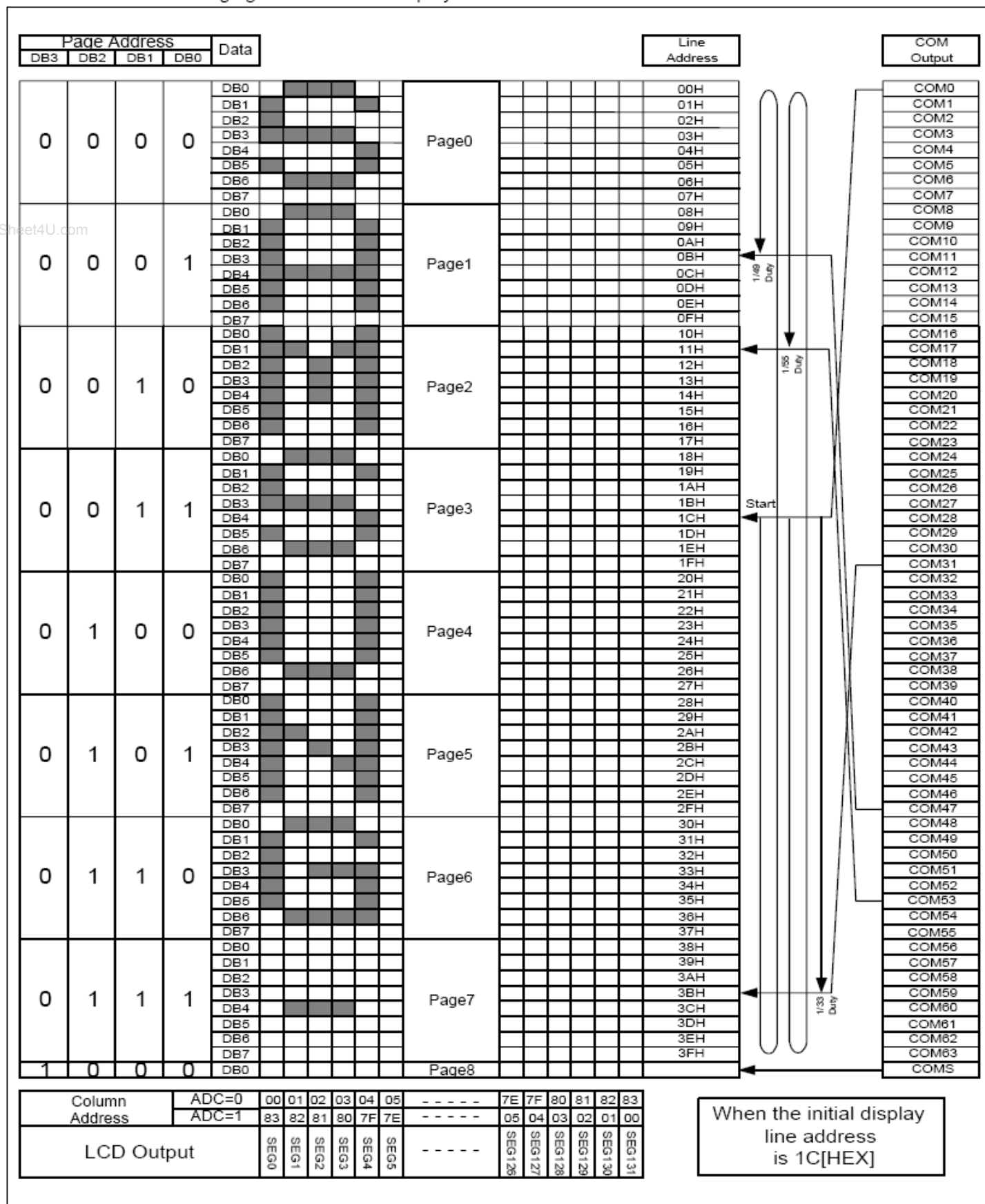


Figure 10. Display Data RAM Map

**■ INTERFACE PIN CONNECTIONS**

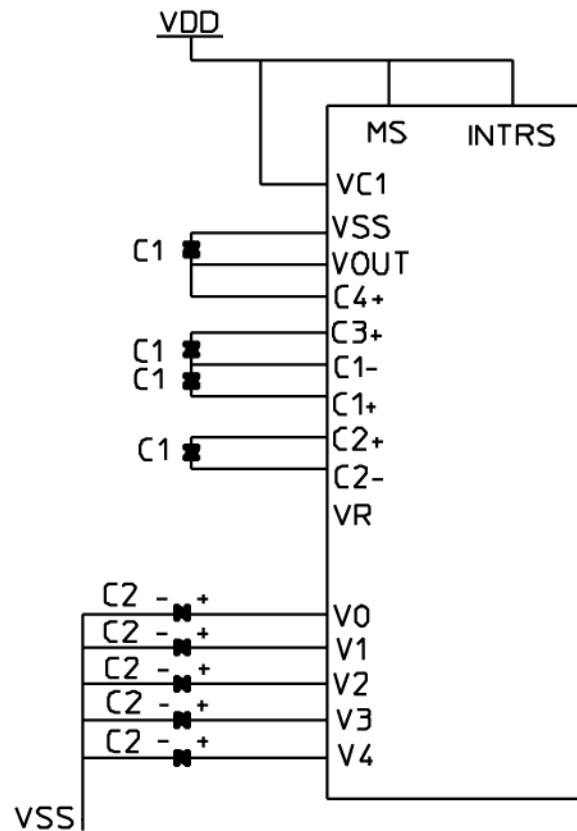
Pin No.	Symbol	Level	Description
1	CSB1	H/L	Chip select input pin
2	RESETB	L	Reset signal
3	RS	H/L	Register/Memory Select
4	RW_WEB	H/L	Read / Write execution control pin
5	E_RDB	H/L	Read / Write execution control pin
6	DB0	H/L	Data bit 0
7	DB1	H/L	Data bit 1
8	DB2	H/L	Data bit 2
9	DB3	H/L	Data bit 3
10	DB4	H/L	Data bit 4
11	DB5	H/L	Data bit 5
12	DB6-SCLK	H/L	Data bit 6
13	DB7-SID	H/L	Data bit 7
14	VDD	2.4~3.6	Supply voltage for logic
15	VSS	---	Ground
16	VOUT	8.7V	Voltage convert input / output pin
17	C4+	---	Capacitor 4 negative connection pin for voltage convert
18	C3+	---	Capacitor 3 negative connection pin for voltage convert
19	C1-	---	Capacitor 1 negative connection pin for voltage convert
20	C1+	---	Capacitor 1 negative connection pin for voltage convert
21	C2+	---	Capacitor 2 negative connection pin for voltage convert
22	C2-	---	Capacitor 2 negative connection pin for voltage convert
23	V1	---	Bias supply voltage
24	V2	---	Bias supply voltage
25	V3	---	Bias supply voltage
26	V4	---	Bias supply voltage
27	V0	---	Bias supply voltage
28	PS	H/L	Parallel / serial data input select pin

## ■ INTERFACE PIN CONNECTIONS

### Reference circuit example

Value of external capacitors:

Item	Value	Unit
C1	1.0 to 4.7	uF
C2	0.47 to 1.0	uF

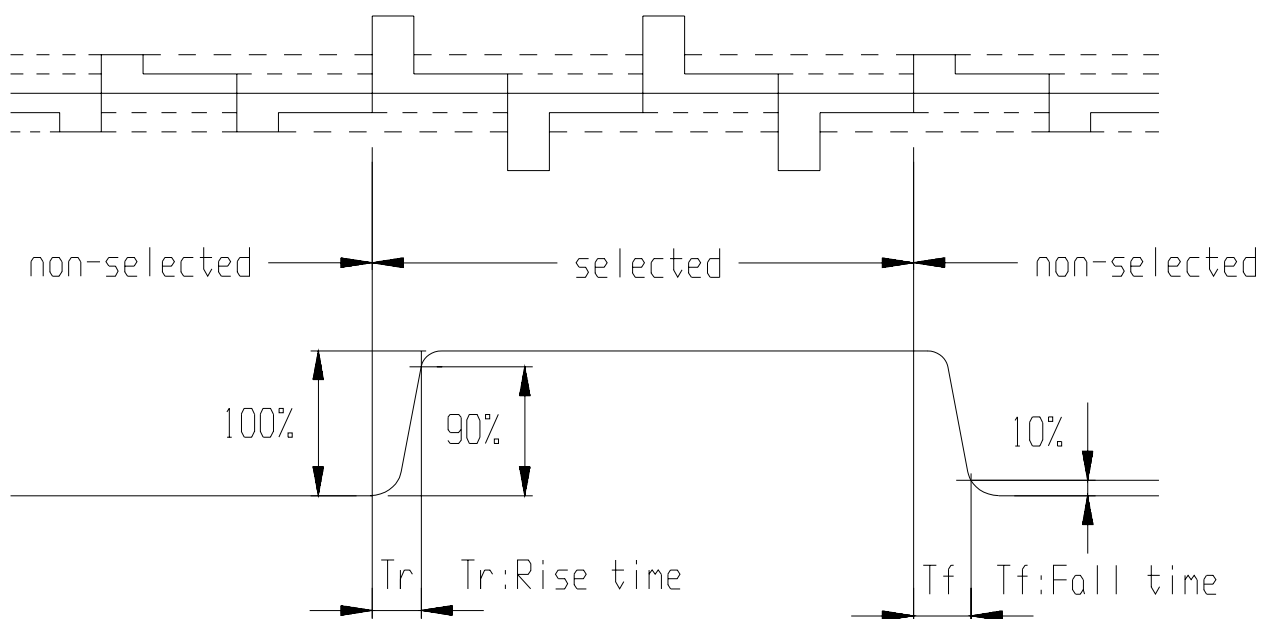


# ELECTRO-OPTICAL CHARACTERISTICS ( VLCD =11V, Ta = 25 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response time	Tr	Ta = 25 °C	---	161	---	ms	---	1
	Tf		---	198	---	ms	---	1
Contrast ratio	Cr	---	---	9.6	---	---	---	2
Viewing angle range	$\theta$	$Cr \geq 2$	32	---	---	deg	$\varnothing = 90$	3
			32	---	---	deg	$\varnothing = 270$	3
			54	---	---	deg	$\varnothing = 0$	3
			34	---	---	deg	$\varnothing = 180$	3

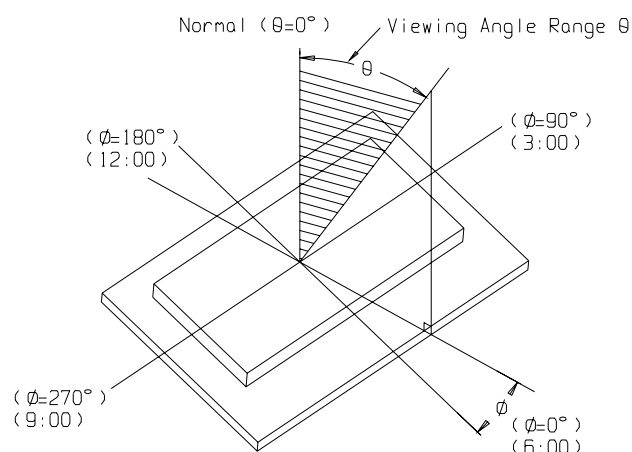
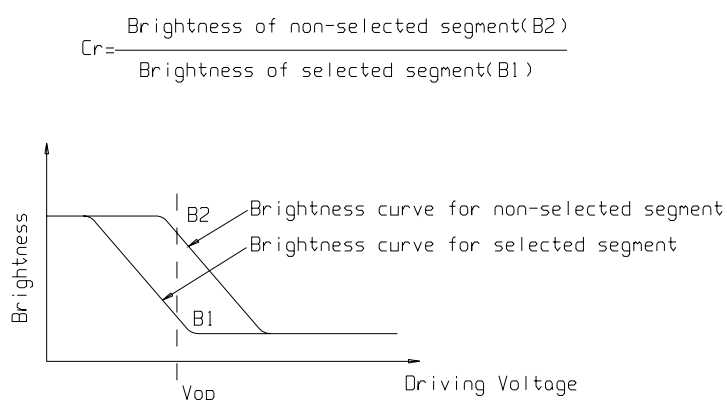
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Note1: Definition of response time.

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Note2: Definition of contrast ratio Cr .

Note3: Definition of viewing angle range ' $\theta$ '.



## ■ RELIABILITY

### ◇ Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Inspection Criterion
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200 hrs	1,Functional test is OK Missing segment, shorts , unclear segment, nondisplay, display abnormally, liquid crystal leak is unallowed. 2,After testing , the current IDD should be within initial value ± 20% . 3,No low temperature bubbles, end seal loose and fall, frame rainbow, ACF bubble growing are allowable in the appearance test.
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C 200 hrs	
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200 hrs	
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20 °C 200 hrs	
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	50°C , 90 %RH 96 hrs	
6	Temperature cycle	Endurance test applying the low and high temperature cycle. <div><div><div>-20°C 30min</div><div>⇌</div><div>25°C 5min.</div><div>⇌</div><div>70°C 30min</div></div><div>← 1 cycle →</div></div>	-20°C /70°C 10 cycles	
Mechanical Test				
7	Vibration test	Endurance test applying the vibration during transportation and using.	10~55Hz → 1.5mmp-p X,Y,Z-axes Total 2/3hrs	1,Functional test is OK. 2,No glass crack, chipped glass, end seal loose and fall, epoxy frame crack and so on. 3,No structure loose and fall
8	Dropping test	Pack it into the carton box and drop it from one meter to ground. Drop it one time for every side of the carton.	---	
Others				
9	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V , RS=1.5 kΩ CS=100 pF 1 time	After test ,current IDD should be below double of initial value

Remark:

- 1,Vibration test: it is not necessary to test for those products without assembly frame, back-light ,PCB and so on.
- 2,Dropping test: the OQA should take the test while affirming its new package.
- 3,For the test item of 1~~6
  - I. Each test item applies for a test LCD only once. The tested LCD is not used in any other tests.
  - II. Number of examinations for each test item is 5pcs to 10pcs.
  - III. For the high temperature and high humidity test., Pure water should be used.
  - IV. The test LCD is inspected after 2 hours or more of storage at room temperature and room humidity after each test is finished.

### ◇ Failure Judgment Criterion

Criterion Item	Failure Judgment Criterion									
	1	2	3	4	5	6	7	8	9	
Basic specification	O	O	O	O	O	O	O	O	O	Out of the Basic Specification
Electrical characteristic	O	O	O	O	O	O	O	O	O	Out of the DC and AC Characteristic
Mechanical characteristic	O	O	O	O	O	O	O	O	O	Out of the Mechanical Specification Color change : Out of Limit Appearance Specification
Optical characteristic	O	O	O	O	O	O	O	O	O	Out of the Appearance Standard

Note: O—OK X--NG

## ■ QUALITY GUARANTEE

### ◇ Acceptable Quality Level

Each lot should satisfy the quality level defined as follows.

- Inspection method : MIL-STD-105E LEVEL II Normal one time sampling
- AQL

Partition	AQL	Definition
A: Major	0.65%	Functional defective as product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

### ◇ Definition of 'LOT'

One lot means the delivery quantity to customer at one time.

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### ◇ Conditions of Cosmetic Inspection

- Environmental condition

The inspection should be performed at the 1m of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25°C and normal humidity 60±15%RH).

- Inspection method

The visual check should be performed vertically at more than 30cm distance from the LCD panel.

# INSPECTION CRITERIA

TRULY SEMICONDUCTORS LTD.

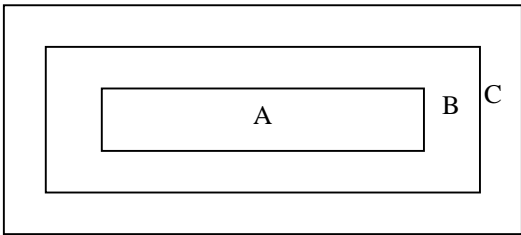
OUTGOING QUALITY STANDARD

FOR

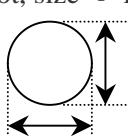
STN LCM MODULE

DOCUMENT CONTROL RELEASE EFFECTIVE DATE

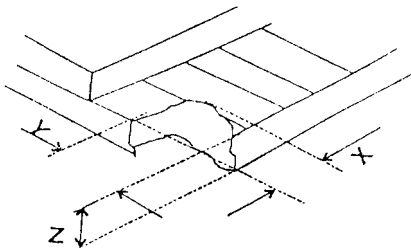
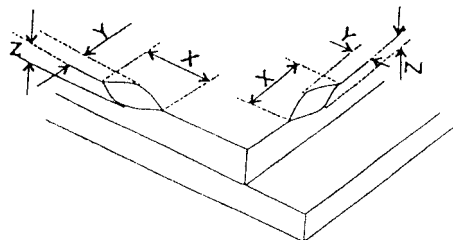
CUSTOMER:		TRULY SEMICONDUCTORS LTD.	
CONFIRMED BY/DATE:		Prepared by:	Liu Dong
		Approved by:	Lin Jun Long
		Date:	2001/05/11

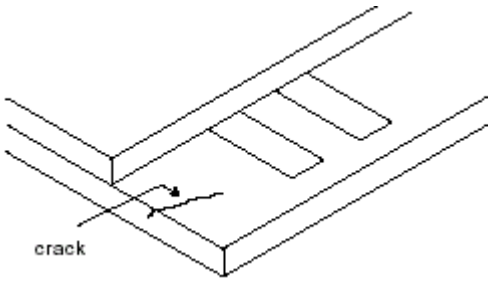
OUTGOING QUALITY CONTROL SPECIFICATION	PAGE 1 OF 5	
	SPECIFICATION NUMBER	REV
TITLE:FUNCTIONAL TEST & INSPECTION CRITERIA	TSTN-001	A
<p>This specification is made to be used as the standard acceptance/rejection criteria for STN LCM.</p> <p>1. Sample plan</p> <p>Sampling plan according to MIL-STD-105D level 2, and acceptance/rejection criteria is based on:</p> <p>Major defect: AQL 0.65</p> <p>Minor defect: AQL 1.5</p> <p>2. Inspection condition</p> <p>Viewing distance for cosmetic inspection is about 30cm with bare eyes, and under an environment of 20~40W light intensity, all directions for inspecting the sample should be within 45° against perpendicular line.</p> <p>3. Definition of inspection zone in LCD.</p> <div data-bbox="453 1151 976 1384" data-label="Diagram">  </div> <p>Zone A: character/Digit area</p> <p>Zone B: viewing area except Zone A (ZoneA+ZoneB=minimum Viewing area)</p> <p>Zone C: Outside viewing area (invisible area after assembly in customer's product)</p> <p>Fig.1 Inspection zones in an LCD.</p> <p>Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.</p>		



OUTGOING QUALITY CONTROL SPECIFICATION		PAGE 2 OF 5																												
		SPECIFICATION NUMBER	REV																											
TITLE:FUNCTIONAL TEST & INSPECTION CRITERIA		TSTN-001	A																											
4. Major Defect																														
Item No	Items to be inspected	Inspection Standard	Classification of defects																											
4.1	All functional defects	1) No display 2) Display abnormally 3) Open or missing segment 4) Short circuit 5) Excess power consumption 6) Back-light unlighted	Major																											
4.2	Missing	Missing component																												
4.3	Outline dimension	Overall outline dimension beyond the drawing is not allowed.																												
5. Cosmetic Defect																														
Item No	Items to be inspected	Inspection Standard	Classification of defects																											
5.1	Black Spot white Spot Pinhole	<table><tr><th rowspan="2">Zone Size(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td><math>\Phi \leq 0.10</math></td><td colspan="3">Acceptable (cluttering of spot not allowed)</td></tr><tr><td><math>0.10 &lt; \Phi \leq 0.15</math></td><td colspan="3">3</td></tr><tr><td><math>0.15 &lt; \Phi \leq 0.20</math></td><td colspan="3">2</td></tr><tr><td><math>0.20 &lt; \Phi \leq 0.25</math></td><td colspan="3">1</td></tr><tr><td><math>\Phi &gt; 0.25</math></td><td colspan="3">0</td></tr></table> <p>Remarks: For dark/white spot, size <math>\Phi</math> is defined</p> <p>as <math>\Phi = (X+Y) / 2</math></p> <div><div>y</div><div>x</div></div>	Zone Size(mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.10$	Acceptable (cluttering of spot not allowed)			$0.10 < \Phi \leq 0.15$	3			$0.15 < \Phi \leq 0.20$	2			$0.20 < \Phi \leq 0.25$	1			$\Phi > 0.25$	0			Minor
Zone Size(mm)	Acceptable Qty																													
	A	B	C																											
$\Phi \leq 0.10$	Acceptable (cluttering of spot not allowed)																													
$0.10 < \Phi \leq 0.15$	3																													
$0.15 < \Phi \leq 0.20$	2																													
$0.20 < \Phi \leq 0.25$	1																													
$\Phi > 0.25$	0																													

OUTGOING QUALITY CONTROL SPECIFICATION		PAGE 3 OF 5																																		
		SPECIFICATION NUMBER		REV																																
TITLE:FUNCTIONAL TEST & INSPECTION CRITERIA		TSTN-001		A																																
5. Cosmetic Defect																																				
Item No	Items to be inspected	Inspection Standard			Classification of defects																															
5.2	Line defect (Defects in line form)	<table><tr><td colspan="2">Size(mm)</td><td colspan="3">Acceptable Qty</td></tr><tr><td rowspan="2">L(Length)</td><td rowspan="2">W(Width)</td><td colspan="3">Zone</td></tr><tr><td>A</td><td>B</td><td>C</td></tr><tr><td>Acceptable</td><td><math>W \leq 0.02</math></td><td colspan="2">Acceptable</td><td rowspan="3">Accept</td></tr><tr><td><math>L \leq 3.0</math></td><td><math>0.02 &lt; W \leq 0.05</math></td><td colspan="2">2</td></tr><tr><td><math>L \leq 2.0</math></td><td><math>0.05 &lt; W \leq 0.08</math></td><td colspan="2">1</td></tr><tr><td>---</td><td><math>W &gt; 0.08</math></td><td colspan="3">Counted as spot defect (follows item 5.1)</td></tr></table> <p>Remarks: The total of spot defect and line defect shall not exceed four</p>			Size(mm)		Acceptable Qty			L(Length)	W(Width)	Zone			A	B	C	Acceptable	$W \leq 0.02$	Acceptable		Accept	$L \leq 3.0$	$0.02 < W \leq 0.05$	2		$L \leq 2.0$	$0.05 < W \leq 0.08$	1		---	$W > 0.08$	Counted as spot defect (follows item 5.1)			Minor
Size(mm)		Acceptable Qty																																		
L(Length)	W(Width)	Zone																																		
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$L \leq 2.0$	$0.05 < W \leq 0.08$	1																																		
---	$W > 0.08$	Counted as spot defect (follows item 5.1)																																		
5.3	polarizing	<p>5.3.1 Polarizer Position</p> <p>(i) Shifting in position should not exceed the glass outline dimension</p> <p>(ii) Incomplete covering of the viewing area due to shifting is not allowed.</p> <p>5.3.2 Polarizer Nick &amp; Dent</p> <table><tr><td rowspan="3">Sizes(mm)</td><td colspan="3">Acceptable Qty</td></tr><tr><td colspan="3">Zone</td></tr><tr><td>A</td><td>B</td><td>C</td></tr><tr><td><math>\Phi \leq 0.1</math></td><td colspan="2">Acceptable</td><td rowspan="3">Acceptable</td></tr><tr><td><math>0.1 &lt; \Phi \leq 0.25</math></td><td colspan="2">2</td></tr><tr><td><math>\Phi &gt; 0.25</math></td><td colspan="2">0</td></tr></table>			Sizes(mm)	Acceptable Qty			Zone			A	B	C	$\Phi \leq 0.1$	Acceptable		Acceptable	$0.1 < \Phi \leq 0.25$	2		$\Phi > 0.25$	0		Minor											
Sizes(mm)	Acceptable Qty																																			
	Zone																																			
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OUTGOING QUALITY CONTROL SPECIFICATION		PAGE 4 OF 5																						
		SPECIFICATION NUMBER	REV																					
TITLE:FUNCTIONAL TEST & INSPECTION CRITERIA		TSTN-001	A																					
5. Cosmetic Defect																								
Item No	Items to be inspected	Inspection Standard	Classification of defects																					
5.3	Polarizing	<div>5.3.3 Air bubbles between glass &amp; polarizer:</div> <table><tr><th>Zone Size(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th></th><th>A</th><th>B</th><th>C</th></tr><tr><td><math>\Phi \leq 0.15</math></td><td colspan="3" rowspan="4">Acceptable</td></tr><tr><td><math>0.15 &lt; \Phi \leq 0.30</math></td><td>2</td><td>3</td></tr><tr><td><math>0.30 &lt; \Phi \leq 0.50</math></td><td>1</td><td>2</td></tr><tr><td><math>\Phi &gt; 0.50</math></td><td>0</td><td>0</td></tr></table>	Zone Size(mm)	Acceptable Qty				A	B	C	$\Phi \leq 0.15$	Acceptable			$0.15 < \Phi \leq 0.30$	2	3	$0.30 < \Phi \leq 0.50$	1	2	$\Phi > 0.50$	0	0	Minor
Zone Size(mm)	Acceptable Qty																							
	A	B	C																					
$\Phi \leq 0.15$	Acceptable																							
$0.15 < \Phi \leq 0.30$				2	3																			
$0.30 < \Phi \leq 0.50$				1	2																			
$\Phi > 0.50$				0	0																			
5.4	Glass defect	<div>(i) Chips on corner</div>  <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td><math>\leq 2.0</math></td><td><math>\leq S</math></td><td>Disregard</td></tr></table> <div>Notes: S=contact pad length</div> <div>Chips on the corner of terminal shall not be allowed to extend into the ITO pad.</div> <div>(ii) Chips on usual surface</div>  <table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td><math>\leq 1/6a</math></td><td><math>\leq 1.0</math></td><td><math>\leq t</math></td></tr></table> <div>Note: 1. Chips on corners are allowed but can't extend into or expose perimeter seal.</div> <div>2. The total number of the glass defect should not be more than four.</div>	X	Y	Z	$\leq 2.0$	$\leq S$	Disregard	X	Y	Z	$\leq 1/6a$	$\leq 1.0$	$\leq t$	Minor									
X	Y	Z																						
$\leq 2.0$	$\leq S$	Disregard																						
X	Y	Z																						
$\leq 1/6a$	$\leq 1.0$	$\leq t$																						

OUTGOING QUALITY CONTROL SPECIFICATION		PAGE 5 OF 5	
		SPECIFICATION NUMBER	REV
TITLE:FUNCTIONAL TEST & INSPECTION CRITERIA		TSTN-001	A
Item No	Items to be inspected	Inspection Standard	Classification of defects
5.4	Glass defect	(iii) Creak Creaks tend to break are not allowed. 	Major
5.5	Back-light	1) The brightness and color of backlight should correspond it is specification. 2) Not allow flash on back-light 3) Dust and black dot on back-light: $\Phi \leq 0.25\text{mm}$	Minor
	Conductive foreign matter	Not allow removable and $\Phi > 0.15\text{mm}$ solder splash or solder ball on PCB/FPC.	
	Parts alignment	1) Not allow IC and FPC/heat-seal lead width is more than 50% beyond lead pattern. 2) Not allow chip or solder component is off center more than 50% of the pad outline.	

## ■ PRECAUTIONS FOR USING LCD MODULES

### ◇ Handling Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :
  - Isopropyl alcohol
  - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
  - Water
  - Ketone
  - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- (8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
- (9) Do not attempt to disassemble or process the LCD module.
- (10) NC terminal should be open. Do not connect anything.
- (11) If the logic circuit power is off, do not apply the input signals.
- (12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - Be sure to ground the body when handling the LCD modules.
  - Tools required for assembling, such as soldering irons, must be properly grounded.
  - To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
  - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

### ◇ Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

### ◇ Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

## ■ USING LCD MODULES

### ◇ Liquid Crystal Display Modules

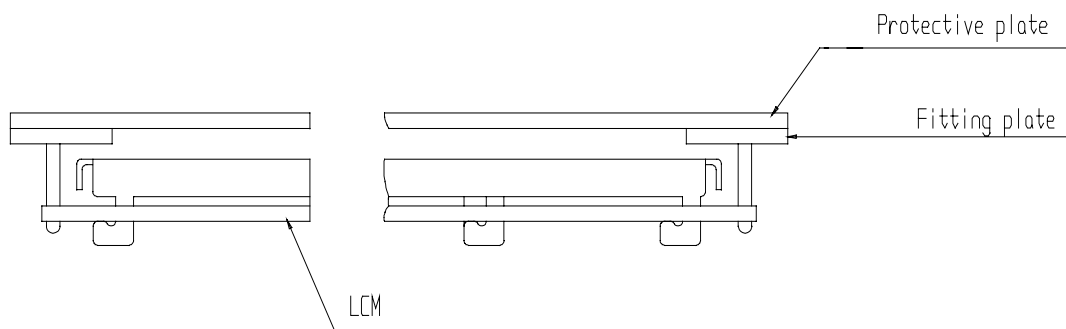
LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- (2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.
- (5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
- (6) Avoid contacting oil and fats.
- (7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming in contact with room temperature air.
- (8) Do not put or attach anything on the display area to avoid leaving marks on.
- (9) Do not touch the display with bare hands. This will stain the display area and degrade insulation between terminals (some cosmetics are detrimental to the polarizers).
- (10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

### ◇ Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

- (1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



- (2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be  $\pm 0.1\text{mm}$ .

### ◇ Precaution for Handling LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

- (1) Do not alter, modify or change the shape of the tab on the metal frame.
- (2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- (3) Do not damage or modify the pattern writing on the printed circuit board.
- (4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
- (5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- (6) Do not drop, bend or twist LCM.

### ◇ Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

- (1) Make certain that you are grounded when handling LCM.
- (2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- (3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- (4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
- (5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
- (6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

### ◇ Precaution for soldering to the LCM

- (1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.
  - Soldering iron temperature :  $280^{\circ}\text{C} \pm 10^{\circ}\text{C}$ .
  - Soldering time : 3-4 sec.
  - Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electoluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

### ◇ Storage

When storing LCDs as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between  $0^{\circ}\text{C}$  and  $35^{\circ}\text{C}$ .
- (3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)
- (4) Environmental conditions :
  - Do not leave them for more than 168hrs. at  $90^{\circ}\text{C}$ .
  - Should not be left for more than 48hrs. at  $-20^{\circ}\text{C}$ .

### ◇ Safety

- (1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

### ◇ Limited Warranty

Unless agreed between TRULY and customer, TRULY will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with TRULY LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TRULY limited to repair and/or replacement on the terms set forth above. TRULY will not be responsible for any subsequent or consequential events.

### ◇ Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.