1.2V to 3.6V, 12-Bit, Nanopower, 4-Wire Micro TOUCH SCREEN CONTROLLER with SPI™

Check for Samples: TSC2008-Q1

FEATURES

- **Qualified for Automotive Applications**
- **4-Wire Touch Screen Interface**
- **Single 1.2V to 3.6V Supply/Reference**
- **Ratiometric Conversion**
- **Effective Throughput Rate:**
  - **Up to 20kHz (8-Bit) or 10kHz (12-Bit)**
- **Preprocessing to Reduce Bus Activity**
- **High-Speed SPI (up to 25MHz)**
- **Simple Command-Based User Interface:**
  - **TSC2046 Compatible**
  - **8- or 12-Bit Resolution**
- **On-Chip Temperature Measurement**
- **Touch Pressure Measurement**
- **Digital Buffered $\overline{\text{PENIRQ}}$**
- **On-Chip, Programmable $\overline{\text{PENIRQ}}$ Pull-up**
- **Auto Power-Down Control**
- **Low Power (12-Bit, 8.2kHz Eq Rate):**
  - **30.4µA at 1.2V, f_{SCLK} = 5MHz**
  - **35.5µA at 1.8V, f_{SCLK} = 10MHz**
  - **44.6µA at 2.7V, f_{SCLK} = 10MHz**
- **Power-On, Software, and SureSet™ Resets**
- **Enhanced ESD Protection:**
  - **±8kV HBM**
  - **±1kV CDM**
  - **±25kV Air Gap Discharge**
  - **±15kV Contact Discharge**
- **Latch-Up Exceeds 100 mA per JESD78B - Class I**
- **4 x 4 QFN-16 Package**

U.S. Patent No. 6246394; other patents pending.

APPLICATIONS

- **Multi-Screen Touch Control Systems**

DESCRIPTION

The TSC2008-Q1 is a very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on advanced low-voltage processors. It works with a supply voltage as low as 1.2V, which can be supplied by a single-cell battery. It contains a complete, ultra-low power, 12-bit, analog-to-digital (A/D) resistive touch screen converter, including drivers and the control logic to measure touch pressure.

In addition to these standard features, the TSC2008-Q1 offers preprocessing of the touch screen measurements to reduce bus loading, thus reducing the consumption of host processor resources that can then be redirected to more critical functions.

The TSC2008-Q1 supports an SPI serial bus and data transmission. It offers programmable resolution of 8 or 12 bits to accommodate different screen sizes and performance needs.

The TSC2008-Q1 is available in a 16-pin,4 x 4 QFN package. The TSC2008-Q1 is characterized for the –40°C to +105°C industrial temperature range.

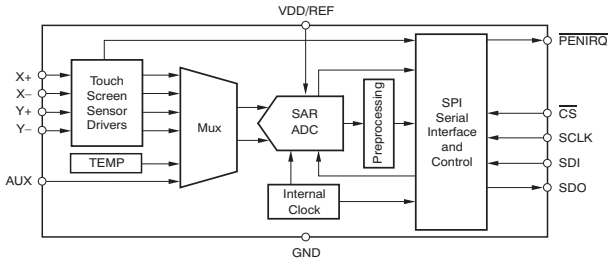


Figure 1. Block Diagram

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	QFN - RGV	Tape and Reel	TSC2008TRGVRQ1	TSC2008T

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TSC2008-Q1	UNIT
Voltage	Analog input X+, Y+, AUX to GND	–0.4 to VDD + 0.1	V
	Analog input X–, Y– to GND	–0.4 to VDD + 0.1	V
Voltage range	VDD to GND	–0.3 to +5	V
Digital input voltage to GND		–0.3 to VDD + 0.3	V
Digital output voltage to GND		–0.3 to VDD + 0.3	V
Power dissipation		$(T_J$ Max - $T_A)/\theta_{JA}$	
Thermal impedance, θ_{JA}	QFN package	47	°C/W
Operating free-air temperature range, T_A		–40 to +105	°C
Storage temperature range, T_{STG}		–65 to +150	°C
Junction temperature, T_J Max		+150	°C
Lead temperature	Vapor phase (60 sec)	+215	°C
	Infrared (15 sec)	+220	°C
IEC contact discharge(2)	X+, X–, Y+, Y–	±15	kV
IEC air discharge(2)	X+, X–, Y+, Y–	±25	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) Test method based on IEC standard 61000-4-2. Device powered by battery. Contact Texas Instruments for test details.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +105°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TSC2008-Q1 MIN	TSC2008-Q1 TYP	TSC2008-Q1 MAX	UNIT
AUXILIARY ANALOG INPUT							
Input voltage range				0		V_{DD}	V
Input capacitance					12		pF
Input leakage current				–1		+1	µA
A/D CONVERTER							
Resolution		Programmable: 8 or 12 bits				12	Bits
No missing codes		12-bit resolution		11			Bits
Integral linearity					±1.5		LSB(1)
Differential linearity					±1		LSB
Offset error		V_{DD} = 1.8V			–1.2		LSB
		V_{DD} = 3.0V			–3.1		LSB
Gain error		V_{DD} = 1.8V			0.7		LSB
		V_{DD} = 3.0V			0.1		LSB
TOUCH SENSORS							
$\overline{\text{PENIRQ}}$ pull-up resistor, R_{IRQ}		T_A = +25°C, V_{DD} = 1.8V, setup command '10100000'			50		kΩ
		T_A = +25°C, V_{DD} = 1.8V, setup command '10101000'			90		kΩ
Switch on-resistance	Y+, X+				6		Ω
	Y–, X–				5		Ω
Switch drivers drive current(2)		100ms duration				50	mA
INTERNAL TEMPERATURE SENSOR							
Temperature range				–40		+105	°C
Resolution		Differential method(3)	V_{DD} = 3V		1.94		°C/LSB
			V_{DD} = 1.6V		1.04		°C/LSB
		TEMP1(4)	V_{DD} = 3V		0.35		°C/LSB
			V_{DD} = 1.6V		0.19		°C/LSB
Accuracy		Differential method(3)	V_{DD} = 3V		±2		°C/LSB
			V_{DD} = 1.6V		±2		°C/LSB
		TEMP1(4)	V_{DD} = 3V		±3		°C/LSB
			V_{DD} = 1.6V		±3		°C/LSB
INTERNAL OSCILLATOR							
Internal clock frequency, f_{CCLK}		8-bit	V_{DD} = 1.2V		3.19		MHz
			V_{DD} = 1.8V		3.66		MHz
			V_{DD} = 2.7V		3.78		MHz
			V_{DD} = 3.6V		3.82		MHz
		12-bit	V_{DD} = 1.2V		1.6		MHz
			V_{DD} = 1.8V		1.83		MHz
			V_{DD} = 2.7V		1.88		MHz
			V_{DD} = 3.6V		1.91		MHz
Frequency drift		V_{DD} = 1.6V			0.0056		%/°C
		V_{DD} = 3.0V			0.012		%/°C

(1) LSB means *least significant bit*. With V_{DD} (REF) = +2.5V, 1LSB is 610µV.
(2) Ensured by design, but not production tested. Exceeding 50 mA source current may result in device degradation.
(3) Difference between TEMP1 and TEMP2 measurement; no calibration necessary.
(4) Temperature drift is –2.1mV/°C.

ELECTRICAL CHARACTERISTICS (continued)

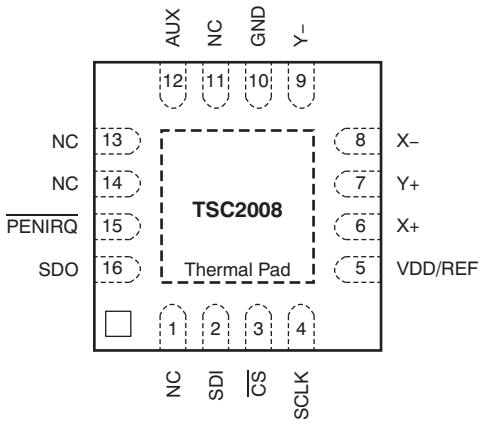
At T_A = –40°C to +105°C, V_{DD} = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS			TSC2008-Q1 MIN	TSC2008-Q1 TYP	TSC2008-Q1 MAX	UNIT
DIGITAL INPUT/OUTPUT								
Logic family						CMOS		
Logic level	V_{IH}	1.2V ≤ V_{DD} < 3.6V			0.7 × V_{DD}		V_{DD} + 0.3	V
	V_{IL}	1.2V ≤ V_{DD} < 1.6V			–0.3		0.2 × V_{DD}	V
		1.6V ≤ V_{DD} ≤ 3.6V			–0.3		0.3 × V_{DD}	V
	I_{IL}	$\overline{CS}$, SCLK, and SDI pins			–1		1	µA
	C_{IN} (5)	$\overline{CS}$, SCLK, and SDI pins					10	pF
	V_{OH}	I_{OH} = 2 TTL loads			V_{DD} – 0.2		V_{DD}	V
	V_{OL}	I_{OL} = 2 TTL loads			0		0.2	V
	I_{LEAK} (5)	Floating output			–1		1	µA
	C_{OUT} (5)	Floating output					10	pF
Data format						Straight Binary		
POWER SUPPLY REQUIREMENTS								
Power-supply voltage								
V_{DD}		Specified performance			1.2		3.6	V
Quiescent supply current (V_{DD} with sensor off)		12-bit, f_{SCLK} = 5MHz, f_{ADC} = 2MHz, PD[1:0] = 0,0	V_{DD} = 1.2V	69.6k eq rate (6)		285.0	375.0	µA
				8.2k eq rate (6)		30.4	42.2	µA
		12-bit, f_{SCLK} = 10MHz, f_{ADC} = 2MHz, PD[1:0] = 0,0	V_{DD} = 1.8V	82.6k eq rate (6)		344.0	500.0	µA
				8.2k eq rate (6)		34.5	37.7	µA
			V_{DD} = 2.7V	84.8k eq rate (6)		461.0	630.0	µA
				8.2k eq rate (6)		44.6	55.1	µA
Power-down supply current		$\overline{CS}$ = 1, SDI = SCLK = 1, $\overline{PENIRQ}$ = 1, PD[1:0] = 0,0				0	5.5	µA
POWER ON/OFF SLOPE REQUIREMENTS (5) (see Figure 38)								
$t_{VDD\_OFF\_RAMP}$		T_A = –40°C to +85°C			2			kV/s
t_{VDD_OFF}		T_A = –40°C to +85°C, VDD = 0V			1			s
		T_A = –20°C to +85°C, VDD = 0V			0.3			s
$t_{VDD\_ON\_RAMP}$		T_A = –40°C to +85°C			12			kV/s
t_{DEVICE_READY}		T_A = –40°C to +85°C			2			ms

(5) Ensured by design, but not production tested
(6) See the Throughput Rate and SPI Bus Traffic section for calculation information.

PIN CONFIGURATION

RGV PACKAGE
4 x 4 QFN-16
(TOP VIEW)



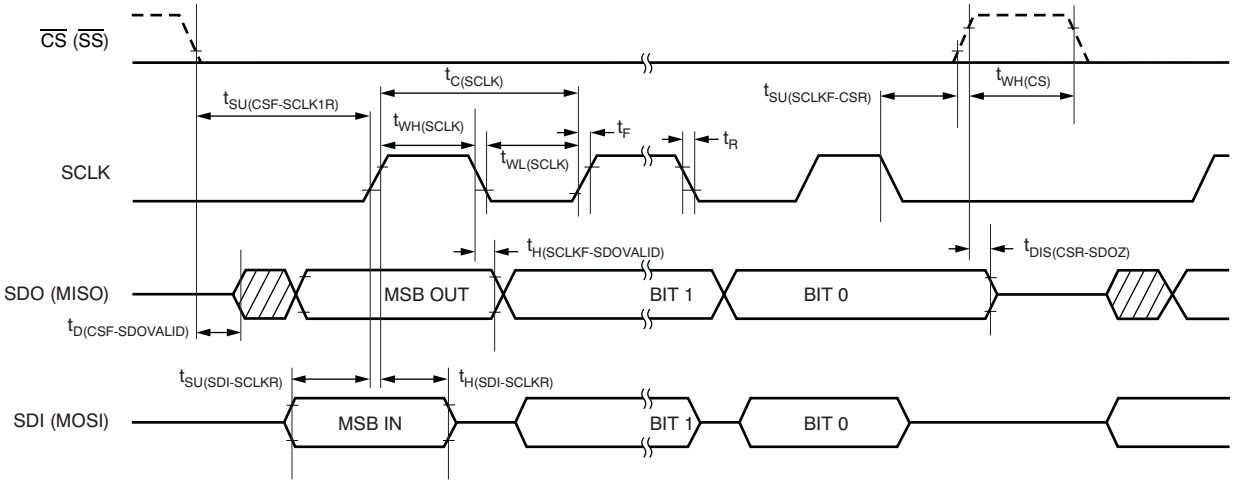
(1) The thermal pad is internally connected to the substrate. The thermal pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

PIN ASSIGNMENTS

PIN NO.	PIN NAME	I/O	A/D	DESCRIPTION
1	NC			No connection
2	SDI	I	D	Serial data input
3	$\overline{CS}$	I	D	Chip select
4	SCLK	I	D	Serial clock input
5	VDD/REF			Supply voltage and external reference input
6	X+	I	A	X+ channel input
7	Y+	I	A	Y+ channel input
8	X–	I	A	X– channel input
9	Y–	I	A	Y– channel input
10	GND			Ground
11	NC			No connection
12	AUX	I	A	Auxiliary channel input. If not used, this input should be grounded.
13	NC			No connection
14	NC			No connection
15	$\overline{PENIRQ}$	O	D	Pen touch interrupt output. Active low when pen is touched. The output remains low until conversion is complete or pen touch is released. The rising edge signals the end of conversion (EOC).
16	SDO	O	D	Serial data output

TIMING INFORMATION

The TSC2008-Q1 supports SPI programming in mode CPOL = 0 and CPHA = 0. The falling edge of SCLK is used to change the output (MISO) data, and the rising edge is used to latch the input (MOSI) data. Eight SCLKs are required to complete the command byte cycle, and an additional eight or 16 SCLKs are required for the data to be read, depending on the mode used.



NOTE: CPOL = 0, CPHA = 0, Byte 0 cycle requires 24 SCLKs, and Byte 1 cycle requires 8 SCLKs.

Figure 2. Detailed I/O Timing

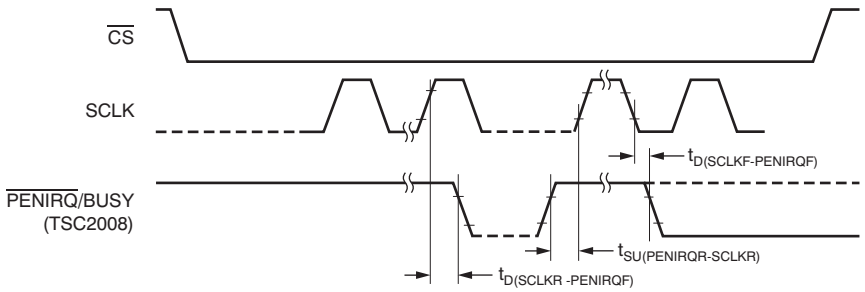


Figure 3. PENIRQ Timing

TIMING REQUIREMENTS(1)

All specifications typical at –40°C to +105°C, VDD = 1.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{C(SCLK)}$	SPI serial clock cycle time	1.2V ≤ VDD < 1.6V, 40% to 60% duty cycle	182		ns
		1.6 ≤ VDD < 2.7V, 40% to 60% duty cycle	62.5		ns
		2.7V ≤ VDD ≤ 3.6V, 40% to 60% duty cycle	40		ns
f_{SCLK}	SPI serial clock frequency	1.2V ≤ VDD < 1.6V, 10pF load		5.5	MHz
		1.6 ≤ VDD < 2.7V, 10pF load		16	MHz
		2.7V ≤ VDD ≤ 3.6V, 10pF load		25	MHz
$t_{WH(SCLK)}$	SPI serial clock high time		0.4 × $t_{C(SCLK)}$	0.6 × $t_{C(SCLK)}$	ns
$t_{WL(SCLK)}$	SPI serial clock low time		0.4 × $t_{C(SCLK)}$	0.6 × $t_{C(SCLK)}$	ns
$t_{SU(CSF-SCLK1R)}$	Enable lead time	1.2V ≤ VDD < 1.6V	22		ns
		1.6 ≤ VDD < 3.6V	14		ns
$t_{D(CSF-SDOVALID)}$	Slave access time	1.2V ≤ VDD < 1.6V		55	ns
		1.6 ≤ VDD < 3.6V		25	ns
$t_{H(SCLKF-SDOVALID)}$	MISO data hold time	1.2V ≤ VDD < 1.6V	40	80	ns
		1.6 ≤ VDD < 3.6V	6	30	ns
$t_{WH(CS)}$	Sequential transfer delay	1.2V ≤ VDD < 1.6V	50		ns
		1.6 ≤ VDD < 3.6V	20		ns
$t_{SU(SDI-SCLKR)}$	MOSI data setup time	1.2V ≤ VDD < 1.6V	25		ns
		1.6 ≤ VDD < 3.6V	10		ns
$t_{H(SDI-SCLKR)}$	MOSI data hold time		5		ns
$t_{DIS(CSR-SDOZ)}$	Slave MISO disable time	1.2V ≤ VDD < 1.6V		55	ns
		1.6 ≤ VDD < 3.6V		25	ns
$t_{SU(SCLKF-CSR)}$	Enable lag time	1.2V ≤ VDD < 1.6V	50		ns
		1.6 ≤ VDD < 3.6V	20		ns
$t_{D(SCLKR-PENIRQF)}$	$\overline{\text{PENIRQ}}$ (used as BUSY) delay from SCLK rising edge	1.2V ≤ VDD < 1.6V		55	ns
		1.6 ≤ VDD < 3.6V		25	ns
$t_{SU(PENIRQR-SCLKR)}$	Setup time from $\overline{\text{PENIRQ}}$ (used as BUSY) to the rising edge of SCLK	1.2V ≤ VDD < 1.6V	50		ns
		1.6 ≤ VDD < 3.6V	20		ns
$t_{D(RESET)}$	Reset period requirement		200		ns
t_R	Rise time	VDD = 3V, f_{SCLK} = 25MHz		3	ns
t_F	Fall time	VDD = 3V, f_{SCLK} = 25MHz		3	ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of VDD) and timed from a voltage level of (V_{IL} + V_{IH})/2.

TYPICAL CHARACTERISTICS

At T_A = –40°C to +105°C, VDD = +1.2V to +3.6V, PD1 = PD0 = 0, f_{SCLK} = 10MHz, f_{ADC} = f_{OSC}/2 = 2MHz, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

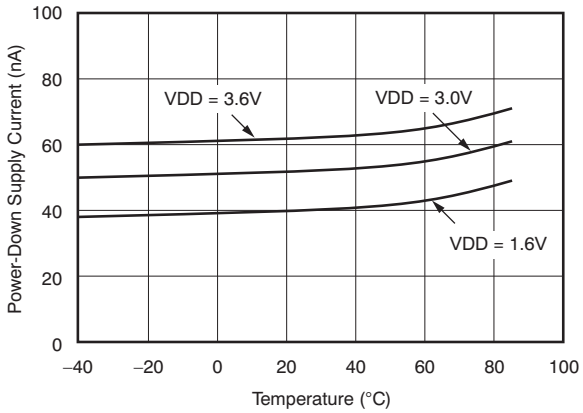


Figure 4.

SUPPLY CURRENT vs TEMPERATURE

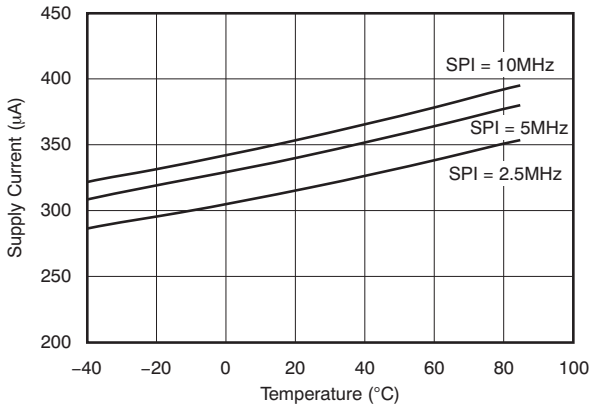


Figure 5.

SUPPLY CURRENT AUX CONVERSION

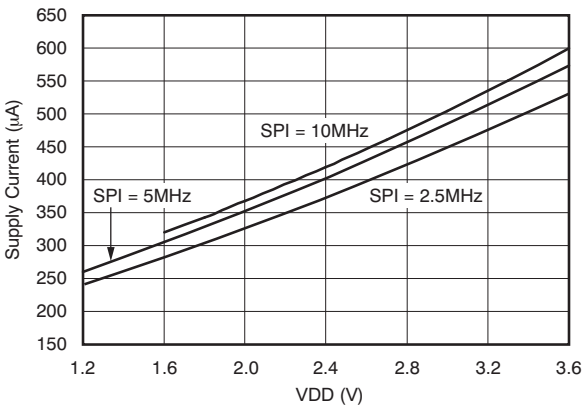


Figure 6.

SUPPLY CURRENT vs SUPPLY VOLTAGE

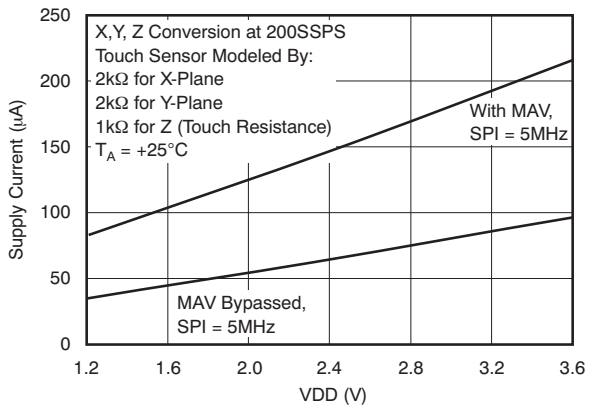


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, VDD = +1.2V to +3.6V, PD1 = PD0 = 0, f_{SCLK} = 10MHz, f_{ADC} = f_{OSC}/2 = 2MHz, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

SUPPLY CURRENT (Part Not Addressed) vs TEMPERATURE

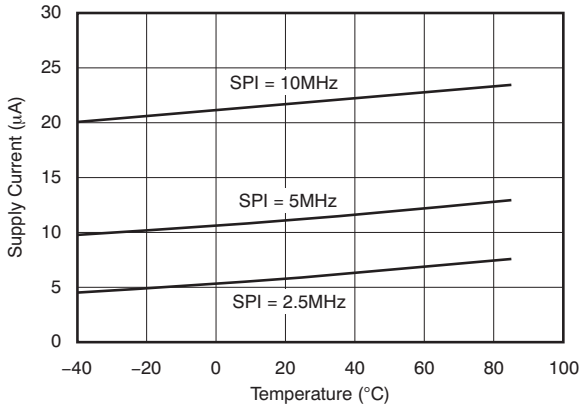


Figure 8.

SUPPLY CURRENT (Part Not Addressed) vs SUPPLY VOLTAGE

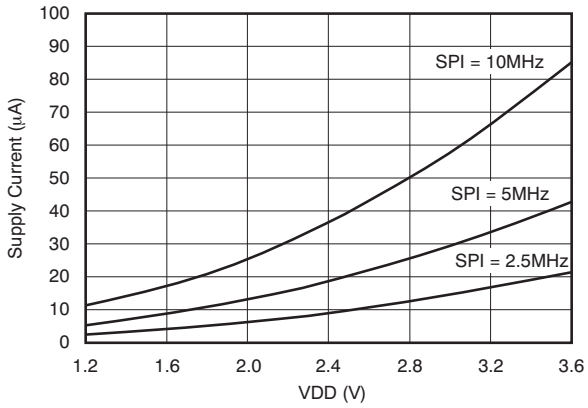


Figure 9.

CHANGE IN GAIN vs TEMPERATURE

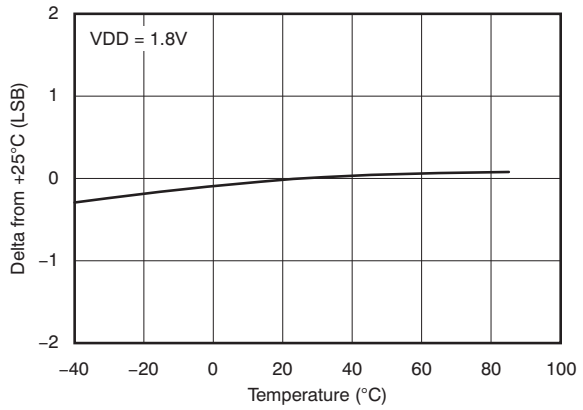


Figure 10.

CHANGE IN OFFSET vs TEMPERATURE

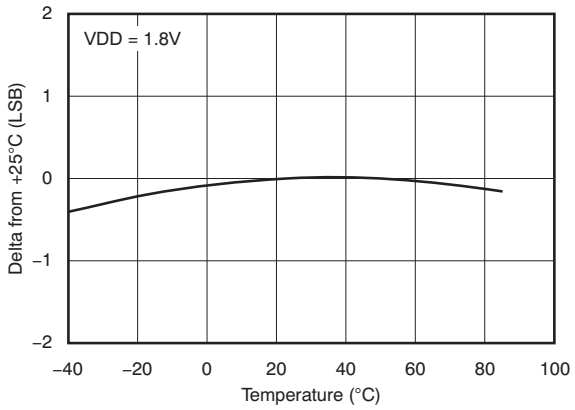


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, VDD = +1.2V to +3.6V, PD1 = PD0 = 0, f_{SCLK} = 10MHz, f_{ADC} = f_{OSC}/2 = 2MHz, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

SWITCH ON-RESISTANCE vs SUPPLY VOLTAGE

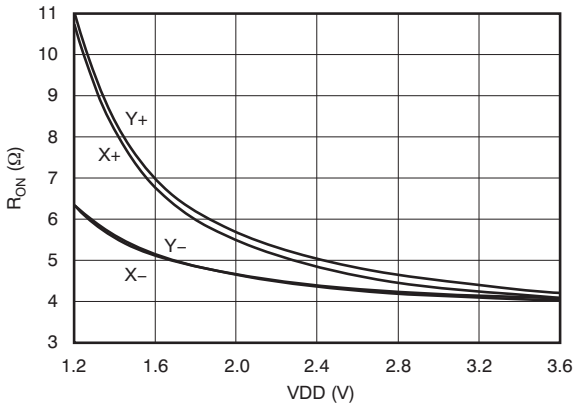


Figure 12.

SWITCH ON-RESISTANCE vs TEMPERATURE

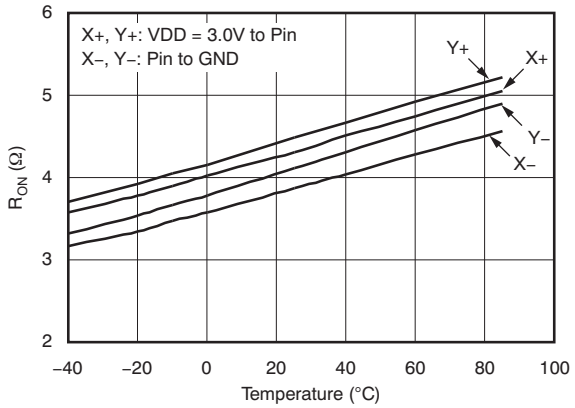


Figure 13.

SWITCH ON-RESISTANCE vs TEMPERATURE

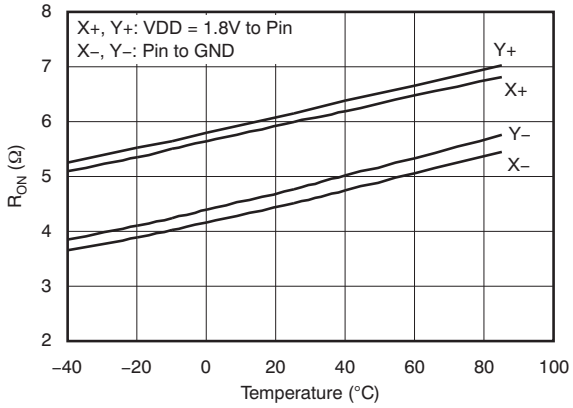


Figure 14.

TEMP DIODE VOLTAGE vs TEMPERATURE

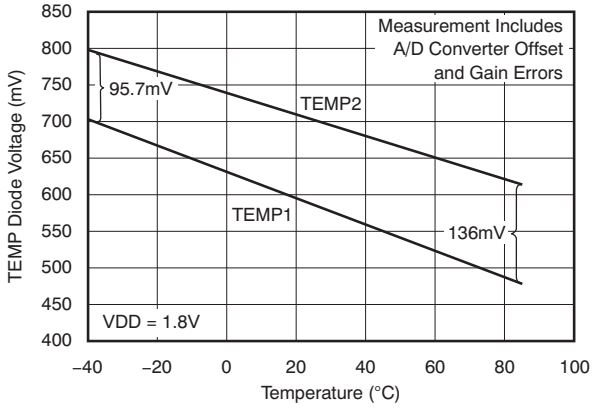


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +105°C, VDD = +1.2V to +3.6V, PD1 = PD0 = 0, f_{SCLK} = 10MHz, f_{ADC} = f_{OSC}/2 = 2MHz, 12-bit mode, non-continuous AUX measurement, and MAV filter enabled (see MAV Filter section), unless otherwise noted.

TEMP1 DIODE VOLTAGE vs SUPPLY VOLTAGE

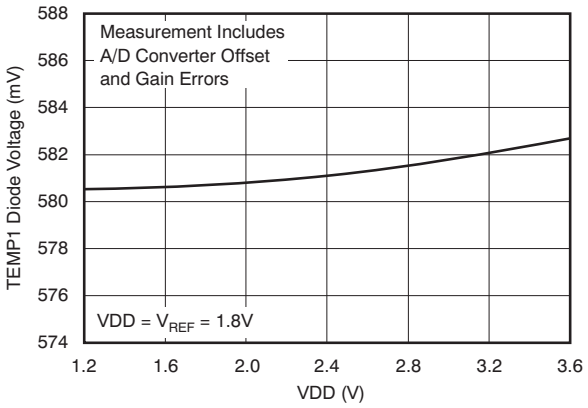


Figure 16.

TEMP2 DIODE VOLTAGE vs SUPPLY VOLTAGE

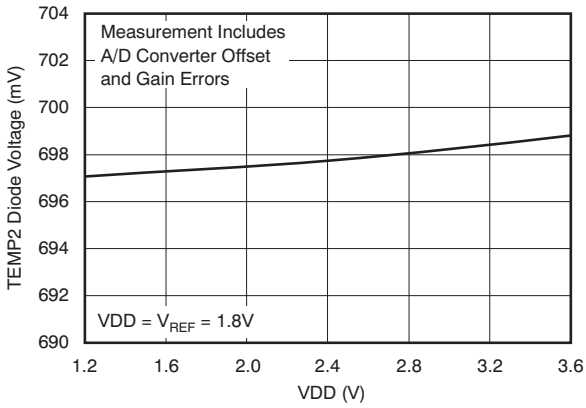


Figure 17.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

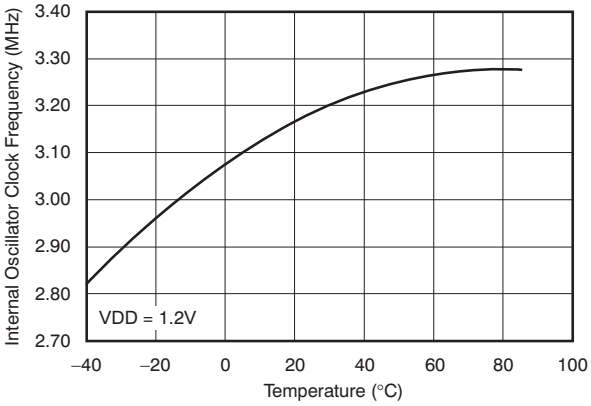


Figure 18.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

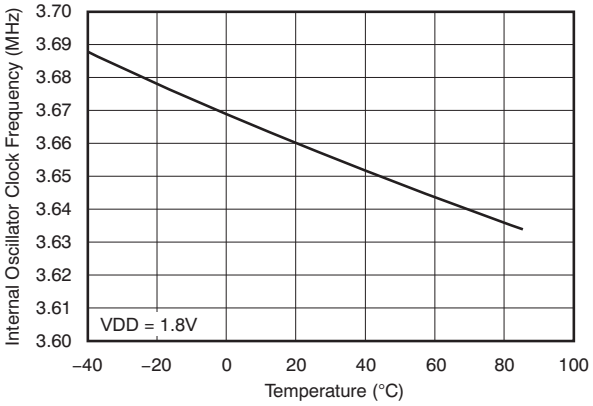


Figure 19.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

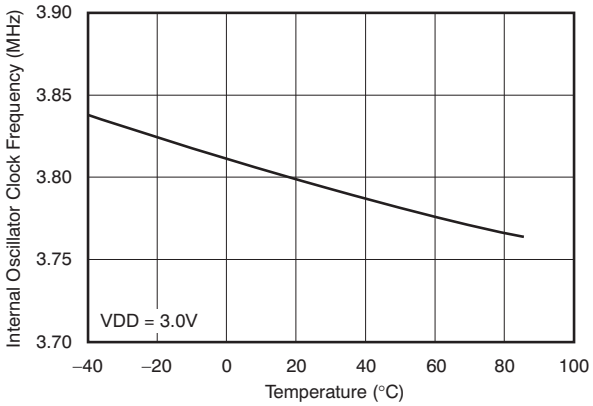


Figure 20.

OVERVIEW

The TSC2008-Q1 is an analog interface circuit for a human interface touch screen device. All peripheral functions are controlled through the command byte and onboard state machines. While maintaining similarity in hardware, command, and software to its predecessor, the TSC2046 (or TSC2046E), the TSC2008-Q1 includes significant improvements such as:

- Much stronger and more comprehensive electrostatic discharge (ESD) protection
- Uses only 1/13 power for equivalent performance
- 1/7 bus traffic
- 3/16 size
- Direct 1.8V interface
- Prudent reset scheme
- Saves 1/7 power if 8-bit SDO adjusted output mode used

The TSC2008-Q1 consists of the following blocks (see Figure 1):

- Touch Screen Sensor Drivers
- Auxiliary Input (AUX)
- Temperature Sensor
- Acquisition Activity Preprocessing
- Internal Conversion Clock
- SPI Interface

Communication with the TSC2008-Q1 is done via an SPI serial interface. The TSC2008-Q1 is an SPI slave device; therefore, data are shifted into or out of the TSC2008-Q1 under the control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2008-Q1 and its functions is accomplished by writing to the command register of an internal state machine. A simple command protocol (compatible with SPI) is used to address this register.

A typical application of the TSC2008-Q1 is shown in Figure 21.

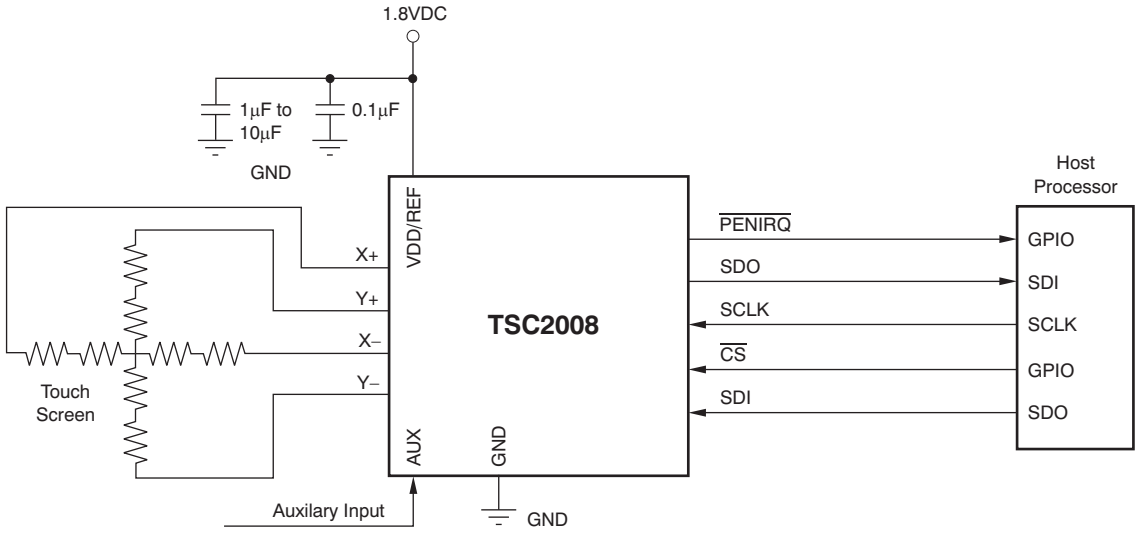


Figure 21. Typical Circuit Configuration

TOUCH SCREEN OPERATION

A resistive touch screen operates by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus, pen, or finger). The change in the resistance ratio marks the location on the touch screen.

The TSC2008-Q1 supports resistive 4-wire configurations, as shown in Figure 22. The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

4-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 4-wire touch screen is typically constructed as shown in Figure 22. It consists of two transparent resistive layers separated by insulating spacers.

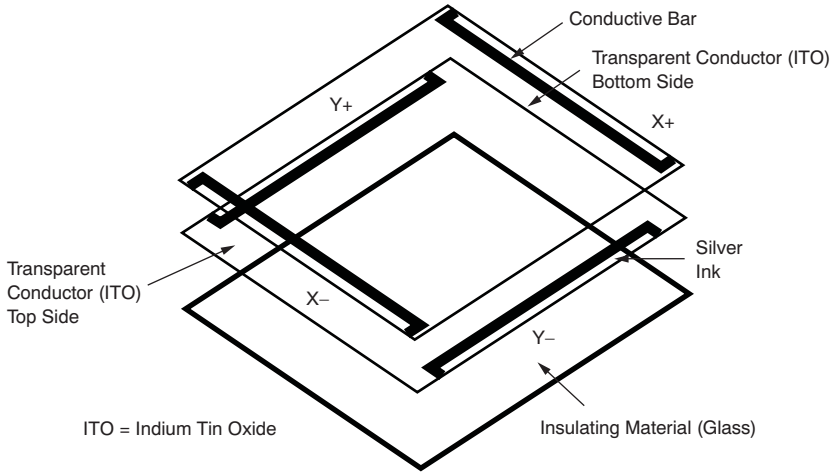


Figure 22. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converter converts the voltage measured at the point where the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion because of the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converter converts the voltage representing the X position on the screen. This process provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2008-Q1. To determine pen or finger touch, the pressure of the *touch* must be determined. Generally, it is not necessary to have very high performance for this test; therefore, 8-bit resolution mode may be sufficient (however, data sheet calculations are shown using 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2008-Q1 supports two methods. The first method requires knowing the X-plate resistance, the measurement of the X-Position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen (see Figure 23). Equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \cdot \frac{X_{Postition}}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \cdot X_{Postition}}{4096}\left(\frac{4096}{Z_1} - 1\right) - R_{Y-plate} \cdot \left(1 - \frac{Y_{Position}}{4096}\right) \quad (2)$$

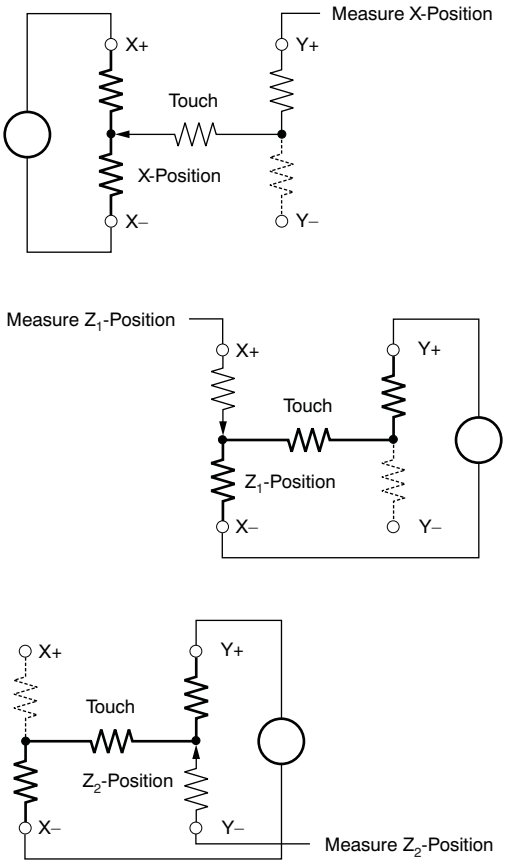


Figure 23. Pressure Measurement

When the touch panel is pressed or touched and the drivers to the panel are turned on, the voltage across the touch panel will often overshoot and then slowly settle down (decay) to a stable dc value. This effect is a result of mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value is incorrect. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time a measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or back-light circuitry). The value of these capacitors provides a low-pass filter to reduce the noise, but creates an additional settling time requirement when the panel is touched. The settling time typically shows up as gain error. The TSC2008-Q1 has a built-in noise filter (see the *Preprocessing* section). These capacitors can be reduced to minimal value or not installed.

The TSC2008-Q1 touch screen interface can measure position (X,Y) and pressure (Z).

INTERNAL TEMPERATURE SENSOR

In some applications, such as battery recharging, an ambient temperature measurement is required. The temperature measurement technique used in the TSC2008-Q1 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2008-Q1 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. The TEMP1 diode, shown in Figure 24, is used during this measurement cycle. This voltage is typically 580mV at +25°C with a 10µA current. The absolute value of this diode voltage can vary by a few millivolts; the temperature coefficient (T_C) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage is stored at a known room temperature, in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (1LSB = 610µV with V_{REF} = 2.5V).

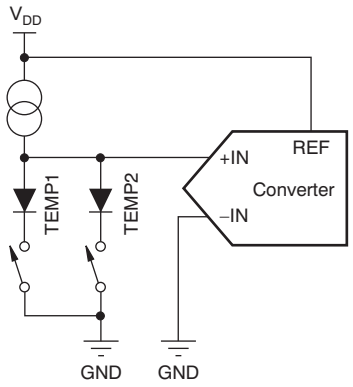


Figure 24. Functional Block Diagram of Temperature Measurement Mode

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion of the voltage across the TEMP2 diode with a resistance 91 times larger than the TEMP1 diode. The voltage difference between the first (TEMP1) and second (TEMP2) conversion is represented by:

$$\Delta V = \frac{kT}{q} \cdot \ln(N) \tag{3}$$

Where:

N = the resistance ratio = 91.

k = Boltzmann's constant = 1.3807×10^{-23} J/K (joules/kelvins).

q = the electron charge = 1.6022×10^{-19} C (coulombs).

T = the temperature in kelvins (K).

This method can provide much improved absolute temperature measurement, but a lower resolution of 1.6°C/LSB. The resulting equation to solve for T is:

$$T = \frac{q \cdot \Delta V}{k \cdot \ln(N)} \tag{4}$$

Where:

$\Delta V = V_{BE}$ (TEMP2) – V_{BE}(TEMP1) (in mV).

$\therefore T = 2.573 \cdot \Delta V$ (in K),

or $T = 2.573 \cdot \Delta V – 273$ (in °C).

Temperature 1 and/or temperature 2 measurements have the same timing as shown in Figure 31 to Figure 34.

ANALOG-TO-DIGITAL CONVERTER

Figure 25 shows the analog inputs of the TSC2008-Q1. The analog inputs (X, Y, and Z touch panel coordinates, chip temperature and auxiliary inputs) are provided via a multiplexer to the Successive Approximation Register (SAR) analog-to-digital converter (ADC). The A/D architecture is based on capacitive redistribution architecture, which inherently includes a sample-and-hold function.

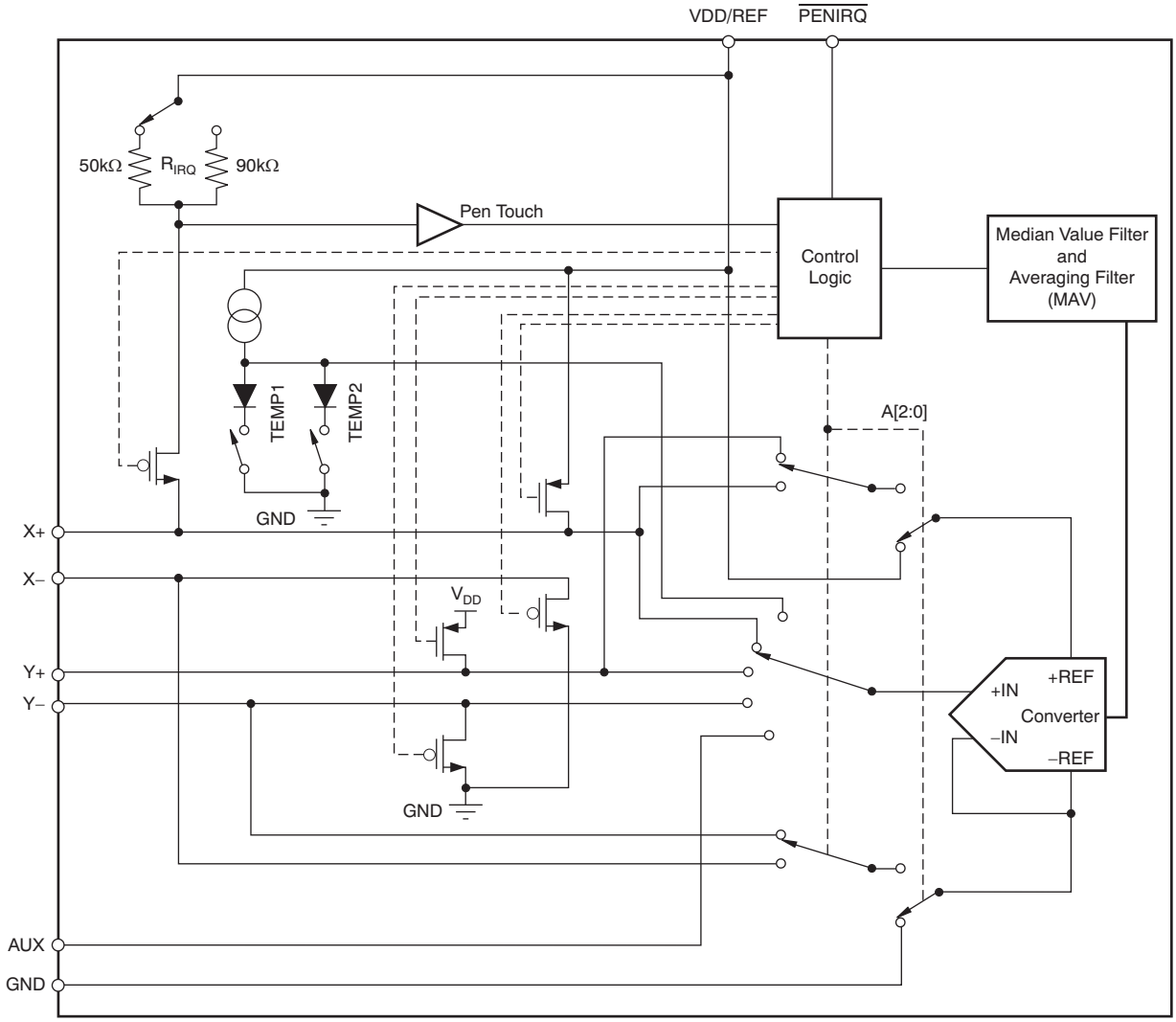


Figure 25. Analog Input Section (Simplified Diagram)

A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistance.

Reference

The TSC2008-Q1 uses an external voltage reference applied to the VDD/REF pin. The upper reference voltage range is the same as the supply voltage range, which allows for simple, 1.2V to 3.6V single-supply operation of the chip.

Reference Mode

There is a critical item regarding the reference when making measurements while the switch drivers are on. For this discussion, it is useful to consider the basic operation of the TSC2008-Q1 (see Figure 21). This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the A/D converter, turning on the Y+ and Y– drivers, and digitizing the voltage on X+, as shown in Figure 26. For this measurement, the resistance in the X+ lead does not affect the conversion; it does affect the settling time, but the resistance is usually small enough that this is not a concern. However, because the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

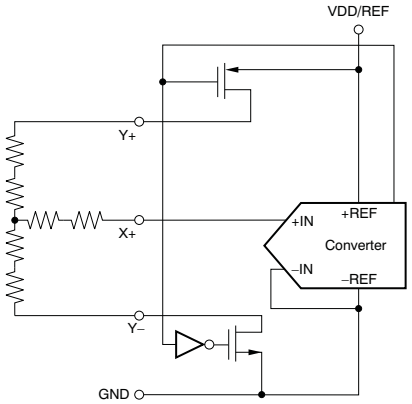


Figure 26. Simplified Diagram of Single-Ended Reference

This situation is resolved, as shown in Figure 27, by using the differential mode; the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This mode makes the A/D converter ratiometric. The result of the conversion is always a percentage of the external reference, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation (see the *Power Dissipation* section for more details).

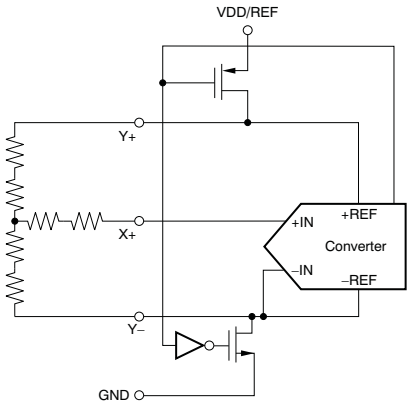


Figure 27. Simplified Diagram of Differential Reference (Both Y Switches are Enabled, and X+ is the Analog Input)

Touch Screen Settling

In some applications, external capacitors may be required across the touch screen to filter noise picked up by the touch screen (that is, noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but they also cause a settling time requirement when the panel is touched. The settling time typically shows up as a gain error. The problem is that the input and/or reference has not settled to its final steady-state value before the A/D converter samples the input(s) and provides the digital output. Additionally, the reference voltage may continue to change during the measurement cycle.

There are two ways to resolve this issue. Option 1 is to stop or slow down the TSC2008-Q1 SCLK for the required touch screen settling time. This option allows the input and reference to have stable values for the Acquire period (three clock cycles of the TSC2008-Q1; see Figure 31). This option works for both the single-ended and the differential modes. Option 2 is to operate the TSC2008-Q1 in the differential mode only for the touch screen measurements and command the TSC2008-Q1 to remain on (touch screen drivers ON) and not go into power-down (PD0 = 1). Several conversions are made, depending on the settling time required and the TSC2008-Q1 data rate. Once the required number of conversions have been made, the processor commands the TSC2008-Q1 to go into its power-down state on the last measurement. This process is required for X-Position, Y-Position, and Z-Position measurements.

Touch Detect

The $\overline{\text{PENIRQ}}$ can be used as an interrupt to the host. R_{IRQ} is an internal pull-up resistor with a programmable value of either 50kΩ (default) or 90kΩ (which allows the total resistance from X+ to Y– to be as high as 30kΩ). Write command '1010' (setup command) followed by data '1xx0' sets the pull-up resistor to 90kΩ. **NOTE:** The first three bits must be '0's and the select bit is the last bit. To change the pull-up resistor back to 50kΩ, issue write command '1010' followed by data '0xx0'.

An example for the Y-position measurement is detailed in Figure 28. The $\overline{\text{PENIRQ}}$ output is pulled high by an internal pull-up resistor. While in power-down mode with PD0 = 0, the Y– driver is on and connected to GND, and the $\overline{\text{PENIRQ}}$ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and $\overline{\text{PENIRQ}}$ output goes low because of the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input is disconnected from the $\overline{\text{PENIRQ}}$ pull-down transistor to eliminate any pull-up resistor leakage current from flowing through the touch screen, thus causing no errors.

If the last command byte written to the TSC2008-Q1 contains PD0 = 1, the pen-interrupt output function is disabled and cannot detect when the panel is touched. In order to re-enable the pen-interrupt output function under these circumstances, a command byte must be written to the TSC2008-Q1 with PD0 = 0.

If the last command byte contains PD0 = 0, then the pen-interrupt function is enabled at the end of a conversion. The end of conversion (EOC) occurs on the rising edge of $\overline{\text{PENIRQ}}$.

In both cases previously listed, it is recommended that whenever the host writes to the TSC2008-Q1, the master processor masks the interrupt associated to $\overline{\text{PENIRQ}}$. This masking prevents false triggering of interrupts when the $\overline{\text{PENIRQ}}$ line is disabled in the cases previously listed.

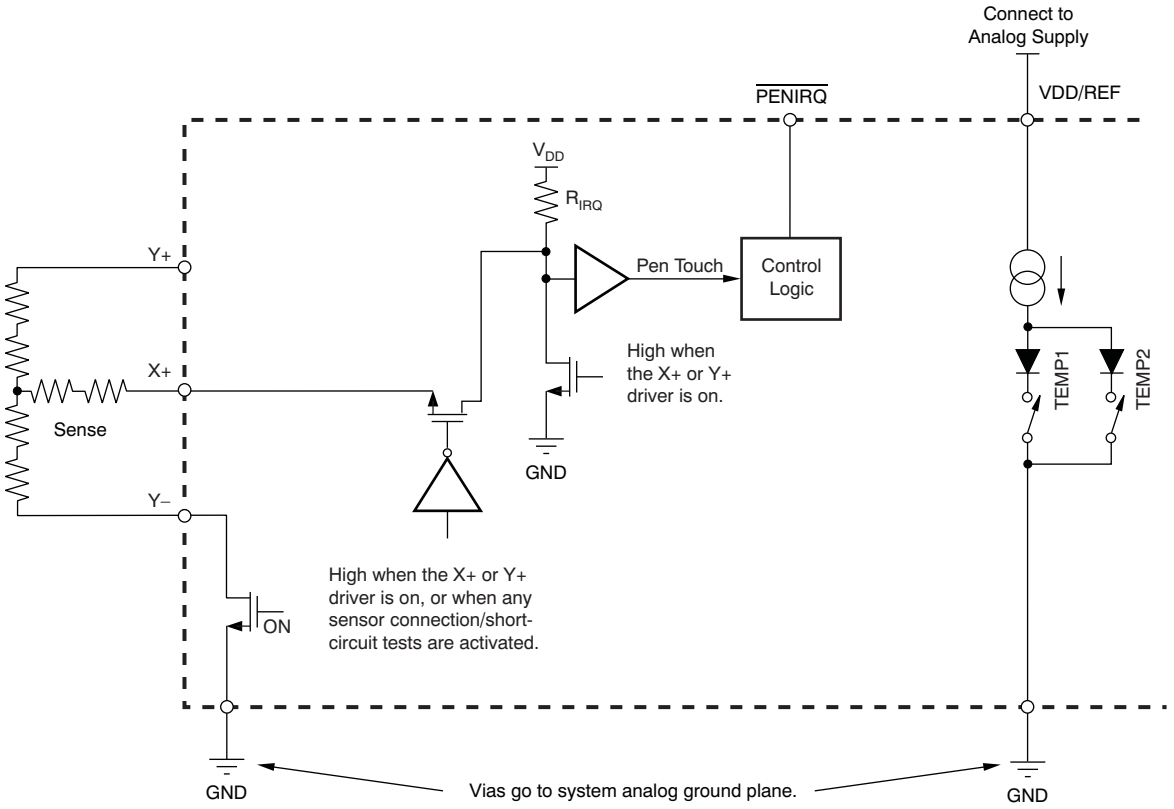


Figure 28. Example of a Pen-Touch Induced Interrupt via the $\overline{\text{PENIRQ}}$ Pin

Preprocessing

The TSC2008-Q1 has a fixed combined MAV filter (median value filter and averaging filter).

MAV Filter

If the acquired signal source is noisy because of the digital switching circuit, it may necessary to evaluate the data without noise. In this case, the median value filter operation helps remove the *noise*. The array of seven converted results is sorted first. The middle three values are then averaged to produce the output value of the MAV filter.

The MAV filter is applied to all measurements for all analog inputs including the touch screen inputs, temperature measurements TEMP1 and TEMP2, and auxiliary input AUX. To shorten the conversion time, the MAV filter may be bypassed though the setup command; see Table 2 and Table 4.

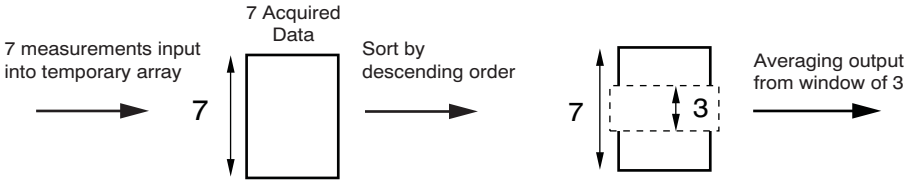


Figure 29. MAV Filter Operation (Patent Pending)

DIGITAL INTERFACE

The TSC2008-Q1 communicates through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by a master SPI. The byte from the master SPI begins shifting in on the slave SDI (MOSI—master out, slave in) pin under the control of the master serial clock. As the byte shifts in on the SDI (MOSI) pin, a byte shifts out on the SDO (MISO—master in, slave out) pin to the master shift register.

The idle state of the TSC2008-Q1 serial clock is logic low, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The TSC2008-Q1 interface is designed so that with a clock phase bit setting of 0 (typical microprocessor SPI control bit CPHA = 0), the master begins driving its MOSI pin and the slave begins driving its MISO pin half an SCLK before the first serial clock edge. The $\overline{CS}$ ($\overline{SS}$, slave select) pin can remain low between transmissions.

Table 1. Standard SPI Signal Names vs Common Serial Interface Signal Names

SPI SIGNAL NAMES	COMMON SERIAL INTERFACE NAMES
$\overline{SS}$ (Slave Select)	$\overline{CS}$ (Chip Select)
MISO (Master In Slave Out)	SDO (Serial Data Out)
MOSI (Master Out Slave In)	SDI (Serial Data In)

As a comparison to the popular TSC2046 timing characteristics, a few differences between the interfaces are worth notice:

1. Unlike the TSC2046, there is not a 15 SCLK cycle for the TSC2008-Q1.
2. There is an adjusted SDO timing that allows an 8-bit, back-to-back cycle.
3. The TSC2008-Q1 uses an internal conversion clock; therefore, the SPI serial clock (SCLK) can only affect the acquiring period and I/O transfer.
4. The TSC2008-Q1 uses an internal clock to perform the conversion. $\overline{PENIRQ}$ rises when the conversion is complete. If the host issues an SCLK before the conversion is complete, $\overline{PENIRQ}$ also rises, but the conversion result is invalid.
5. If a new command is issued before a conversion is complete (indicated by EOC), then the conversion is aborted.
6. Releasing the SPI bus (by raising $\overline{CS}$) during the conversion is OK, but releasing the SPI during the I/O transfer (for example, read result) aborts the data transfer.

CONTROL BYTE

The control byte (on SDI), as shown in Table 2, provides the start conversion, addressing, A/D converter resolution, configuration, and power-down of the TSC2008-Q1. Figure 31, Table 2, and Table 3 give detailed information regarding the order and description of these control bits within the control byte.

Table 2. Order of the Control Bits in the Control Byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	COMMENT
S	A2	A1	A0	MODE	SER/$\overline{\text{DFR}}$	PD1	PD0	Excludes setup command
S	0	1	0	Pull-up	Bypass	Timing	Reset	Setup command

Table 3. Description of the Control Bits in the Control Byte

BIT	DESCRIPTION	
7	Start Bit. When this bit = '1', it indicates this is one of the user commands. A new control byte can start every 16th clock cycle in 12-bit conversion mode or every 12th clock cycle in 8-bit conversion mode (see Figure 31 through Figure 34).	
6-4	Bit[6:4] = A[2:0]. Channel select command if A[2:0] ≠ '010'. These channel select bits, along with the SER/$\overline{\text{DFR}}$ bit, control the setting of the multiplexer input, touch driver switches, and reference inputs (see Table 4 and Figure 31 through Figure 34).	Bit[6:4] = A[2:0]. Setup command if A[2:0] = '010'.
3	Mode Select Bit. This bit controls the number of bits for the next conversion. 0: 12 bits (low) 1: 8 bits (high).	Pull-up Resistor Select Bit(1). 0: 50kΩ $\overline{\text{PENIRQ}}$ pull-up resistor (default). 1: 90kΩ $\overline{\text{PENIRQ}}$ pull-up resistor.
2	Single-Ended/Differential Reference Select Bit (SER/$\overline{\text{DFR}}$). Along with the channel select bits, A[2:0], this bit controls the setting of the multiplexer input, touch driver switches, and reference inputs (see Table 4).	Bypass Noise Filter Bit(1). 0: MAV noise filter enabled (default). 1: MAV noise filter bypassed.
1-0	Bit[1:0] = PD[1:0]. Power Down Mode Select Bits. See Table 5 for details.	Bit 1: Timing Select Bit(1). 0: TSC2046-compatible timing for SDO during data read (default) 1: Adjusted SDO timing; MSB appears before 1st rising clock edge.
		Bit 0: Software Reset Bit. 0: Nothing happens (default). 1: Software reset.

(1) These bits configure the pull-up resistor value, control the filter bypass, and select the SDO output timing. The bits are static and the values are stored in register bits that will only be reset to default by a reset condition (power-on reset, software reset, or SureSet) or changed with the setup command.

The control byte begins with a start bit followed by seven control bits. For the command to be valid, the start bit must be '1'. Do not use '0' for the start bit; it is reserved for factory use.

Initiate Start—The first bit is the start bit (S), and must always be high to initiate the start of a user-controllable control byte. When the start bit = '0', it is reserved for factory use.

Addressing and Command Decoding—The next three bits in the control byte following the start bit are three addressing bits A[2:0] used to select the active input channel(s) of the input multiplexer (see Table 4 and Figure 25), enable the touch screen drivers, select the reference inputs, or decode other commands.

Bit[6:4] = '010' is the setup command that is used to configure the TSC.

Bit[3:0] followed by the setup command are the configuration bits and are used to select the pull-up resistor value, bypass the noise filter (in the preprocessing unit), select the SDO output timing, and perform the software reset. Bit[3:1] are static—that is, they do not change once programmed unless either the device is powered off, one of the reset conditions occur (power-on reset, software reset, or SureSet), or unless changed with the setup command. Note that if any reset occurs, bit[3:1] is set to the default values listed in Table 3. Any function decoded as shown in Table 4 (excluding the setup command) has no access to these four configuration bits.

Table 4. Converter Function Select (CFS) Information

A[2:0]	BIT 2(1) SER/$\overline{\text{DFR}}$	+REF	–REF = –IN	INPUT TO ADC = +IN	X-DRIVERS	Y-DRIVERS	DESCRIPTION
0h	Don't care	VDD	GND	TEMP1	All OFF	All OFF	Measure TEMP1
1h	1 (single-ended)	VDD	GND	X+	All OFF	All ON	Measure Y position
1h	0 (differential mode)	Y+	Y–	X+	All OFF	All ON	Measure Y position
2h	Used as noise filter bypass	—	—	—	All OFF	All OFF	Setup command(2)
3h	1 (single-ended)	VDD	GND	X+	X– ON	Y+ ON	Measure Z1 position
3h	0 (differential mode)	Y+	X–	X+	X– ON	Y+ ON	Measure Z1 position
4h	1 (single-ended)	VDD	GND	Y–	X– ON	Y+ ON	Measure Z2 position
4h	0 (differential mode)	Y+	X–	Y–	X– ON	Y+ ON	Measure Z2 position
5h	1 (single-ended)	VDD	GND	Y+	All ON	All OFF	Measure X position
5h	0 (differential mode)	X+	X–	Y+	All ON	All OFF	Measure X position
6h	Don't care	VDD	GND	AUX	All OFF	All OFF	Measure AUX
7h	Don't care	VDD	GND	TEMP2	All OFF	All OFF	Measure TEMP2

(1) Bit 2 is the SER/$\overline{\text{DFR}}$ control bit for all commands except for the setup command.
(2) Use the setup command to configure the touch screen controller or access the software reset function.

MODE—The mode bit sets the resolution of the A/D converter. With this bit low, the next conversion has 12 bits of resolution; with this bit high, the next conversion has eight bits of resolution.

SER/$\overline{\text{DFR}}$ —The SER/DFR bit controls the reference mode: either single-ended (high) or differential (low). The differential mode is also referred to as the ratiometric conversion mode and is preferred for X-Position, Y-Position, and Pressure-Touch measurements for optimum performance. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a reference voltage is not needed because the reference voltage to the A/D converter is the same as the voltage across the touch screen. In single-ended mode, the converter reference voltage is always the difference between the VREF and GND pins (see Table 4 and Figure 25 through Figure 27, for further information).

If X-Position, Y-Position, and Pressure-Touch are measured in the single-ended mode, then VDD is used as the reference.

NOTE: The differential mode can only be used for X-Position, Y-Position, and Pressure-Touch measurements. All other measurements require the single-ended mode.

PD0 and PD1—The power-down bits select the power-down mode that the TSC2008-Q1 will be in after the current command completes, as shown in Table 5.

It is recommended to set PD0 = '0' in each command byte to get the lowest power consumption possible. If multiple X-, Y-, and Z-position measurements are performed sequentially (such as when averaging), PD0 = '1' leaves the touch screen drivers on at the end of each conversion cycle.

Table 5. Power-Down and Internal Reference Selection

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-Down Between Conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to ensure full operation, and the very first conversion is valid. The Y– switch is on when in power-down.
0	1	Disabled	A/D converter on. $\overline{\text{PENIRQ}}$ disabled.
1	0	Enabled	A/D converter off. $\overline{\text{PENIRQ}}$ enabled.
1	1	Disabled	A/D converter on. $\overline{\text{PENIRQ}}$ disabled.

Variable Resolution

The TSC2008-Q1 provides either 8-bit or 12-bit resolution for the A/D converter. Lower resolution is often practical for measuring slow changing signals such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the A/D converter to complete its conversion process, which also lowers power consumption.

8- and 12-Bit Conversion

The TSC2008-Q1 provides both 12-bit or 8-bit conversion modes.

The 12-bit conversion mode can be done in 24 SCLKs per cycle or 16 SCLKs per cycle timing; see Figure 31 and Figure 32 for details. The 8-bit conversion can be done in 24 SCLKs per cycle (although this mode is unlikely to be selected), 16 SCLKs per cycle, or even 8 SCLKs per cycle (when adjusted SDO timing is selected); see Figure 33 and Figure 34 for details.

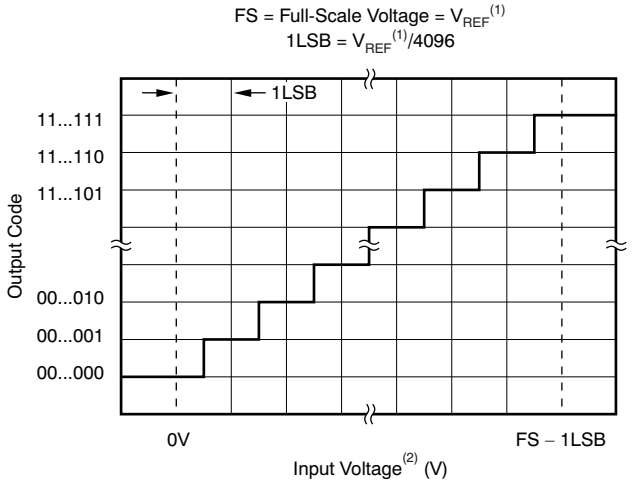
The 8-bit mode can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit conversion mode, a conversion is complete four internal conversion clock cycles earlier and also takes less time to transfer the result. The internal conversion clock runs at twice the speed (4MHz typical) than the 12-bit conversion mode. This faster conversion and transfer saves power.

Conversion Clock and Conversion Time

The TSC2008-Q1 contains an internal clock that drives the state machines that perform the many functions of the device. This clock is divided down to provide a clock that runs the A/D converter. The 8-bit ADC mode uses a 4MHz clock and the 12-bit ADC mode uses a 2MHz clock. The actual frequency of this internal clock is slower than the name suggests, and varies with the supply voltage.

Data Format

The TSC2008-Q1 output data are in Straight Binary format as shown in Figure 30. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



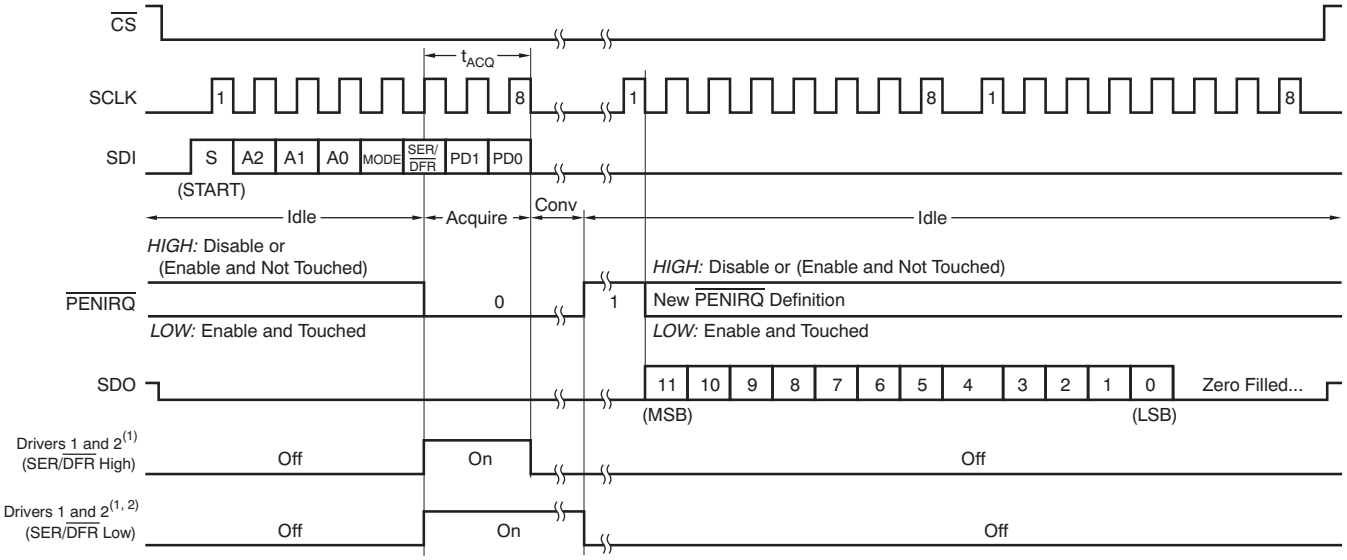
(1) Reference voltage at converter: +REF – (–REF). See Figure 25.

(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 25.

Figure 30. Ideal Input Voltages and Output Codes

12-BIT OPERATION TIMING

A single touch result can be easily achieved using 24 SCLKs per cycle operation when the 12-bit ADC mode is used, as shown in Figure 31. However, because this operation uses slightly more bus bandwidth, a more efficient method is to overlap the control bytes with the conversion result using 16 SCLKs per cycle operation; see Figure 32.



NOTES: (1) For Y-Position, Driver 1 is on X+ is selected, and Driver 2 is off. For X-Position, Driver 1 is off, Y+ is selected, and Driver 2 is on. Y– will turn on when power-down mode is entered and PD0 = 0.

(2) Drivers will remain on if PD0 = 1 (no power down) until selected input channel, or power-down mode is changed, or $\overline{CS}$ is high.

Figure 31. Conversion Timing—12-Bit Mode, 24 SCLKs per Cycle, 8-Bit Bus Interface

The control bits for conversion *n* + 1 can be overlapped with conversion *n* to allow for a conversion every 16 clock cycles, as shown in Figure 32. After submitting the control bits, the TSC2008-Q1 uses the internal clock to acquire data from seven conversions (see Figure 29). Deselecting the TSC2008-Q1 ($\overline{CS}$ = '1') during this time period allows the host to communicate with the other peripherals using the same SPI bus before reading out the ADC data.

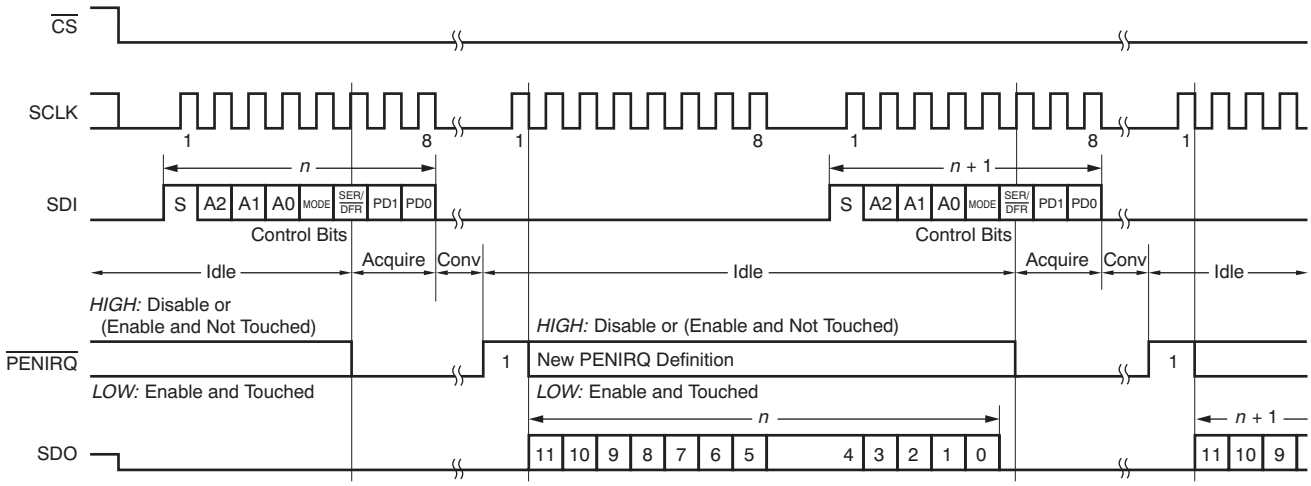


Figure 32. Conversion Timing—12-Bit Mode, 16 SCLKs per Cycle, 8-Bit Bus Interface, with Earliest Start of New Command

8-BIT OPERATION TIMING

If the 8-bit ADC mode produces an acceptable result, then 16 SCLKs per cycle operation can also be used, as shown in Figure 33. If SDO is released one-half SCLK cycle earlier (with the SDO adjusted option), the fastest transfer (eight SCLKs per cycle) is achievable; see Figure 34.

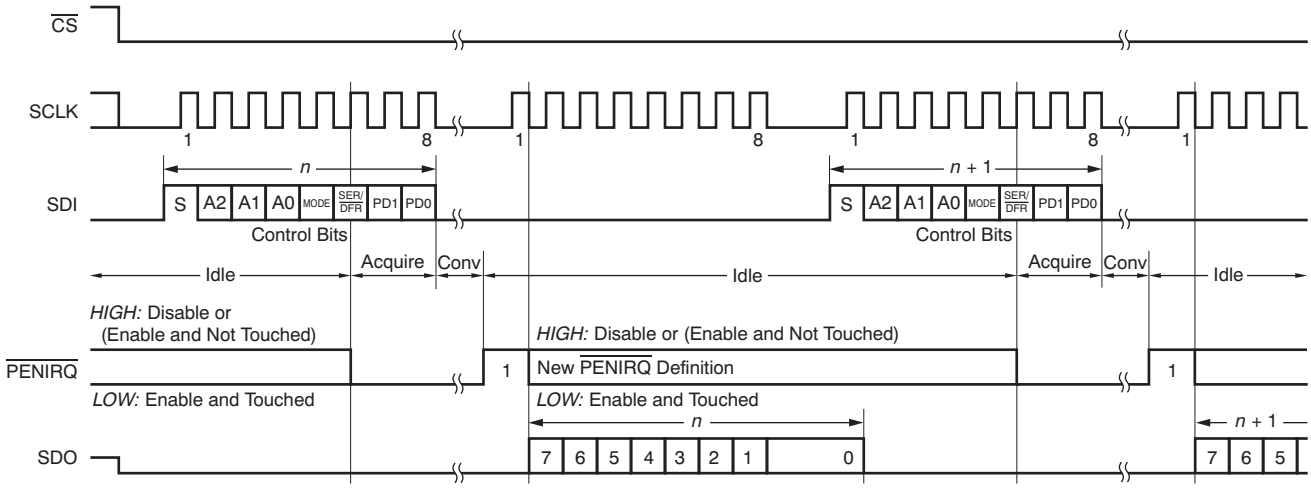


Figure 33. Conversion Timing—8-Bit Mode, 16 SCLKs per Cycle, 8-Bit Bus Interface, without Adjusted SDO Timing (TSC2046-Compatible)

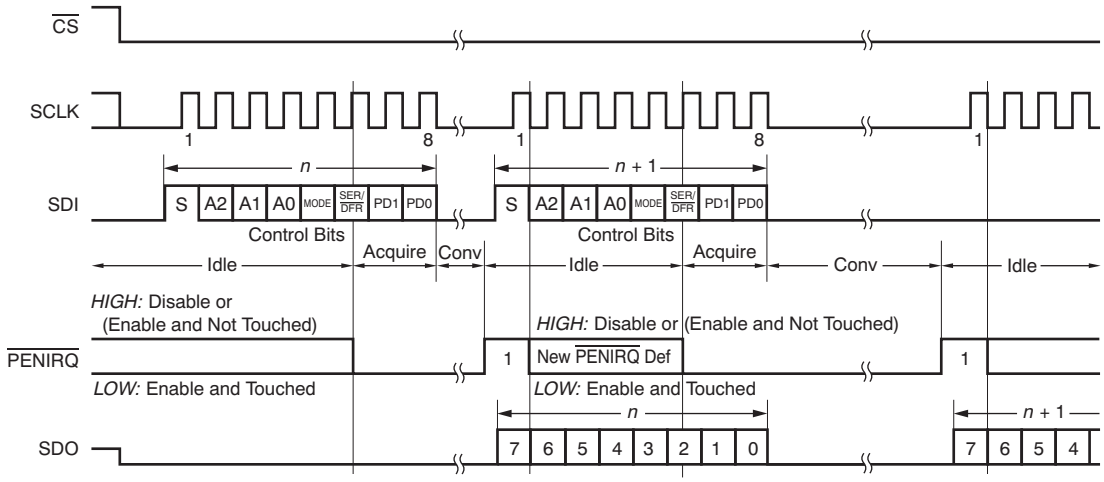


Figure 34. Conversion Timing—8-Bit Mode, 8 SCLKs per Cycle, 8-Bit Bus Interface, with Adjusted SDO Timing

POWER DISSIPATION

There are two major power modes for the TSC2008-Q1: full-power (PD0 = '1') and auto power-down (PD0 = '0'). Unlike its predecessor, the TSC2046/2046E (where operation is synchronous to SCLK and therefore power depends on the SCLK frequency), the TSC2008-Q1 uses an internal clock for conversion and is asynchronous to SCLK. TSC2008-Q1 power consumption depends on the sample rate and is minimally affected by the SCLK frequency. Figure 31 shows a timing example using 12-bit resolution and 24 SCLKs per cycle. There are approximately 2.5 SCLKs of acquisition time used at the end of the 8-bit command cycle. When the preprocessing filter is on, the next six acquisition cycles are controlled by the internal conversion clock instead of relying on the external SCLK. A conversion time follows each acquisition time. Because there are six more conversions to be completed, and also because of the power used from preprocessing, the power consumption when the filter is on is higher than the power consumed without the filter at the same output rate, as shown in Figure 35. This timing sequence also applies to Figure 32 to Figure 34. Thus, using the TSC2008-Q1, power consumption can be very low, even with a low SCLK frequency.

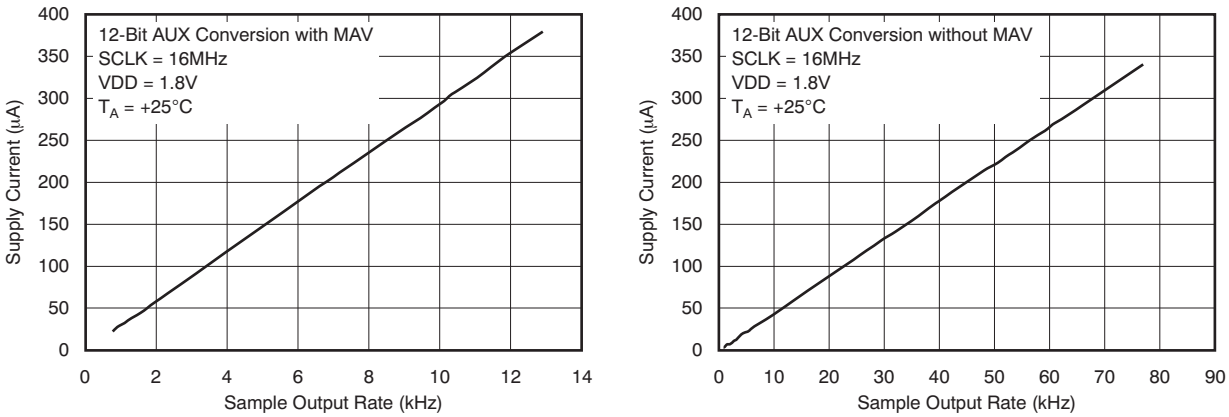


Figure 35. Sample Output Rate vs Supply Current (with and without MAV filter)

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the touch panel drivers are on only when the analog input voltage is being acquired (see Figure 31 and Table 4). The external device (for example, a resistive touch screen), therefore, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 31). If the conversion rate is high, using this mode could substantially increase power dissipation.

THROUGHPUT RATE AND SPI BUS TRAFFIC

Although the internal A/D converter has a sample rate of up to 200kSPS, the throughput presented at the bus is much lower. The rate is reduced because preprocessing manages the redundant work of filtering out noise. The throughput is further limited by the SPI bus bandwidth, which is determined by the supply voltage and what the host processor can support. The effective throughput is approximately 20kSPS at 8-bit resolution, or 10kSPS at 12-bit resolution. The preprocessing saves a large portion of the SPI bandwidth for the system to use on other devices.

Each sample and conversion takes 19 CCLK cycles (12-bit), or 16 CCLK cycles (8-bit). The TSC2008-Q1 contains an internal clock that drives the state machines that perform the many functions of the device. This clock is divided down to provide a clock that runs the A/D converter. The 8-bit ADC mode uses a 4MHz clock and the 12-bit ADC mode uses a 2MHz clock. The actual frequency of this internal clock is slower than the name suggests, and varies with the supply voltage. For a typical internal 4MHz OSC clock, the frequency actually ranges from 3.66MHz to 3.82MHz. For VDD = 1.2V, the frequency reduces to 3.19MHz, which gives a 3.19MHz/16 = 199kSPS raw A/D converter sample rate.

12-Bit Operation

For 12-bit operation, sending the conversion result across the SPI bus takes 16 or 24 bus clocks (SCLK clock); see Figure 32 and Figure 31. There is an additional SCLK to be added to accommodate the cycle overhead (time between consecutive cycles) so that the total bus cycle time used for calculating the throughput is actually 17 or 25 bus clocks (SCLK clock), respectively. Using a TSC2046-compatible SDO output mode or an SDO-adjusted output mode does not affect the transmission time.

Seven sample-and-conversions take (19 x 7) internal clocks to complete. The MAV filter loop requires 19 internal clocks. For VDD = 1.2V, the complete processed data cycle time calculations are shown in Table 6. Because the first acquisition cycle overlaps with the I/O cycle, four CCLKs must be deducted from the total CCLK cycles. The total time required is (19 × 7 + 19) – 4 = 148 CCLKs plus I/O.

8-Bit Operation

For 8-bit operation, sending the conversion result across the SPI bus takes 8, 16, or 24 bus clocks (SCLK clock); see Figure 34, Figure 33, and Figure 31. There is an additional SCLK to be added to accommodate the cycle overhead (time between consecutive cycles) so that the total bus cycle time used for calculating the throughput is actually 9, 17, or 25 bus clocks (SCLK clock), respectively. Sending the conversion result takes 17 or 25 SCLKs using 8-bit resolution and a TSC2046-compatible SDO output mode. If an SDO-adjusted output mode is used with 8-bit resolution, it takes only 9 or 17 SCLKs to send the result back to host.

Seven sample-and-conversions take (16 x 7) internal clocks to complete. The MAV filter loop takes 19 internal clocks. For VDD = 1.2V, the complete processed data cycle time calculations are shown in Table 6. Because the first acquisition cycle is overlapped with the I/O cycle, four CCLKs must be deducted from the total CCLK cycles. The total time required is (16 × 7 + 19) – 4 = 127 CCLKs plus I/O.

Table 6. Measurement Cycle Time Calculations(1) (2)

f_{SCLK} = 100kHz (Period = 10µs)	
8-Bit	17 × 10µs + 127 × 322.6ns = 211.0µs
12-Bit	25 × 10µs + 148 × 645.2ns = 345.5µs
f_{SCLK} = 1MHz (Period = 1µs)	
8-Bit	17 × 1µs + 127 × 322.6ns = 58.0µs
12-Bit	25 × 1µs + 148 × 645.2ns = 120.5µs
f_{SCLK} = 2MHz (Period = 500ns)	
8-Bit	17 × 500ns + 127 × 322.6ns = 49.5µs
12-Bit	25 × 500ns + 148 × 645.2ns = 108.0µs
f_{SCLK} = 2.5MHz (Period = 400ns)	
8-Bit	17 × 400ns + 127 × 322.6ns = 47.8µs
12-Bit	25 × 400ns + 148 × 645.2ns = 105.5µs
f_{SCLK} = 4MHz (Period = 250ns)	
8-Bit	17 × 250ns + 127 × 322.6ns = 45.2µs
12-Bit	25 × 250ns + 148 × 645.2ns = 101.7µs
f_{SCLK} = 10MHz (Period = 100ns)	
8-Bit	17 × 100ns + 127 × 322.6ns = 42.7µs
12-Bit	25 × 100ns + 148 × 645.2ns = 98.0µs
f_{SCLK} = 16MHz (Period = 62.5ns)	
8-Bit	17 × 62.5ns + 127 × 322.6ns = 42.0µs
12-Bit	25 × 62.5ns + 148 × 645.2ns = 97.1µs
f_{SCLK} = 25MHz (Period = 40ns)	
8-Bit	17 × 40ns + 127 × 322.6ns = 41.7µs
12-Bit	25 × 40ns + 148 × 645.2ns = 96.5µs

(1) 8-bit mode cycle time is calculated based on SDO-adjusted output mode.
(2) CCLK period used for calculation is worst-case at 1.2V supply, 322.6ns.

As an example, use V_{DD} = 1.2V and 12-bit mode with 2MHz SPI clock (f_{SCLK} = 2MHz). The equivalent TSC throughput is at least seven times faster than the effective throughput across the bus (9.26k x 7 = 64.82kSPS). The supply current to the TSC for this rate and configuration is 240.08µA. To achieve an equivalent sample throughput of 8.2kSPS using the device without preprocessing, the TSC2008-Q1 consumes only (8.2/64.82) × 240.08µA = 30.37µA.

Table 7. Effective and Equivalent Throughput Rates

SUPPLY VOLTAGE	SPI BUS SPEED (f_{SCLK})	RESOLUTION	TSC CONVERSION CYCLE TIME (µs)	EFFECTIVE THROUGHPUT (kSPS)	EQUIVALENT THROUGHPUT (kSPS)	NO. OF SCL	NO. OF CCLK	f_{CCLK} (kHz)	CCLK PERIODS (ns)
2.7V	100kHz	8-bit	204.3	4.89	34.26	17	127	3700	270.3
		12-bit	330.0	3.03	21.21	25	148	1850	540.5
	1MHz	8-bit	51.3	19.48	136.39	17	127	3700	270.3
		12-bit	105.0	9.52	66.67	25	148	1850	540.5
	2MHz	8-bit	42.8	23.35	163.46	17	127	3700	270.3
		12-bit	92.5	10.81	75.68	25	148	1850	540.5
	2.5MHz	8-bit	41.1	24.32	170.22	17	127	3700	270.3
		12-bit	90.0	11.11	77.78	25	148	1850	540.5
	4MHz	8-bit	38.6	25.92	181.47	17	127	3700	270.3
		12-bit	86.3	11.59	81.16	25	148	1850	540.5
	10MHz	8-bit	36.0	27.76	194.31	17	127	3700	270.3
		12-bit	82.5	12.12	84.85	25	148	1850	540.5
	16MHz	8-bit	35.4	28.26	197.81	17	127	3700	270.3
		12-bit	81.6	12.26	85.82	25	148	1850	540.5
	25MHz	8-bit	35.0	28.57	199.98	17	127	3700	270.3
		12-bit	81.0	12.35	86.42	25	148	1850	540.5
1.8V	100kHz	8-bit	205.3	4.87	34.10	17	127	3600	277.8
		12-bit	332.2	3.01	21.07	25	148	1800	555.6
	1MHz	8-bit	52.3	19.13	133.90	17	127	3600	277.8
		12-bit	107.2	9.33	65.28	25	148	1800	555.6
	2MHz	8-bit	43.8	22.84	159.90	17	127	3600	277.8
		12-bit	94.7	10.56	73.90	25	148	1800	555.6
	2.5MHz	8-bit	42.1	23.77	166.36	17	127	3600	277.8
		12-bit	92.2	10.84	75.90	25	148	1800	555.6
	4MHz	8-bit	39.5	25.30	177.09	17	127	3600	277.8
		12-bit	88.5	11.30	79.12	25	148	1800	555.6
	10MHz	8-bit	37.0	27.04	189.30	17	127	3600	277.8
		12-bit	84.7	11.80	82.62	25	148	1800	555.6
	16MHz	8-bit	36.3	27.52	192.62	17	127	3600	277.8
		12-bit	83.8	11.94	83.55	25	148	1800	555.6
1.2V	100kHz	8-bit	211.0	4.74	33.18	17	127	3100	322.5
		12-bit	345.5	2.89	20.26	25	148	1550	645.2
	1MHz	8-bit	58.0	17.25	120.76	17	127	3100	322.5
		12-bit	120.5	8.3	58.10	25	148	1550	645.2
	2MHz	8-bit	49.5	20.22	141.51	17	127	3100	322.5
		12-bit	108.0	9.26	64.82	25	148	1550	645.2
	2.5MHz	8-bit	47.8	20.93	146.54	17	127	3100	322.5
		12-bit	105.5	9.48	66.36	25	148	1550	645.2
	4MHz	8-bit	45.2	22.12	154.81	17	127	3100	322.5
		12-bit	101.7	9.83	68.81	25	148	1550	645.2
	5MHz	8-bit	44.4	22.54	157.77	17	127	3100	322.5
		12-bit	100.5	9.95	69.66	25	148	1550	645.2

RESET

The TSC2008-Q1 can be reset with three different methods: power-on reset (POR), software reset, and the proprietary SureSet function. The configuration bits (see Table 3, bit[3:1]) accessible through the setup command ('010') are reset to the respective default values listed in Table 3 after any reset occurs (POR, software reset, or SureSet).

Software Reset

The TSC2008-Q1 has a software reset command that can be issued by submitting the 8-bit command '1010 0001' via the SPI, as shown in Figure 36. This command resets the device to the default configuration. All the settings in the control byte are reset to default values (see Table 2 and Table 3).

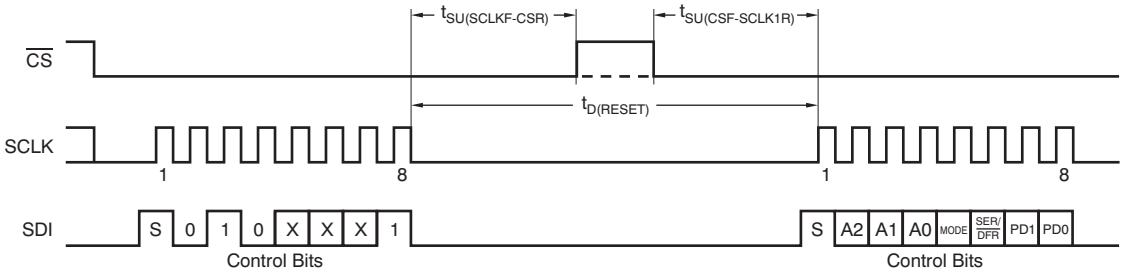


Figure 36. Software Reset Timing

Table 8. Timing Requirements for Figure 36

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{SU(CSF-SCLK1R)}$	Enable lead time	1.2V ≤ VDD < 1.6V	22		ns
		1.6 ≤ VDD < 3.6V	14		ns
$t_{SU(SCLKF-CSR)}$	Enable lag time	1.2V ≤ VDD < 1.6V	50		ns
		1.6 ≤ VDD < 3.6V	20		ns
$t_{D(RESET)}$	Reset period requirement		200		ns

SureSet

The TSC2008-Q1 uses SureSet, a unique reset function. SureSet works in the same way as a hardware reset except that it does not require a dedicated reset pin on the device. SureSet works independently from the software reset and power-on reset. For example, the software reset works only after the interface (internal state machine) is fully functional, whereas SureSet works without the interface. In the unlikely event that the host becomes out-of-sync with the TSC2008-Q1, and forcing CS high does not reset the state machine, the host can submit a 24-bit sequence (0x06D926) that resets the device to a default state (the same as the power-up state), as shown in Figure 37. In order to reset the TSC2008-Q1, the device must be selected (CS low) before submitting this sequence.

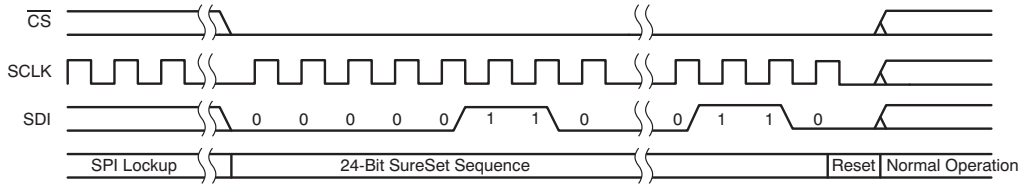


Figure 37. SureSet Timing

Power-On Reset

During TSC2008-Q1 power up, an internal power-on reset (POR) is triggered if the power-supply ramping meets the timing requirements shown in Figure 38 and listed in Table 9. The recommended and typical V_{DD} off times are shown in Figure 39. The POR brings the TSC2008-Q1 to the default working condition. If the system is not able to meet the power ramping timing requirements, or if the system is not properly reset (even after a POR), then including the SureSet reset in the initialization routine is recommended.

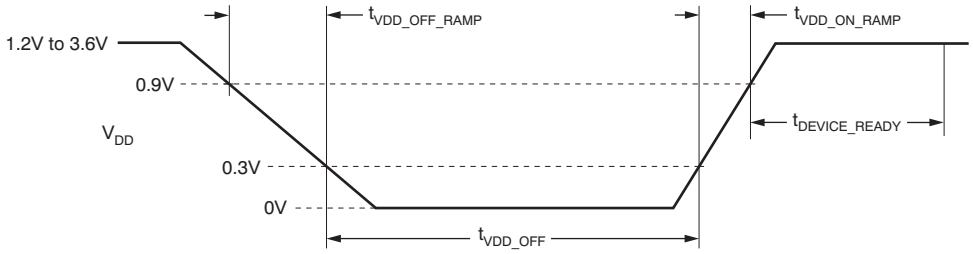


Figure 38. Power-On Reset Timing

Table 9. Timing Requirements for Figure 38

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{VDD\_OFF\_RAMP}$	T_A = –40°C to +105°C	2		kV/s
t_{VDD_OFF}	T_A = –40°C to +105°C	1		s
	T_A = –20°C to +105°C	0.3		s
$t_{VDD\_ON\_RAMP}$	T_A = –40°C to +105°C	12		kV/s
t_{DEVICE_READY}	T_A = –20°C to +105°C	2		ms

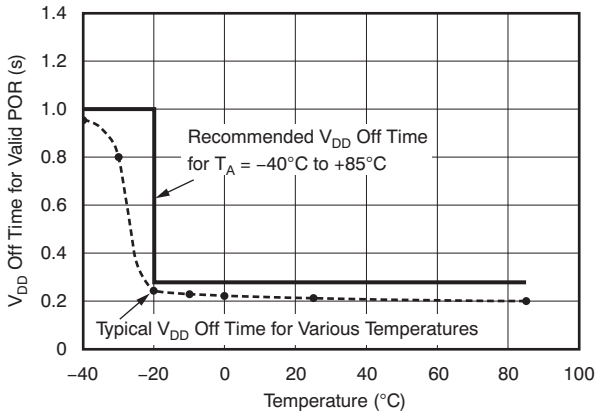


Figure 39. V_{DD} Off Time vs Temperature

LAYOUT

The following layout suggestions should obtain optimum performance from the TSC2008-Q1. Keep in mind that many portable applications have conflicting requirements for power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter power and less concern regarding grounding. However, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2008-Q1 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just before latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCLK input.

With this in mind, power to the TSC2008-Q1 should be clean and well-bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1μF to 10μF capacitor may also be needed if the impedance of the connection between VDD/REF and the power supply is high.

A bypass capacitor is generally not needed on the VDD/REF pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2008-Q1 architecture offers no inherent rejection of noise or voltage variation with regard to using an external reference input, which is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation as a result of line frequency (50Hz or 60Hz) can be difficult to remove. Some package options have pins labeled as VOID. Avoid any active trace going under any pin marked as VOID unless it is shielded by a ground or power plane.

The GND pin should be connected to a clean ground point. In many cases, this point is the analog ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Because resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (for example, applications that require a back-lit LCD panel). This electromagnetic interference (EMI) noise can be coupled through the LCD panel to the touch screen and cause flickering of the converted A/D converter data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground, which couples the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires a longer time for panel voltages to stabilize. The resistor value varies depending on the touch screen sensor used. The $\overline{\text{PENIRQ}}$ pull-up resistor (R_{IRQ}) may be adequate for most of sensors. If not used, the general-purpose analog input to the converter (AUX) should be connected to the analog ground plane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2008TRGVRQ1	ACTIVE	VQFN	RGV	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 105	TSC 2008T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TSC2008-Q1 :

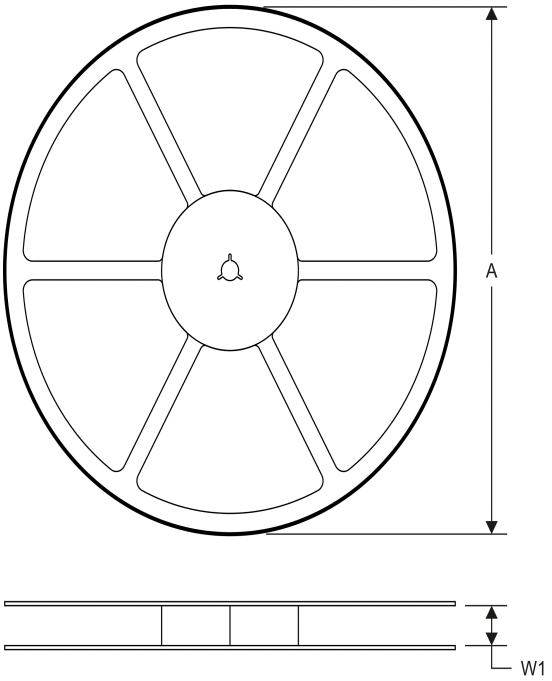
- Catalog: TSC2008

NOTE: Qualified Version Definitions:

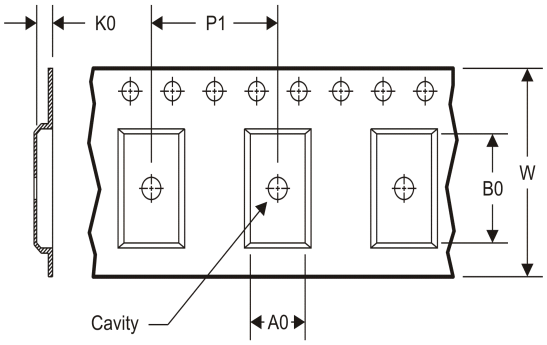
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



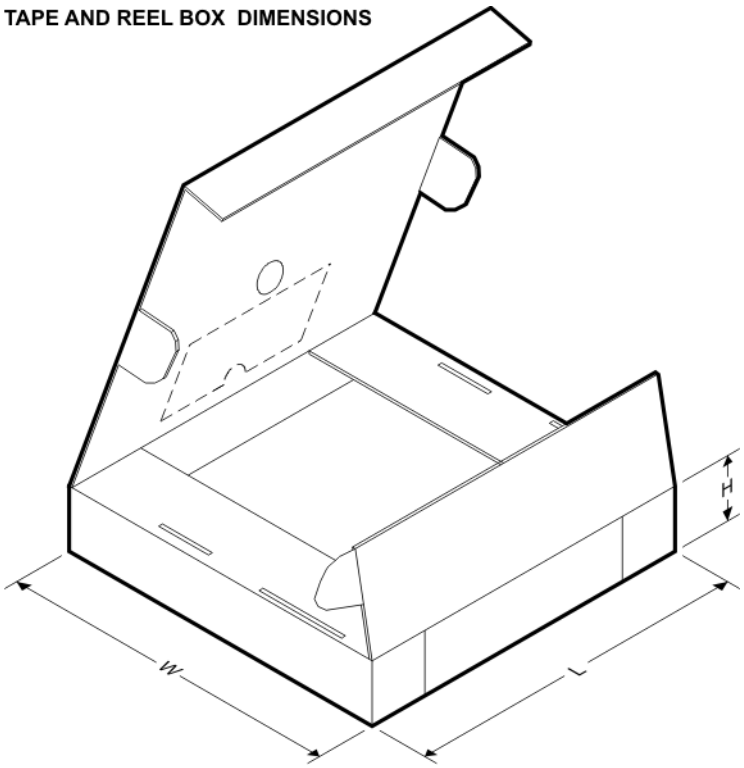
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2008TRGVRQ1	VQFN	RGV	16	2000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

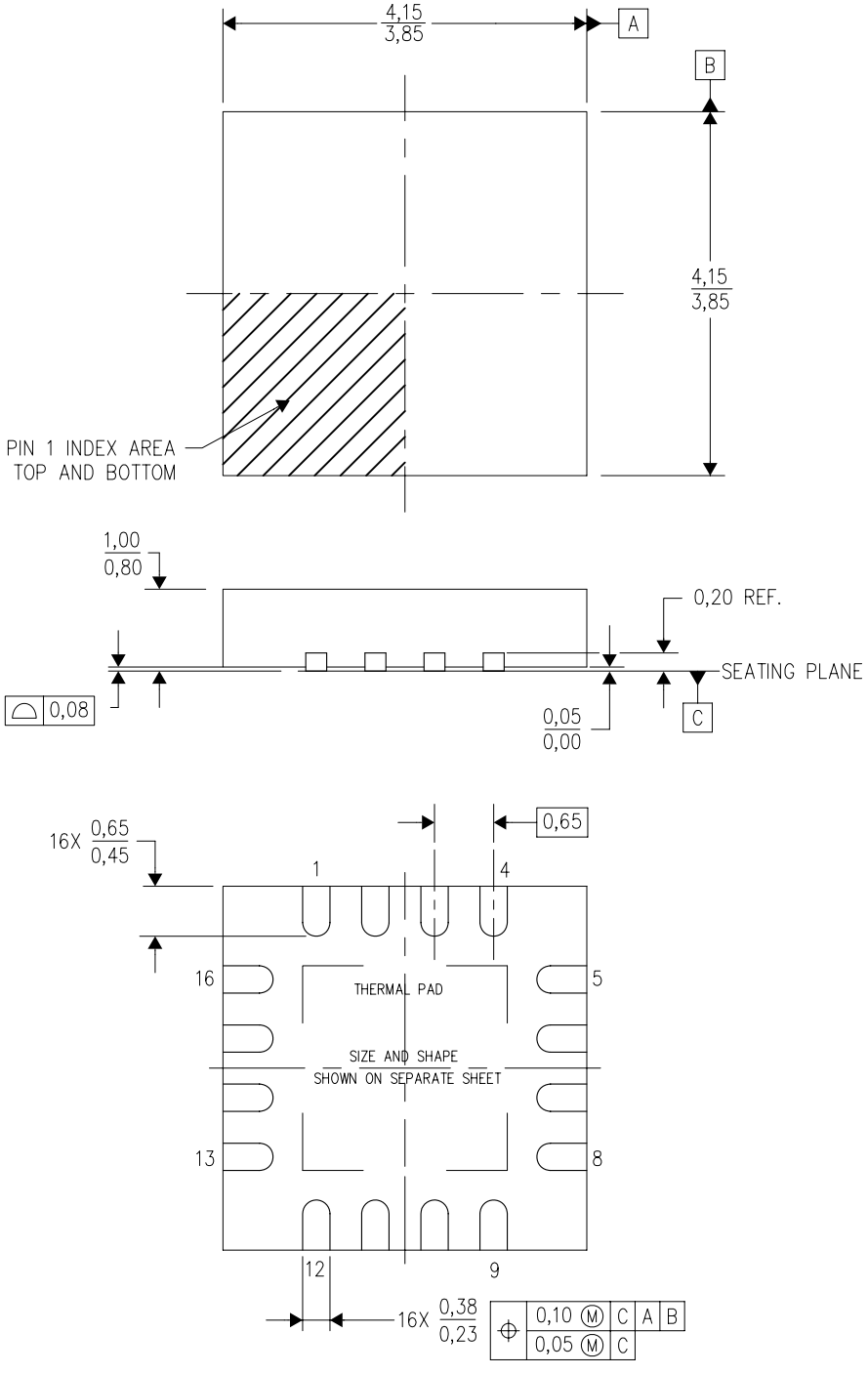
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2008TRGVRQ1	VQFN	RGV	16	2000	367.0	367.0	35.0

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

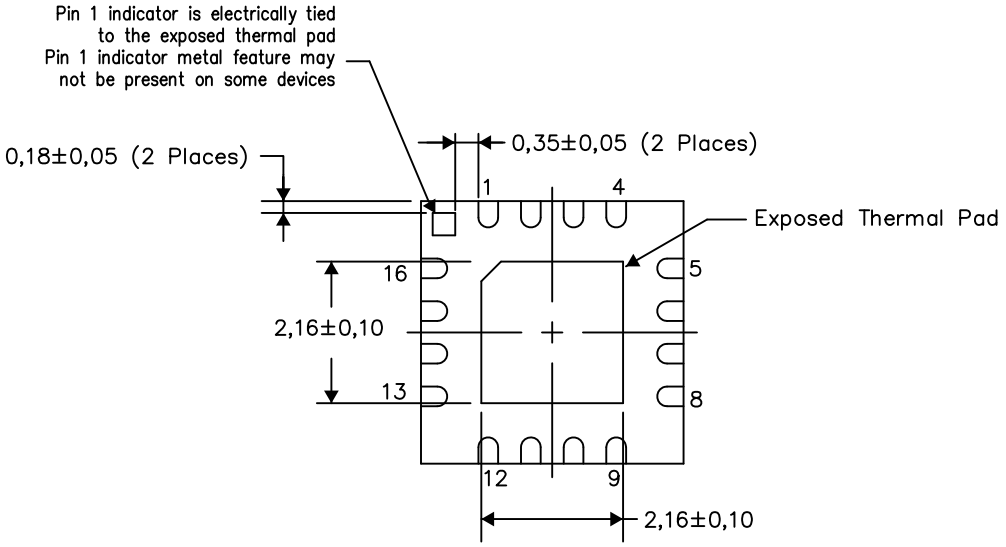
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



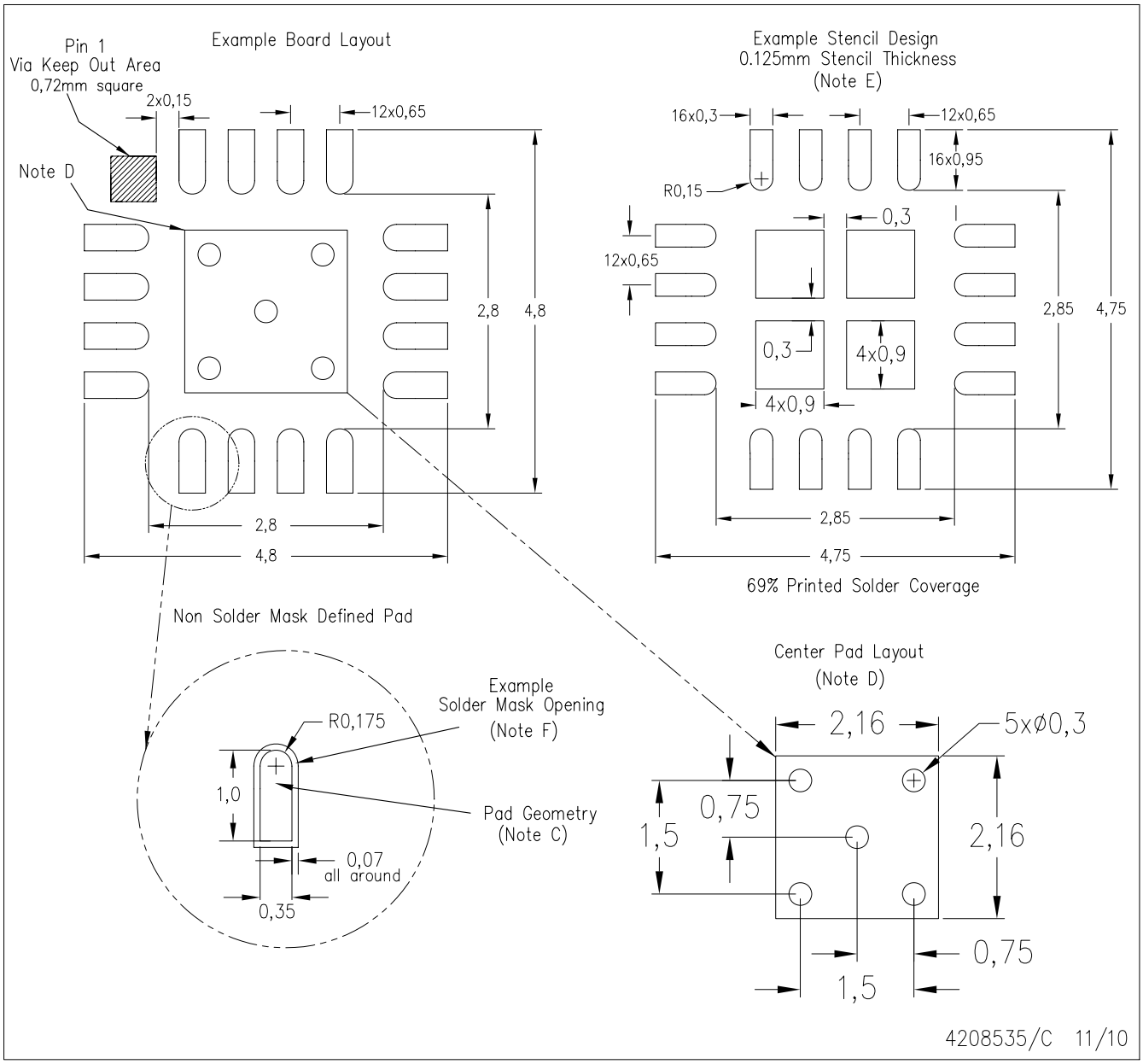
Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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