TS86436P – SP4T 200W Average Power Switch 30 MHz to 1 GHz

1.0 Features

- Low insertion loss: 0.09dB @ 30 MHz
- High isolation: 70 dB @ 30 MHz, 36 dB @ 1 GHz
- 200W CW Power
- No external DC blocking capacitors on RF lines
- All RF ports OFF state
- Versatile 2.6-5.25V power supply
- Operating frequency: 30 MHz to 1000 MHz

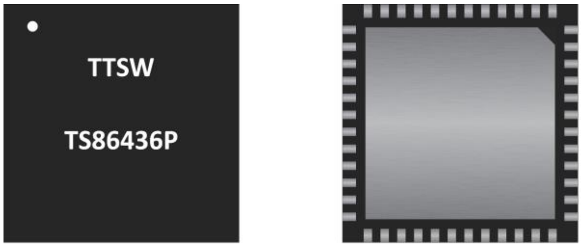

Figure 1 Device Image
(48 Pin 7×7×0.85mm QFN Package)

2.0 Applications

Private mobile and military radios
Public safety handsets
Cellular infrastructure
LTE relays and microcells
Satellite terminals

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS86436P is a 2nd Generation symmetrical reflective Single Pole Dual Throw (SP4T) switch designed for high power switching applications. The TS86436P covers 30MHz to 1000MHz bandwidth and provides low insertion loss, high isolation, and high linearity within a small package size. The TS86436P is a 200W-CW switch suitable for applications requiring low insertion loss, high isolation, and high linearity.

The TS86436P is packaged into a compact Quad Flat No lead (QFN) 7x7mm 48 leads plastic package.

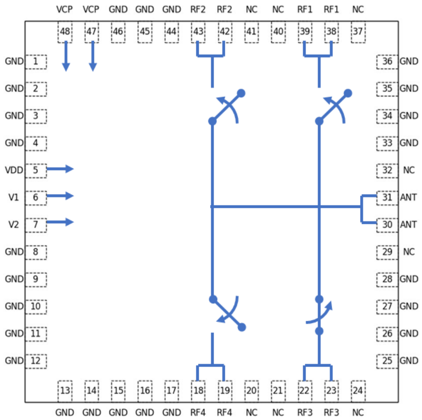

Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1a Ordering Information

Device Part Number	Package Type	Eval Board Part Number
TS86436P	48 Pin 7×7×0.85mm QFN	TS86436P-EVB

Table 1b Tape and Reel Information

Form	Quantity	Reel Diameter	Reel Width
Tape and Reel	3,000	13" (330mm)	18mm

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
47,48	VCP	Short PIN 47 and 48 and connect a 1nF capacitor to GND on this node to improve switching time.
5	VDD	DC power supply
6	V1	Switch control input 1
7	V2	Switch control input 2
1,2,3,4,8,9,10,11,12,13,14,15,16,17,18,19,20, 25,26,27,28, 33,34,35,36,41,42,43,44,45,46	NC	No internal connection, can be grounded
21,24,29,32,37,40	NC	No internal connection. Do not connect to ground
38,39	RF1	RF port 1
42,43	RF2	RF port 2
22,23	RF3	RF port 3
18,19	RF4	RF port 4
30,31	ANT	Antenna port

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias, and adequate heat sinking must be used to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
Maximum RF input power(30MHz).	RFx/ANT	54.0	dBm
Maximum RF input power(500MHz).	RFx/ANT	54.5	dBm

Maximum RF input power (30MHz, VSWR 8:1).	RFx/ANT	TBD	dBm
Maximum RF input Peak Voltage (30MHz, VSWR 8:1).	RFx/ANT	160	V
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	30	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		30		1000	MHz
Insertion loss, RFx	30 MHz		0.08		dB
	200 MHz		0.13		
	800 MHz (Matched)		0.34		
	1200 MHz (Matched)		0.39		
Isolation ANT-RFx	30 MHz		70		dB
	200 MHz		53		
	800 MHz (Matched)		41		
	1200 MHz (Matched)		33		
Return loss ANT, RFx	30 MHz		39		dB
	200 MHz		25		
	800 MHz (Matched)		18		
	1200 MHz (Matched)		20		
Harmonic distortion					
H2	30MHz, Pin=50dBm		88		dBc
H3	30MHz, Pin=50dBm		91		dBc
H2	800MHz, Pin=50dBm		75		dBc
H3	800MHz, Pin=50dBm		83		dBc
P0.1dB[1]	30MHz, CW		54		dBm
P0.1dB[1]	500MHz, CW		54		dBm
Peak P0.1dB[1]	30MHz, 1% duty cycle, 1 ms period		55.5		dBm
CP switching Noise	RBW = 1KHz		-140		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. CP=1nF to ground on VCP pin.		40		μs
Control voltage	Power Supply VDD	2.6	3.3	5.25	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current consumption, IDD	Active mode (VDD on)		160	260	μA

Note:

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5. Switch Truth Table

V1	V2	Active RF Path
0	0	ANT-RF1 ON
1	0	ANT-RF2 ON
0	1	ANT-RF3 ON
1	1	ANT-RF4 ON

Attention:

[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.

[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-RF1 ON.

9.0 Schematic and Evaluation Board

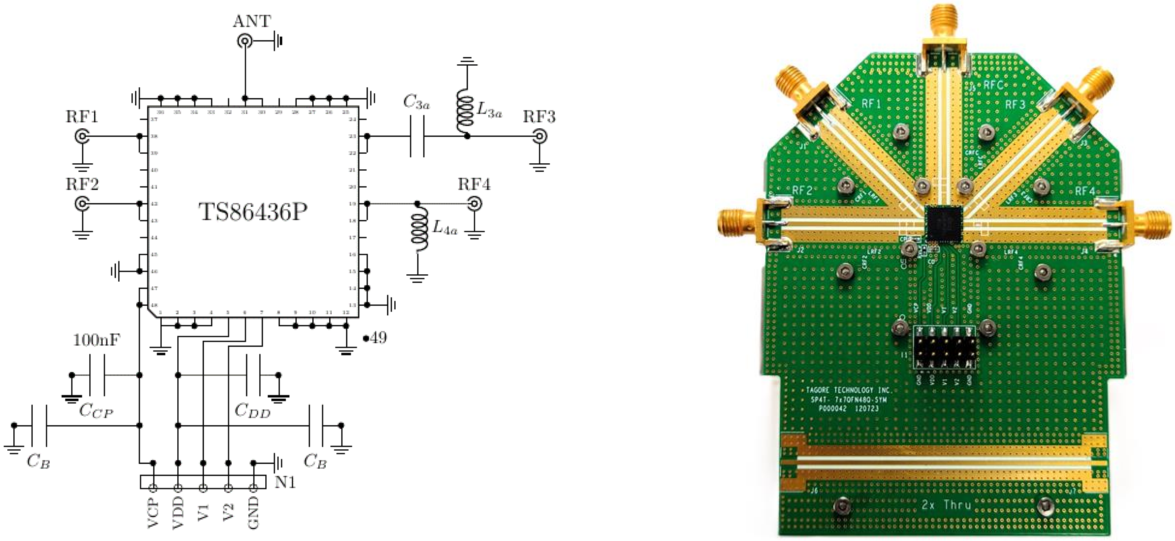

Figure 3 Evaluation Board and Schematic.

Attention:

[1] 49 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this ground pad and adequate heat sinking should be used.

[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

10.0 Typical Characteristics – Unmatched (<500 MHz)

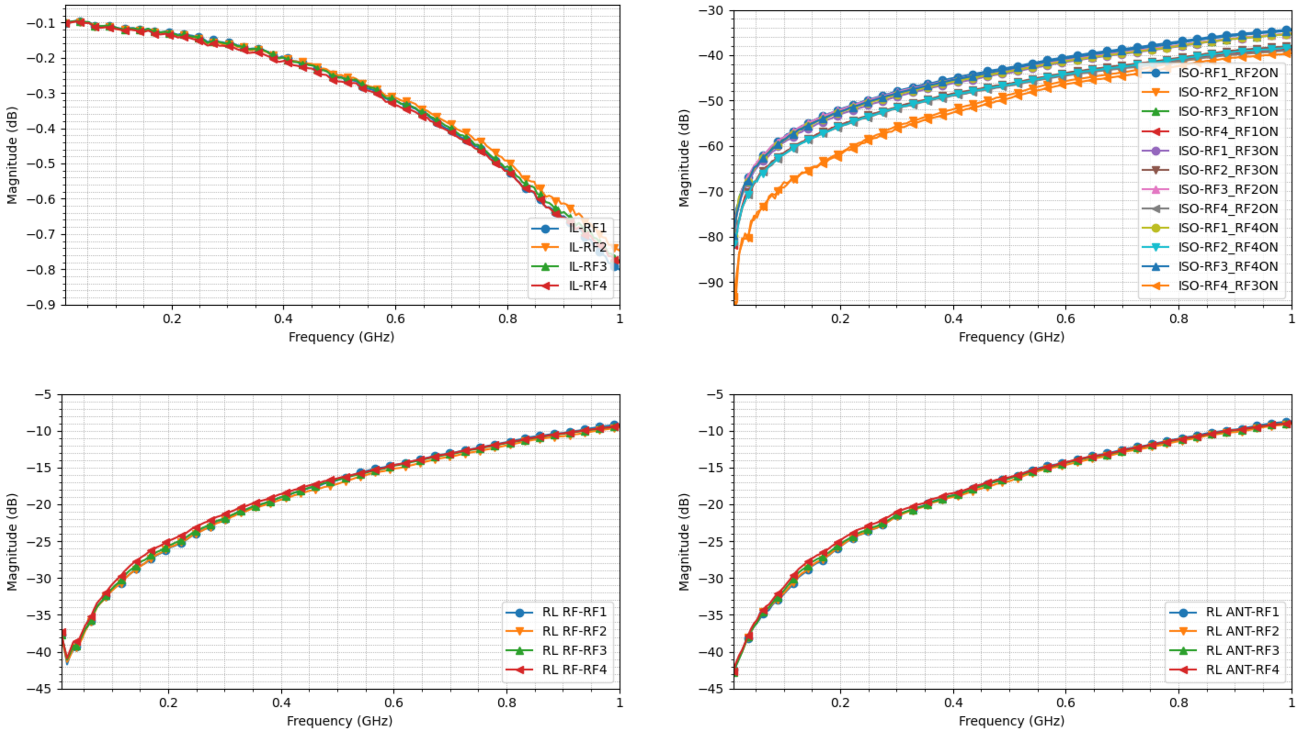

Figure 4 Typical characteristics

10.1 Typical Characteristics – Matched (760 MHz – 870 MHz)

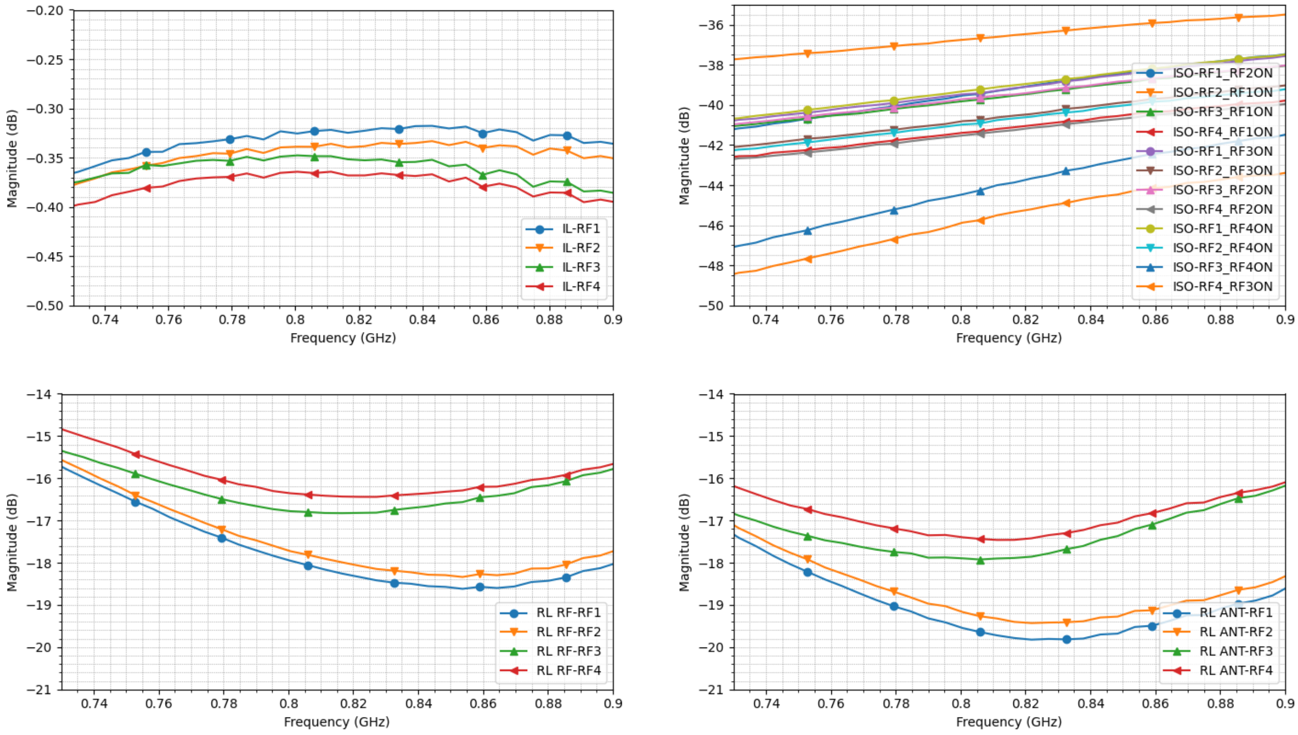

Figure 5 Typical characteristics (760 MHz – 870 MHz)

10.2 Typical Characteristics – Matched (1100 MHz – 1200 MHz)

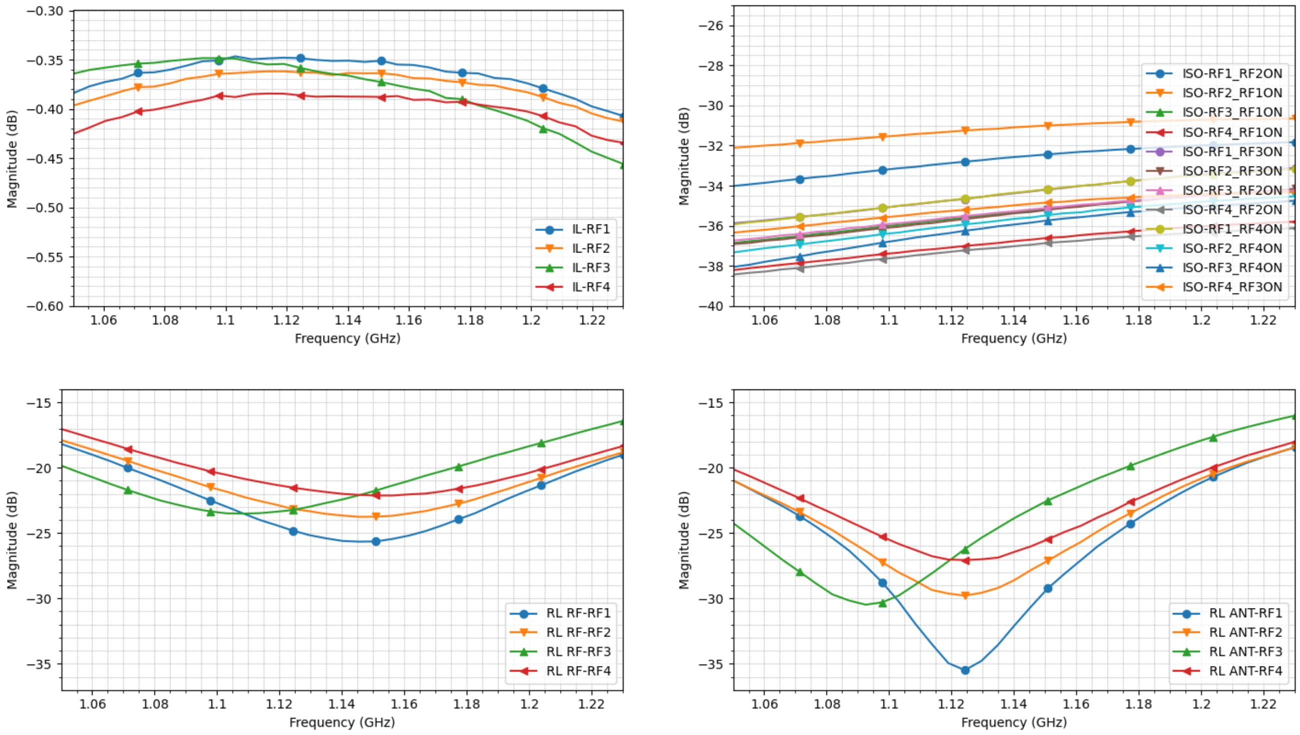

Figure 6 Typical characteristics (1100 MHz – 1200 MHz)

Table 6.1 Bill of Materials – Matching* (<500 MHz)

Component	Part Number	Description	Notes
C_{CP}	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_{DD}	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
C_{B}	UQCL2A270GAT2A	Ceramic capacitor, 27 pF, 200 V, ±2%.	Optional
L_{T}			DNP
L_{0a}			DNP
C_{0a}			DNP
L_{2a}			DNP
C_{2a}			DNP

Table 6.2 Bill of Materials – Matching* (760 MHz – 870 MHz)

Component	Part Number	Description	Notes
C_{CP}	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_{DD}	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
$L_{1a,2a,3a,4a}$	0908SQ-12N_L_	Air core chip inductor, 12.1 nH, ± 5%.	Shunt inductor at any desired RF port.
			Matching as shown in Fig. 3 RF4 example.

Table 6.3 Bill of Materials – Matching* (1100 MHz – 1200 MHz)

Component	Part Number	Description	Notes
C_{CP}	GRM155R61E104KA87D	Ceramic capacitor, 0.1 µF, 25 V, ±10%.	
C_{DD}	GRM155R71H103KA88	Ceramic capacitor, 10 nF, 50 V, ±15%.	
$C_{1a,2a,3a,4a}$	0603N100JW251	Ceramic capacitor, 10 pF, 2550 V, ±5%.	Series capacitor at any RF port.
$L_{1a,2a,3a,4a}$	0806SQ-6N0_L_	Air core chip inductor, 6.0 nH, ± 5%.	Shunt inductor at any RF port.
			Matching as shown in Fig. 3 RF3 example.

* For additional details, please contact the Tagore Technology support team.

11.0 Device Package Information

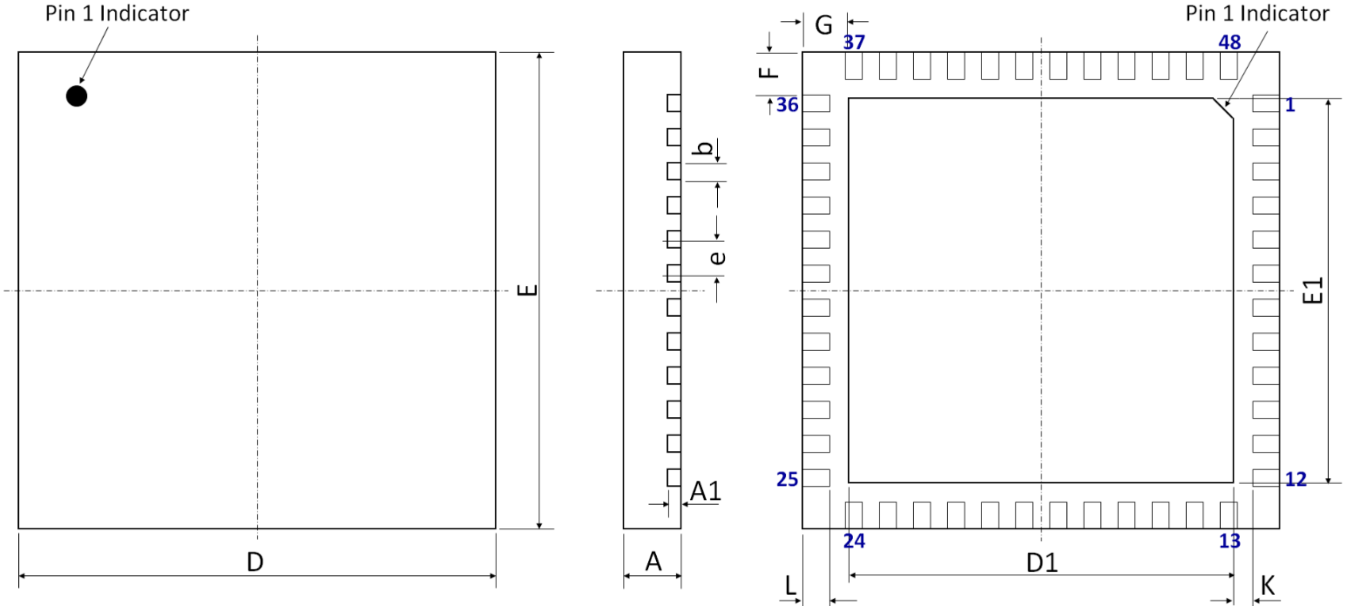

Figure 5 Device Package Drawing
(All dimensions are in mm)

Table 7 Device Package Dimensions

Dimension	**Value** (mm)	**Tolerance** (mm)	**Dimension**	**Value** (mm)	**Tolerance** (mm)
A	0.85	±0.05	E	7.00 BSC	±0.05
A1	0.203	±0.02	E1	5.65	±0.06
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	7.00 BSC	±0.05	G	0.625	±0.05
D1	5.65	±0.06	L	0.40	±0.05
e	0.50 BSC	±0.05	K	0.275	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:

[1] 4-layer PCB is recommended.
[2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 11(X)×11(Y)=121.

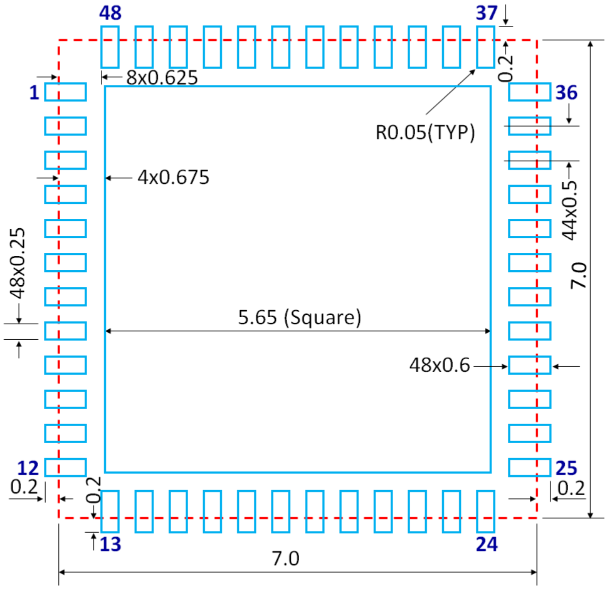

Figure 6 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 7 Solder Mask Pattern
(Dimensions are in mm)

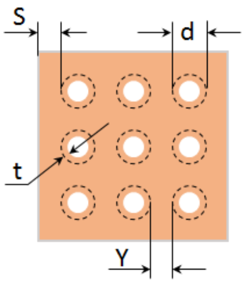

Figure 8 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.3mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125µm.

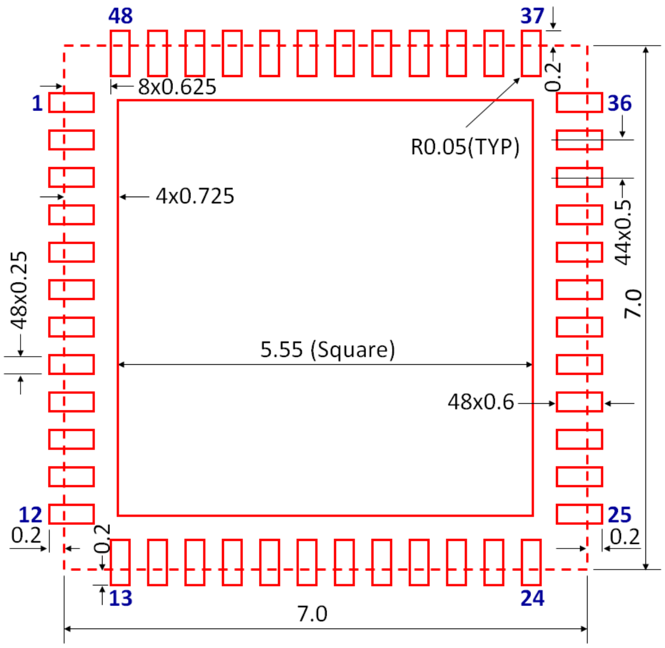

Figure 9 Stencil Openings
(Dimensions are in mm)

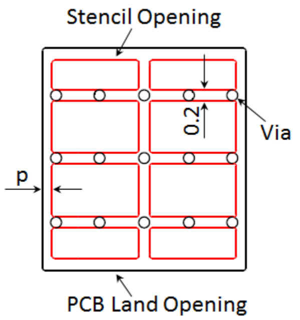

Figure 10 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

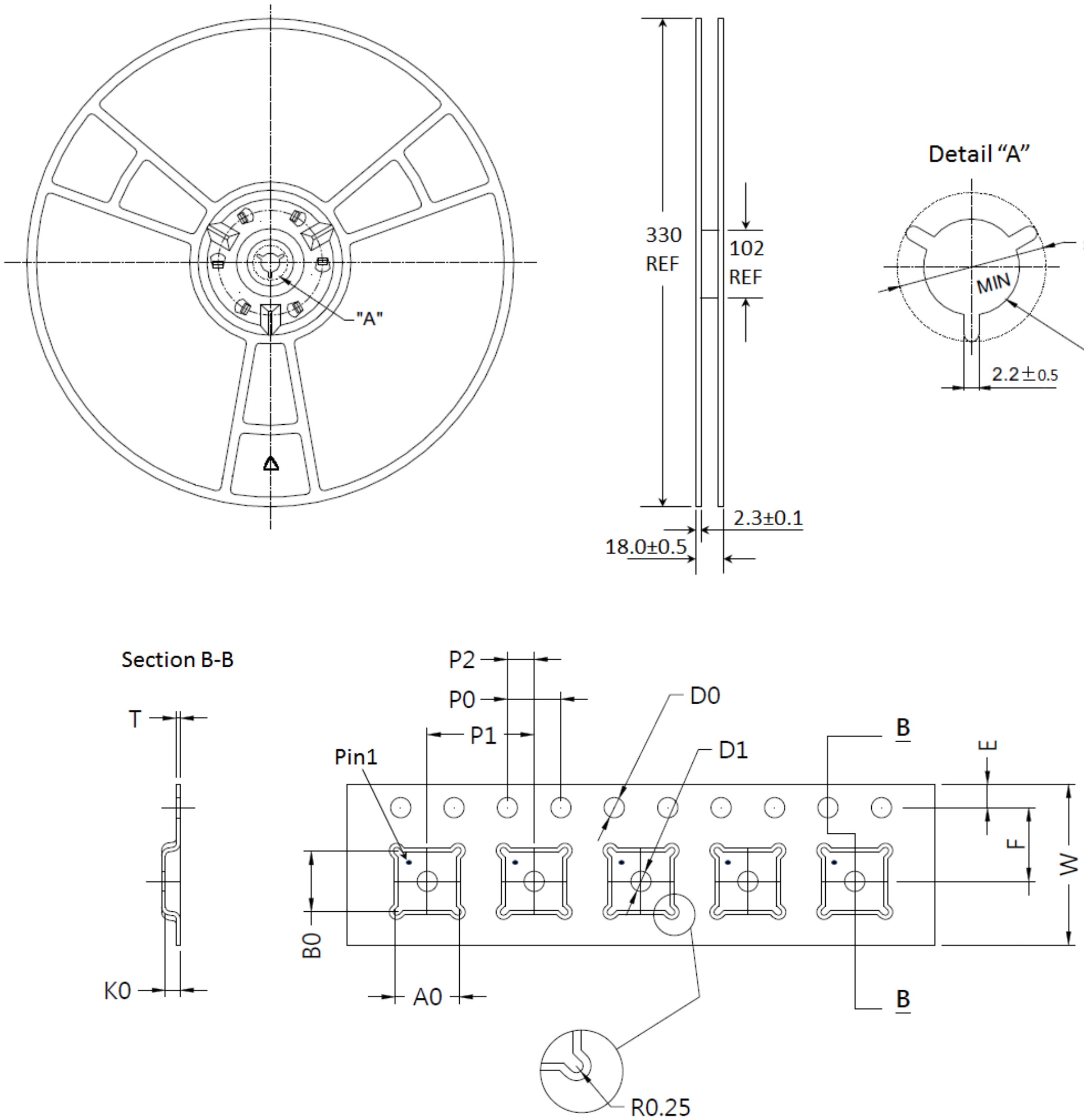

Figure 11 Tape and Reel Drawing

Table 8 Tape and Reel Dimensions

Dimension	**Value** (mm)	**Tolerance** (mm)	**Dimension**	**Value** (mm)	**Tolerance** (mm)
A0	7.35	±0.10	K0	1.10	±0.10
B0	7.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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