TS85410L - 50W CW GaN Broadband RF Switch SP4T, charge pump disabled.

1.0 Features

- Low insertion loss: 0.25dB @ 800MHz
- High isolation: 45dB @ 800MHz
- High linear power handling capability
- No external DC blocking capacitors on RF lines
- Versatile 2.6-5.5V power supply
- Internal charge pump disabled for Low noise application

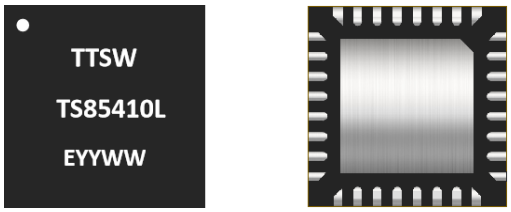

Figure 1 Device Image
(32 Pin 4×4×0.8mm QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS85410L is a symmetrical reflective Single Pole Four Throws (SP4T) switch designed for broadband, high power switching applications. Its broadband behavior from 30MHz to 3.0GHz frequencies makes the TS85410L an excellent switch for all the applications requiring low insertion loss, high isolation and high linearity within a small package size. Part can also be used below 30MHz with reduced power handling. This part has the internal charge pump disabled to eliminate the charge pump spurs. A -18V supply is needed on the VCP pin.

The TS85410L is packaged into a compact Quad Flat No lead (QFN) 4x4mm 32 leads plastic package.

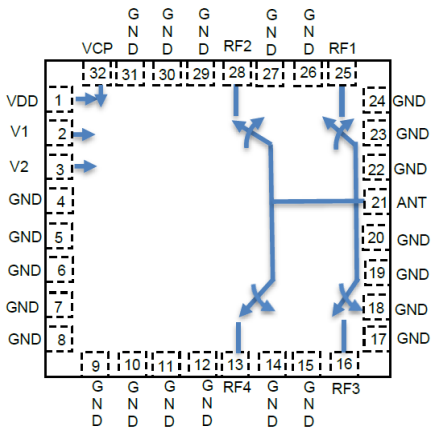

Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS85410L	32 Pin 4×4×0.8mm QFN	Tape and Reel	3000	13” (330mm)	18mm	TS85410LMTRPBF
Evaluation Board						TS85410L-EVB

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VDD	DC power supply
2	V1	Switch control input 1
3	V2	Switch control input 2
4,5,6,7,8,9,10,11,12,14,15,17, 18,19,20,22,23,24,26,27,29,30,31	NC	No internal connection, can be grounded
13	RF4	RF port 4
16	RF3	RF port 3
21	ANT	Antenna port
28	RF2	RF port 2
25	RF1	RF port 1
32	VCP	Internal charge pump is disabled.

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, 250MHz-1.2GHz	RFx	47	dBm
RF Input Power CW, 30MHz -100MHz	RFx	47	dBm
Maximum RF input power (30MHz, VSWR 8:1)	RFx/ANT	46	dBm
Maximum RF input Peak Voltage (30MHz, VSWR 8:1)	RFx/ANT	120	V
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	5	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 37	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		30		3000	MHz
Insertion Loss, RFx	400MHz		0.20		dB
	800MHz		0.25		
	3000MHz		0.87		
	3000MHz (matched)		0.52		
Isolation, ANT-RFx	400MHz		55		dB
	800MHz		45		
	3000MHz		24		
	3000MHz (matched)		23		
Return Loss, ANT-RFx	400MHz		28		dB
	800MHz		25		
	3000MHz		10		
	3000MHz (matched)		18		
H2	800MHz, Pin=40dBm		-84		dBc
H3	800MHz, Pin=40dBm		-86		dBc
IIP3	800MHz		70		dBm
P0.1dB[1]	250MHz – 1.2GHz, CW	47	49		dBm
P0.1dB[1]	100MHz – <250MHz, CW	47	48		dBm
P0.1dB[1]	30MHz – <100MHz, CW	47	48		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled.		2.3		μs
VCP	Iload of 10uA	-19	-18	-17	V
VCP Sourcing Current	Sourcing current of external VCP supply	100			uA
Control Voltage	Power supply VDD	2.6	3.3	5.5	V
	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
Control Current	All control pins low, I_{il}		0		μA
	All control pins high, I_{ih}			7.5	μA
Current Consumption, IDD	Active mode		50	75	μA

Note: [1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	0	ANT-RF1
1	0	ANT-RF2
0	1	ANT-RF3
1	1	ANT-RF4

Attention:
[1] VDD should be applied first before VCP. Minimum time between VDD and VCP should be 50usec. Otherwise, may cause damage to the device.
[2] There is an internal pull-down to ground on V1 and V2 control pins, therefore the switch state at start-up without any control voltage applied will be ANT-RF1 on by default.

9.0 Evaluation Board Schematic

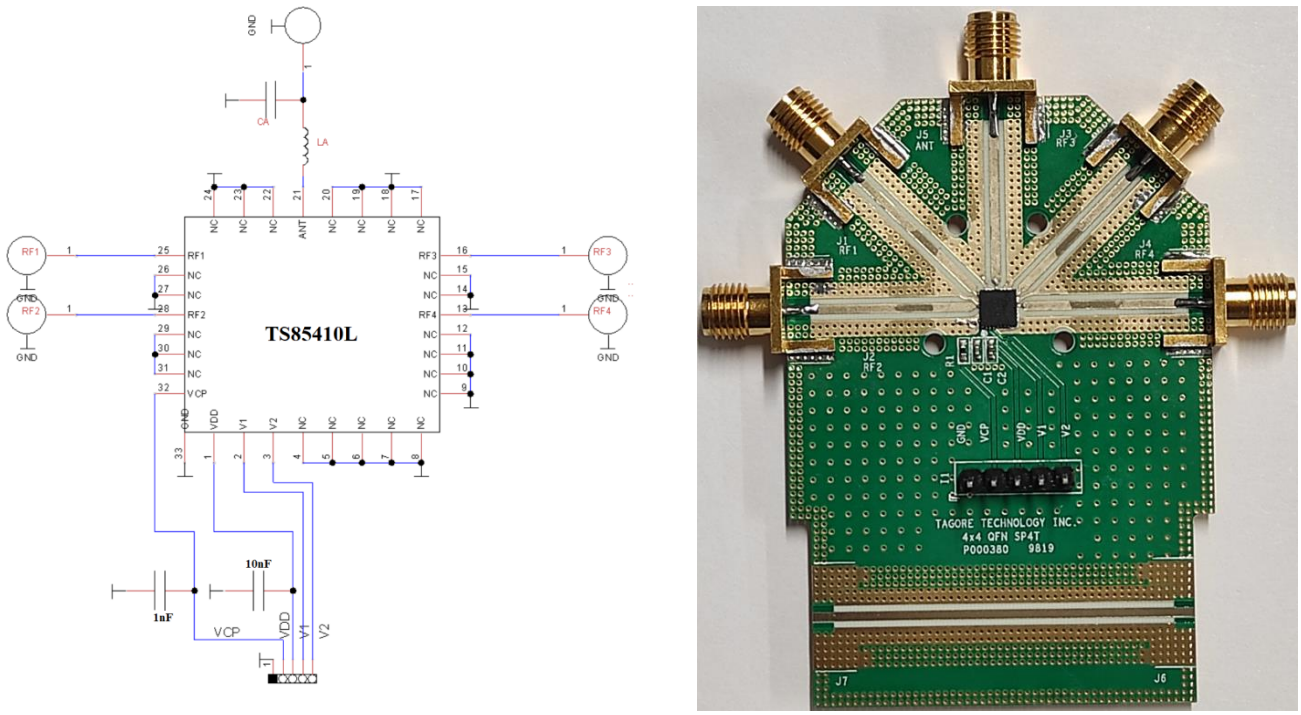

Figure 3 Evaluation Board Schematic and Picture (No Match)

Attention:
[1] **33 refers to the center pad of the device. Multiple Plugged through hole vias should be added to this Ground Pad and adequate heat sinking should be used.**
[2] Place matching components close to pin of the part.

Table 6 Recommended Evaluation Board Component Values

Reference Designator	Value	Part #	Manufacturer
LA	1.6 nH	0603CS-1N6XJLW	Coil Craft
CA	0.6 pF	0603N0R6BW251	Passive Plus Inc

10.0 Typical Characteristics (unmatched)

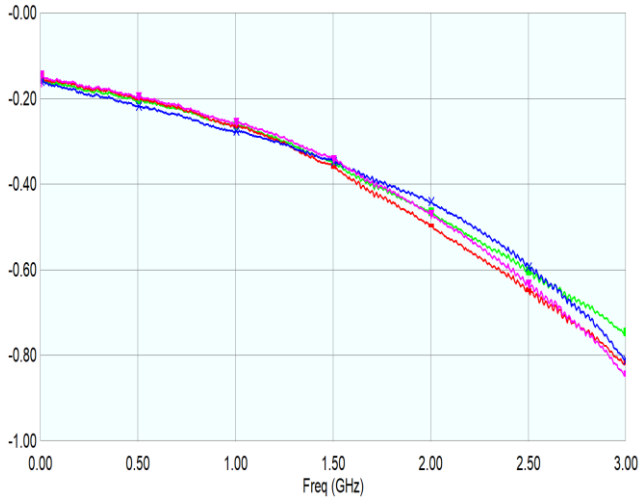

Figure 4 RF1 to RF4 Insertion Loss

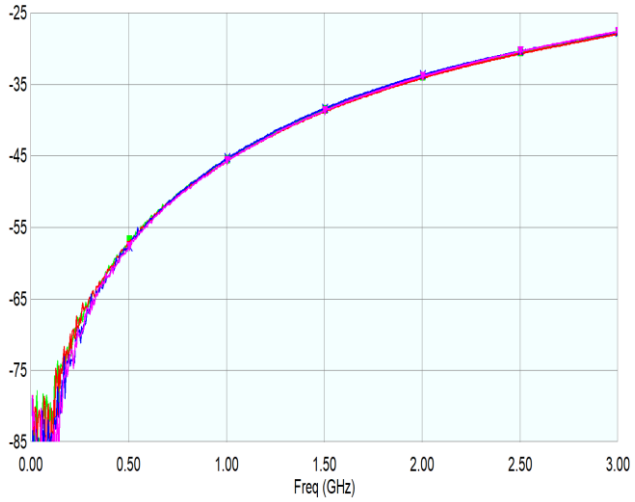

Figure 5 RF1 on, RF2 to RF4 Isolation

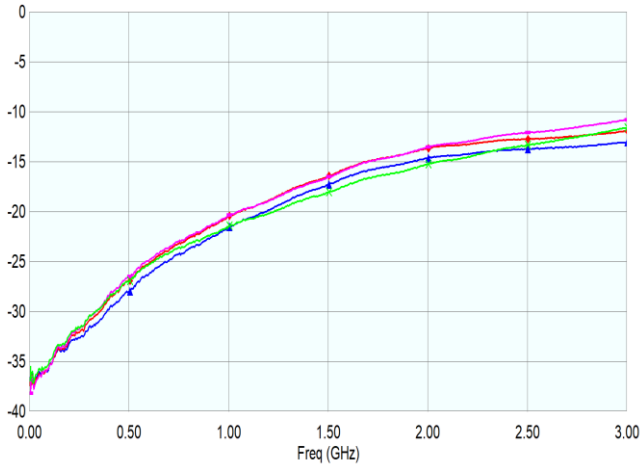

Figure 6 RF1 to RF4 Return Loss

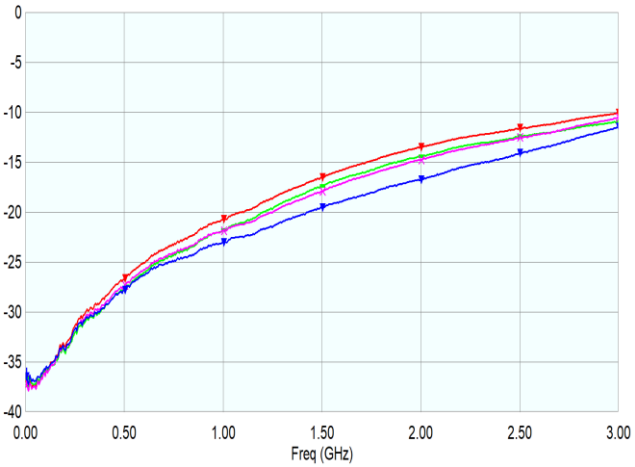

Figure 7 ANT Return Loss

10.0 Typical Characteristics (matched)

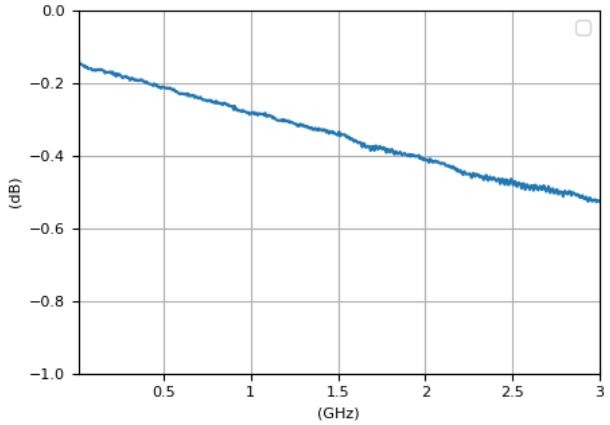

Figure 4 RF1 to RF4 Insertion Loss

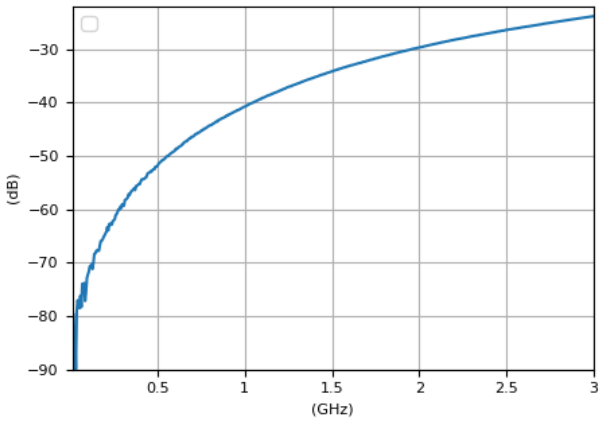

Figure 5 RF1 on, RF2 to RF4 Isolation

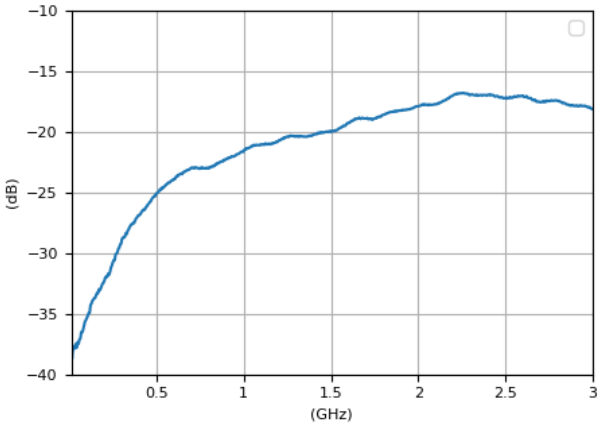

Figure 6 RF1 to RF4 Return Loss

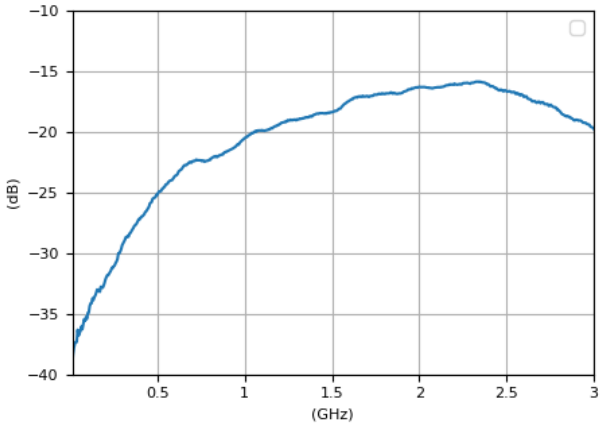

Figure 7 ANT Return Loss

11.0 Device Package Information

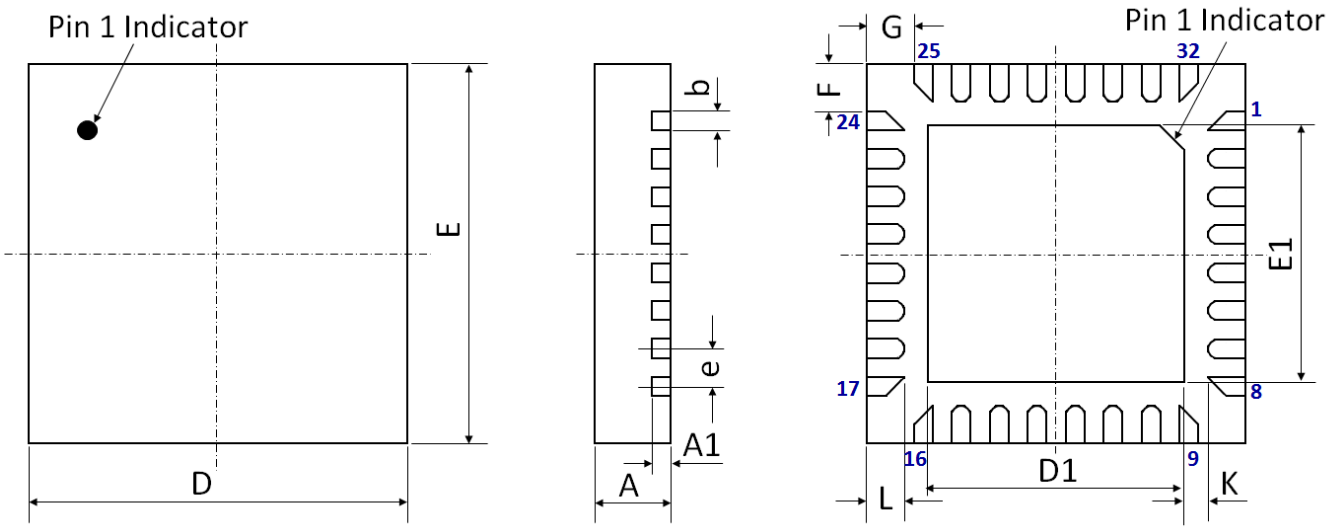

Figure 8 Device Package Drawing
(All dimensions are in mm)

Table 6 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.80	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:

Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering related guidelines.

12.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 4(X)×4(Y)=16.

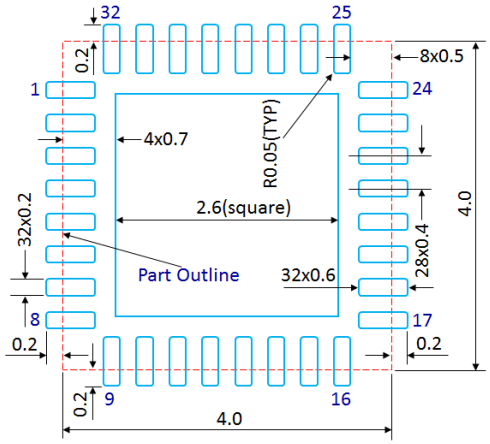

Figure 9 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 10 Solder Mask Pattern
(Dimensions are in mm)

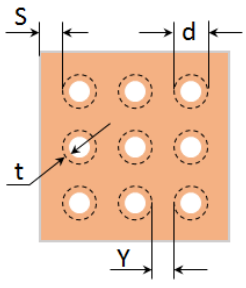

Figure 11 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

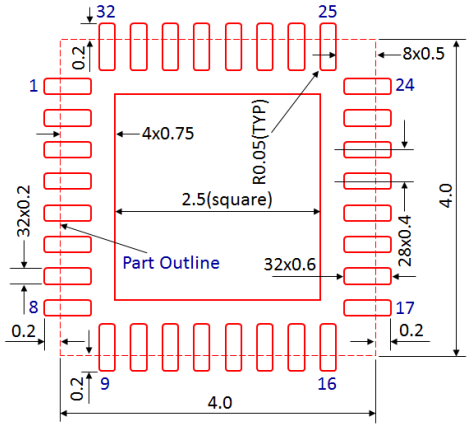

Figure 12 Stencil Openings
(Dimensions are in mm)

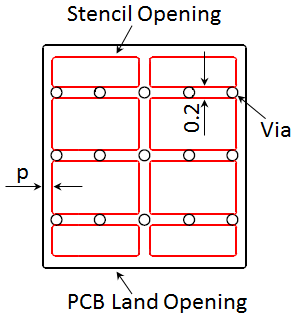

Figure 13 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

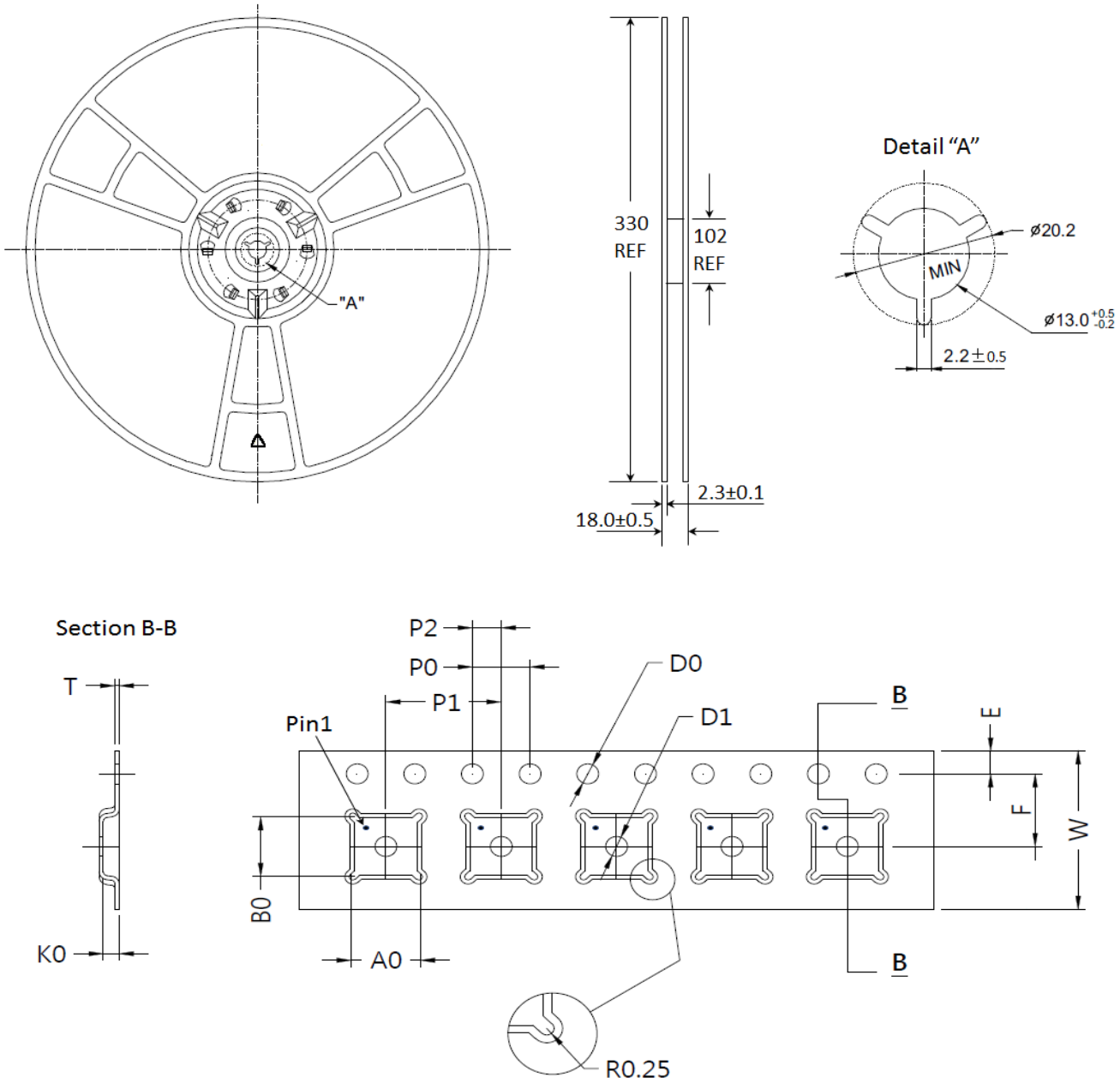

Figure 14 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	4.35	±0.10	K0	1.10	±0.10
B0	4.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

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