

# TS8329K - 100W Asymmetric Peak Power GaN Broadband SPDT Switch

## 1.0 Features

- Low insertion loss (TX/RX): 0.4/0.5dB @ 3000MHz
- High isolation (RX Path): 38dB @ 3000MHz
- High peak power handling capability
- No external DC blocking capacitors on RF lines
- 40 dBm CW hot switching on Ant port
- 42 dBm Average, 10dB PAPR LTE single event (<10 sec)
- All RF ports OFF state
- Versatile 2.6-5.5V power supply
- Operating frequency: 500MHz to 8.5GHz



**Figure 1 Device Image**  
(16 Pin 3x3x0.8mm QFN Package)

## 2.0 Applications

- 4G, 5G systems
- RX protection
- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Radar

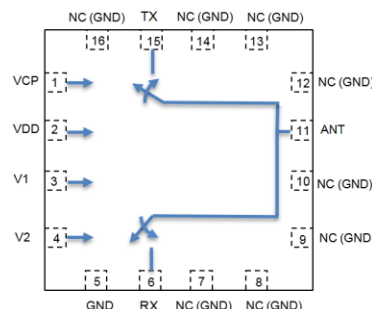


**RoHS/REACH/Halogen Free Compliance**

## 3.0 Description

The TS8329K is an asymmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high peak power switching applications. Its broadband behavior from 500MHz to 8.5GHz frequencies makes the TS8329K an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS8329K is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.



**Figure 2 Function Block Diagram**  
(Top View)

## 4.0 Ordering Information

**Table 1 Ordering Information**

| Base Part Number | Package Type         | Form          | Qty  | Reel Diameter | Reel Width | Orderable Part Number |
|------------------|----------------------|---------------|------|---------------|------------|-----------------------|
| TS8329K          | 16 Pin 3x3x0.8mm QFN | Tape and Reel | 3000 | 13" (330mm)   | 18mm       | TS8329KMTRPBF         |
| Evaluation Board |                      |               |      |               |            | TS8329K-EVB           |

## 5.0 Pin Description

**Table 2 Pin Definition**

| Pin Number           | Pin Name | Description  |
|----------------------|----------|--|
| 1                    | VCP      | Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time. |
| 2                    | VDD      | DC power supply  |
| 3                    | V1       | Switch control input 1   |
| 4                    | V2       | Switch control input 2   |
| 5                    | GND      | Ground   |
| 6                    | RX       | RX port  |
| 7,8,9,10,12,13,14,16 | NC       | No internal connection, Can be grounded  |
| 11                   | ANT      | Antenna port   |
| 15                   | TX       | TX port  |

**Note:** The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

## 6.0 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings** @T<sub>A</sub>=+25°C Unless Otherwise Specified

| Parameter   | Symbol            | Value        | Unit |
|---|-------------------|--------------|------|
| <b>Electrical Ratings</b>                           |                   |              |      |
| Power Supply Voltage                                | VDD               | 2.6 to 5.5   | V    |
| Storage Temperature Range                           | T <sub>st</sub>   | -55 to +125  | °C   |
| Operating Temperature Range                         | T <sub>op</sub>   | -40 to +85   | °C   |
| Maximum Junction Temperature                        | T <sub>J</sub>    | +140         | °C   |
| RF Input Power CW, 800MHz, T <sub>J</sub> =+85°C    | TX-ANT            | 42           | dBm  |
| RF Input Power CW, 800MHz, T <sub>J</sub> =+105°C   | TX-ANT            | 41           | dBm  |
| <b>Thermal Ratings</b>                              |                   |              |      |
| Thermal Resistance (junction-to-case) – Bottom side | R <sub>θJC</sub>  | 25           | °C/W |
| Thermal Resistance (junction-to-top)                | R <sub>θJT</sub>  | 36           | °C/W |
| Soldering Temperature                               | T <sub>SOLD</sub> | 260          | °C   |
| <b>ESD Ratings</b>                                  |                   |              |      |
| Human Body Model (HBM)                              | Level 1B          | 500 to <1000 | V    |
| Charged Device Model (CDM)                          | Level C3          | ≥1000        | V    |
| <b>Moisture Rating</b>                              |                   |              |      |
| Moisture Sensitivity Level                          | MSL               | 1            | -    |

### Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

## 7.0 Electrical Specifications

**Table 4 Electrical Specifications** @T<sub>A</sub>=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

| Parameter                     | Condition   | Minimum | Typical | Maximum | Unit |
|-------------------------------|---|---------|---------|---------|------|
| Operating Frequency           |   | 500     |         | 8500    | MHz  |
| Insertion Loss, TX            | 800MHz  |         | 0.30    | 0.40    | dB   |
|                               | 1.95GHz   |         | 0.35    | 0.45    |      |
|                               | 2.6GHz  |         | 0.38    | 0.55    |      |
|                               | 3.8GHz  |         | 0.40    |         |      |
|                               | 5.0GHz  |         | 0.45    |         |      |
| Insertion Loss, RX            | 800MHz  |         | 0.34    | 0.65    | dB   |
|                               | 1.95GHz   |         | 0.40    | 0.70    |      |
|                               | 2.6GHz  |         | 0.45    | 0.75    |      |
|                               | 3.8GHz  |         | 0.60    |         |      |
|                               | 5.0GHz  |         | 0.80    |         |      |
| Isolation ANT-TX              | 800MHz  | 39      | 48      |         | dB   |
|                               | 1.95GHz   | 30      | 36      |         |      |
|                               | 2.6GHz  | 27      | 32      |         |      |
|                               | 3.8GHz  |         | 25      |         |      |
|                               | 5.0GHz  |         | 21      |         |      |
| Isolation ANT-RX              | 800MHz  | 52      | 58      |         | dB   |
|                               | 1.95GHz   | 42      | 46      |         |      |
|                               | 2.6GHz  | 37      | 41      |         |      |
|                               | 3.8GHz  |         | 35      |         |      |
|                               | 5.0GHz  |         | 32      |         |      |
| Return Loss<br>ANT-TX, RX     | 800MHz  |         | 25      |         | dB   |
|                               | 1.95GHz   |         | 23      |         |      |
|                               | 2.6GHz  |         | 22      |         |      |
|                               | 3.8GHz  |         | 17      |         |      |
|                               | 5.0GHz  |         | 14      |         |      |
| Isolation @ Peak Power        | Peak power=49.2dBm, Isolation RX @3.8GHz                                  |         | 35      |         | dB   |
| <b>Harmonic distortion</b>    |   |         |         |         |      |
| H2                            | 800MHz, Pin=35dBm   |         | -40     |         | dBm  |
| H3                            | 800MHz, Pin=35dBm   |         | -45     |         | dBm  |
| IIP3                          | 800MHz  |         | 71      |         | dBm  |
| P0.1dB <sup>[1]</sup> TX      | 700MHz~6GHz, CW   | 42      | 44      |         | dBm  |
| Peak P0.1dB TX <sup>[2]</sup> | 700MHz~6GHz, pulsed power   | 49.2    | 50      |         | dBm  |
| Peak P0.1dB TX <sup>[2]</sup> | 42 dBm Avg, 10dB PAPR LTE single event (<10 sec)                          |         | 52      |         | dBm  |
| P0.1dB <sup>[1]</sup> RX      | 700MHz~6GHz, CW   | 39      | 41      |         | dBm  |
| Switching Time                | 50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3) |         | 0.4     |         | μs   |
| Control Voltage               | Power supply VDD  | 2.6     | 3.3     | 5.5     | V    |
|                               | All control pins high, V <sub>ih</sub>                                    | 1.0     | 3.3     | 5.25    | V    |
|                               | All control pins low, V <sub>il</sub>                                     | -0.3    |         | 0.5     | V    |
| Control Current               | All control pins low, I <sub>li</sub>                                     |         | 0       |         | μA   |
|                               | All control pins high, I <sub>lh</sub>                                    |         |         | 7.5     | μA   |
| Current Consumption, IDD      | Active mode   |         | 160     | 200     | μA   |

**Note:**

[1] P0.1dB is a figure of merit.

[2] Peak power was verified with 1% duty cycle and 10μs pulse width.

[3] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

## 8.0 Switch Truth Table

**Table 5 Switch Truth Table**

| V1 | V2 | Active RF Path |
|----|----|----------------|
| 0  | 1  | All OFF        |
| 0  | 0  | ANT-RX         |
| 1  | 0  | ANT-TX         |

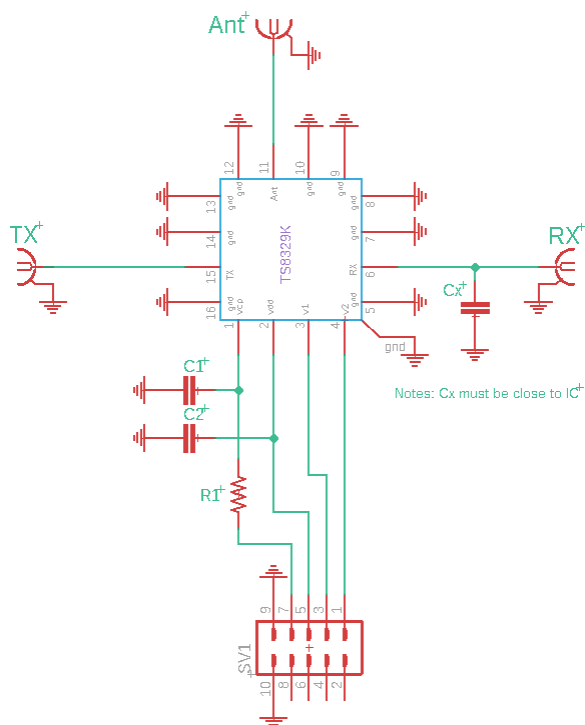
### Attention:

[1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.

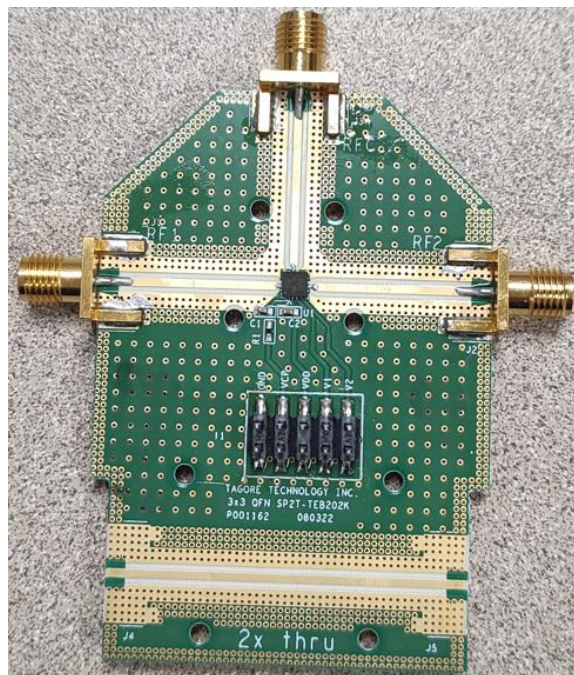
[2] There are internal pull-downs to ground on both V1 and V2 control pins, the state at start-up without any control voltage applied will be ANT-TX ON.

[3] If all OFF state is not used, the switch can be operated with single control pin V1.

## 9.0 Evaluation Board



**Figure 3 Evaluation Board Schematic**



**Figure 4 Evaluation Board Image**

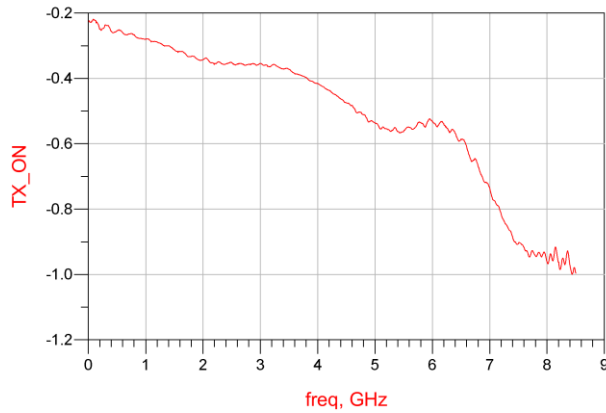
### Attention:

[1] 17 refers to the center pad of the device.

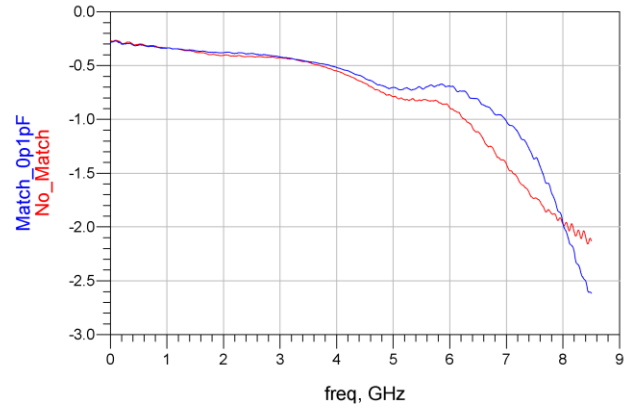
[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

[3] For 5-7GHz matching circuit, at RX port, add a Cx shunt 0.1pF capacitor (PPI 0603N) as close as possible to IC, plot shown in Fig 6.

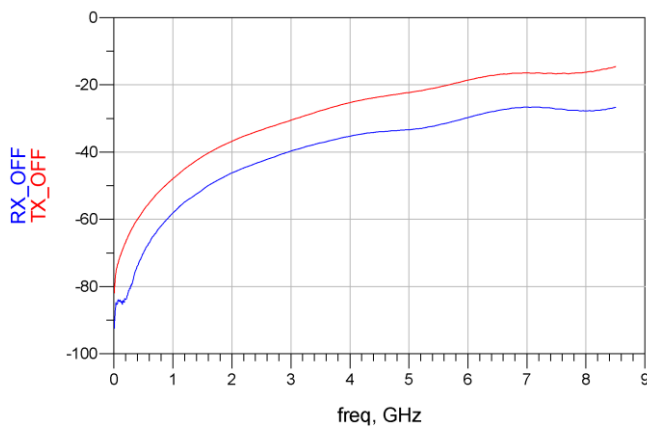
## 10.0 Typical Characteristics



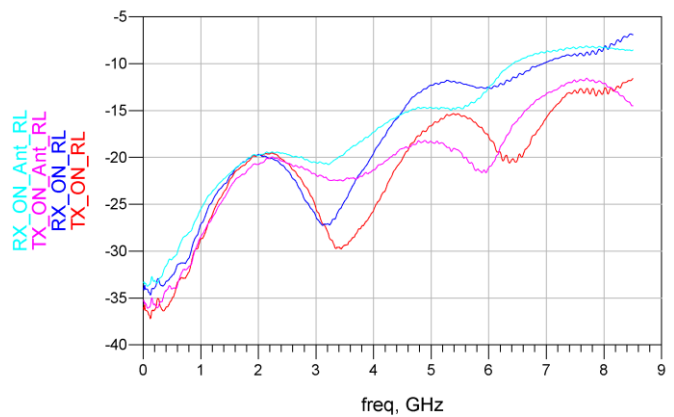
**Figure 5 TX Insertion Loss**



**Figure 6 RX Insertion Loss  
(with/without high-freq match)**

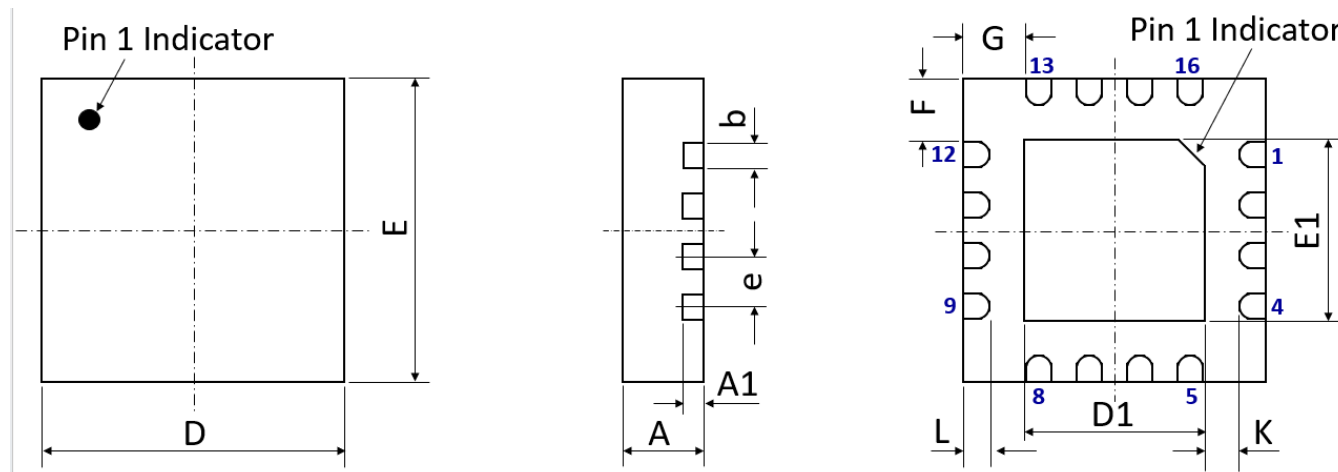


**Figure 7 TX, RX Isolation**



**Figure 8 Return Loss RF & Ant**

## 11.0 Device Package Information



**Figure 13 Device Package Drawing**  
(All dimensions are in mm)

**Table 6 Device Package Dimensions**

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A              | 0.80       | ±0.05          | E              | 3.00 BSC   | ±0.05          |
| A1             | 0.203      | ±0.02          | E1             | 1.70       | ±0.05          |
| b              | 0.25       | ±0.05          | F              | 0.625      | ±0.05          |
| D              | 3.00 BSC   | ±0.05          | G              | 0.625      | ±0.05          |
| D1             | 1.70       | ±0.05          | L              | 0.25       | ±0.05          |
| e              | 0.50 BSC   | ±0.05          | K              | 0.40       | ±0.05          |

**Note:** Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

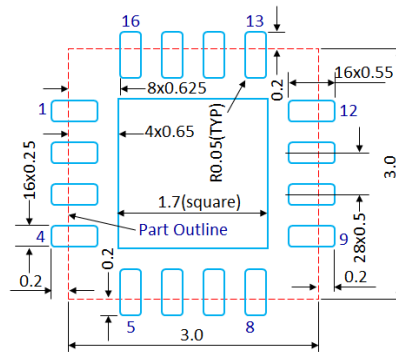
**Attention:**

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering related guidelines.

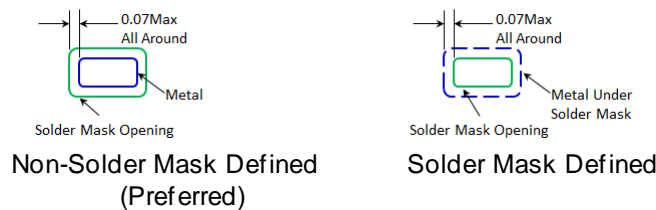
## 12.0 PCB Land Design

### Guidelines:

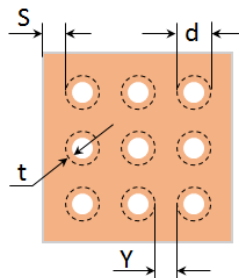
- [1] 4 layer PCB is recommended.
- [2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is  $3(X) \times 3(Y) = 9$ .



**Figure 14 PCB Land Pattern**  
(Dimensions are in mm)



**Figure 15 Solder Mask Pattern**  
(Dimensions are in mm)



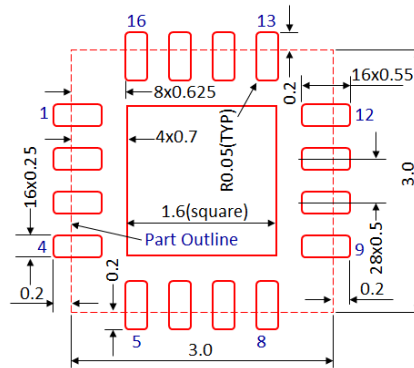
**Figure 16 Thermal Via Pattern**

(Recommended Values:  $S \geq 0.15\text{mm}$ ;  $Y \geq 0.20\text{mm}$ ;  $d = 0.2\text{mm}$ ; Plating Thickness  $t = 25\mu\text{m}$  or  $50\mu\text{m}$ )

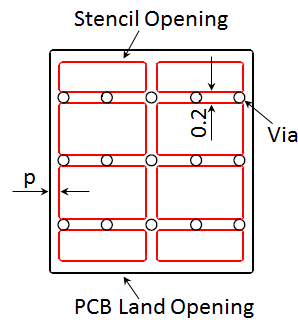
## 13.0 PCB Stencil Design

### Guidelines:

- [1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.
- [2] Stencil thickness is recommended to be 125 $\mu$ m.



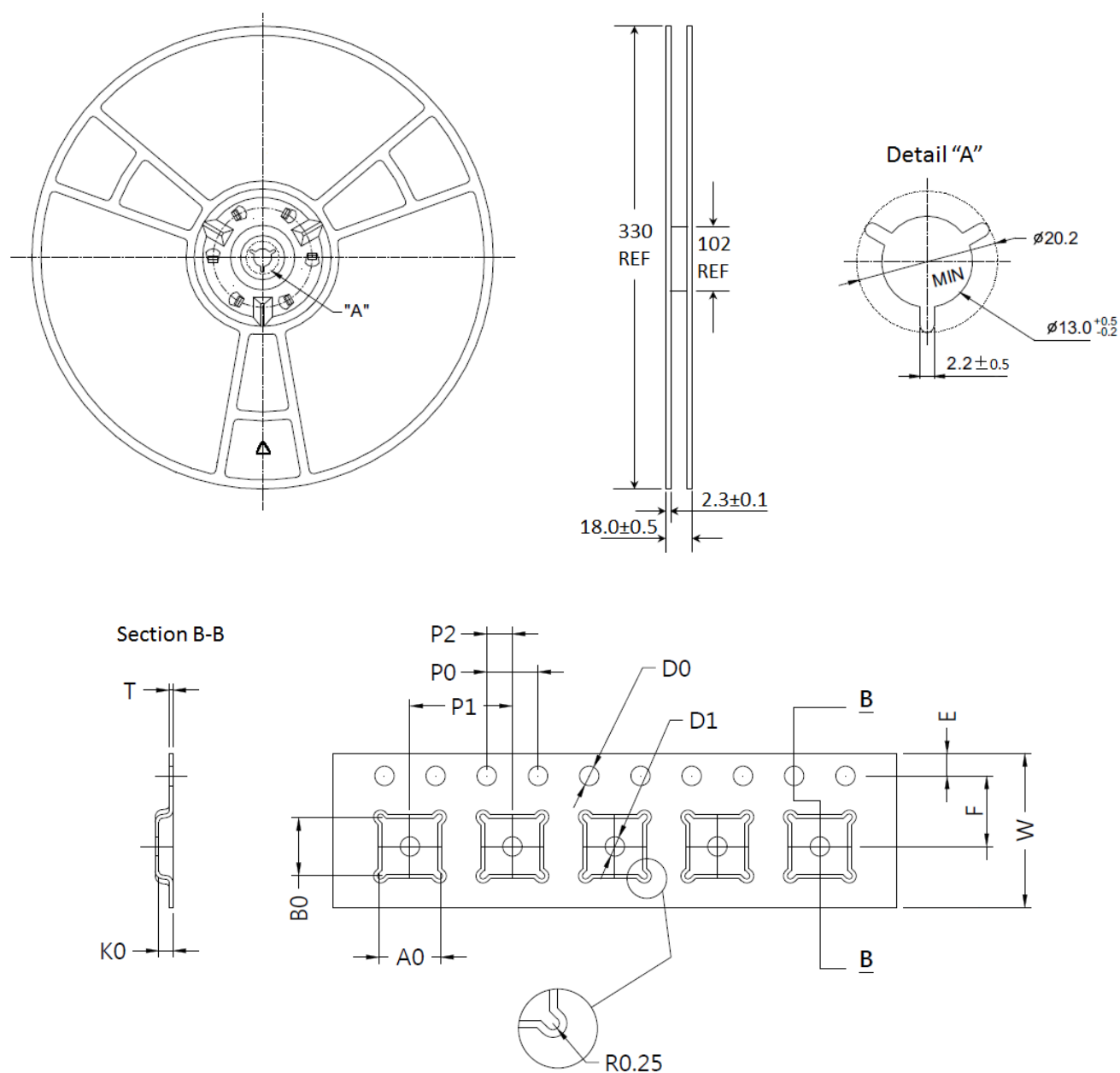
**Figure 17 Stencil Openings**  
(Dimensions are in mm)



**Figure 18 Stencil Openings Shall not Cover Via Areas If Possible**  
(Dimensions are in mm)



## 14.0 Tape and Reel Information



**Figure 19 Tape and Reel Drawing**

**Table 7 Tape and Reel Dimensions**

| Dimension (mm) | Value (mm) | Tolerance (mm) | Dimension (mm) | Value (mm) | Tolerance (mm) |
|----------------|------------|----------------|----------------|------------|----------------|
| A0             | 3.35       | ±0.10          | K0             | 1.10       | ±0.10          |
| B0             | 3.35       | ±0.10          | P0             | 4.00       | ±0.10          |
| D0             | 1.50       | +0.10/-0.00    | P1             | 8.00       | ±0.10          |
| D1             | 1.50       | +0.10/-0.00    | P2             | 2.00       | ±0.05          |
| E              | 1.75       | ±0.10          | T              | 0.30       | ±0.05          |
| F              | 5.50       | ±0.05          | W              | 12.00      | ±0.30          |

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