



TS5A3166-Q1 0.9-Ω SPST Analog Switch

1 Features

- Qualified for Automotive Applications
- Isolation in Powered-Off Mode, $V_+ = 0$
- Low ON-State Resistance (0.9 Ω)
- Control Inputs are 5.5 V Tolerant
- Low Charge Injection
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Radar System
- Infotainment System
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals
- Microphone Switching – Notebook Docking

3 Description

The TS5A3166-Q1 is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3166-Q	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

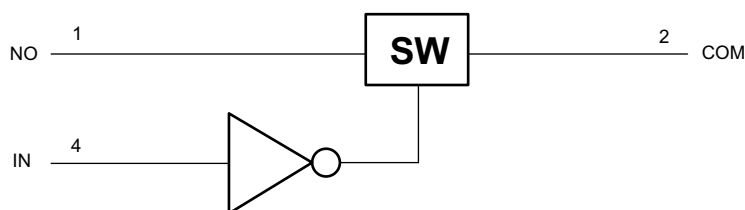


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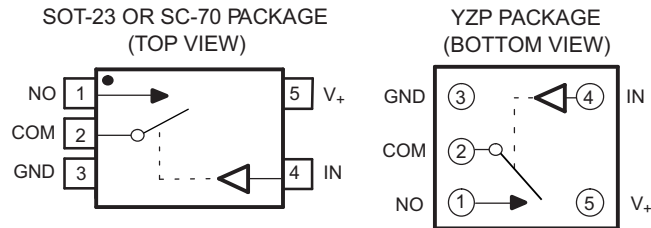
5 Revision History

Changes from Original (July 2014) to Revision A

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• Initial release of full document.	1
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6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NO	1	IO	Normally closed
COM	2	IO	Common
GND	3	GND	Digital ground
IN	4	Input	Digital control pin to connect COM to NO
V ₊	5	Power	Power Supply

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V ₊	Supply voltage range ⁽³⁾		−0.5	6.5	V
V _{NO} V _{COM}	Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾		−0.5	V ₊ + 0.5	V
I _K	Analog port diode current	V _{NO} , V _{COM} < 0	−50		mA
I _{NO} I _{COM}	On-state switch current	V _{NO} , V _{COM} = 0 to V ₊	−200	200	mA
	On-state peak switch current ⁽⁶⁾		−400	400	
V _I	Digital input voltage range ⁽³⁾⁽⁴⁾		−0.5	6.5	V
I _{IK}	Digital clamp current	V _I < 0	−50		mA
I ₊	Continuous current through V ₊		100		mA
I _{GND}	Continuous current through GND		−100		mA
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
V_+	Supply voltage	0	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS5A3166-Q1	UNIT
		DCK	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	283.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	
Ψ_{JT}	Junction-to-top characterization parameter	1.7	
Ψ_{JB}	Junction-to-board characterization parameter	60.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics for 5-V Supply⁽¹⁾

 $V_+ = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch												
Analog signal range	V _{COM} , V _{NO}					0		V ₊	0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	4.5 V	0.8	1.1		0.8	1.1		Ω
				Full			1.2		1.44			
ON-state resistance	r _{on}	V _{NO} = 2.5 V, I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	4.5 V	0.7	0.9		0.7	0.9		Ω
				Full			1		1.2			
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	4.5 V	0.15			0.15			Ω
		V _{NO} = 1 V, 1.5 V, 2.5 V, I _{COM} = −100 mA,		25°C		0.09	0.15		0.09	0.15		
				Full		0.15			0.18			
NO OFF leakage current	I _{NO(OFF)}	V _{NO} = 1 V, V _{COM} = 4.5 V, or V _{NO} = 4.5 V, V _{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	−20	4	20	−80	4	80	nA
				Full		−100		100	−400		400	
	I _{NO(PWROFF)}	V _{NO} = 0 to 5.5 V, V _{COM} = 5.5 V to 0,		25°C	0 V	−5	0.4	5	−5	0.4	5	μA
				Full		−15		15	−30		30	
COM OFF leakage current	I _{COM(OFF)}	V _{COM} = 1 V, V _{NO} = 4.5 V, or V _{COM} = 4.5 V, V _{NO} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	−20	4	20	−80	4	80	nA
				Full		−100		100	−400		400	
	I _{COM(PWROFF)}	V _{COM} = 5.5 V to 0, V _{NO} = 0 to 5.5 V,		25°C	0 V	−5	0.4	5	−5	0.4	5	μA
				Full		−15		15	−30		30	
NO ON leakage current	I _{NO(ON)}	V _{NO} = 1 V, V _{COM} = Open, or V _{NO} = 4.5 V, V _{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	−2	0.3	2	−80	0.3	80	nA
				Full		−20		20	−400		400	
COM ON leakage current	I _{COM(ON)}	V _{COM} = 1 V, V _{NO} = Open, or V _{COM} = 4.5 V, V _{NO} = Open,	Switch ON, See Figure 15	25°C	5.5 V	−2	0.3	2	−80	0.3	80	nA
				Full		−20		20	−400		400	
Digital Control Inputs (IN)												
Input logic high	V _{IH}			Full		2.4		5.5	2.4		5.5	V
Input logic low	V _{IL}			Full		0		0.8	0		0.8	V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	5.5 V	−2	0.3	2				nA
				Full		−20		20	−400		400	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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Electrical Characteristics for 5-V Supply⁽¹⁾ (continued)
 $V_+ = 4.5\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See Figure 17	25°C	5 V	2.5	4.5	7	2.5	4.5	7	ns	
			Full	4.5 V to 5.5 V	1.5		7.5	1.5		7.5		
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω, C _L = 35 pF, See Figure 17	25°C	5 V	6	9	11.5	6	9	11.5	ns	
			Full	4.5 V to 5.5 V	4		12.5	4		12.5		
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0 , C _L = 1 nF, See Figure 20	25°C	5 V		1			1		pC	
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF, See Figure 16	25°C	5 V		19			19		pF	
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF, See Figure 16	25°C	5 V		18			18		pF	
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON, See Figure 16	25°C	5 V		35.5			35.5		pF	
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON, See Figure 16	25°C	5 V		35.5			35.5		pF	
Digital input capacitance	C _I	V _I = V ₊ or GND, See Figure 16	25°C	5 V		2			2		pF	
Bandwidth	BW	R _L = 50 Ω, Switch ON, See Figure 18	25°C	5 V		200			200		MHz	
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz, Switch OFF, See Figure 19	25°C	5 V		−64			−64		dB	
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF, f = 20 Hz to 20 kHz, See Figure 21	25°C	5 V		0.005			0.005		%	
Supply												
Positive supply current	I ₊	V _I = V ₊ or GND, Switch ON or OFF	25°C	5.5 V	0.01	0.1		0.01	0.1		μA	
			Full				0.5		0.8			

7.6 Electrical Characteristics for 3.3-V Supply⁽¹⁾

 $V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT	
						MIN	TYP	MAX	MIN	TYP	MAX		
Analog Switch													
Analog signal range	V _{COM} , V _{NO}					0	V ₊		0	V ₊		V	
Peak ON resistance	r _{peak}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	3 V	1.1	1.5		1.1	1.5	Ω		
				Full		1.7		2.07					
ON-state resistance	r _{on}	V _{NO} = 2 V, I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	3 V	1	1.4		1	1.4	Ω		
				Full		1.5		1.8					
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA, V _{NO} = 2 V, 0.8 V, I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	3 V	0.3			0.3			Ω	
				25°C		0.09	0.15		0.09	0.15			
				Full		0.15		0.18					
NO OFF leakage current	I _{NO(OFF)}	V _{NO} = 1 V, V _{COM} = 3 V, or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	−2	0.5	2	−2	0.5	2	nA	
				Full		−20	20		−360	360			
	I _{NO(PWROFF)}	V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0,			25°C	0 V	−1	0.1	1	−1	0.1	1	μA
					Full		−5	5		−27	27		
COM OFF leakage current	I _{COM(OFF)}	V _{COM} = 1 V, V _{NO} = 3 V, or V _{COM} = 3 V, V _{NO} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	−2	0.5	2	−72	0.5	72	nA	
				Full		−20	20		−360	360			
	I _{COM(PWROFF)}	V _{COM} = 3.6 V to 0, V _{NO} = 0 to 3.6 V,			25°C	0 V	−1	0.1	1	−2	0.1	2	μA
					Full		−5	5		−27	27		
NO ON leakage current	I _{NO(ON)}	V _{NO} = 1 V, V _{COM} = Open, or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	−2	0.2	2	−72	72		nA	
				Full		−20	20		−360	360			
COM ON leakage current	I _{COM(ON)}	V _{COM} = 1 V, V _{NO} = Open, or V _{COM} = 3 V, V _{NO} = Open,	Switch ON, See Figure 15	25°C	3.6 V	−2	0.2	2	−72	72		nA	
				Full		−20	20		−360	360			
Digital Control Inputs (IN)													
Input logic high	V _{IH}			Full		2	5.5		2	5.5		V	
Input logic low	V _{IL}			Full		0	0.8		0	0.8		V	
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	3.6 V	−2	0.3	2			nA		
				Full		−20	20		−360	360			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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Electrical Characteristics for 3.3-V Supply⁽¹⁾ (continued)

$V_+ = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 17	25°C	3.3 V	2	5	10	2	5	10	ns
				Full	3 V to 3.6 V	1.5		11	1.5		11	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 17	25°C	3.3 V	6.5	9	12	6.5	9	12	ns
				Full	3 V to 3.6 V	4		13	4		13	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 21	25°C	3.3 V		1			1		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19			19		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18			18		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36			36		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36			36		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 16	25°C	3.3 V		2			2		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 18	25°C	3.3 V		200			200		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		−64			−64		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	3.3 V		0.01			0.01		%
Supply												
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	3.6 V	0.01	0.1		0.01	0.1		μA
				Full			0.25		0.7			

7.7 Electrical Characteristics for 2.5-V Supply⁽¹⁾

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT			
						MIN	TYP	MAX	MIN	TYP	MAX				
Analog Switch															
Analog signal range	V _{COM} , V _{NO}				2.3 V	0		V ₊	0		V ₊	V			
Peak ON resistance	r _{peak}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	2.3 V	1.8		2.4	1.8		2.4	Ω			
				Full				2.6		3.1					
ON-state resistance	r _{on}	V _{NO} = 2 V, I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	2.3 V	1.2		2.1	1.2		2.1	Ω			
				Full				2.4		2.88					
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA, V _{NO} = 2 V, 0.8 V, I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	2.3 V	0.7			0.7			Ω			
				25°C		0.4		0.6	0.4		0.6				
				Full				0.6		0.72					
NO OFF leakage current	I _{NO(OFF)}	V _{NO} = 1 V, V _{COM} = 3 V, or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	−5		0.3	5	−64		0.3	64	nA	
				Full		−50			50	−320			320		
	I _{NO(PWROFF)}	V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0,			25°C	0 V	−2		0.05	2	−2		0.05	2	μA
					Full		−15			15	−24			24	
COM OFF leakage current	I _{COM(OFF)}	V _{COM} = 1 V, V _{NO} = 3 V, or V _{COM} = 3 V, V _{NO} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	−5		0.3	5	−64		0.3	64	nA	
				Full		−50			50	−320			320		
	I _{COM(PWROFF)}	V _{COM} = 3.6 V to 0, V _{NO} = 0 to 3.6 V,			25°C	0 V	−2		0.05	2	−2		0.05	2	μA
					Full		−15			15	−24			24	
NO ON leakage current	I _{NO(ON)}	V _{NO} = 1 V, V _{COM} = Open, or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	−2		0.3	2	−64		0.3	64	nA	
				Full		−20			20	−320			320		
COM ON leakage current	I _{COM(ON)}	V _{COM} = 1 V, V _{NO} = Open, or V _{COM} = 3 V, V _{NO} = Open,	Switch ON, See Figure 15	25°C	2.7 V	−2		0.3	2	−64		0.3	64	nA	
				Full		−20			20	−320			320		
Digital Control Inputs (IN1, IN2)															
Input logic high	V _{IH}			Full		1.8		5.5	1.8		5.5	V			
Input logic low	V _{IL}			Full		0		0.6	0		0.6	V			
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	2.7 V	−2		0.3	2			nA			
				Full		−20			20	−320				320	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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Electrical Characteristics for 2.5-V Supply⁽¹⁾ (continued)
 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 17	25°C	2.5 V	2	6	10	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	1		12	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 17	25°C	2.5 V	4.5	8	10.5	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	3		15	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 21	25°C	2.5 V		4			4		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		19.5			19.5		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18.5			18.5		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5			36.5		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5			36.5		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 16	25°C	2.5 V		2			2		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 18	25°C	2.5 V		150			150		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		−62			−62		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	2.5 V		0.02			0.02		%
Supply												
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	2.7 V	0.001	0.02		0.001	0.02		μA
				Full			0.25			0.6		

7.8 Electrical Characteristics for 1.8-V Supply⁽¹⁾

 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch												
Analog signal range	V _{COM} , V _{NO}					0		V ₊	0		V ₊	V
Peak ON resistance	r _{peak}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	1.65 V	4.2	25		4.2	25		Ω
				Full			30			36		
ON-state resistance	r _{on}	V _{NO} = 2 V, I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	1.65 V	1.6	3.9		1.6	3.9		Ω
				Full			4.0			4.8		
ON-state resistance flatness	r _{on(flat)}	0 ≤ V _{NO} ≤ V ₊ , I _{COM} = −100 mA,	Switch ON, See Figure 13	25°C	1.65 V	2.8			2.8			Ω
		V _{NO} = 2 V, 0.8 V, I _{COM} = −100 mA,		25°C		4.1	22		4.1	22		
				Full			27			32.4		
NO OFF leakage current	I _{NO(OFF)}	V _{NO} = 1 V, V _{COM} = 3 V, or V _{NO} = 3 V, V _{COM} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	−5	5		−58	58		nA
				Full		−50	50		−320	320		
	I _{NO(PWROFF)}	V _{NO} = 0 to 3.6 V, V _{COM} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−2	2		−2	2		μA
				Full		−10	10		−22	22		
COM OFF leakage current	I _{COM(OFF)}	V _{COM} = 1 V, V _{NO} = 3 V, or V _{COM} = 3 V, V _{NO} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	−5	5		−58	58		nA
				Full		−50	50		−320	320		
	I _{COM(PWROFF)}	V _{COM} = 0 to 3.6 V, V _{NO} = 3.6 V to 0,	Switch OFF, See Figure 14	25°C	0 V	−2	2		−2	2		μA
				Full		−10	10		−22	22		
NO ON leakage current	I _{NO(ON)}	V _{NO} = 1 V, V _{COM} = Open, or V _{NO} = 3 V, V _{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	−2	2		−58	58		nA
				Full		−20	20		−320	320		
COM ON leakage current	I _{COM(ON)}	V _{COM} = 1 V, V _{NO} = Open, or V _{COM} = 3 V, V _{NO} = Open,	Switch ON, See Figure 15	25°C	1.95 V	−2	2		−58	58		nA
				Full		−20	20		−320	320		
Digital Control Inputs (IN1, IN2)												
Input logic high	V _{IH}			Full		1.5	5.5		1.5	5.5		V
Input logic low	V _{IL}			Full		0	0.6		0	0.6		V
Input leakage current	I _{IH} , I _{IL}	V _I = 5.5 V or 0		25°C	1.95 V	−2	0.3	2				nA
				Full		−20	20		−320	320		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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Electrical Characteristics for 1.8-V Supply⁽¹⁾ (continued)
 $V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 17	25°C	1.8 V	3	9	18	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	1		20	
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 17	25°C	1.8 V	5	10	15.5	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	4		18.5	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 21	25°C	1.8 V		2			2		pC
NO OFF capacitance	C _{NO(OFF)}	V _{NO} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19.5			19.5		pF
COM OFF capacitance	C _{COM(OFF)}	V _{COM} = V ₊ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18.5			18.5		pF
NO ON capacitance	C _{NO(ON)}	V _{NO} = V ₊ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5			36.5		pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5			36.5		pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 16	25°C	1.8 V		2			2		pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 18	25°C	1.8 V		150			150		MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		−62			−62		dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz See Figure 21	25°C	1.8 V		0.055			0.055		%
Supply												
Positive supply current	I ₊	V _I = V ₊ or GND,	Switch ON or OFF	25°C	1.95 V	0.001	0.01		0.001	0.01		μA
				Full			0.15			0.6		

7.9 Typical Characteristics

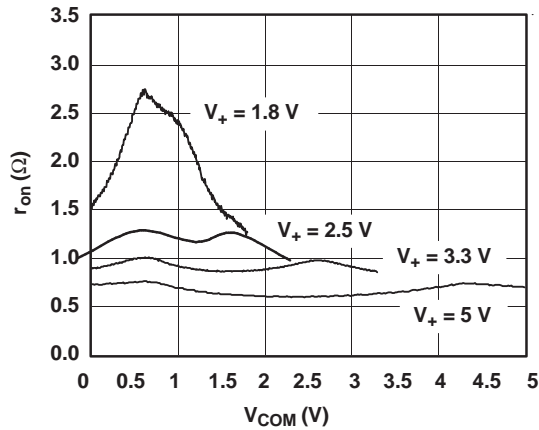


Figure 1. r_{on} vs V_{COM}

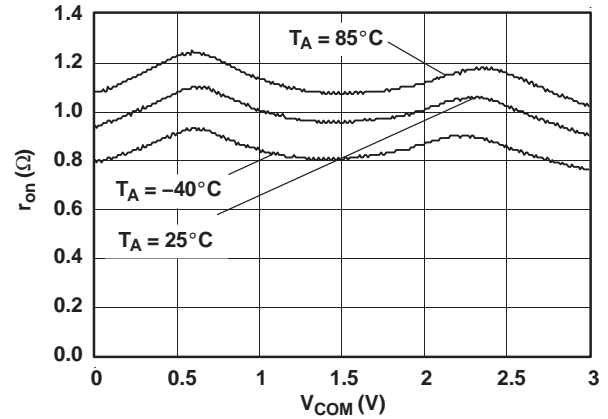


Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)

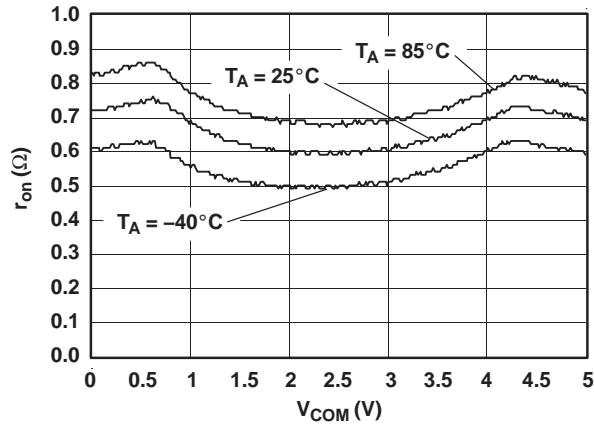


Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)

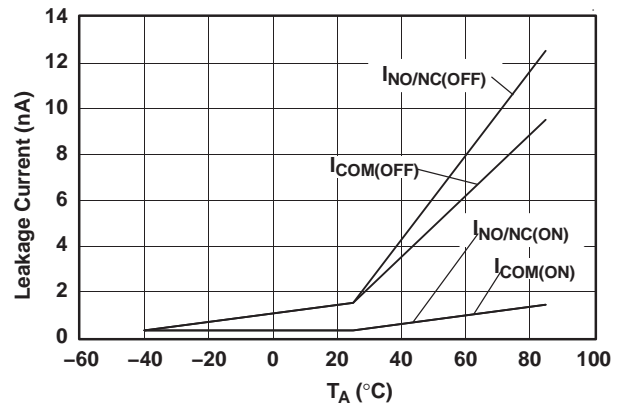


Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)

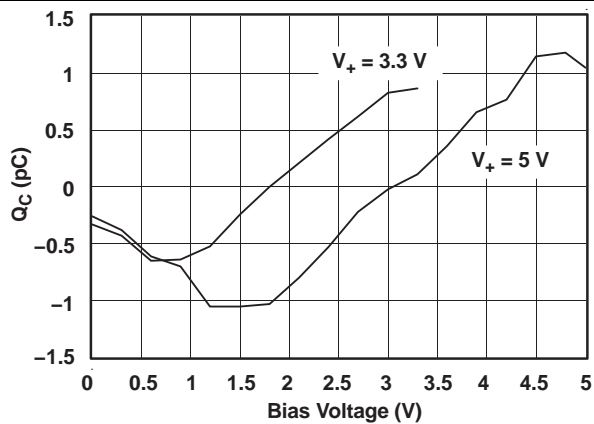


Figure 5. Charge Injection (Q_C) vs V_{COM}

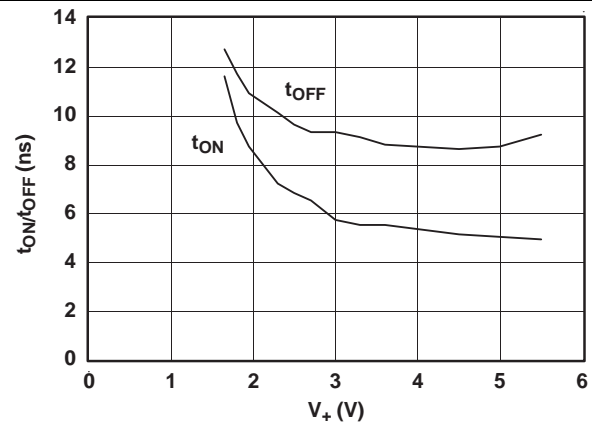


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

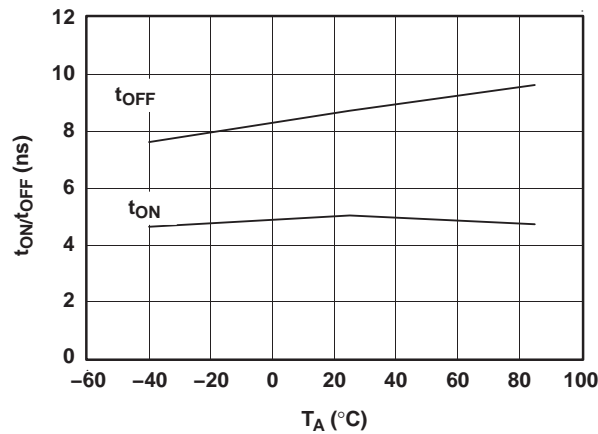


Figure 7. t_{ON} and t_{OFF} vs Temperature ($V_+ = 5$ V)

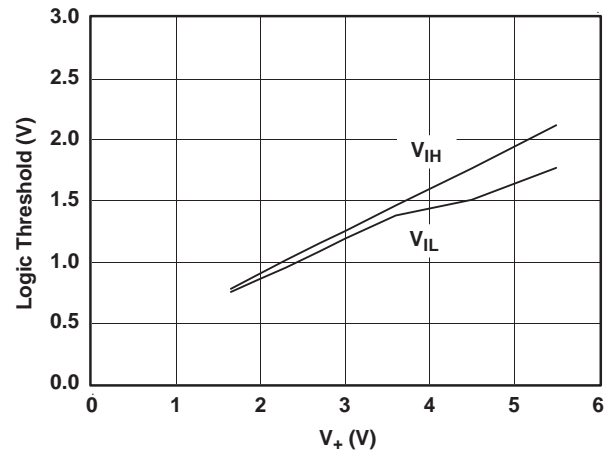


Figure 8. Logic Threshold vs V_+

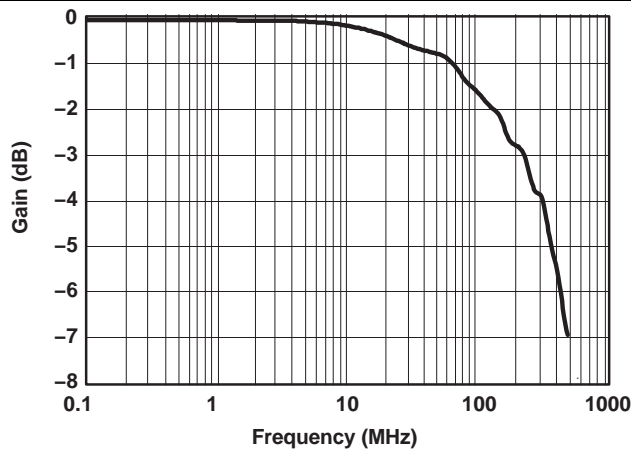


Figure 9. Gain vs Frequency ($V_+ = 5$ V)

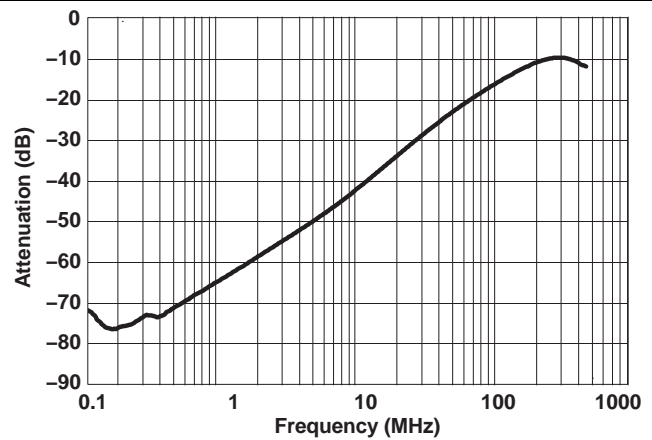


Figure 10. OFF Isolation vs Frequency ($V_+ = 5$ V)

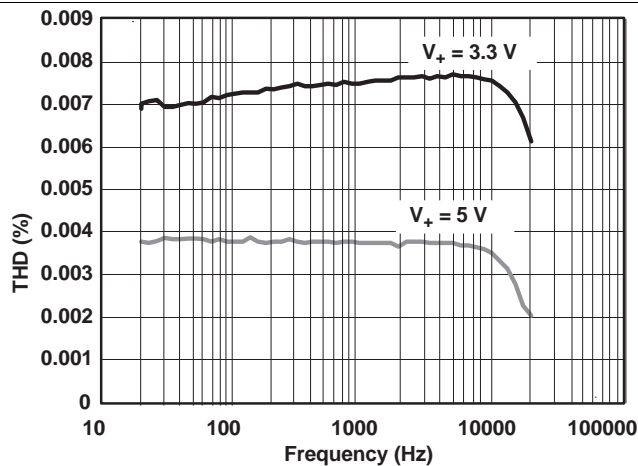


Figure 11. Total Harmonic Distortion vs Frequency ($V_+ = 5$ V)

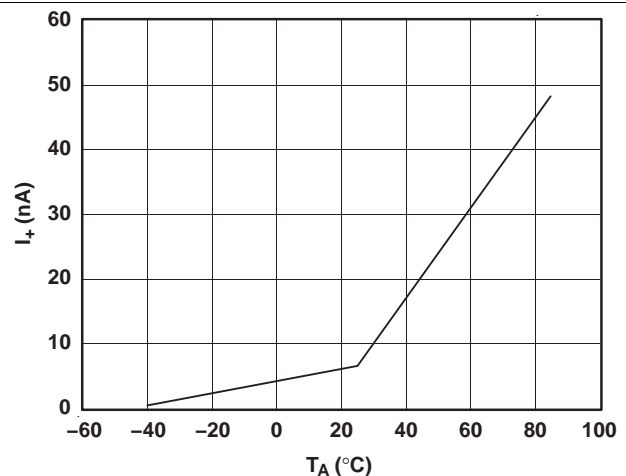


Figure 12. Power-Supply Current vs Temperature ($V_+ = 5$ V)

8 Parameter Measurement Information

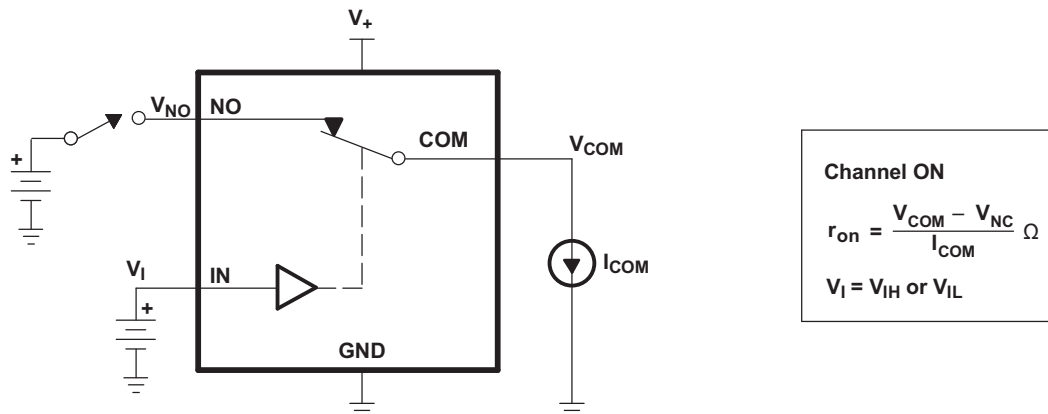


Figure 13. ON-State Resistance (r_{on})

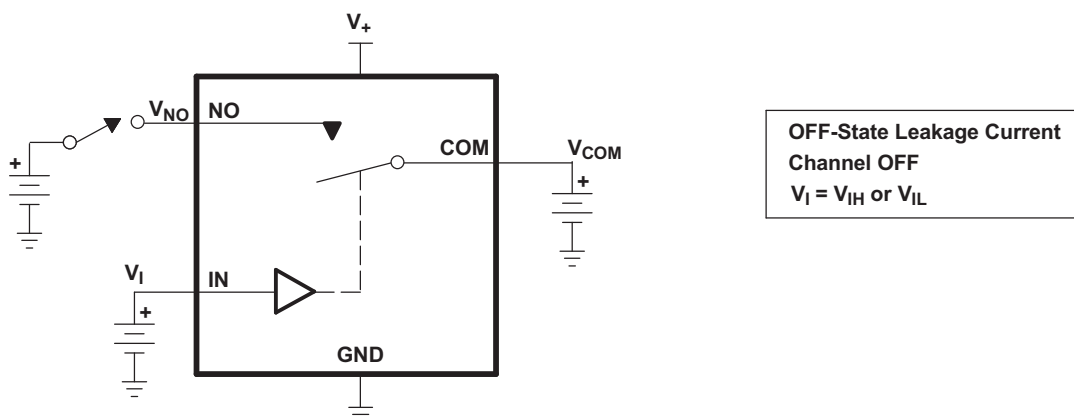


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$, $I_{COM(PWROFF)}$, $I_{NO(PWROFF)}$)

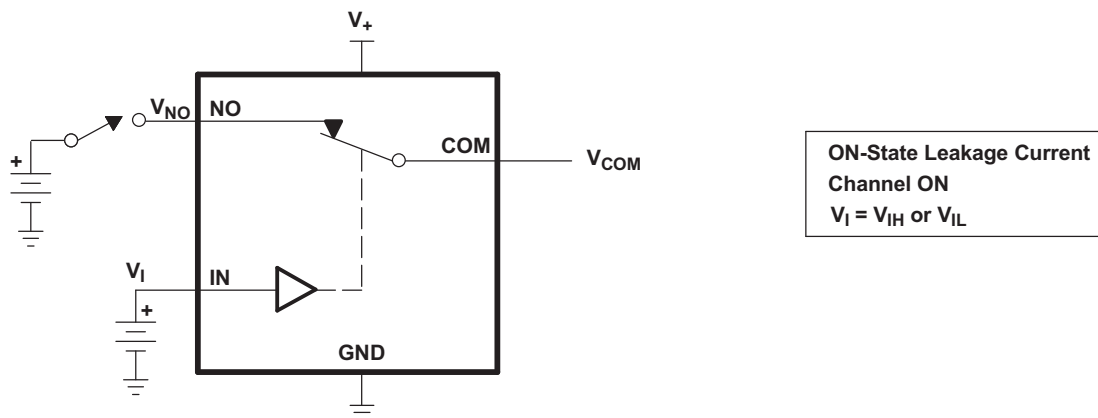


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

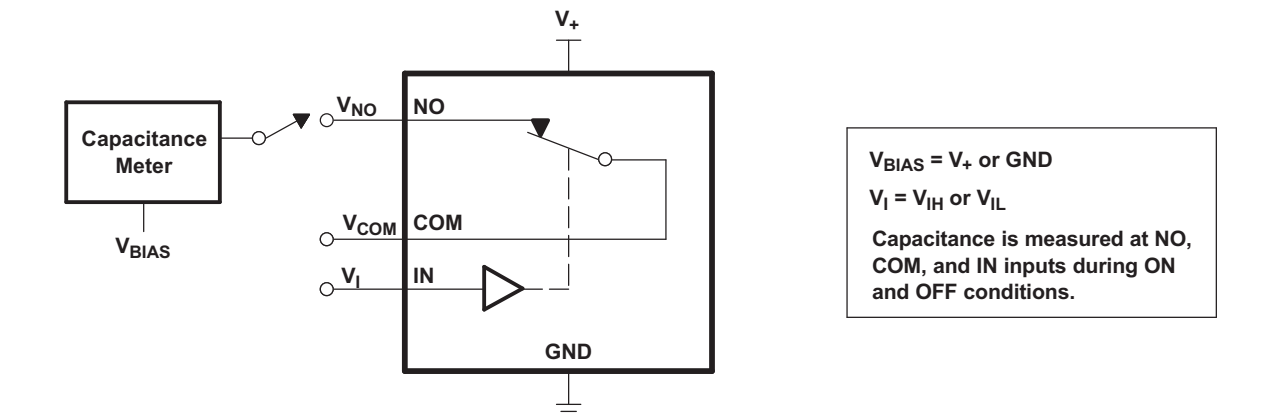
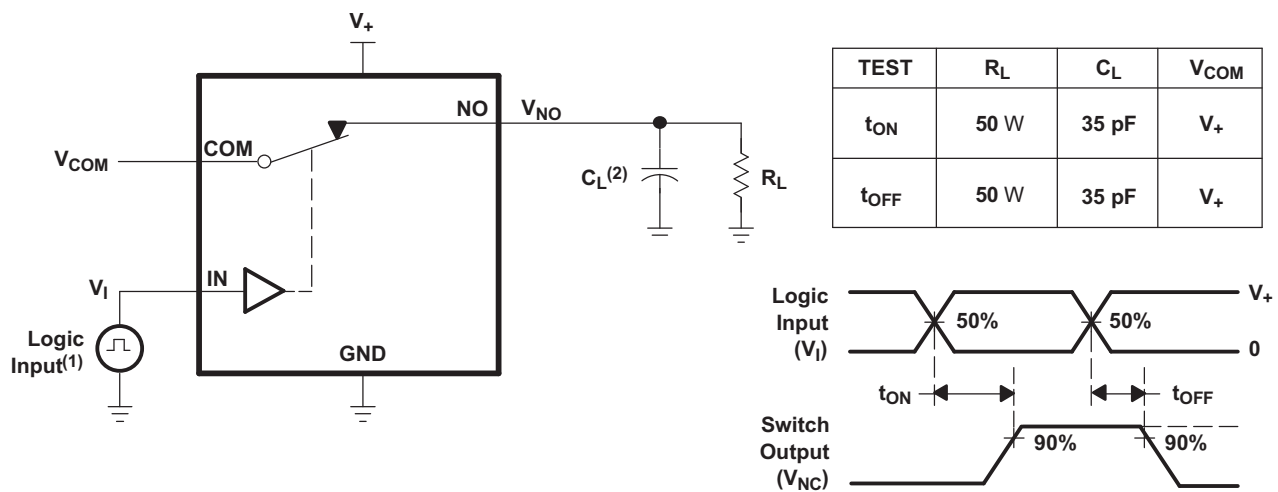


Figure 16. Capacitance (C_I , $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



- (1) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- (2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

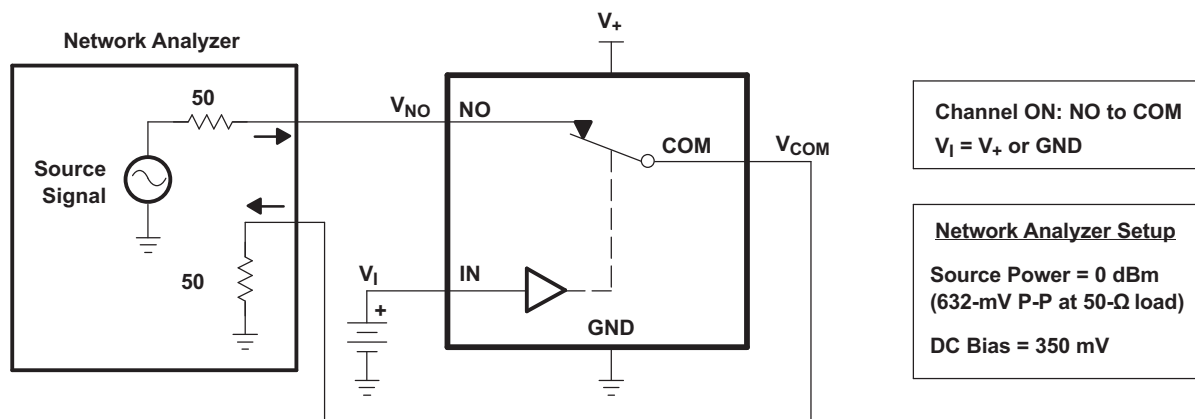


Figure 18. Bandwidth (BW)

Parameter Measurement Information (continued)

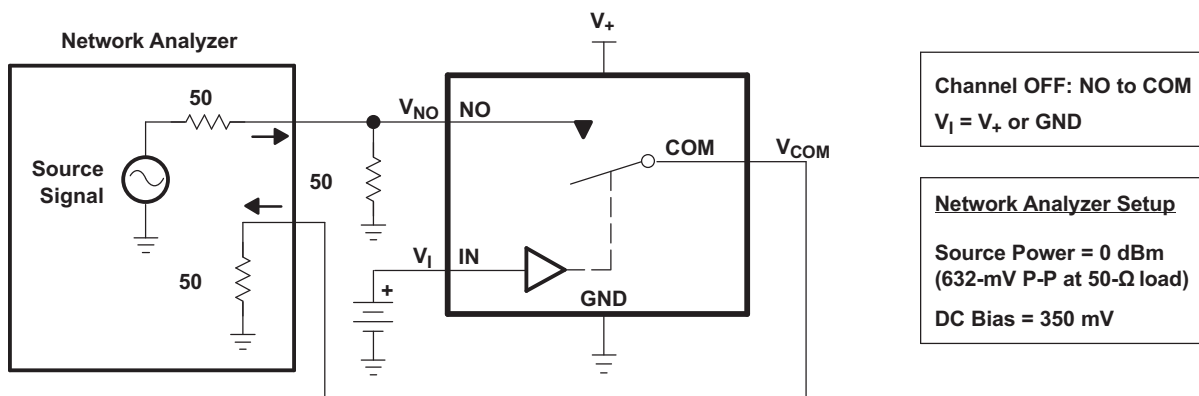
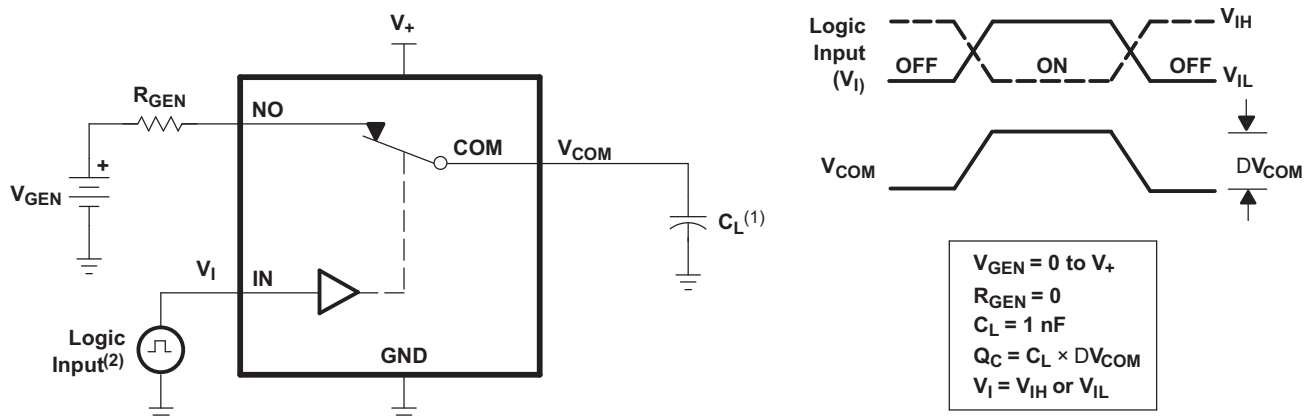
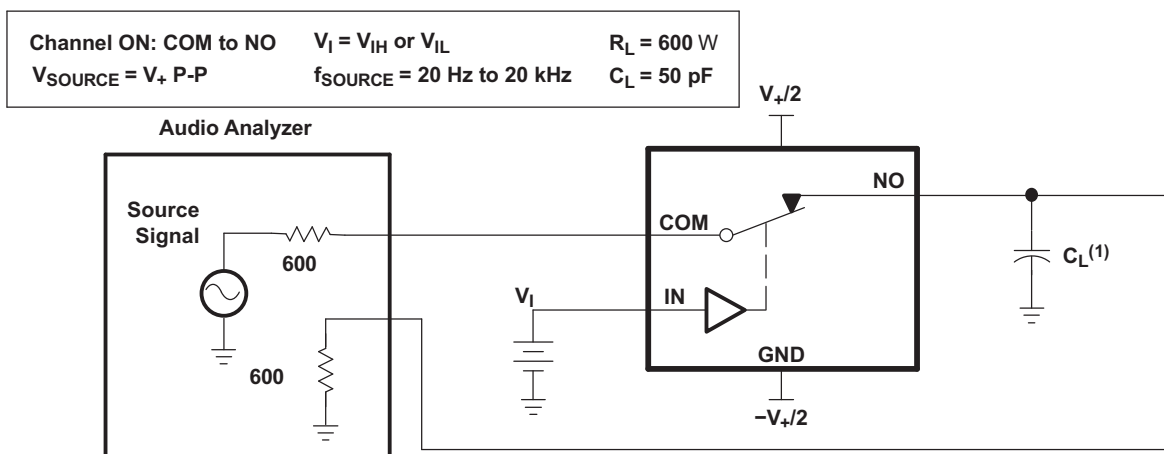


Figure 19. OFF Isolation (O_{ISO})



- (1) C_L includes probe and jig capacitance.
- (2) All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.

Figure 20. Charge Injection (Q_C)



- (1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

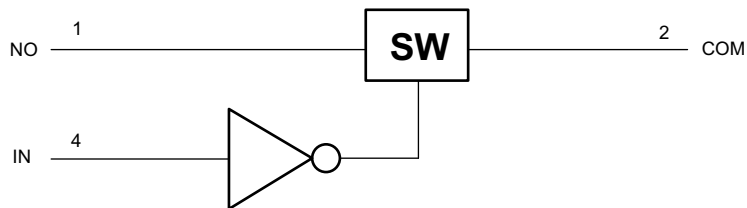
9 Detailed Description

9.1 Overview

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on(Flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

9.2 Functional Block Diagram



9.3 Feature Description

Table 2. Summary Of Characteristics⁽¹⁾

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance (r_{on})	0.9 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	7.5 ns/12.5 ns
Charge injection (Q_C)	1 pC
Bandwidth (BW)	200 MHz
OFF isolation (O_{ISO})	-64 dB at 1 MHz
Total harmonic distortion (THD)	0.005%
Leakage current ($I_{COM(OFF)}$)	± 4 nA
Power-supply current (I_+)	0.5 μ A
Package option	5-pin DSBGA, SOT-23, or SC-70

(1) $V_+ = 5$ V, $T_A = 25^\circ\text{C}$

9.4 Device Functional Modes

Table 3. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

SPST analog switch is a basic component that could be used in any electrical system design. The following are some basic applications that utilize the TS5A3166, more detailed applications may be found in the [Typical Application](#) section.

1. Gain-control circuit for amplifier
 - (a) Additional details are available in the [Typical Application](#) section.
2. Improve lock time of a PLL by changing the time constant
 - (a) Example Diagram:

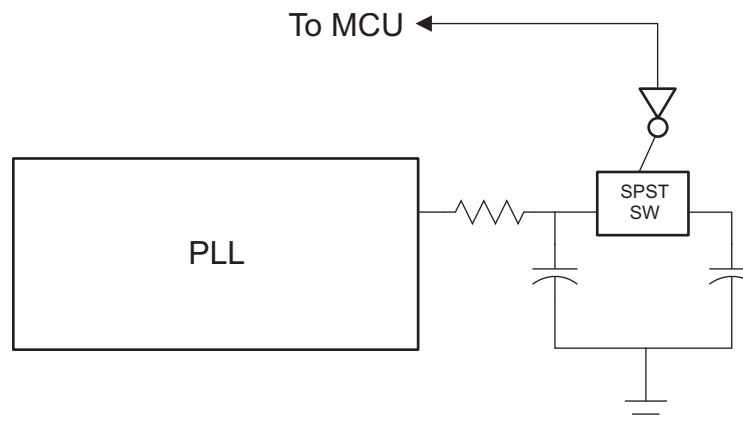


Figure 22. Improved Lock Time Circuit Simplified Block Diagram

1. Improve power consumption for PLL
 - (a) Example Diagram:

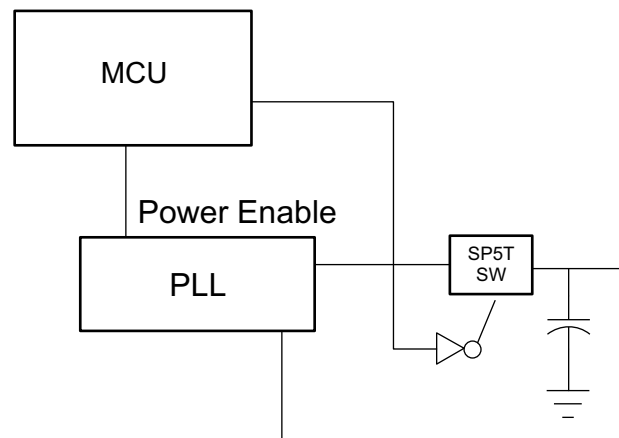


Figure 23. PLL Improved Power Consumption Simplified Block Diagram

10.2 Typical Application

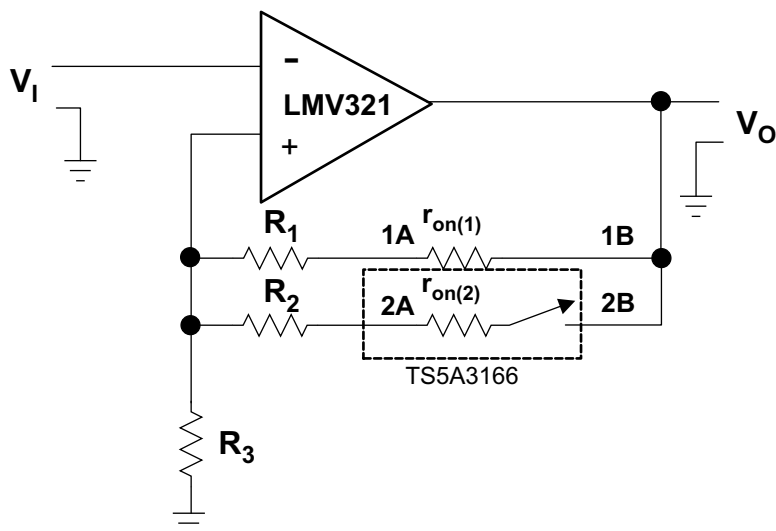


Figure 24. Gain-Control Circuit for OP Amplifier

10.2.1 Design Requirements

Place a switch in series with the input of the op amp. Since the op amp input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

10.2.2 Detailed Design Procedure

By choosing values of R_1 and R_2 , such that $R_x \gg r_{on(x)}$, r_{on} of TS5A3166 can be ignored. The gain of op amp can be calculated as follow:

$$V_o / V_i = 1 + R_2 / R_3 \quad (1)$$

$$R_2 = (R_1 + r_{on(1)}) \parallel (R_3 + r_{on(2)}) \quad (2)$$

10.2.3 Application Curves

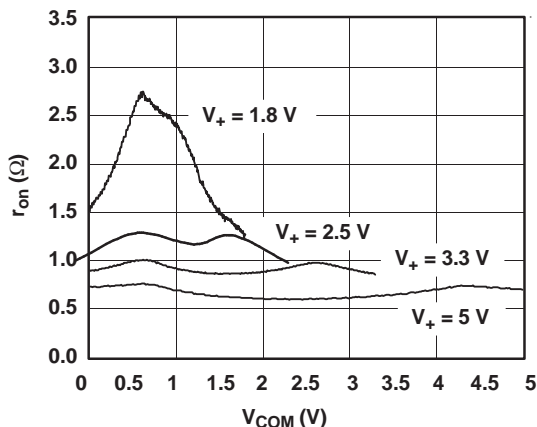


Figure 25. r_{on} vs V_{COM}

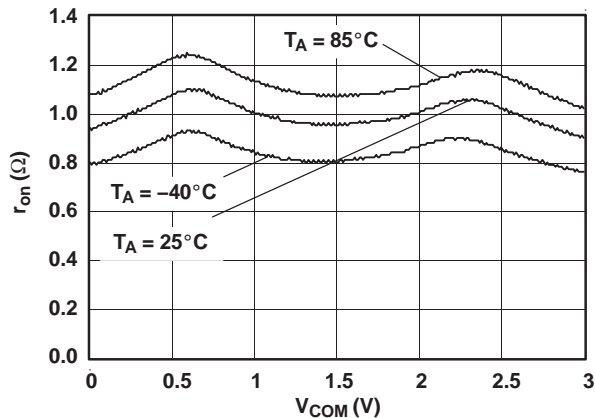


Figure 26. r_{on} vs V_{COM} ($V_+ = 3$ V)

Typical Application (continued)

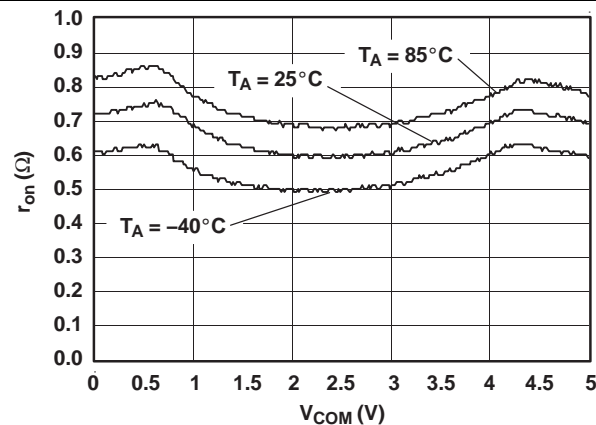


Figure 27. r_{on} vs V_{COM} ($V_+ = 5$ V)

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If there are multiple V_{CC} terminals then a 0.01 μF or 0.022 μF capacitor is recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

12.2 Layout Example

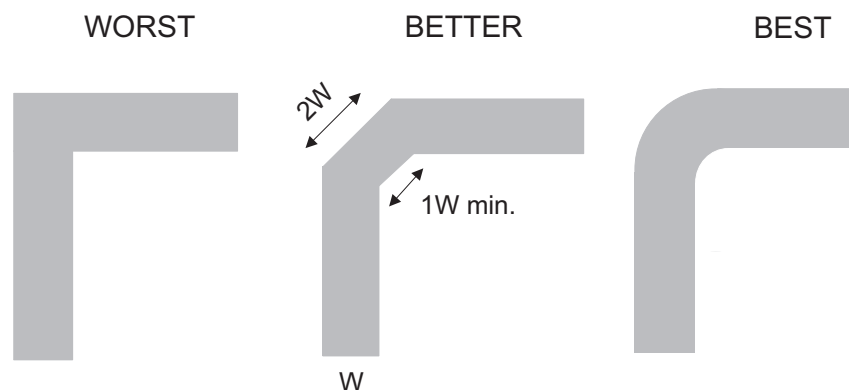


Figure 28. Trace Example

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3166QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TS5A3166-Q1 :

-
- Catalog: [TS5A3166](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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