TS4872

RAIL TO RAIL INPUT/OUTPUT
1W AUDIO POWER AMPLIFIER WITH STANDBY MODE

NOT FOR NEW DESIGN

- OPERATING FROM **V_{CC} = 2.2V to 5.5V**
- RAIL TO RAIL **INPUT/OUTPUT**
- **1W** OUTPUT POWER @ Vcc=5V, THD=1%, f=1kHz, with **8**Ω Load
- ULTRA LOW CONSUMPTION IN STANDBY MODE **(10nA)**
- **75dB** PSRR @ 217Hz @ 5 & 2.6V
- ULTRA LOW POP & CLICK
- ULTRA LOW DISTORTION **(0.05%)**
- UNITY GAIN STABLE
- **8 X170µm BUMPS FLIP CHIP PACKAGE**

DESCRIPTION

The TS4872 is an Audio Power Amplifier capable of delivering 1W of continuous RMS Ouput Power into 8Ω load @ 5V.

This Audio Amplifier is exhibiting 0.1% distortion level (THD) from a 5V supply for a Pout = 250mW RMS. An external standby mode control reduces the supply current to less than 10nA. An internal shutdown protection is provided.

The TS4872 has been designed for high quality audio applications such as mobile phones and to minimize the number of external components.

The unity-gain stable amplifier can be configured by external gain setting resistors.

APPLICATIONS

- Mobile Phones (Cellular / Cordless)
- PDAs
- Laptop/Notebook computers
- Portable Audio Devices

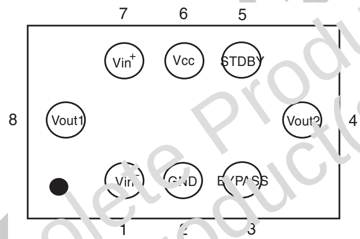
ORDER CODE

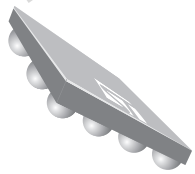
Part Number	Temperature Range	Package J	Marking
TS4872IJT	-40, +85°C	●	YW4872

J = Flip Chip Package - only available in Tape & Reel (JT)

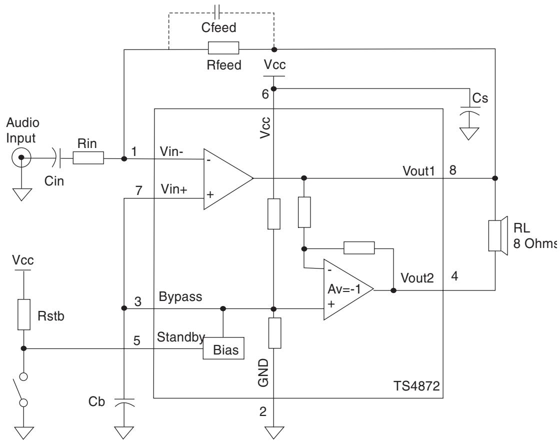
PIN CONNECTIONS (Top View)

TS4872IJT - FLIP CHIP





TYPICAL APPLICATION SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient [3]	200	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
Latch-up	Latch-up Immunity	Class A	
	Lead Temperature (soldering, 10sec)	250	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.2 to 5.5	V
V_{ICM}	Common Mode Input Voltage Range V_{CC} from 2.6V to 5V V_{CC} < 2.6V	G_{ND} to V_{CC} V_{CC} / 2	
V_{STB}	Standby Voltage Input : Device ON Device OFF	$G_{ND} \leq V_{STB} \leq 0.5V$ $V_{CC} - 0.5V \leq V_{STB} \leq V_{CC}$	V
RL	Load Resistor	4 - 32	Ω
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient [1]	95	°C/W

1. With Heat Sink Surface = 125mm^2

ELECTRICAL CHARACTERISTICS

V_{CC} = **+5V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		6	8	mA
$I_{STANDBY}$	Standby Current [1)] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		1		W
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2)] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		75		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

V_{CC} = **+3.3V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified) [3)]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1)] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		450		mW
THD + N	Total Harmonic Distortion + Noise Po = 250mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2)] f = 217Hz, RL = 8Ω, RFeed = 22KΩs, Vripple = 100mV rms		68		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz
3 All electrical values are made by correlation between 2.6v and 5v measurements

ELECTRICAL CHARACTERISTICS

V_{CC} = **2.6V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		5.5	8	mA
$I_{STANDBY}$	Standby Current [1)] No input signal, Vstdby = Vcc, RL = 8Ω		10	1000	nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		5	20	mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		260		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2)] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 200mV rms		75		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

V_{CC} = **2.2V**, GND = **0V**, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		4.5		mA
$I_{STANDBY}$	Standby Current [1)] No input signal, Vstdby = Vcc, RL = 8Ω		10		nA
Voo	Output Offset Voltage No input signal, RL = 8Ω		2		mV
Po	Output Power THD = 1% Max, f = 1kHz, RL = 8Ω		180		mW
THD + N	Total Harmonic Distortion + Noise Po = 200mW rms, Gv = 2, 20Hz < f < 20kHz, RL = 8Ω		0.1		%
PSRR	Power Supply Rejection Ratio [2)] f = 217Hz, RL = 8Ω, RFeed = 22KΩ, Vripple = 100mVpp		75		dB
Φ_M	Phase Margin at Unity Gain R_L = 8Ω, C_L = 500pF		70		Degrees
GM	Gain Margin R_L = 8Ω, C_L = 500pF		20		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz

1. Standby mode is actived when Vstdby is tied to Vcc
2. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz

Components	Functional Description
Rin	Inverting input resistor which sets the closed loop gain in conjunction with Rfeed. This resistor also forms a high pass filter with Cin (fc = 1 / (2 x Pi x Rin x Cin))
Cin	Input coupling capacitor which blocks the DC voltage at the amplifier input terminal
Rfeed	Feed back resistor which sets the closed loop gain in conjunction with Rin
Cs	Supply Bypass capacitor which provides power supply filtering
Cb	Bypass pin capacitor which provides half supply filtering
Cfeed	Low pass filter capacitor allowing to cut the high frequency (low pass filter cut-off frequency 1 / (2 x Pi x Rfeed x Cfeed))
Rstb	Pull-up resistor which fixes the right supply level on the standby pin
Gv	Closed loop gain in BTL configuration = 2 x (Rfeed / Rin)

REMARKS

1. All measurements, except PSRR measurements, are made with a supply bypass capacitor Cs = 100µF.
2. External resistors are not needed for having better stability when supply @ Vcc down to 3V. By the way, the quiescent current remains the same.
3. The standby response time is about 1µs.

Obsolete Product(s) - Obsolete Product(s)

Fig. 1 : Open Loop Frequency Response

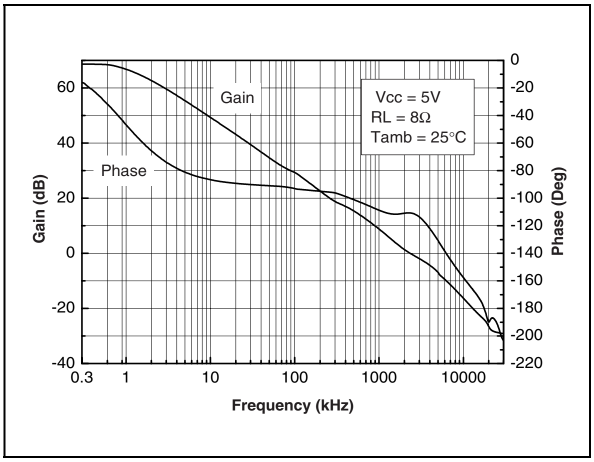


Fig. 2 : Open Loop Frequency Response

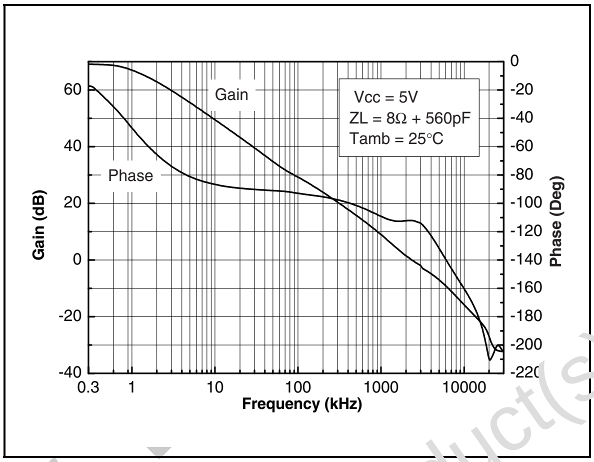


Fig. 3 : Open Loop Frequency Response

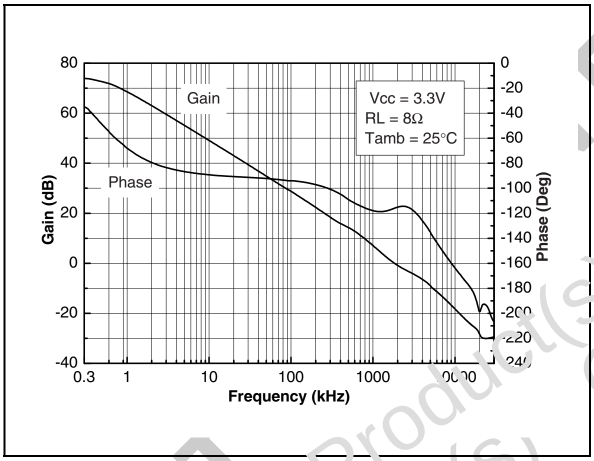


Fig. 4 : Open Loop Frequency Response

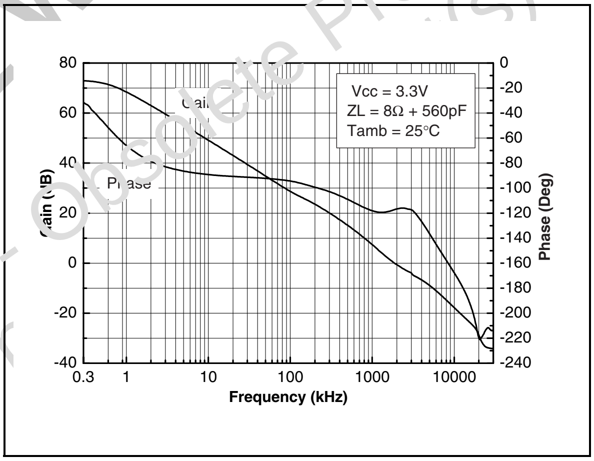


Fig. 5 : Open Loop Frequency Response

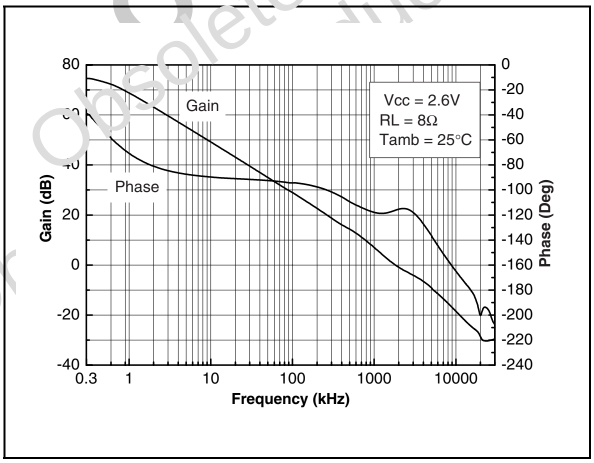


Fig. 6 : Open Loop Frequency Response

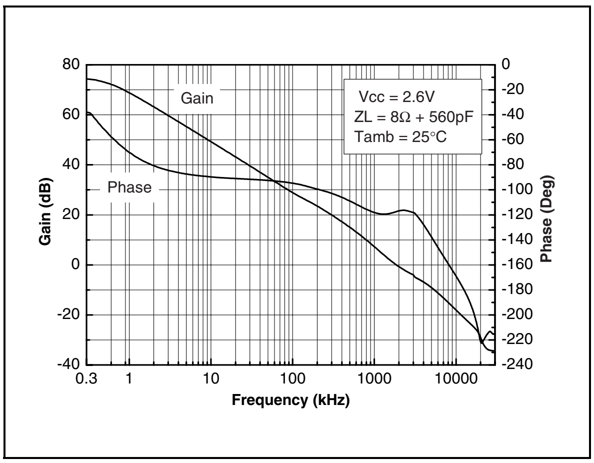


Fig. 7 : Open Loop Frequency Response

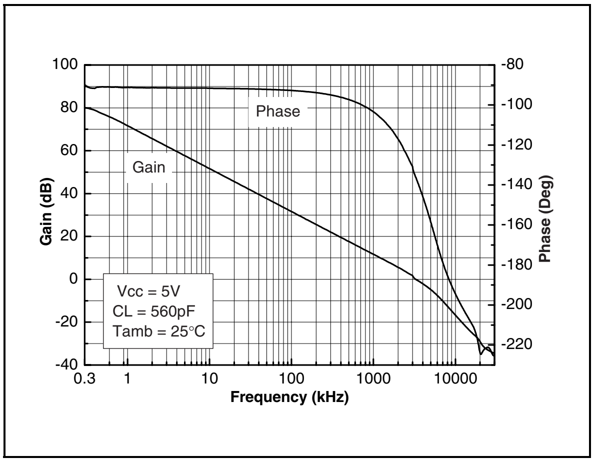


Fig. 8 : Open Loop Frequency Response

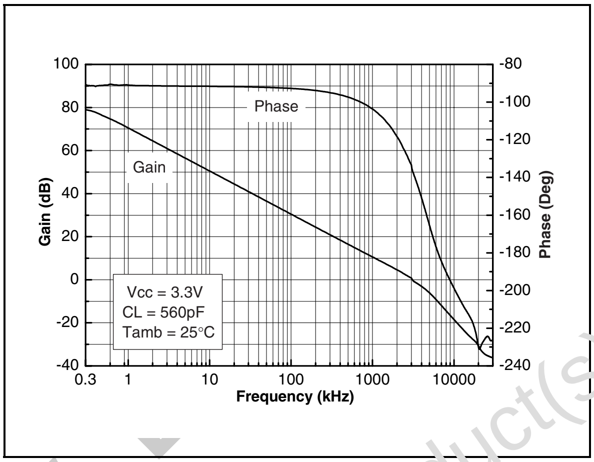


Fig. 9 : Open Loop Frequency Response

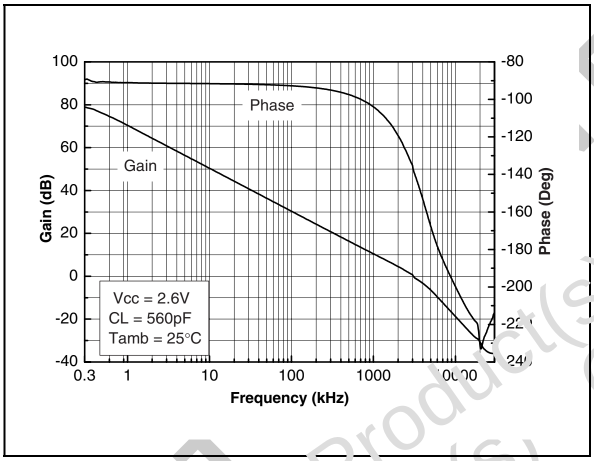


Fig. 10 : Power Supply Rejection Ratio (PSRR) vs Power Supply

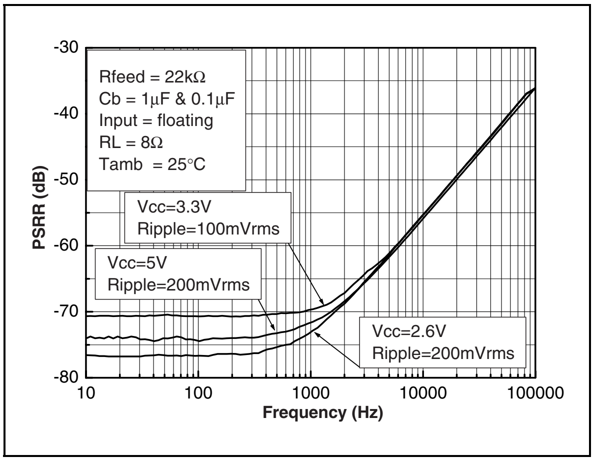


Fig. 11 : Power Supply Rejection Ratio (PSRR) vs Feedback Capacitor

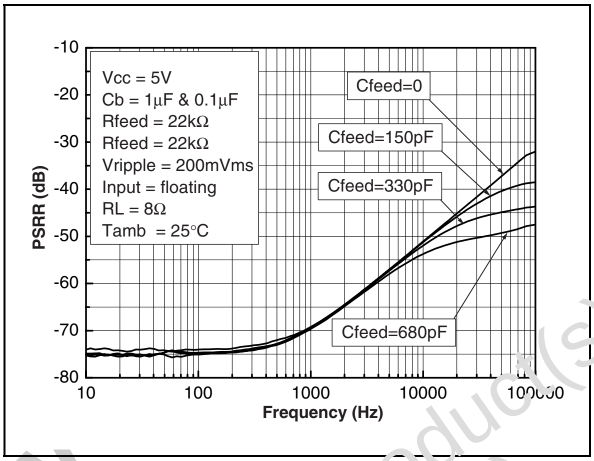


Fig. 12 : Power Supply Rejection Ratio (PSRR) vs Bypass Capacitor

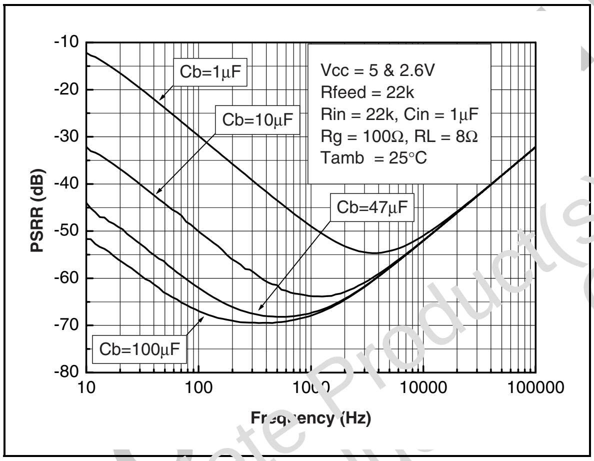


Fig. 13 : Power Supply Rejection Ratio (PSRR) vs Input Capacitor

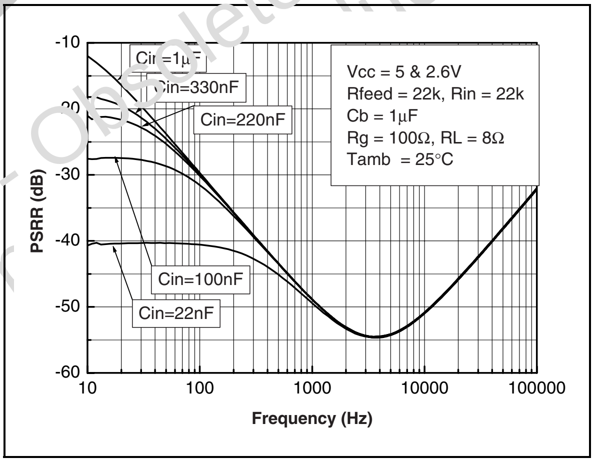


Fig. 14 : Power Supply Rejection Ratio (PSRR) vs Feedback Resistor

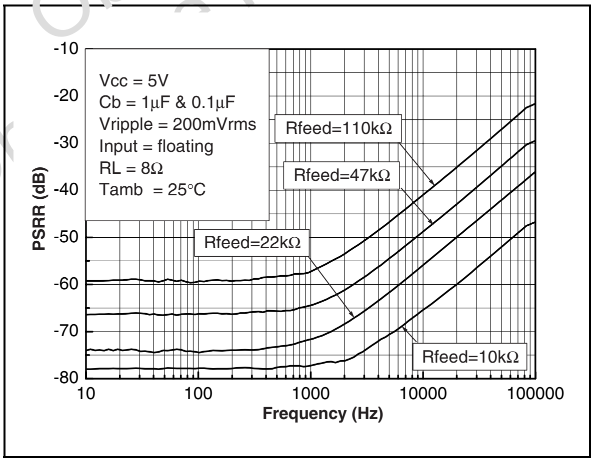


Fig. 15 : Pout @ THD + N = 1% vs Supply Voltage vs RL

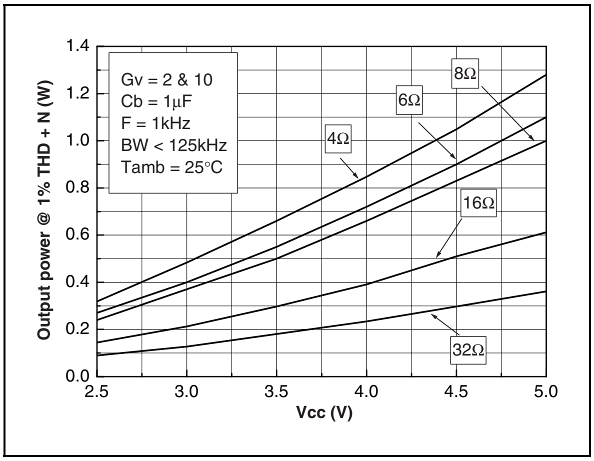


Fig. 16 : Pout @ THD + N = 10% vs Supply Voltage vs RL

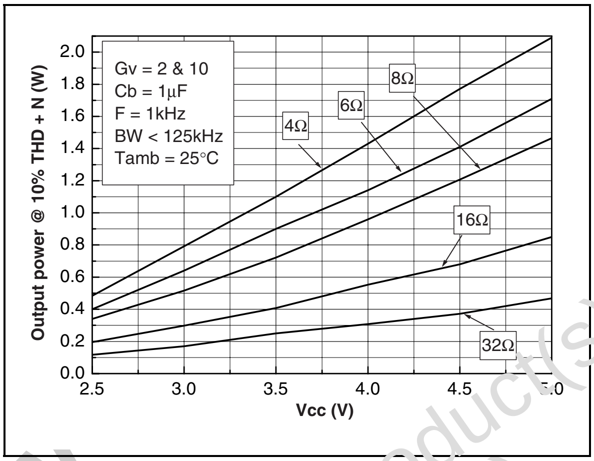


Fig. 17 : Power Dissipation vs Pout

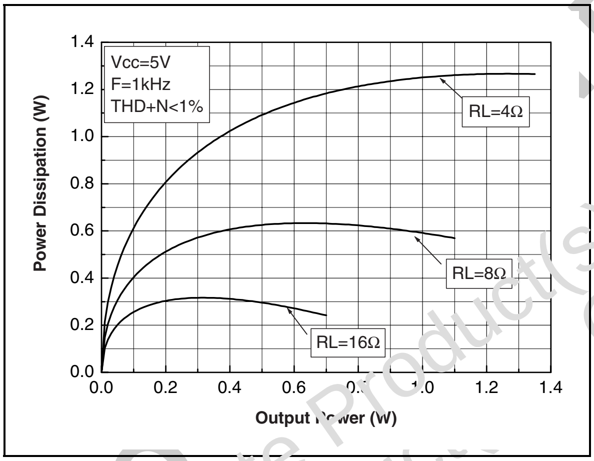


Fig. 18 : Power Dissipation vs Pout

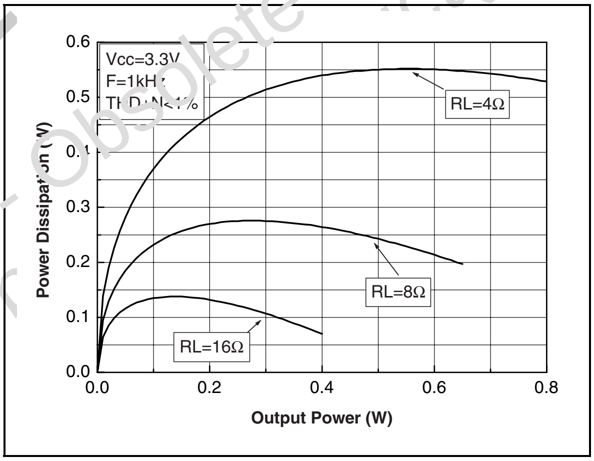


Fig. 19 : Power Dissipation vs Pout

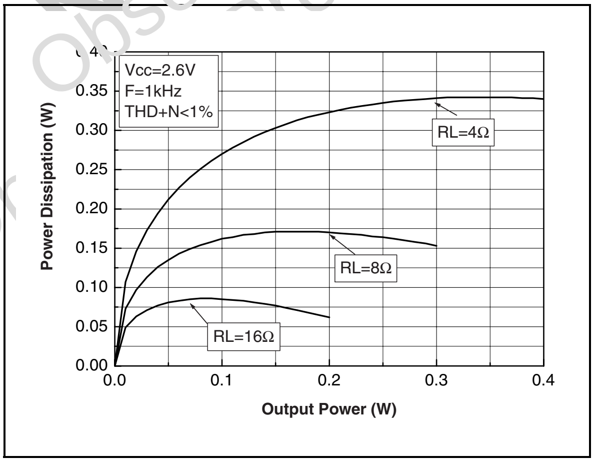


Fig. 20 : Power Derating Curves

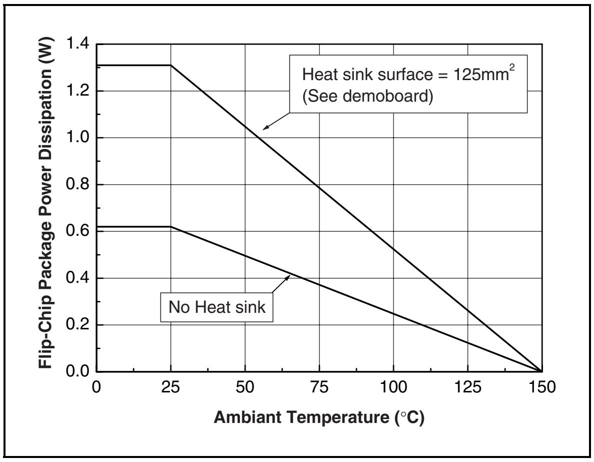


Fig. 21 : THD + N vs Output Power

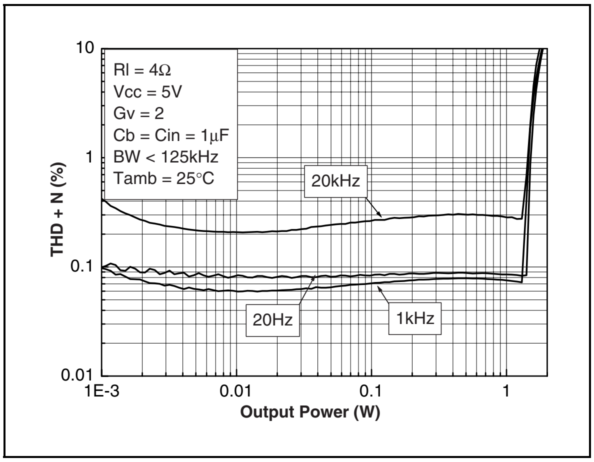


Fig. 22 : THD + N vs Output Power

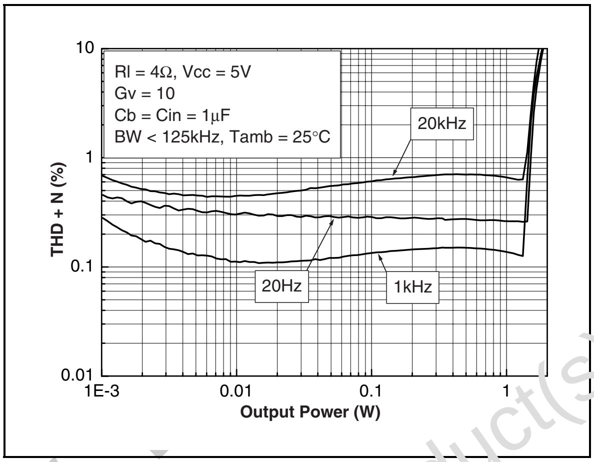


Fig. 23 : THD + N vs Output Power

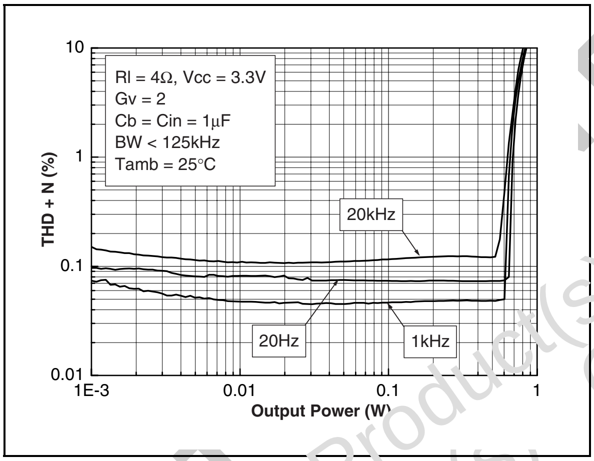


Fig. 24 : THD + N vs Output Power

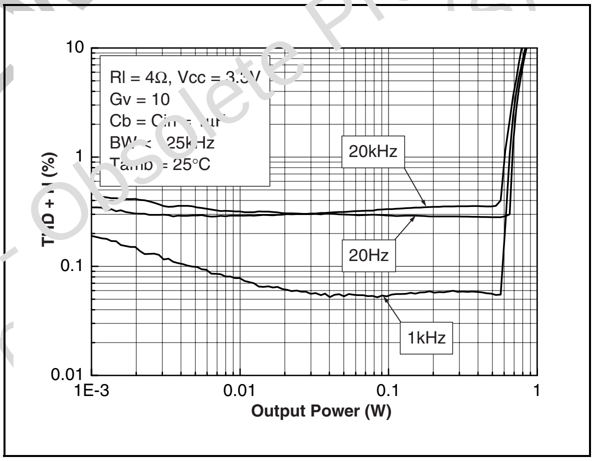


Fig. 25 : THD + N vs Output Power

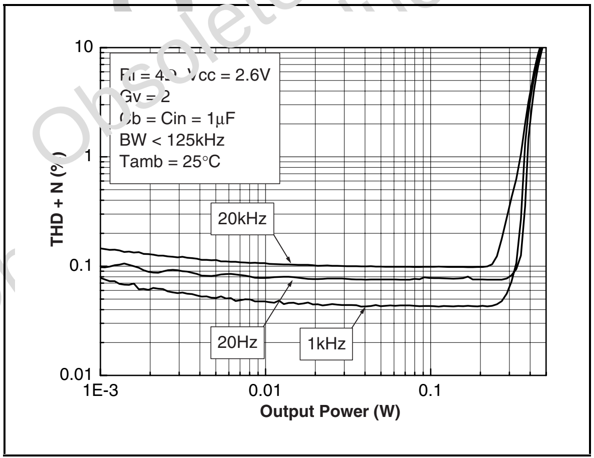


Fig. 26 : THD + N vs Output Power

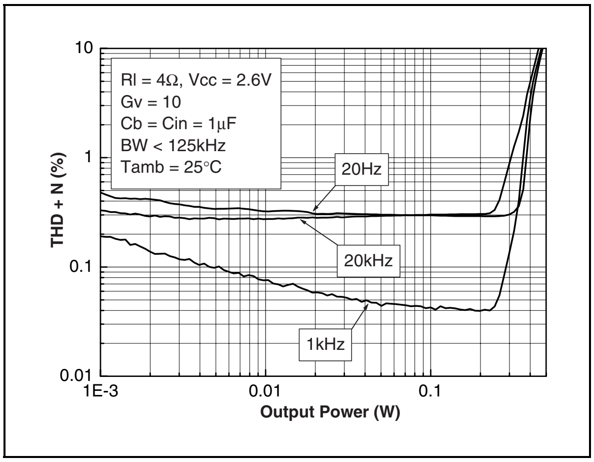


Fig. 27 : THD + N vs Output Power

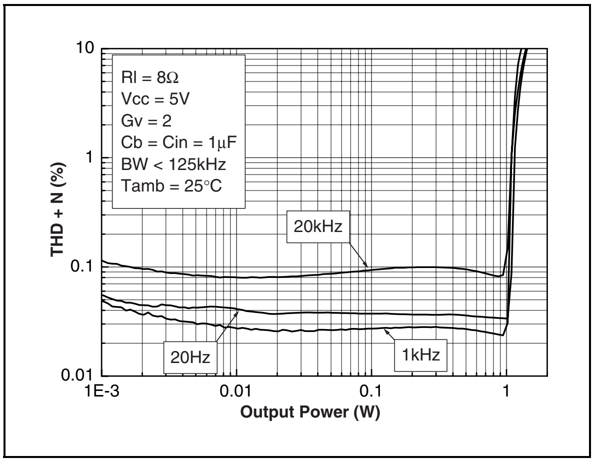


Fig. 28 : THD + N vs Output Power

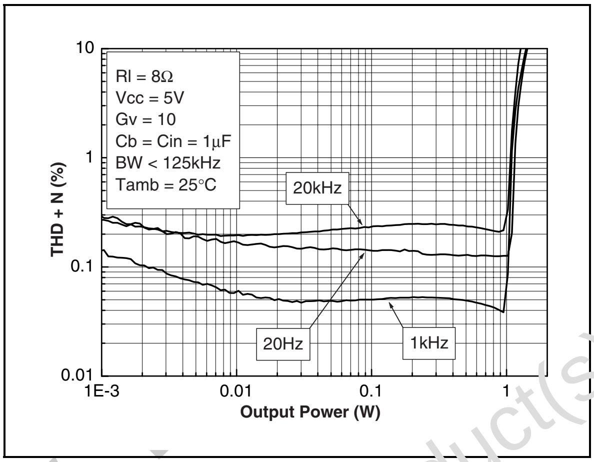


Fig. 29 : THD + N vs Output Power

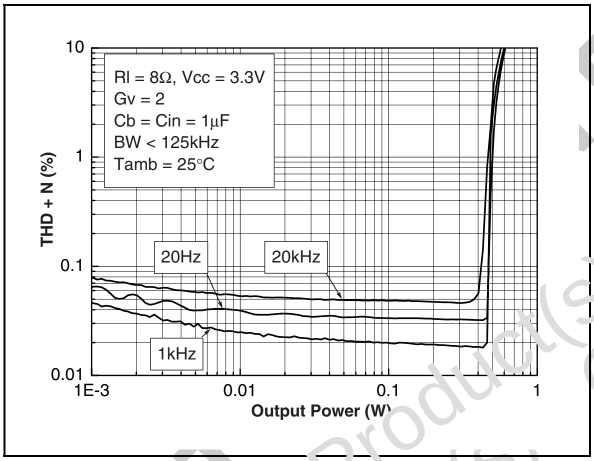


Fig. 30 : THD + N vs Output Power

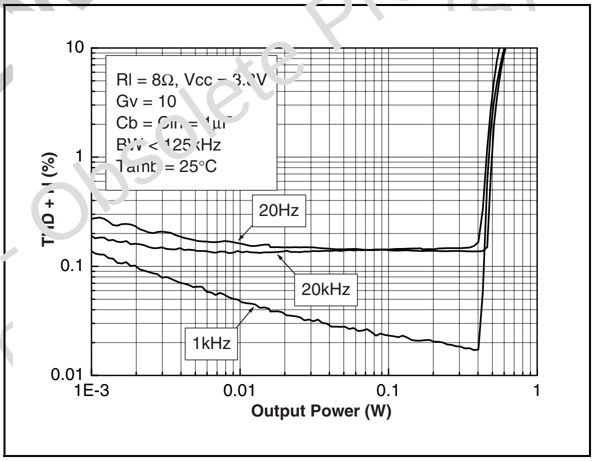


Fig. 31 : THD + N vs Output Power

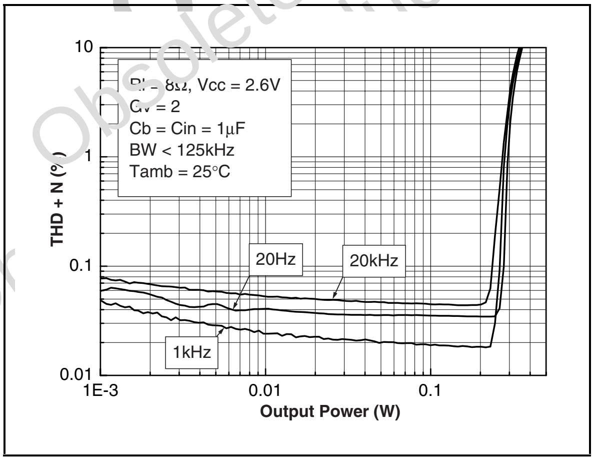


Fig. 32 : THD + N vs Output Power

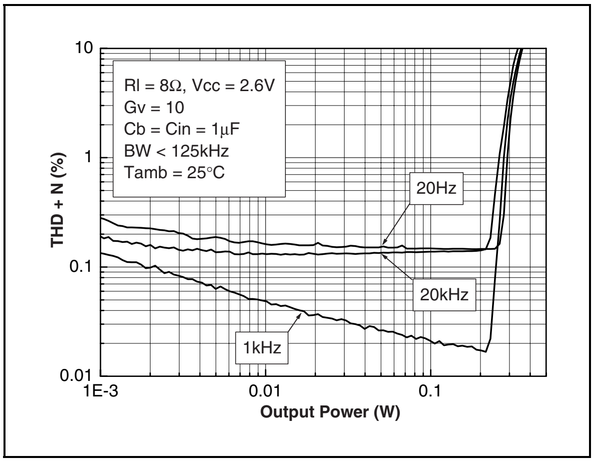


Fig. 33 : THD + N vs Output Power

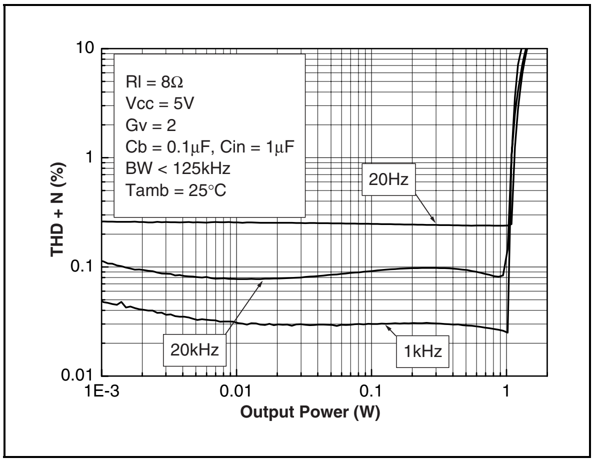


Fig. 34 : THD + N vs Output Power

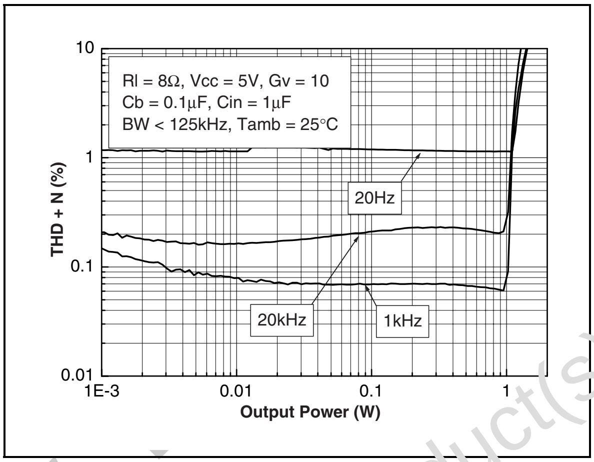


Fig. 35 : THD + N vs Output Power

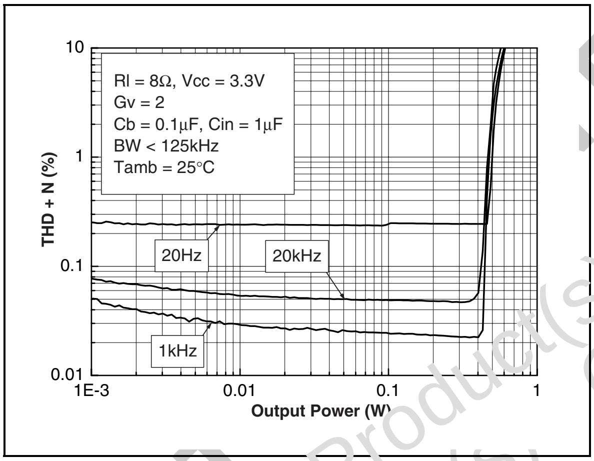


Fig. 36 : THD + N vs Output Power

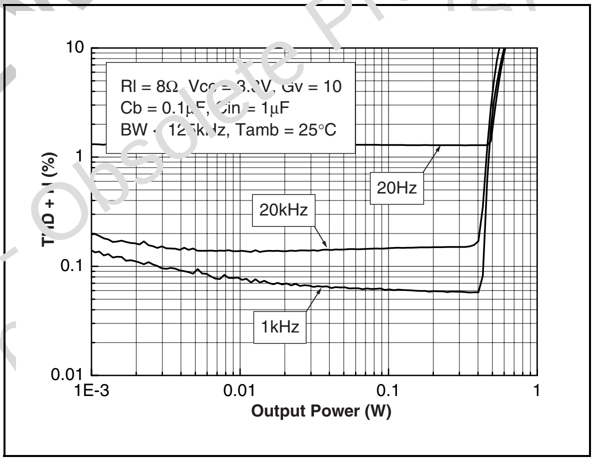


Fig. 37 : THD + N vs Output Power

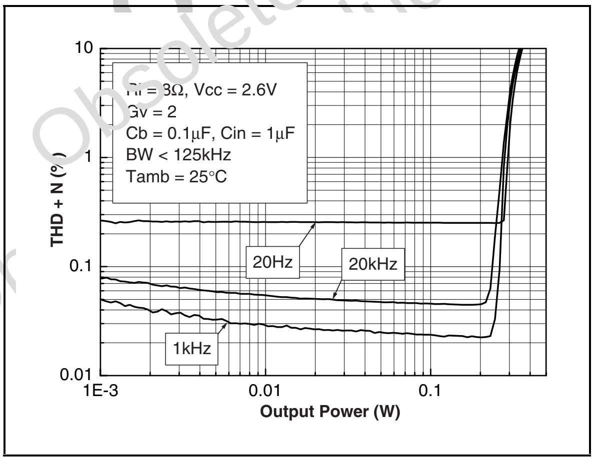


Fig. 38 : THD + N vs Output Power

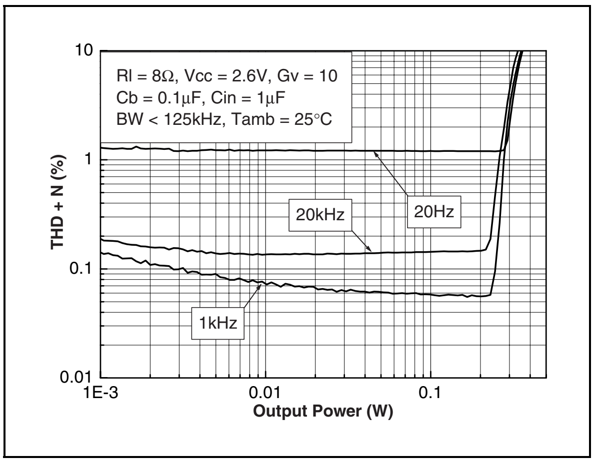


Fig. 39 : THD + N vs Output Power

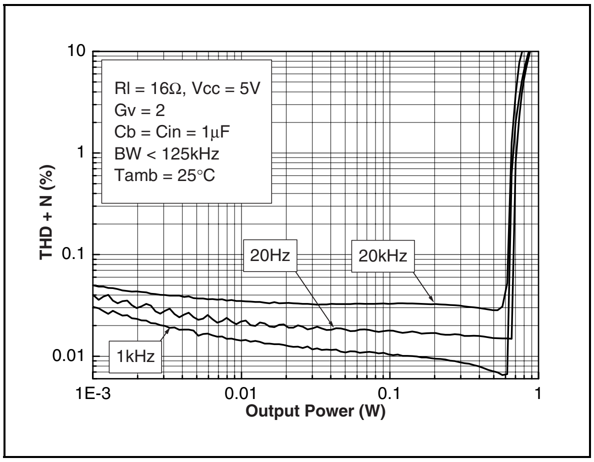


Fig. 40 : THD + N vs Output Power

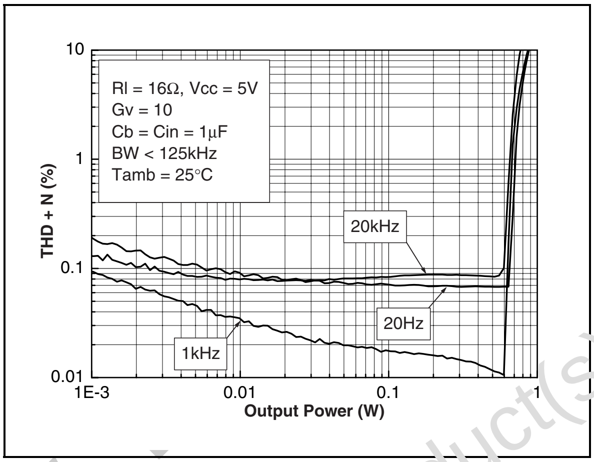


Fig. 41 : THD + N vs Output Power

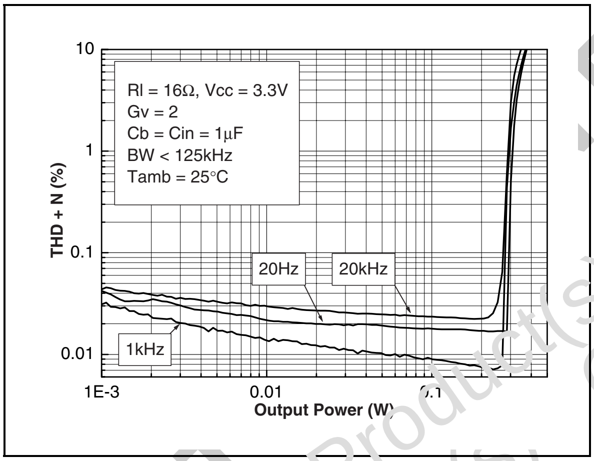


Fig. 42 : THD + N vs Output Power

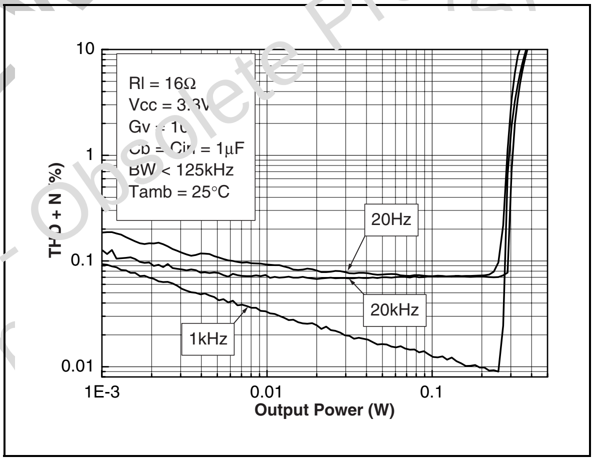


Fig. 43 : THD + N vs Output Power

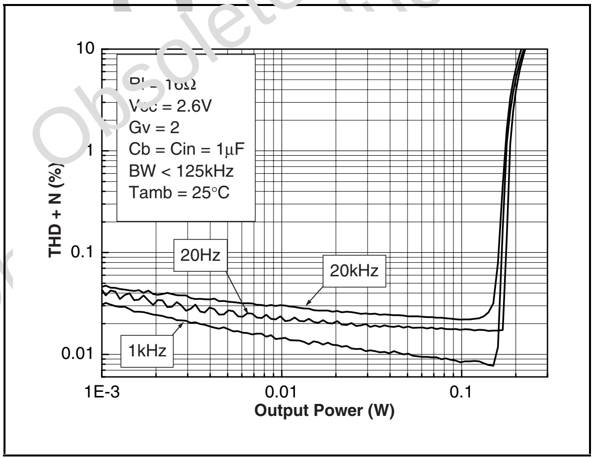


Fig. 44 : THD + N vs Output Power

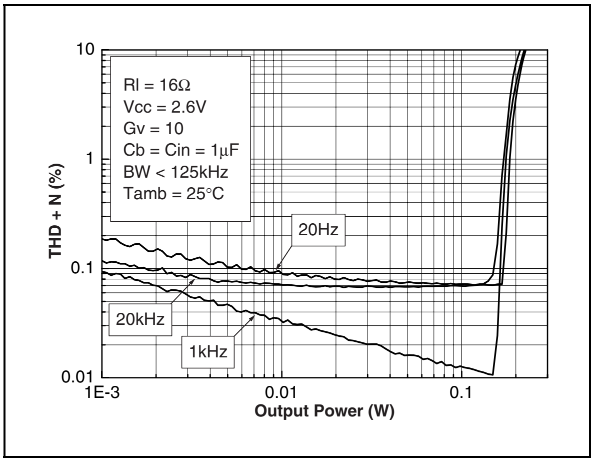


Fig. 45 : THD + N vs Frequency

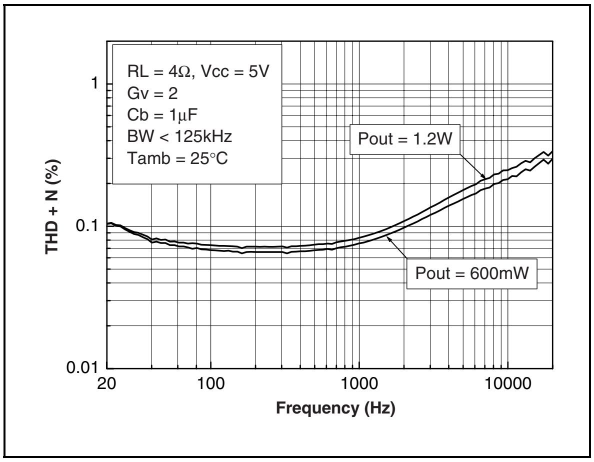


Fig. 46 : THD + N vs Frequency

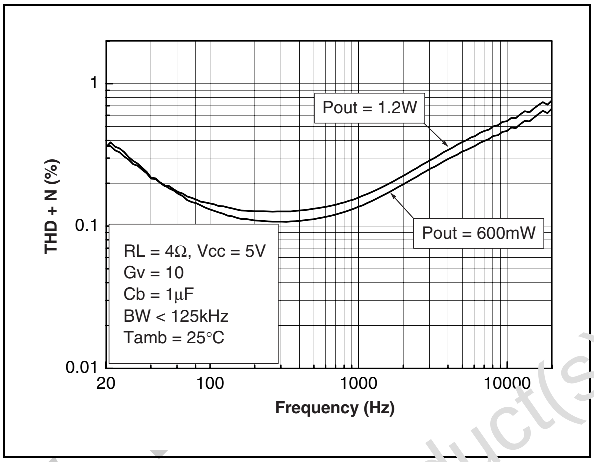


Fig. 47 : THD + N vs Frequency

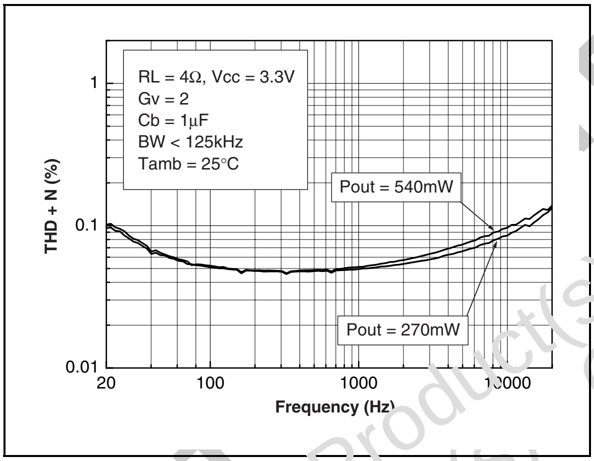


Fig. 48 : THD + N vs Frequency

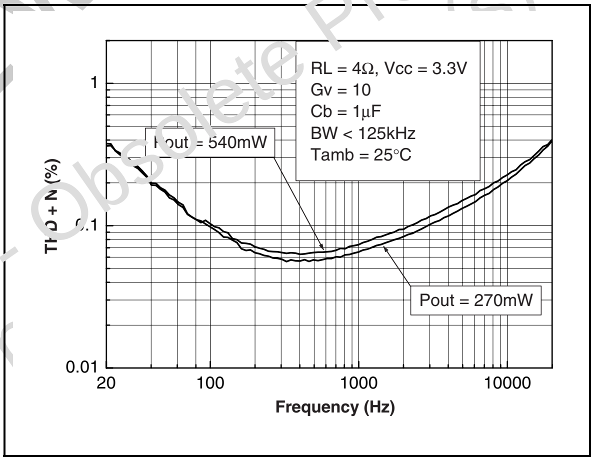


Fig. 49 : THD + N vs Frequency

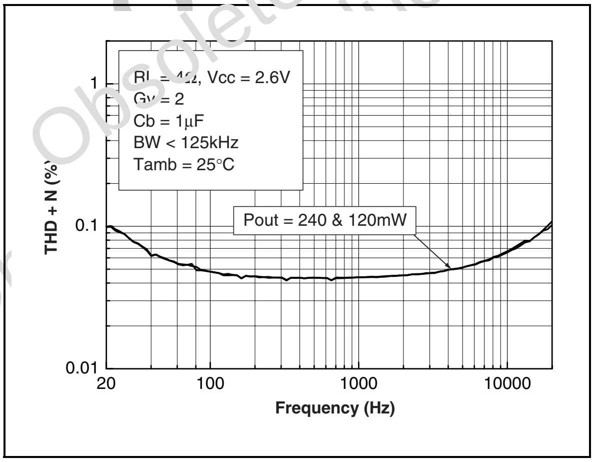


Fig. 50 : THD + N vs Frequency

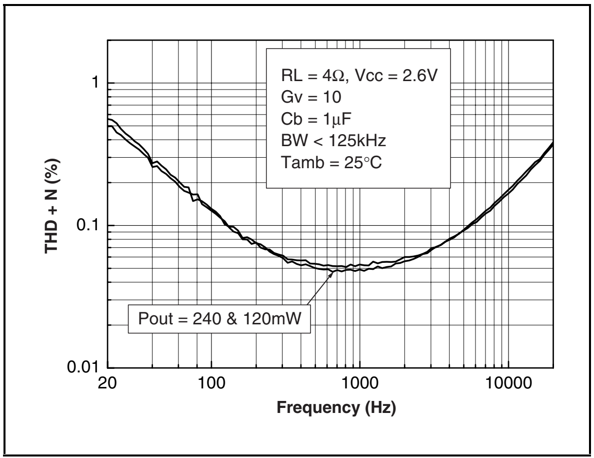


Fig. 51 : THD + N vs Frequency

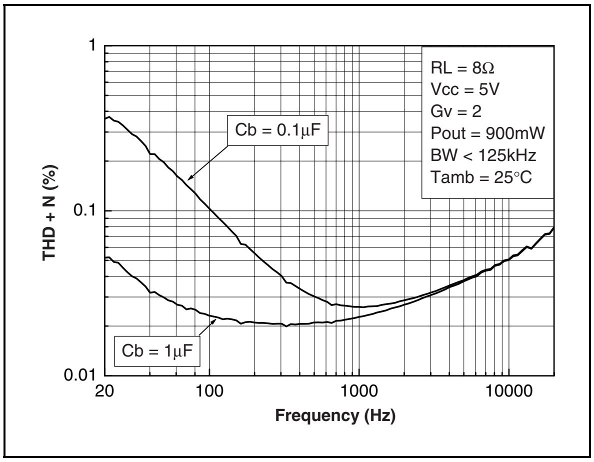


Fig. 52 : THD + N vs Frequency

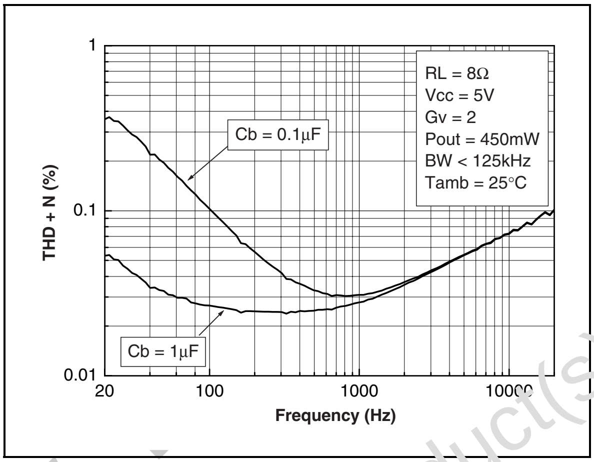


Fig. 53 : THD + N vs Frequency

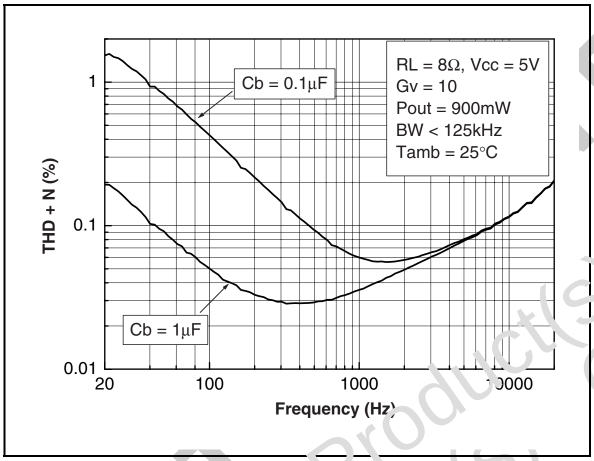


Fig. 54 : THD + N vs Frequency

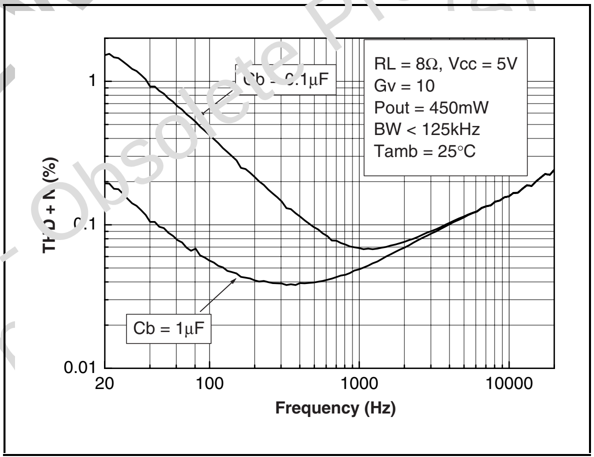


Fig. 55 : THD + N vs Frequency

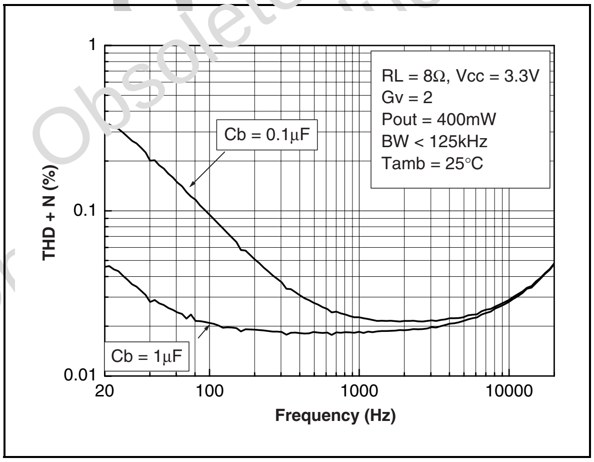


Fig. 56 : THD + N vs Frequency

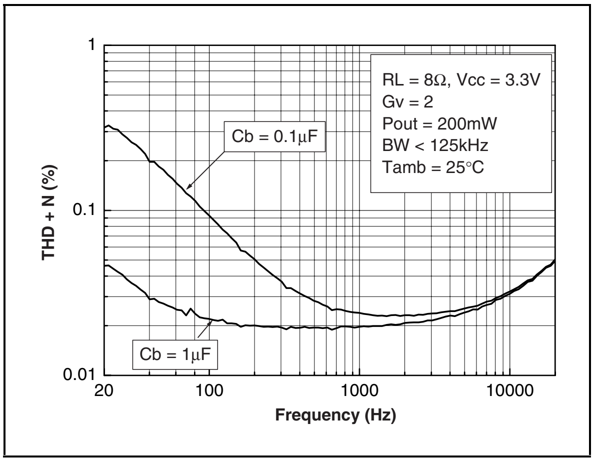


Fig. 57 : THD + N vs Frequency

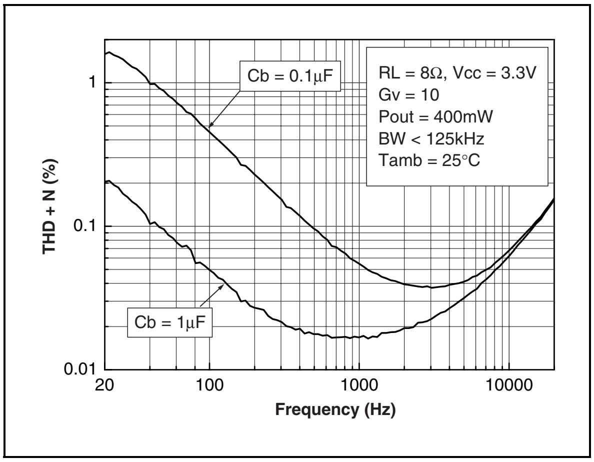


Fig. 58 : THD + N vs Frequency

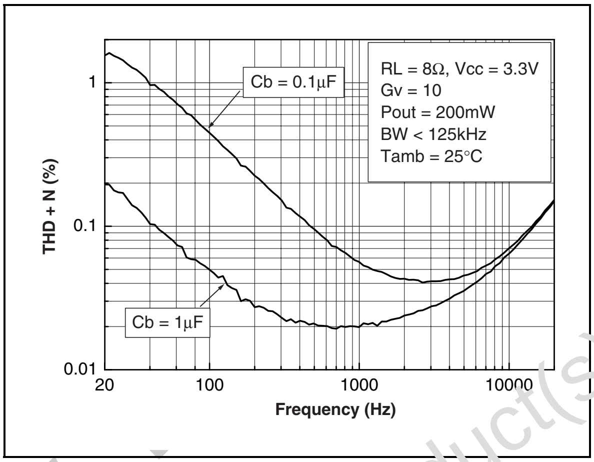


Fig. 59 : THD + N vs Frequency

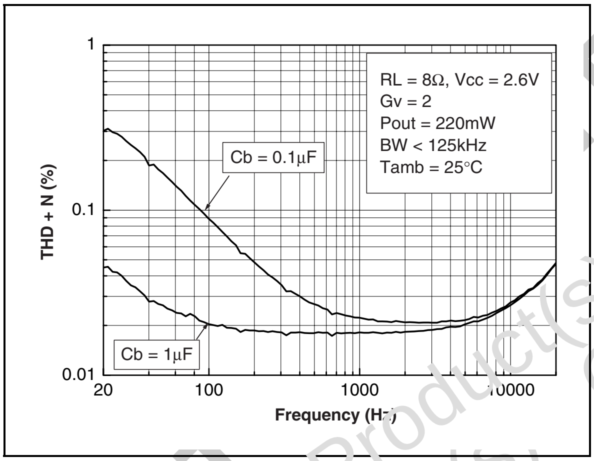


Fig. 60 : THD + N vs Frequency

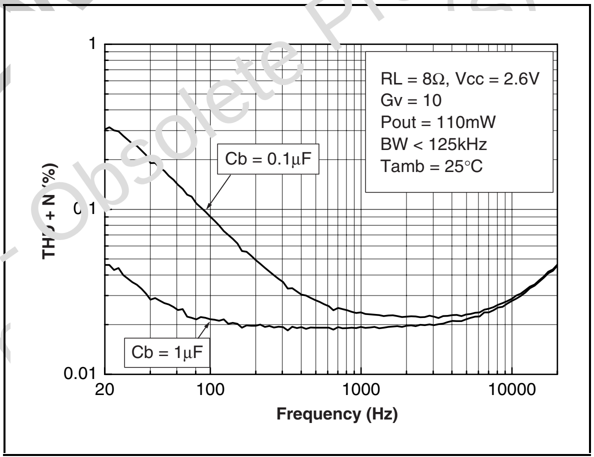


Fig. 61 : THD + N vs Frequency

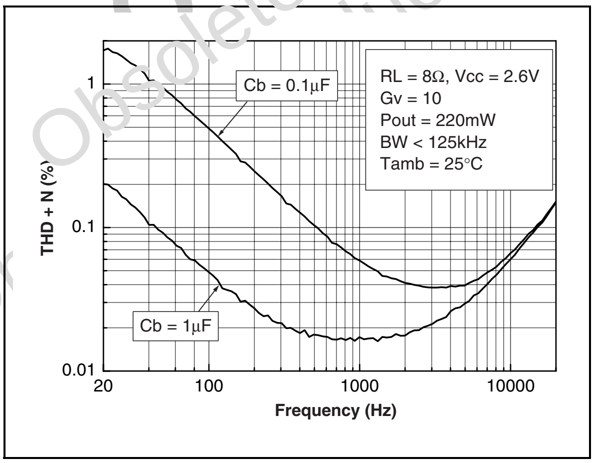


Fig. 62 : THD + N vs Frequency

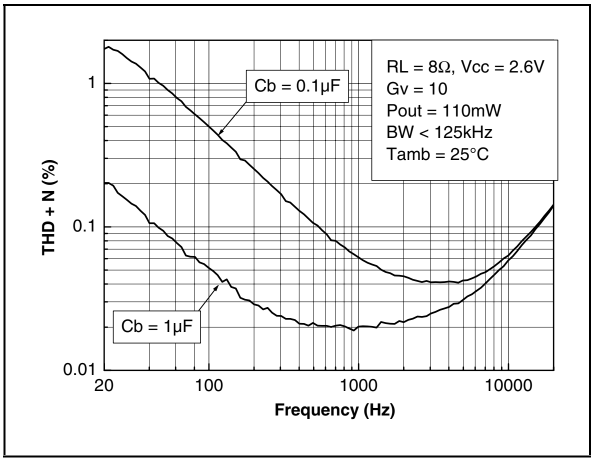


Fig. 63 : THD + N vs Frequency

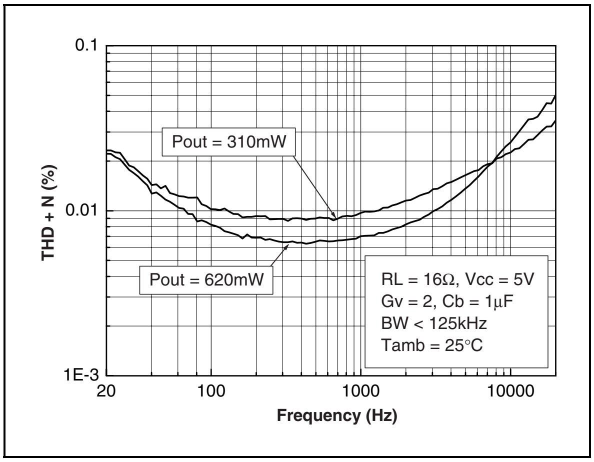


Fig. 64 : THD + N vs Frequency

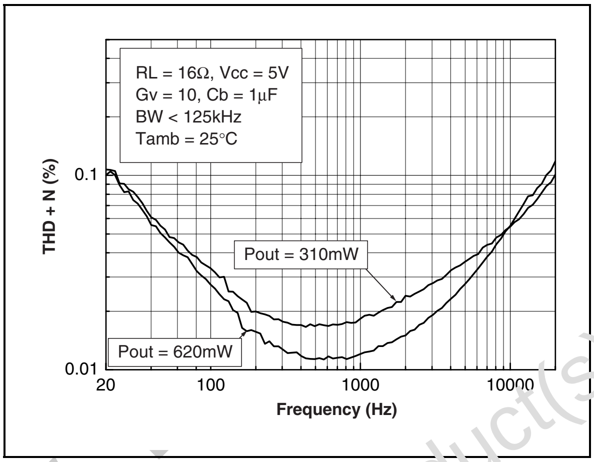


Fig. 65 : THD + N vs Frequency

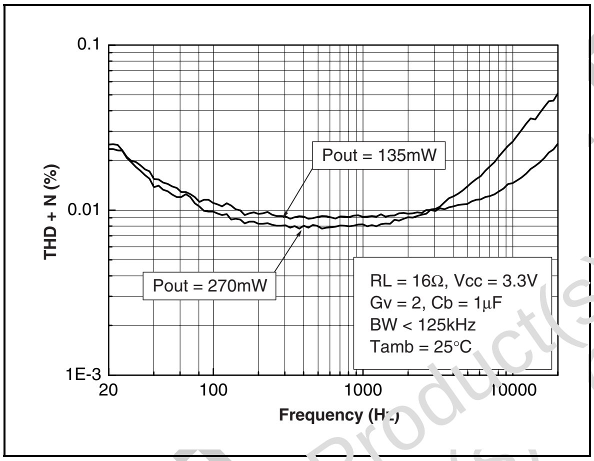


Fig. 66 : THD + N vs Frequency

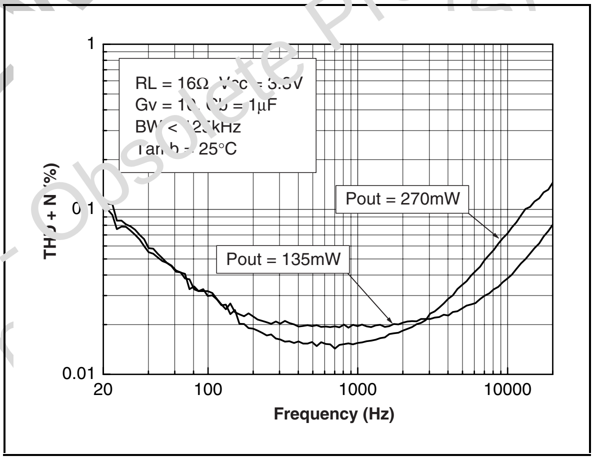


Fig. 67 : THD + N vs Frequency

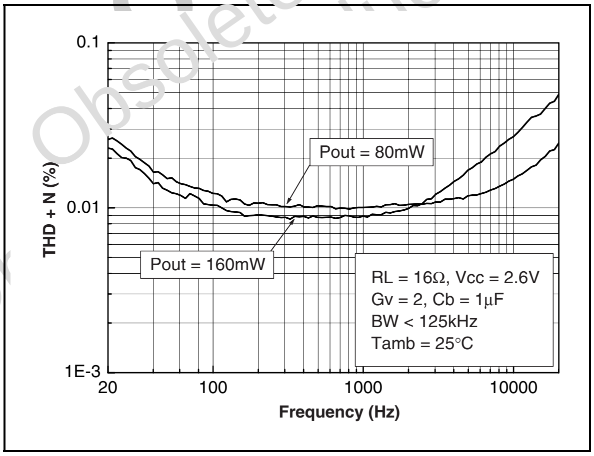


Fig. 68 : THD + N vs Frequency

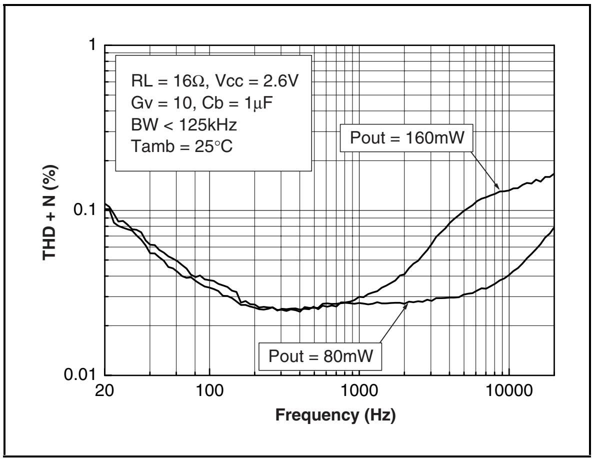


Fig. 69 : Signal to Noise Ratio vs Power Supply with Unweighted Filter (20Hz to 20kHz)

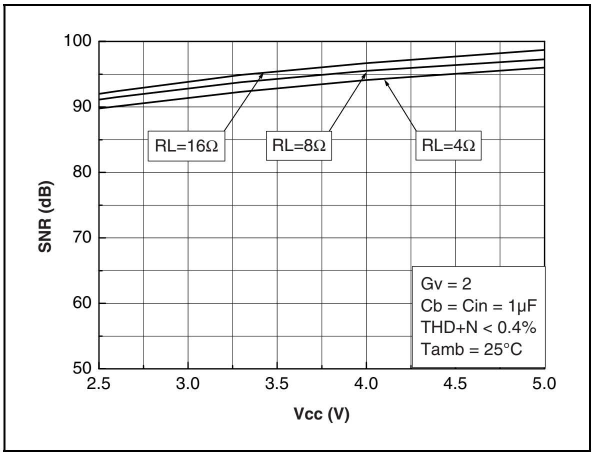


Fig. 70 : Signal to Noise Ratio Vs Power Supply with Unweighted Filter (20Hz to 20kHz)

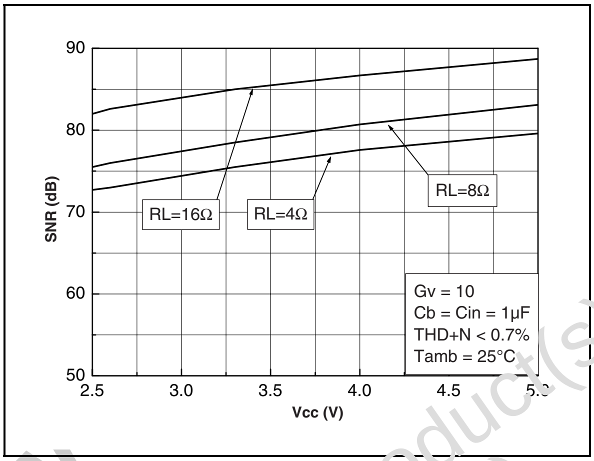


Fig. 71 : Signal to Noise Ratio vs Power Supply with Weighted Filter type A

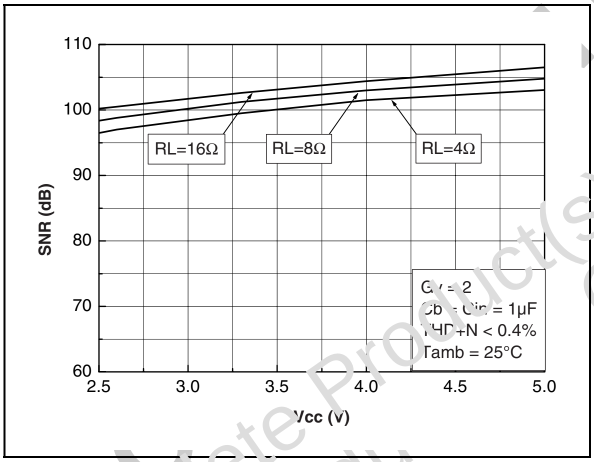


Fig. 72 : Signal to Noise Ratio vs Power Supply with Weighted Filter Type A

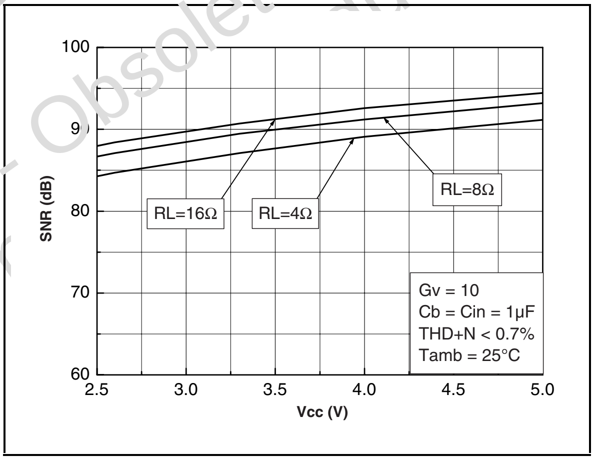


Fig. 73 : Frequency Response Gain vs Cin, & Cfeed

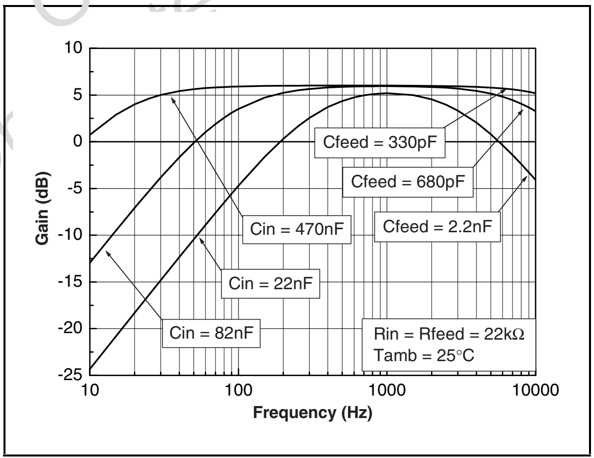


Fig. 74 : Current Consumption vs Power Supply Voltage

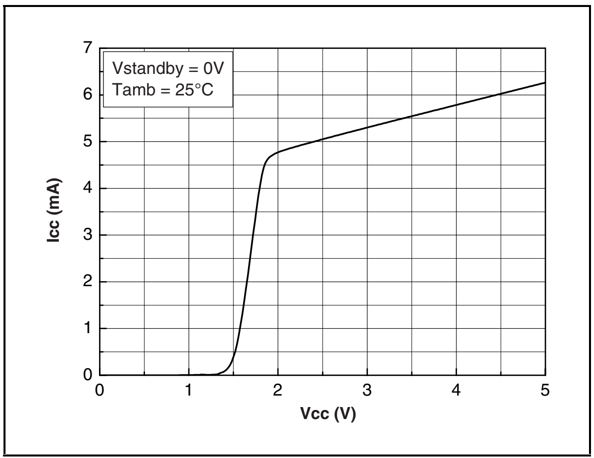


Fig. 75 : Current Consumption vs Standby Voltage @ Vcc = 5V

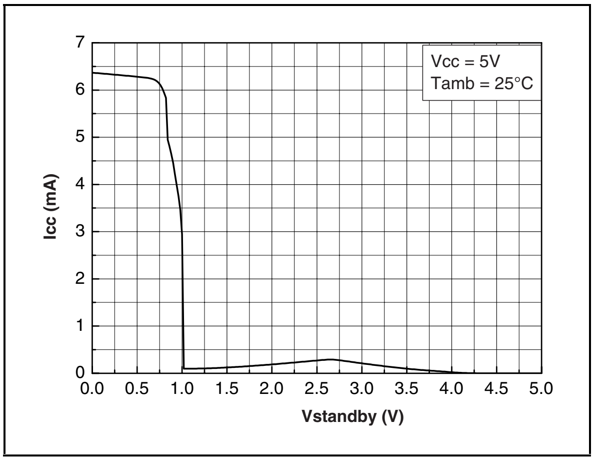


Fig. 76 : Current Consumption vs Standby Voltage @ Vcc = 3.3V

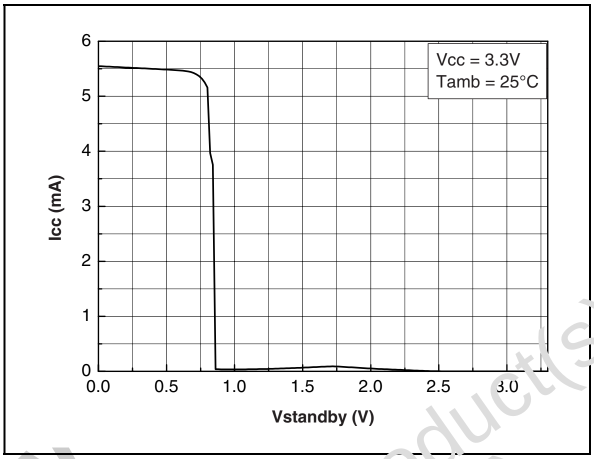


Fig. 77 : Current Consumption vs Standby Voltage @ Vcc = 2.6V

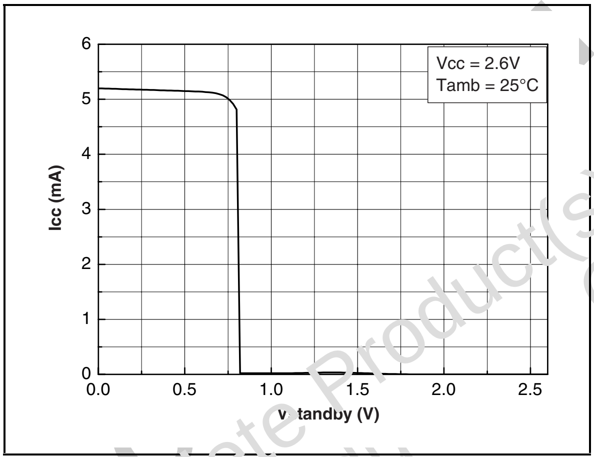


Fig. 78 : Clipping Voltage vs Power Supply Voltage and Load Resistor

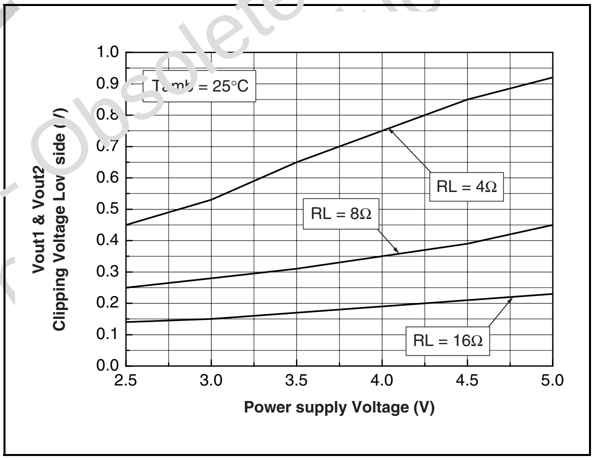
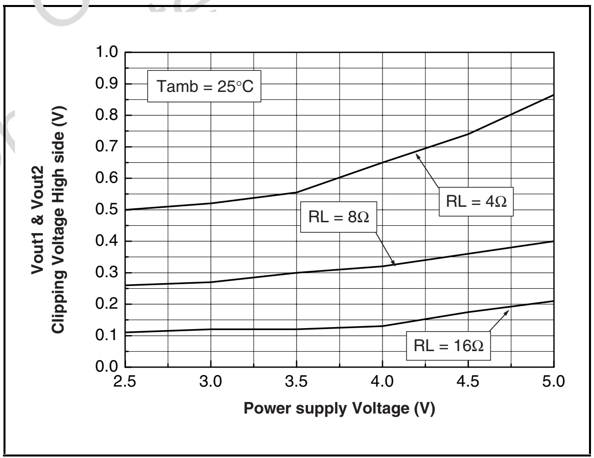


Fig. 79 : Clipping Voltage vs Power Supply Voltage and Load Resistor



APPLICATION INFORMATION

Fig. 80 : Demoboard Schematic

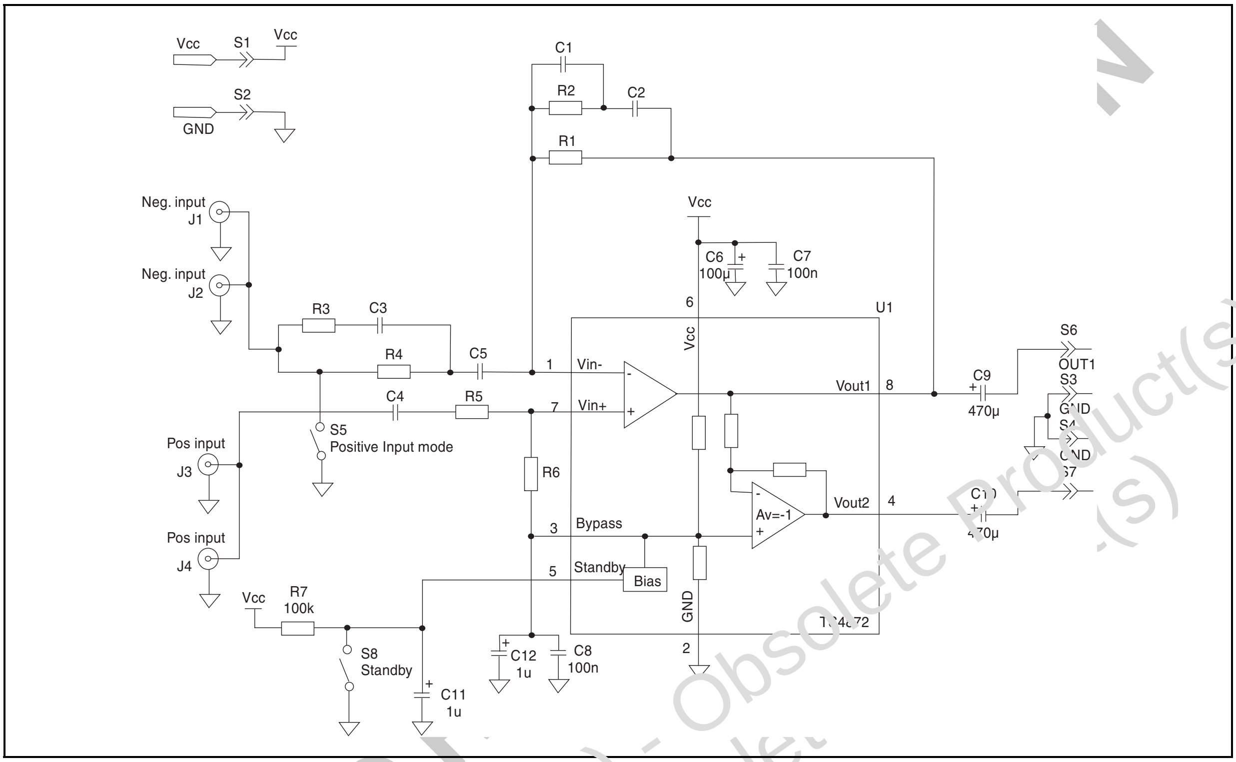


Fig. 81 : Flip Chip Demoboard Components Side

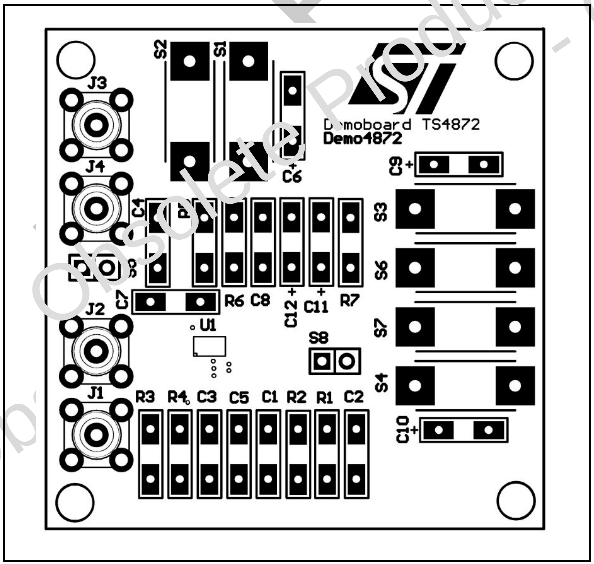


Fig. 82 : Flip Chip Demoboard Top Layer

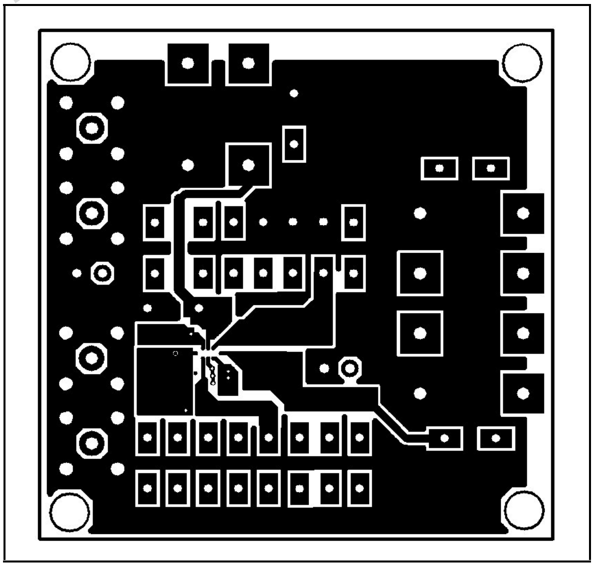
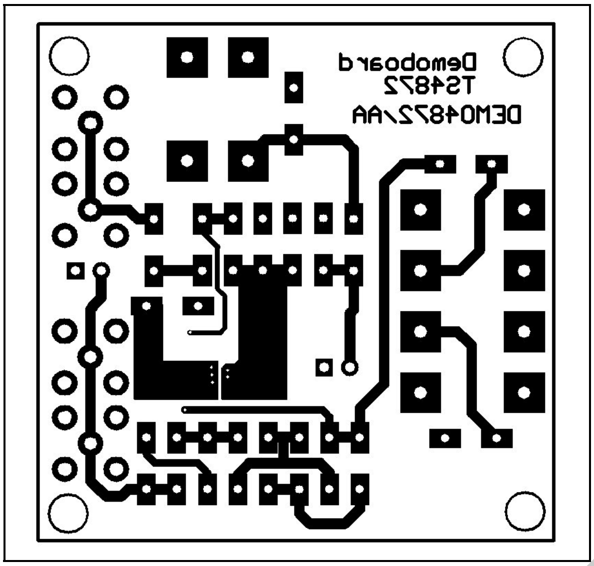


Fig. 83 : Flip Chip Demoboard Bottom Layer



■ BTL Configuration Principle

The TS4872 is a monolithic power amplifier with a BTL output type. BTL (Bridge Tied Load) means that each end of the load is connected to two single ended output amplifiers. Thus, we have :

Single ended output 1 = Vout1 = Vout (V)
Single ended output 2 = Vout2 = -Vout (V)

And Vout1 - Vout2 = 2Vout (V)

The output power is :

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L}\ (W)$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

■ Gain In Typical Application Schematic (cf. page 1)

In flat region (no effect of Cin), the output voltage of the first stage is :

$$Vout1 = -Vin\,\frac{Rfeed}{Rin}\ (V)$$

For the second stage : Vout2 = -Vout1 (V)

The differential output voltage is

$$Vout2 - Vout1 = 2Vin\,\frac{Rfeed}{Rin}\ (V)$$

The differential gain named gain (Gv) for more convenient usage is :

$$Gv = \frac{Vout2 - Vout1}{Vin} = 2\,\frac{Rfeed}{Rin}$$

Remark : Vout2 is in phase with Vin and Vout1 is 180 phased with Vin. It means that the positive terminal of the loudspeaker should be connected to Vout2 and the negative to Vout1.

■ Low and high frequency response

In low frequency region, the effect of Cin starts. Cin with Rin forms a high pass filter with a -3dB cut off frequency

$$F_{CL} = \frac{1}{2\pi\ Rin\ Cin}\ (Hz)$$

In high frequency region, you can limit the bandwidth by adding a capacitor (Cfeed) in parallel on Rfeed. Its form a low pass filter with a -3dB cut off frequency

$$F_{CH} = \frac{1}{2\pi\ Rfeed\ Cfeed}\ (Hz)$$

■ Power dissipation and efficiency

Hypothesis :

• Voltage and current in the load are sinusoidal (Vout and Iout)
• Supply voltage is a pure DC source (Vcc)

Regarding the load we have :

$$V_{OUT} = V_{PEAK}\sin\omega t\ (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L}\ (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L}\ (W)$$

Then, the average current delivered by the supply voltage is:

$$I_{CC\ AVG} = 2\frac{V_{PEAK}}{\pi R_L}\ (A)$$

Then, the **power dissipated by the amplifier** is Pdiss = Psupply - Pout (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT}\ (W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{OUT}} = 0$$

and its value is:

$$P_{diss\,max} = \frac{2V_{CC}^2}{\pi^2 R_L}\ (W)$$

Remark : This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

■ Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4872. A power supply bypass capacitor Cs and a bias voltage bypass capacitor Cb.

Cs has especially an influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.
With 100µF, you can expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 100µF, in high frequency increases, THD+N and disturbances on the power supply rail are less filtered.
To the contrary, if Cs is higher than 100µF, those disturbances on the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its function is critical on the final result of PSRR with input grounded in lower frequency.

If Cb is lower than 1µF, THD+N increase in lower frequency (see THD+N vs frequency curves) and the PSRR worsens up
If Cb is higher than 1µF, the benefit on THD+N in lower frequency is small but the benefit on PSRR is substantial (see PSRR vs. Cb curve : fig.12)

Note that Cin has a non-negligible effect on PSRR in lower frequency. Lower is its value, higher is the PSRR (see fig. 13).

■ Pop and Click performance

Pop and Click performance is intimately linked with the size of the input capacitor Cin and the bias voltage bypass capacitor Cb.

Size of Cin is due to the lower cut off frequency and PSRR value request and size of Cb is due to THD+N and PSRR request always in lower frequency.

Moreover, Cb determines the speed at which the amplifier turns ON. The slower the speed is , the softer turns ON noise.

The charge time of Cb is directly proportional to the internal generator resistance 50kΩ.
Then, the charging time constant for Cb is
τb = 50kΩxCb (s)
As Cb is directly connected to the non-inverting input (pin 3 & 7) and if we want to minimize, in amplitude and duration, the output spike on Vout1 (pin 8), Cin must be charged faster than Cb. The charge time constant of Cin is
τin = (Rin+Rfeed)xCin (s)

Thus we have the relation
τin << τb (s)

The respect of this relation permits to minimize the pop and click noise.

Remark : Minimize Cin and Cb has a benefit on pop and click phenomena but also on cost and size of the application.

Example : your target for the -3dB cut off frequency is 100 Hz. With Rin=Rfeed=22 kΩ, Cin=72nF (in fact 82nF or 100nF).

With Cb=1µF, if you choose the one of the latest two values of Cin, the pop and click phenomena at power supply ON or standby function ON/OFF will be very small

50 kΩx1µF >> 44kΩx100nF (50ms >> 4.4ms).

Increase Cin value increases the pop and click phenomena to an unpleasant sound at power supply ON and standby function ON/OFF.

Why Cs is not important in pop and click consideration ?

Hypothesis :

- Cs = 100µF
- Supply voltage = 5V
- Supply voltage internal resistor = 0.1Ω
- Supply current of the amplifier Icc = 6mA

At power ON of the supply, the supply capacitor is charged through the internal power supply resistor. So, to reach 5V you need about five to ten times the charging time constant of Cs (τs = 0.1xCs (s)).

Then, this time equal 50µs to 100µs << τb in the majority of application.

At power OFF of the supply, Cs is discharged by a constant current Icc. The discharge time from 5V to 0V of Cs is

$$t_{Discharge} = \frac{5Cs}{Icc} = 83\ \text{ms}$$

Now, we must consider the discharge time of Cb. At power OFF or standby ON, Cb is discharged by a 100kΩ resistor. So the discharge time is about $\tau b_{Disch} \approx 3xCbx100k\Omega$ (s).

In the majority of application, Cb=1µF, then $\tau b_{Disch} \approx 300ms >> t_{dischCs}$.

■ Power amplifier design examples

Given :

- Load impedance : 8Ω
- Output power @ 1% THD+N : 0.5W
- Input impedance : 10kΩ min.
- Input voltage peak to peak : 1Vpp
- Bandwidth frequency : 20Hz to 20kHz (0, -3dB)
- Ambient temperature max = 50°C

First of all, we must calculate the minimum power supply voltage to obtain 0.5W into 8Ω. With curves in fig. 15, we can read 3.5V.

Thus, the power supply voltage value min. will be 3.5V.

Following the maximum power dissipation equation

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L}\ (W)$$

with 3.5V we have Pdissmax=0.31W.

Referring to power derating curves (fig. 20), with 0.31W the maximum ambient temperature will be 100°C. This last value could be higher if you follow the example layout shown on the demoboard (better dissipation).

The gain of the amplifier in flat region will be

$$G_V = \frac{V_{OUTPP}}{V_{INPP}} = \frac{2\sqrt{2R_L P_{OUT}}}{V_{INPP}} = 5.65$$

We have Rin > 10kΩ. Let's take Rin = 10kΩ, then Rfeed = 28.25kΩ. We could use for Rfeed = 30kΩ in normalized value and the gain will be Gv = 6.

In lower frequency we want 20 Hz (-3dB cut off frequency). Then

$$C_{IN} = \frac{1}{2\pi\ R_{in}F_{CL}} = 795nF$$

So, we could use for Cin a 1µF capacitor value that gives 16Hz.

In Higher frequency we want 20kHz (-3dB cut off frequency). The Gain Bandwidth Product of the TS4872 is 2MHz typical and doesn't change when the amplifier delivers power into the load.

The first amplifier has a gain of

$$\frac{Rfeed}{Rin} = 3$$

and the theoretical value of the -3dB cut-off higher frequency is 2MHz/3 = 660kHz.

We can keep this value or limit the bandwidth by adding a capacitor Cfeed, in parallel on Rfeed.

Then

$$C_{FEED} = \frac{1}{2\pi\ R_{FEED} F_{CH}} = 265pF$$

So, we could use for Cfeed a 220pF capacitor value that gives 24kHz.

Now, we can calculate the value of Cb with the formula $\tau b = 50k\Omega x Cb >> \tau in = (Rin+Rfeed)xCin$ which permits to reduce the pop and click effects. Then Cb >> 0.8µF.
We can choose for Cb a normalized value of 2.2µF that gives good results in THD+N and PSRR.

In the following tables, you could find three another examples with values required for the demoboard.

Remark : components with (*) marking are optional.

Application n°1 : 20Hz to 20kHz bandwidth and 6dB gain BTL power amplifier.

Components :

Designator	Part Type
R1	22k / 0.125W
R4	22k / 0.125W
R6	Short Cicuit
R7	330k / 0.125W
C5	470nF
C6	100µF
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1µF
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	2 pts connector 2.54mm pitch
J1	SMB plug
U1	TS4872IJ

Application n°2 : 20Hz to 20kHz bandwidth and 20dB gain BTL power amplifier.

Components :

Designator	Part Type
R1	110k / 0.125W
R4	22k / 0.125W
R6	Short Cicuit
R7	330k / 0.125W
C5	470nF
C6	100µF
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1µF
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	2 pts connector 2.54mm pitch
J1	SMB Plug
U1	TS4872IJ

Application n°3 : 50Hz to 10kHz bandwidth and 10dB gain BTL power amplifier.

Components :

Designator	Part Type
R1	33k / 0.125W
R2	Short Circuit
R4	22k / 0.125W
R6	Short Cicuit
R7	330k / 0.125W
C2	470pF
C5	150nF
C6	100µF
C7	100nF
C9	Short Circuit

Designator	Part Type
C10	Short Circuit
C12	1µF
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	2 pts connector 2.54mm pitch
J1	SMB Plug
U1	TS4872IJ

Application n°4 : Differential inputs BTL power amplifier.

In this configuration, we need to place these components : R1, R4, R5, R6, R7, C4, C5, C12.

We have also : R4 = R5, R1 = R6, C4 = C5.

The gain of the amplifier is :

$$G_{VDIFF} = 2\,\frac{R1}{R4}\,(\text{Pos. Input - Neg.Input})$$

For a 20Hz to 20kHz bandwidth and 6dB gain BTL power amplifier you could follow the bill of material below.

Components :

Designator	Part Type
R1	22k / 0.125W
R4	22k / 0.125W
R5	22k / 0.125W
R6	22k / 0.125W
R7	330k / 0.125W
C4	470nF
C5	470nF

Designator	Part Type
C6	100µF
C7	100nF
C9	Short Circuit
C10	Short Circuit
C12	1µF
S1, S2, S6, S7	2mm insulated Plug 10.16mm pitch
S8	2 pts connector 2.54mm pitch
J1, J3	SMB Plug
U1	TS4872IJ

■ Note on how to use the PSRR curves (page 8)

We have finished a design and we have chosen the components :

- Rin=Rfeed=22kΩ
- Cin=100nF
- Cb=1µF

Now, on fig. 13, we can see the PSRR (input grounded) vs frequency curves. At 217Hz we have a PSRR value of -36dB.
In reality we want a value about -70dB. So, we need a gain of 34dB !
Now, on fig. 12 we can see the effect of Cb on the PSRR (input grounded) vs. frequency. With Cb=100µF, we can reach the -70dB value.
The process to obtain the final curve (Cb=100µF, Cin=100nF, Rin=Rfeed=22kΩ) is a simple transfer point by point on each frequency of the curve on fig. 13 to the curve on fig. 12.
The measurement results is shown on **figure 84**.

Fig. 84 : PSRR changes with Cb

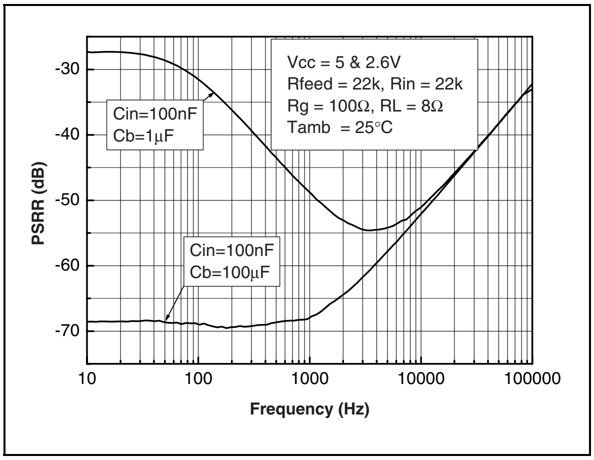
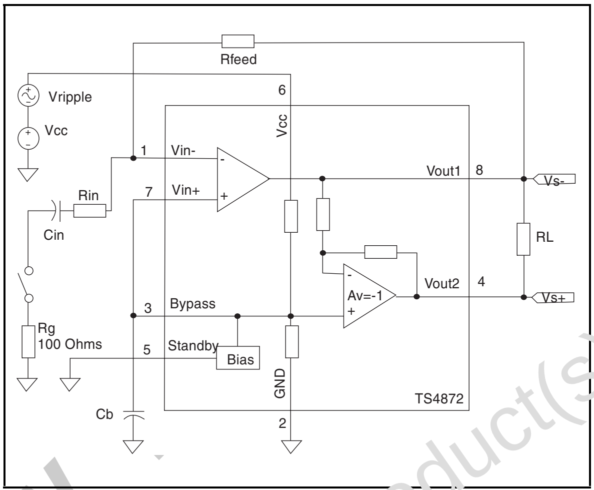


Fig. 85 : PSRR measurement schematic



■ Note on PSRR measurement

What is the PSRR ?

The PSRR is the Power Supply Rejection Ratio. It's a kind of SVR in a determined frequency range. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output.

We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How we measure the PSRR ?

For PSRR measurement schematic see **figure 85**

■ Principle of operation

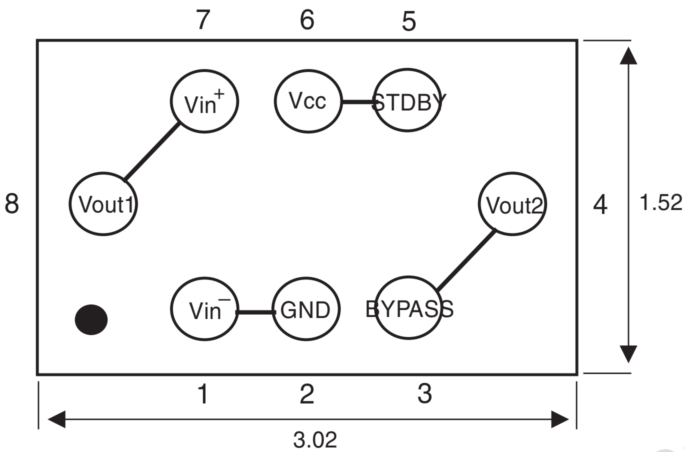
- We fixed the DC voltage supply (Vcc)
- We fixed the AC sinusoidal ripple voltage (Vripple)
- No bypass capacitor Cs is used

The PSRR value for each frequency is :

$$PSRR(dB) = 20 \times Log_{10}\left[\frac{Rms(V_{ripple})}{Rms(Vs_{+} - Vs_{-})}\right]$$

Remark : The measure of the Rms voltage is not a Rms selective measure but a full range (2 Hz to 125 kHz) Rms measure. It means that we measure the effective Rms signal + the noise.

TOP VIEW OF THE DAISY CHAIN MECHANICAL DATA (all drawings dimensions are in millimeters)



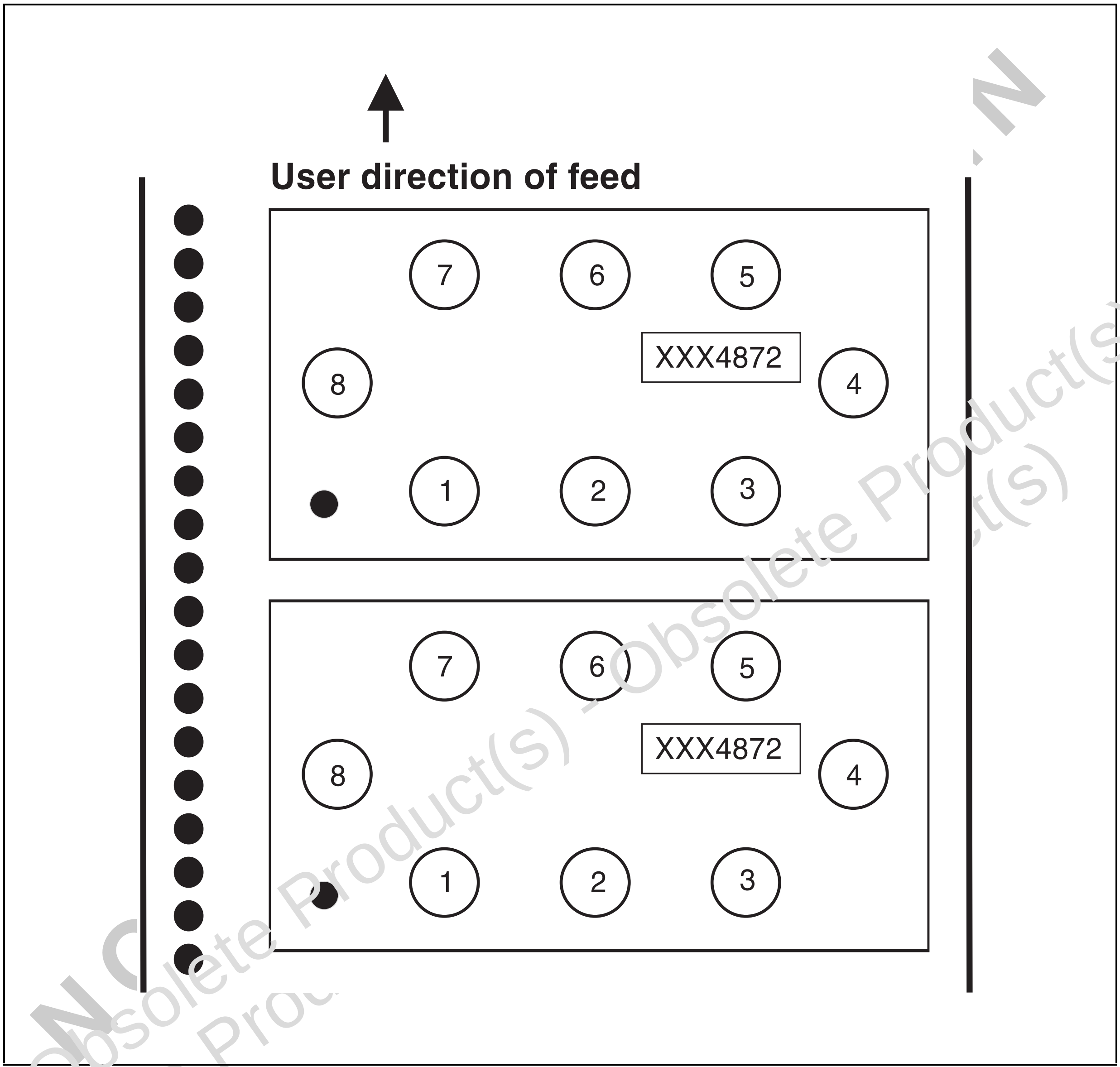
REMARKS

Daisy chain sample is featuring pins connection two by two. The schematic above is illustrating the way connecting pins each other. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting an Ohmeter between pin 8 and pin 1, the soldering process continuity can be tested.

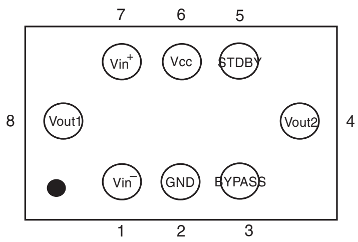
ORDER CODE

Part Number	Temperature Range	Package	Marking
		J	
TSDC4872IJT	-40, +85°C	•	DC01

TAPE & REEL SPECIFICATION (top view)

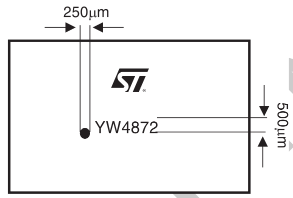


PIN OUT (top view)



- Balls are underneath

MARKING (top view)

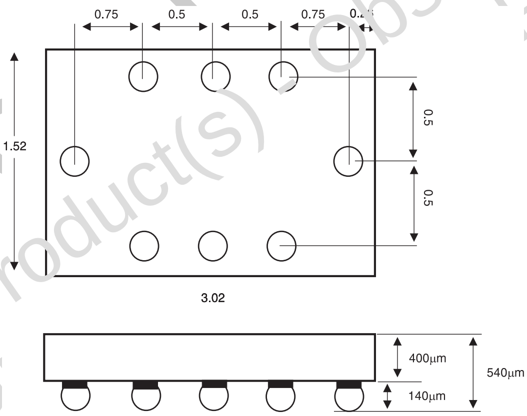


- Y : Year
- W : Week with two digits
- Example : 1254872

PACKAGE MECHANICAL DATA

FLIP CHIP - 8 BUMPS

- Die size : (3.02mm±10%) x (1.52mm ±10%)
- Die height (including bumps) : 540µm ±50µm
- Bump height : 140µm ±15µm (i.e. bump diameter of 185µm ±15µm)
- Silicon thickness : 400µm±25µm
- Pitch: 500µm ±10µm and 750µm±10µm



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