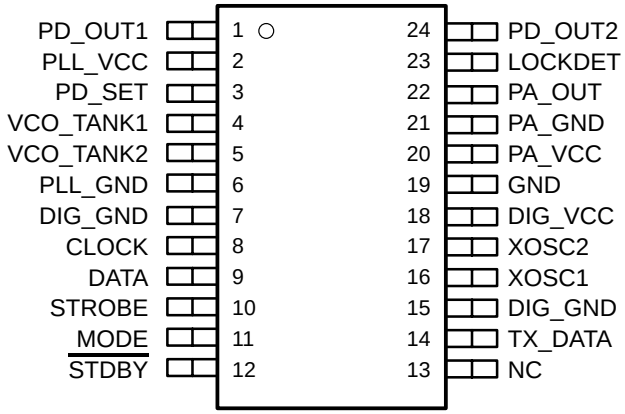
- **Single-Chip RF Transmitter for 433 MHz ISM Band**
- **420-MHz to 450-MHz Operation**
- **FM/FSK Operation for Transmit**
- **24-Bit Direct Digital Synthesizer (DDS) With 11-Bit DAC**
- **On-Chip Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL)**
- **On-Chip Reference Oscillator**
- **Minimal External Components Required**
- **Low Power Consumption**
- **Typical Output Power of 7 dBm**
- **Typical Output Frequency Resolution of 230 Hz**
- **Ultrafast Lock Times From DDS Implementation**
- **Two Fully-Programmable Operational Modes**
- **2.2-V to 3.6-V Operation**
- **Flexible Serial Interface to TI MSP430 Microcontroller**
- **24-Pin Plastic Thin-Shrink Small-Outline Package (TSSOP)**

PW PACKAGE
(TOP VIEW)



description

The TRF4400 single-chip solution is an integrated circuit intended for use as a low cost FSK transmitter to establish a frequency-agile RF link. The device is available in a 24-lead TSSOP package and is designed to provide a fully-functional multichannel transmitter. The chip is intended for linear (FM) or digital (FSK) modulated applications in the 433-MHz ISM band. The single-chip transmitter operates down to 2.2 V and is expressly designed for low power consumption. The synthesizer has a typical channel spacing of approximately 230 Hz to allow narrow-band as well as wide-band applications. Due to the narrow channel spacing of the direct digital synthesizer (DDS), the DDS can be used to adjust the TX frequency and allows the use of inexpensive reference crystals.

Two fully-programmable operation modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings (e.g., TX_frequency_0/TX_frequency_1) without reprogramming the device. Each functional block of the transmitter can be specifically enabled or disabled via the serial interface.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

transmitter

The transmitter consists of an integrated VCO, a complete fully-programmable direct digital synthesizer, and a power amplifier. The internal VCO can be used with an external tank circuit or an external VCO. The divider, prescaler, and reference oscillator require only the addition of an external crystal and a loop filter to provide a complete DDS with a typical frequency resolution of 230 Hz.

The 8-bit FSK frequency deviation register determines the frequency deviation in FSK mode. The modulation itself is done in the direct digital synthesizer, hence no additional external components are necessary.

Since the typical RF output power is approximately 7 dBm, no additional external RF power amplifier is necessary in most applications.

The TRF4400 RF transmitter is suitable for use in applications that include the TRF6900 RF transceiver.

baseband interface

The TRF4400 can easily be interfaced to a baseband processor such as the Texas Instruments MSP430 ultralow-power microcontroller (see Figure 1). The TRF4400 serial control registers are programmed by the MSP430, and the MSP430 performs baseband operations in software.

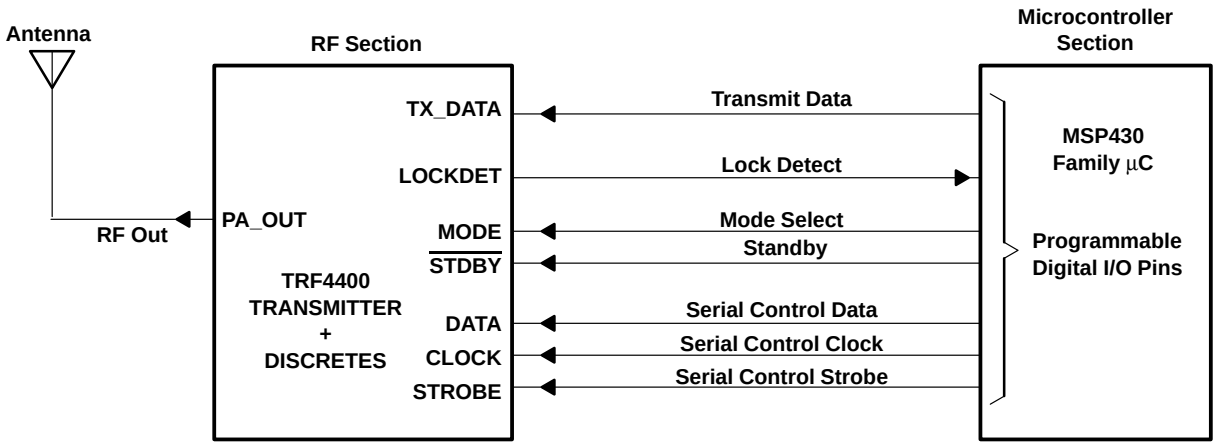
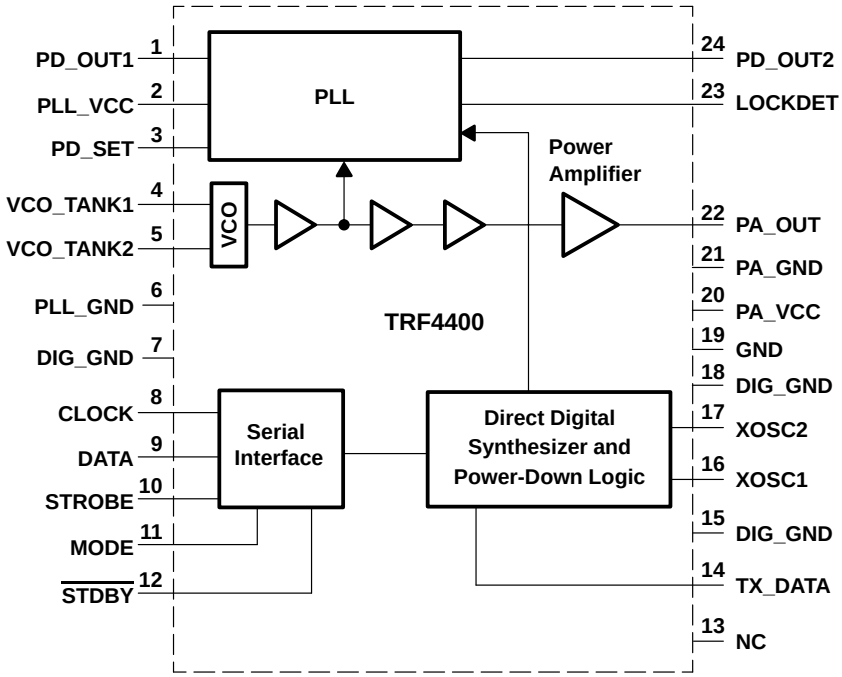


Figure 1. System Block Diagram for Interfacing to the MSP430 Microcontroller

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLOCK	8	I	Serial interface clock signal
DATA	9	I	Serial interface data signal
DIG_GND	7, 15		Digital ground
DIG_VCC	18		Digital supply voltage
GND	19		Ground
LOCKDET	23	O	PLL lock detect output, active high. PLL locked when LOCKDET = 1.
MODE	11	I	Mode select input. The functionality of the device in Mode0 or Mode1 can be programmed via the A-, B-, C-, and D-words of the serial control interface.
NC	13		No connection
PA_GND	21		Power amplifier ground
PA_OUT	22	O	Power amplifier output, open collector
PA_VCC	20		Power amplifier supply voltage
PD_OUT1	1	O	Charge pump output – PLL in locked condition
PD_OUT2	24	O	Charge pump output – PLL in unlocked condition
PD_SET	3		Charge pump current setting terminal. An external resistor (R_{PD}) is connected to this terminal to set the nominal charge pump current.
PLL_GND	6		PLL ground
PLL_VCC	2		PLL supply voltage
$\overline{\text{STDBY}}$	12	I	Standby control for the TRF4400, active low. While $\overline{\text{STDBY}}$ = 0, the contents of the control registers are still valid and can be programmed via the serial control interface.
STROBE	10	I	Serial interface strobe signal
TX_DATA	14	I	Digital modulation input for FSK/FM modulation of the carrier, active high
VCO_TANK1	4	I	VCO tank circuit connection. Should be left open if an external VCO is used.
VCO_TANK2	5	I	VCO tank circuit connection. May also be used to input an external VCO signal.
XOSC1	16	O	Reference crystal oscillator connection
XOSC2	17	I	Reference crystal oscillator connection. May be used as a single-ended clock input if an external crystal is not used.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, PA_VCC, PLL_VCC, DIG_VCC, VCC (see Note 1) . . . . . –0.6 to 4.5 Vdc
Input voltage, V_I (logic signals) . . . . . –0.6 to 4.5 Vdc
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
ESD integrity‡ . . . . . 2 kV HBM

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ RF terminal 22, PA_OUT, is not protected against voltage stress higher than 800 V HBM.
NOTE 1: All GND and VCC terminals must be connected to either ground or supply, respectively, even if the function block is not used.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, PA_VCC, PLL_VCC, DIG_VCC, DDS_VCC, VCC	2.2		3.6	V
Operating temperature	–20		60	°C
High-level input voltage, V_{IH} (DATA, CLOCK, STROBE, TX_DATA, MODE, $\overline{\text{STDBY}}$)	V_{CC}–0.5			V
Low-level input voltage, V_{IL} (DATA, CLOCK, STROBE, TX_DATA, MODE, $\overline{\text{STDBY}}$)			0.5	V
High-level output voltage, V_{OH} (LOCKDET); I_{OH} = 0.5 mA	V_{CC}–0.5			V
Low-level output voltage, V_{OL} (LOCKDET); I_{OL} = 0.5 mA			0.5	V

electrical characteristics over full range of operating conditions, (typical values are at PA_VCC, PLL_VCC, DIG_VCC, VCC = 3 V, T_A = 25°C) (unless otherwise noted)

supply current consumption in each mode

MODE		ACTIVE STAGES	MIN	TYP	MAX	UNIT
Power down (standby mode)		None		0.5		μA
TX	PA STATE	DDS, PLL, VCO, PA				mA
	0 dB attenuation			57	75	
	10 dB attenuation			29		
	20 dB attenuation			22		
	PA disabled			10	12.5	

VCO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		420	433	450	MHz
Phase noise	50-kHz offset		–100		dBc/Hz
Tuning voltage		0.5		V_{CC} – 0.4	V

electrical characteristics over full range of operating conditions, (typical values are at PA_VCC, PLL_VCC, DIG_VCC, VCC = 3 V, T_A = 25°C) (unless otherwise noted) (continued)

direct digital synthesizer (DDS)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference oscillator input frequency, f_{ref}	As oscillator		15		26	MHz
	As buffer		15		26	
Programmable DDS divider ratio		22 bits	0		4194303	
DDS divider resolution, Δf			$N \times f_{ref} \div 2^{24}$			
FSK – modulation register ratio		8 bits	0		1020	
FSK – modulation resolution			$N \times f_{ref} \div 2^{22}$			

PLL

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF input frequency		420	433	450	MHz
RF input power	Internal VCO bypassed; external input applied to VCO_TANK2		–10		dBm
RF input divider ratio, N		256		512	
RF output frequency resolution			$N \times f_{ref} \div 2^{24}$		
Charge pump current	Programmable with external resistor, 100-kΩ nominal, APLL = 0		70		µA

power amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		420	433	450	MHz
Amplifier output power (see Note 2)	0-dB attenuation		7		dBm
	10-dB attenuation		–3		
	20-dB attenuation		–12		
	Amplifier off		–70		
Optimal load impedance			See Figure 11		Ω
2nd-order harmonic	V_{CC} = 3 V, 0-dB attenuation		–10		dBc
3rd-order harmonic	V_{CC} = 3 V, 0-dB attenuation		–20		dBc

NOTE 2: The device and output matching network (see *Application Information* section) is designed to provide the output power into a 50-Ω load. The device stability was tested (no parasitic oscillations) with an output VSWR of 10:1 over all phase angles and is not tested in production.

typical mode switching and lock times

OPERATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby to transmit time†	From rising edge of $\overline{\text{STDBY}}$ to valid RF signal at PA_OUT, APLL = 111b (maximum)		500		µs

† Highly dependent upon loop filter topology

timing data for serial interface (see Figure 2)

PARAMETER		MIN	MAX	UNIT
$f_{(CLOCK)}$	CLOCK frequency		20	MHz
$t_{w(CLKHI)}$	CLOCK high-time pulse width, CLOCK high	25		ns
$t_{w(CLKLO)}$	CLOCK low-time pulse width, CLOCK low	25		ns
$t_{su(DATA)}$	Setup time, data valid before CLOCK high	25		ns
$t_{h(DATA)}$	Hold time, data valid after CLOCK high	25		ns
$t_{w(STROBEHI)}$	Strobe high-time pulse width, STROBE high (see Note 3)	25		ns
$t_{w(STROBELO)}$	Strobe low-time pulse width, STROBE low	25		ns

NOTE 3: CLOCK and DATA must both be low when STROBE is asserted (STROBE = 1).

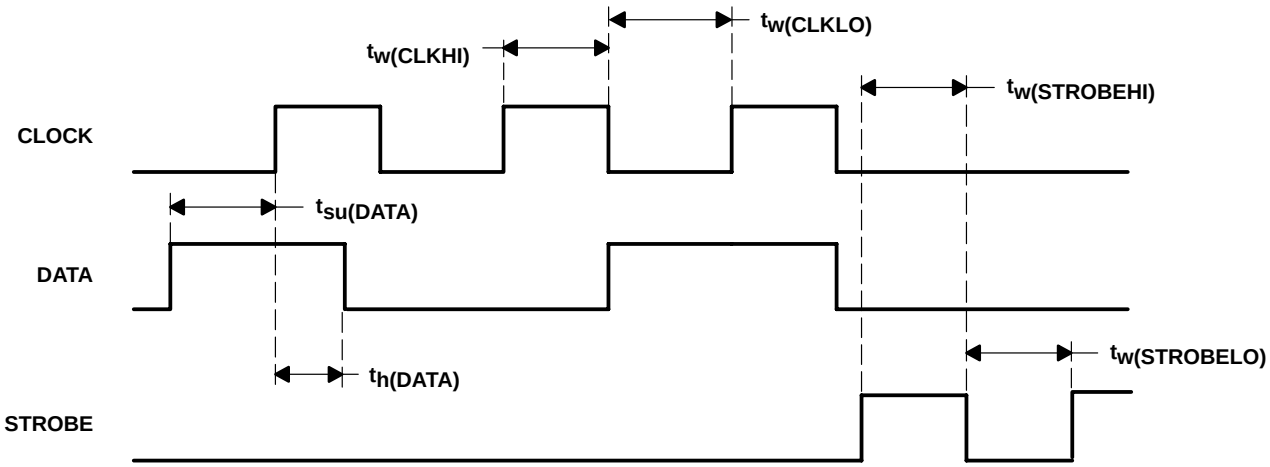


Figure 2. Serial Data Interface Timing

detailed description

reference oscillator

The reference oscillator provides the DDS system clock. It allows operation, with a suitable external crystal, between 15 MHz and 26 MHz.

An external oscillator can be used to supply clock frequencies between 15 MHz and 26 MHz. The external oscillator should be directly connected to XOSC2, terminal 17. The other oscillator terminal (XOSC1, terminal 16) should be left open or can be used as a buffered version of the signal applied at terminal 17 (see Figure 3). The same crystal or externally supplied oscillator signal is used to derive both the transmit and receive frequencies.

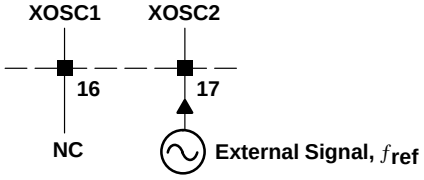


Figure 3. Applying an External Oscillator Signal

direct digital synthesizer

general principles of DDS operation

In general, a direct digital synthesizer (DDS) is based on the principle of generating a sinewave signal in the digital domain. Benefits include high precision, wide frequency range, a high degree of software programmability, and extremely fast lock times.

Figure 4 shows a block diagram of a typical DDS. It generally consists of an accumulator, sine lookup table, a digital-to-analog converter, and a low-pass filter. All digital blocks are clocked by the reference oscillator.

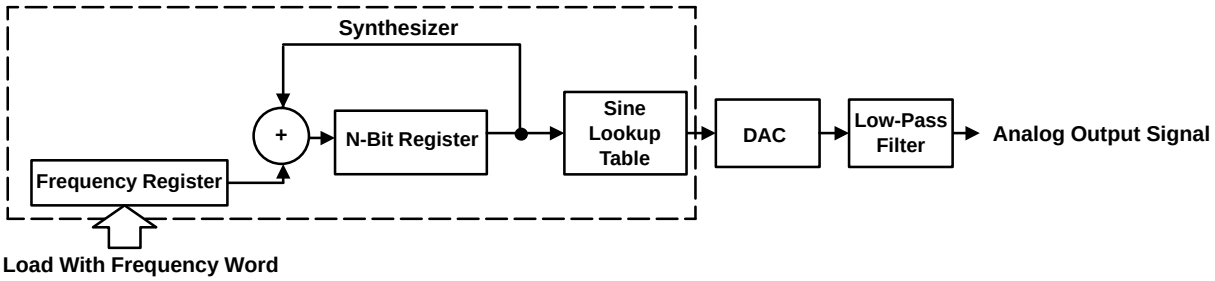


Figure 4. Typical DDS Block Diagram

The DDS constructs an analog sine waveform using an N-bit adder counting up from 0 to 2^N in steps of the frequency register whereby generating a digital ramp waveform. Each number in the N-bit output register is used to select the corresponding sine wave value out of the sine lookup table. After the digital-to-analog conversion, a low-pass filter is necessary to suppress unwanted spurious responses.

The analog output signal can be used as a reference input signal for a phase-locked loop (PLL). The PLL circuit multiplies the reference frequency by a predefined factor.

TRF4400 direct digital synthesizer implementation

Figure 5 shows a block diagram of the DDS implemented in the TRF4400. It consists of a 24-bit accumulator clocked by the reference oscillator along with control logic settings.

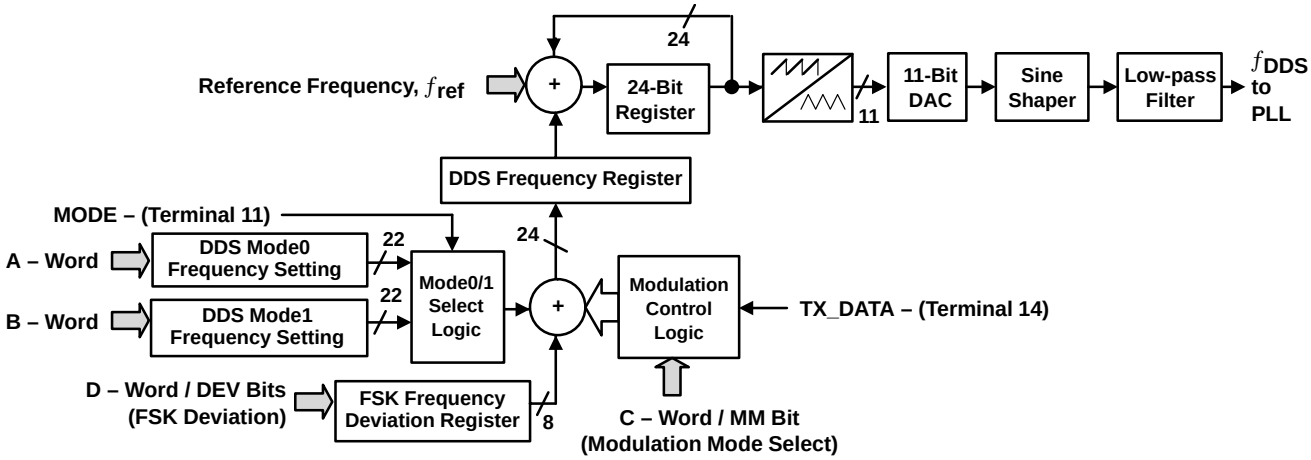


Figure 5. DDS Block Diagram as Implemented in the TRF4400

TRF4400 direct digital synthesizer implementation (continued)

The frequency of the reference oscillator, f_{ref}, is the DDS sample frequency, which also determines the maximum DDS output frequency. Together with the accumulator width (in bits), the frequency resolution of the DDS can be calculated. Multiplied by the divider ratio (prescaler) of the PLL, N, the minimum frequency step size of the TRF4400 is calculated as follows:

$$\Delta f = N \times \frac{f_{ref}}{2^{24}}$$

The 24-bit accumulator can be programmed via two 22-bit frequency setting registers (the A-word determines the mode0 frequency, the B-word determines the mode1 frequency) with the two MSB bits set to 0. Consequently, the maximum bit weight of the DDS system is reduced to 1/8 (see Figure 6). This bit weight corresponds to a VCO output frequency of (f_{ref}/8) × N. Depending on the MODE terminal's (terminal 11) logic level, the internal mode select logic loads the frequency register with either the DDS_0 or DDS_1 frequency (see Figure 5 and Figure 6).

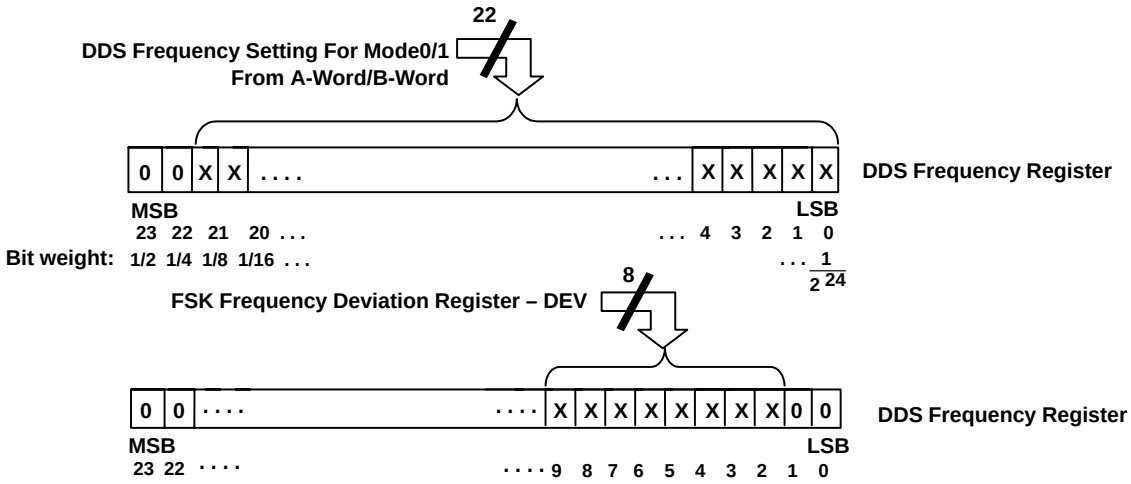


Figure 6. Implementation of the DDS Frequency and FSK Frequency Deviation in the DDS Frequency Register

The VCO output frequency, f_{out}, which is dependent on the DDS_x frequency settings (DDS_0 in the A-word or DDS_1 in the B-word), can be calculated as follows:

$$f_{out} = DDS\_x \times N \times \frac{f_{ref}}{2^{24}} = N \times \frac{f_{ref} \times DDS\_x}{2^{24}}$$

If FSK modulation is selected (MM=0; C-Word, bit 16), then the 8-bit FSK deviation register can be used to program the frequency deviation of the 2-FSK modulation. Figure 6 illustrates where the 8 bits of the FSK deviation register map into the 24-bit DDS frequency register. Since the two LSBs are set to 0, the total FSK deviation can be determined as follows:

$$\Delta f_{2\text{–FSK}} = N \times \frac{DEV \times f_{ref}}{2^{22}}$$

Hence, the 2-FSK frequency, set by the level on the TX_DATA is calculated as follows:

$$f_{out1:TX\_DATA=Low} = N \times \frac{f_{ref} \times DDS\_x}{2^{24}} \qquad f_{out2:TX\_DATA=High} = N \times \frac{f_{ref} \times (DDS\_x + 4 \times DEV)}{2^{24}}$$

This frequency modulated output signal is used as a reference input signal for the PLL circuit. Channel width (frequency deviation) for 2-FSK modulation and channel spacing are software programmable. The minimum channel width and minimum channel spacing depend on the RF system frequency plan.

TRF4400 direct digital synthesizer implementation (continued)

Note that the frequencies f_{out1} and f_{out2} are centered about the frequency $f_{center} = (f_{out1} + f_{out2})/2$. When transmitting FSK, f_{center} is considered to be the effective carrier frequency and any receiver local oscillator (LO) should be set to the same f_{center} frequency ± the receiver's IF frequency (f_{IF}) for proper reception and demodulation.

For the case of low-side injection, the receiver LO would be set to $f_{LO} = f_{center} - f_{IF}$. Conversely, for high-side injection, the receiver LO would be set to $f_{LO} = f_{center} + f_{IF}$.

Since the DDS registers are static, preprogrammed values are retained during standby mode. This feature greatly reduces turnon time, reduces current consumption when coming out of standby mode, and enables very fast lock-times. The PLL lock-times ultimately determine when data can be transmitted or received.

phase-locked loop

The phase-locked loop (PLL) of the TRF4400 consists of a phase detector (PD) and a frequency acquisiton aid (FD) (including two charge pumps), an external loop filter, voltage-controlled oscillator (VCO), and a programmable fixed prescaler (N-divider) in the feedback loop (see Figure 7).

The PLL as implemented in the TRF4400 multiplies the DDS output frequency and further suppresses the unwanted spurious signals produced by the direct digital synthesizer.

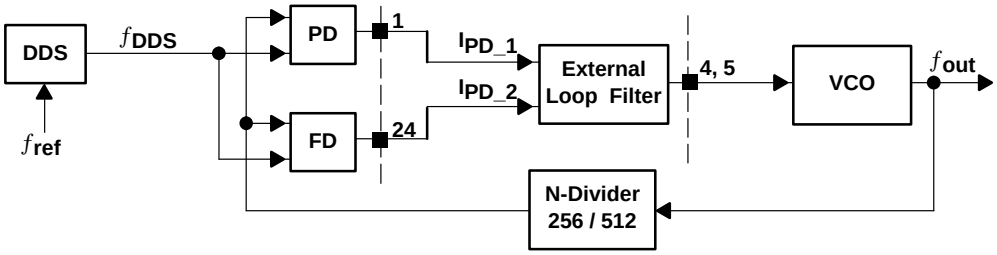


Figure 7. Basic PLL Structure

VCO

A modified Colpitts oscillator architecture with an external resonant circuit is used for the TRF4400. The internal bias current network adjusts the signal amplitude of the VCO. This allows a wide range of Q-factors (30…60) for the external tank circuit.

The VCO can be bypassed by applying an external RF signal at VCO_TANK2, terminal 5. To drive the internal PLL and power amplifier, a typical level of –10 dBm should be applied. When an external VCO is used, the x_VCO bit should be set to 0.

phase detector and charge pumps

The TRF4400 contains two charge pumps for locking to the desired frequency: one for coarse tuning of the frequency differences (called the frequency acquisition aid), and one for fine tuning of the phase differences (used in conjunction with the phase detector).

The XOR phase detector and charge pumps produce a mean output current that is proportional to the phase difference between the reference frequency and the VCO frequency divided by N; N = 256 or 512. The TRF4400 generates the current pulses I_{PD_1} during normal operation (PLL locked).

An additional slip detector and acquisition aid charge pump generates current pulses at terminal PD_OUT2 during the lock-in of the PLL. This charge pump is turned off when the PLL locks in order to reduce current consumption. The multiplication factor of the acquisition aid current I_{PD_2} can be programmed by three bits (APLL) in the C-word.

phase detector and charge pumps (continued)

The slip detector output, PD_OUT2, at terminal 24 should be connected directly to the loop-filter capacitor C_1, as shown in Figure 10. The nominal charge pump current I_0 is determined by the external resistor R_{PD}, connected to terminal 3, and can be calculated as follows:

$$I_0 = \frac{7\ V}{R_{PD}}$$

During normal operation (PLL locked), the acquisition aid charge pump is disabled and the maximum charge pump current I_{PD_1} is determined by the nominal value I_0 (see Figure 8).

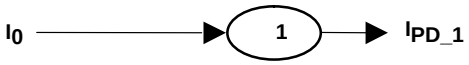


Figure 8. Normal Operation Charge Pump Current, I_{PD_1}

Each time the PLL is in an unlocked condition, the acquisition aid charge pump generates current pulses I_{PD_2}. The I_{PD_2} current pulses are APLL times larger than I_0 (see Figure 9).

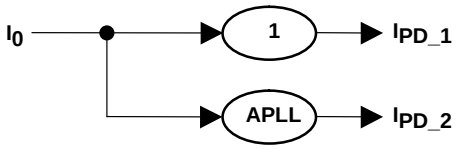


Figure 9. Acquisition Aid, I_{PD_2}, and Normal Operation, I_{PD_1}, Charge Pump Currents

programmable divider

The internal divider ratio, N, can be set to 256 or 512 via the C-word. Since a higher divider ratio adds additional noise within the multiplication loop, the lowest divider ratio possible for the target application should be used.

loop filter

Loop filter designs are a balance between lock-time, noise, and spurious suppression. For the TRF4400, common loop filter design rules can be used to determine an appropriate low-pass filter. Standard formulas can be used as a first approach to calculate a basic loop filter. Figure 10 illustrates a basic 3rd-order loop filter.

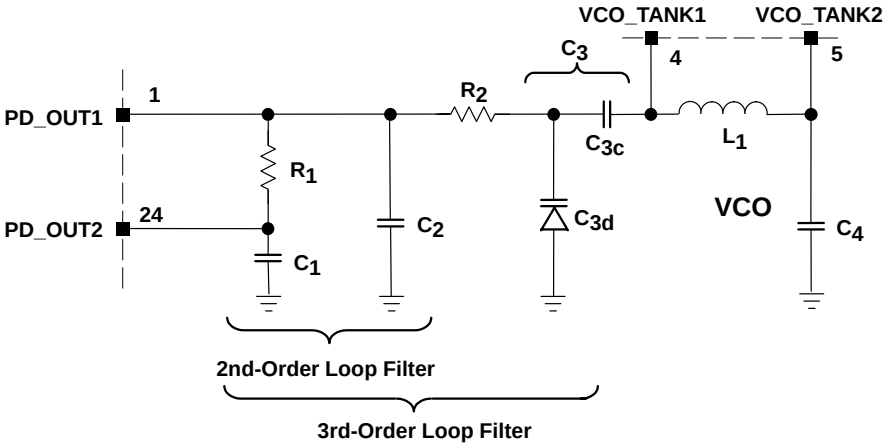


Figure 10. Basic 3rd-Order Loop Filter Structure

loop filter (continued)

For maximum suppression of the unwanted frequency components, the loop filter bandwidth should generally be made as narrow as possible. At the same time, the filter bandwidth has to be wide enough to allow for the 2-FSK modulation and appropriate lock-time. A detailed simulation of the phase-locked loop should be performed and later verified on PCB implementations.

power amplifier

The power amplifier (PA) can be programmed via two bits (P0 and P1 in the D-word) to provide varying output power levels. Several control loops are implemented internally to set the output power and to minimize the sensitivity of the power amplifier to temperature, load impedance, and power supply variations. The output stage of the PA usually operates in Class-C and enables easy impedance matching. PA_OUT, terminal 22, is an open collector output terminal.

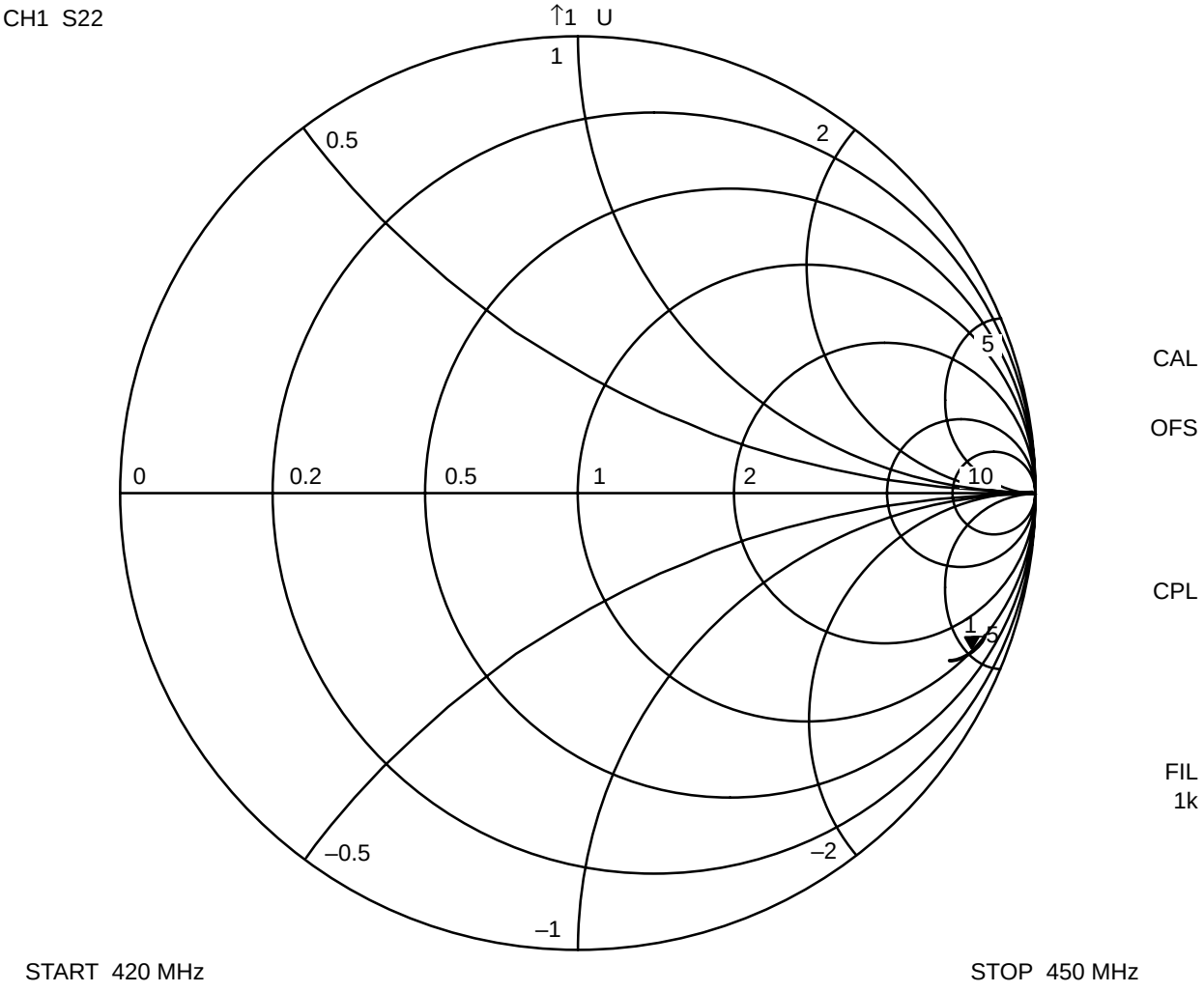


Figure 11. Power Amplifier Output Impedance (S22) at Device Terminal 22

PRINCIPLES OF OPERATION

serial control interface

A 3-wire unidirectional serial bus (CLOCK, DATA, STROBE) is used to program the TRF4400 (see Figure 12). The internal registers contain all user programmable variables including the DDS frequency setting registers, as well as all control registers.

At each rising edge of the CLOCK signal, the logic value on the DATA terminal is written into a 24-bit shift register. Setting the STROBE terminal high loads the programmed information into the selected latch. While the STROBE signal is high, the DATA and CLOCK lines must be low (see Figure 2). Since the CLOCK and STROBE signals are asynchronous, care should be taken to ensure the signals remain free of glitches and noise.

As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. Due to the static CMOS design, the serial interface consumes virtually no current and it can be programmed in active as well as in standby mode.

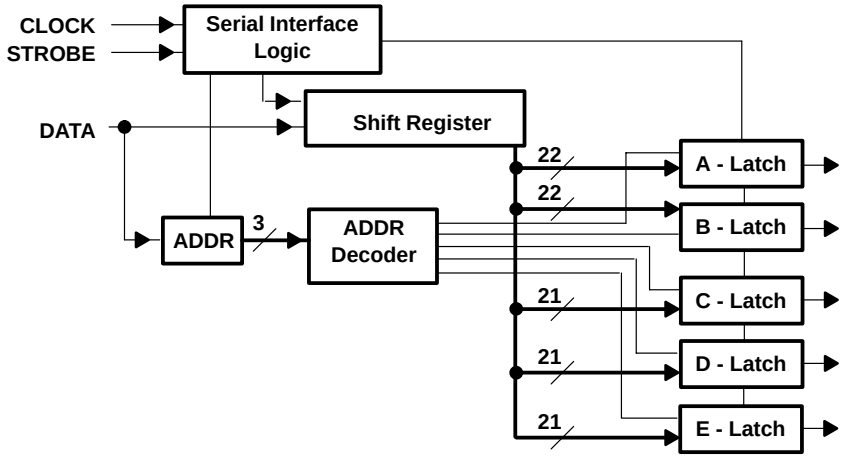


Figure 12. Serial Interface Block Diagram

The control words are 24 bits in length. The first incoming bit functions as the most significant bit (MSB).

To fully program the TRF4400, four 24-bit words must be sent: the A-, B-, C-, and D-words. If individual bits within a word are to be changed, then it is sufficient to program only the appropriate 24-bit word.

Figure 13 shows the definition of the control words. Tables 1, 2, and 3 describe the function of each parameter.

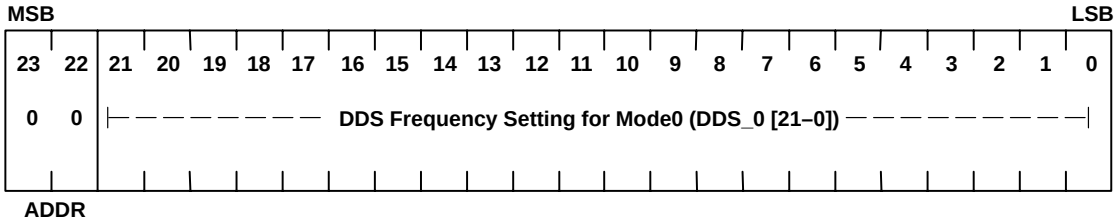
The E-Latch, addressed by an ADDR equal to 111, is reserved for test purposes and should not be used. Inadvertently addressing the E-Latch activates the test modes of the TRF4400.

If the test mode has been inadvertently activated, it can only be exited by switching V_{CC} on and off or by clearing the E-Latch. The E-Latch can be cleared by addressing it and resetting its entire contents by programming 1110 0000 0000 0000 0000 0000.

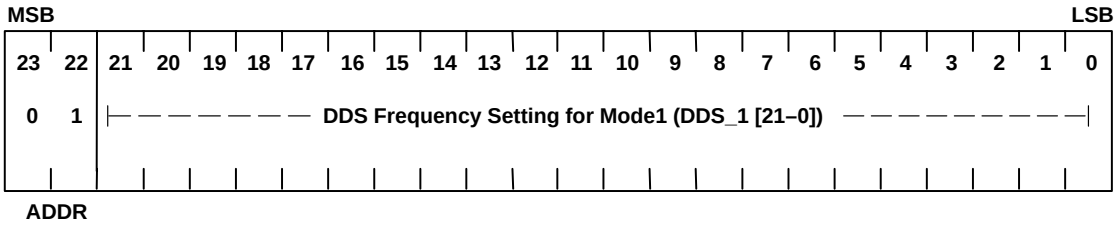
As part of a proper power-up sequence, it is recommended to clear the E-Latch each time V_{CC} is applied before starting further operations with the TRF4400.

PRINCIPLES OF OPERATION

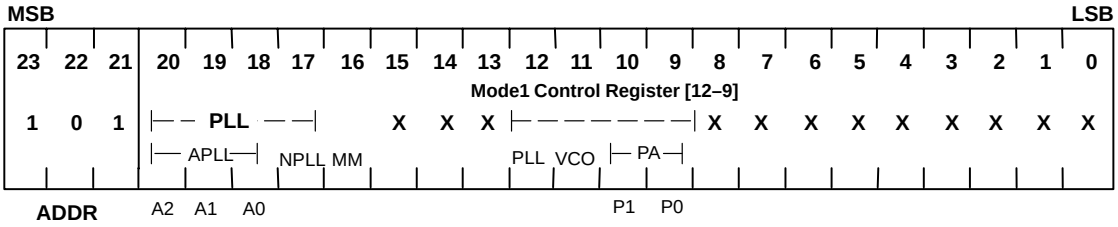
A-Word (Programming of DDS_0)



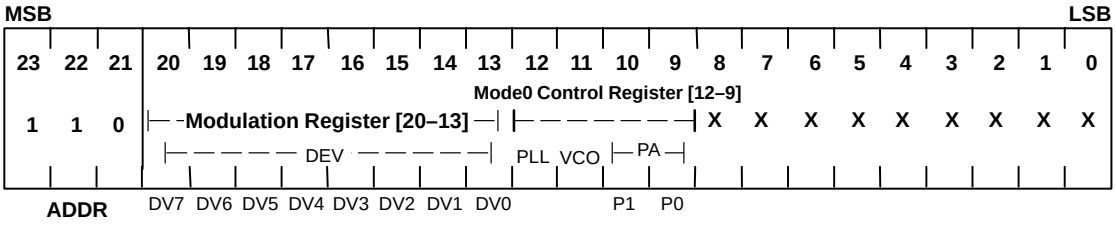
B-Word (Programming of DDS_1)



C-Word (Control Register for PLL, Data Slicer, and Mode1 Settings)



D-Word (Control Register for Modulation and Mode0 Settings)



NOTE: Start programming with MSB and ensure that the CLOCK and DATA lines are low during the rising edge of the strobe signal.

Figure 13. Serial Control Word Format

PRINCIPLES OF OPERATION

Table 1. Mode0 Control Register Description (D-Word)

SYMBOL	BIT LOCATION	NUMBER OF BITS	DESCRIPTION	INITIAL SETTINGS AFTER POWER UP	
				DEFAULT STATE	DEFAULT VALUE
0_PA	[10–9]	2	Power amplifier mode **P1 P0** 0 0 = disabled 0 1 = 10 dB attenuation, enable modulation via TX_DATA 1 0 = 20 dB attenuation, enable modulation via TX_DATA 1 1 = 0 dB attenuation, enable modulation via TX_DATA	Disabled	00b
0_VCO	[11]	1	During operation, this bit should always be enabled (1 = enabled), unless an external VCO is used.	Disabled	0b
0_PLL	[12]	1	Enable PLL (DDS system, VCO, RF divider, phase comparator and charge pump) 1 = enabled 0 = disabled	Disabled	0b

Table 2. Mode1 Control Register Description (C-Word)

SYMBOL	BIT LOCATION	NUMBER OF BITS	DESCRIPTION	INITIAL SETTINGS AFTER POWER UP	
				DEFAULT STATE	DEFAULT VALUE
1_PA	[10–9]	2	Power amplifier mode **P1 P0** 0 0 = disabled 0 1 = 10 dB attenuation, enable modulation via TX_DATA 1 0 = 20 dB attenuation, enable modulation via TX_DATA 1 1 = 0 dB attenuation, enable modulation via TX_DATA	Disabled	00b
1_VCO	[11]	1	During operation, this bit should always be enabled (1 = enabled), unless an external VCO is used.	Disabled	0b
1_PLL	[12]	1	Enable PLL (DDS system, VCO, RF divider, phase comparator and charge pump) 1 = enabled 0 = disabled	Disabled	0b

PRINCIPLES OF OPERATION

Table 3. Miscellaneous Control Register Description

SYMBOL	WORD	BIT LOCATION	NUMBER OF BITS	DESCRIPTION	INITIAL SETTINGS AFTER POWER UP	
					DEFAULT STATE	DEFAULT VALUE
DDS_0	A-word	[21–0]	22	DDS frequency setting in Mode0	0	All 0s
DDS_1	B-word	[21–0]	22	DDS frequency setting in Mode1	0	All 0s
DEV	D-word	[20–13]	8	FSK frequency deviation register	0	All 0s
APLL	C-word	[20–18]	3	Acceleration factor for the frequency acquisition aid charge pump A2 A1 A0 0 0 0 = 1 0 0 1 = 20 0 1 0 = 40 0 1 1 = 60 ⋮ 1 1 1 = 140	0	000b
NPLL	C-word	[17]	1	PLL divider ratio 0 = divide by 256 1 = divide by 512	256	0b
MM	C-word	[16]	1	Modulation mode select. Sets the behavior of pin TX_DATA to FSK data input. 0 = FSK/FM 1 = do not use	FSK mode	0b

operating modes

Tables 4 and 5 illustrate operating modes and transmit frequencies as set by the $\overline{\text{STDBY}}$, MODE, and TX_DATA terminals used in conjunction with the DDS frequency settings.

Table 4. Transmitting Data in FSK Mode (MM bit set to 0)

TERMINAL			TRANSMIT FREQUENCY
$\overline{\text{STDBY}}$	MODE	TX_DATA	
1	0	0	$f_{out} = f_{ref} \times N \times (DDS\_0)/2^{24}$
1	0	1	$f_{out} = f_{ref} \times N \times (DDS\_0 + 4 \times DEV)/2^{24}$
1	1	0	$f_{out} = f_{ref} \times N \times (DDS\_1)/2^{24}$
1	1	1	$f_{out} = f_{ref} \times N \times (DDS\_1 + 4 \times dev)/2^{24}$

PRINCIPLES OF OPERATION

operating modes (continued)

Table 5. Operating Mode Per $\overline{\text{STDBY}}$ Terminal

$\overline{\text{STDBY}}$	OPERATING MODE
0	Standby/programming mode – Power down of all blocks
1	Operating mode and programming mode

Two independent operating modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings by toggling the MODE terminal. Each mode can be viewed as a bank of configuration registers which store the frequency settings and the enable/disable settings for each functional block of the TRF4400. The MODE terminal is then used to asynchronously switch between Mode0 and Mode1 as shown in Figure 14. Table 6 shows several examples of operating sequences.

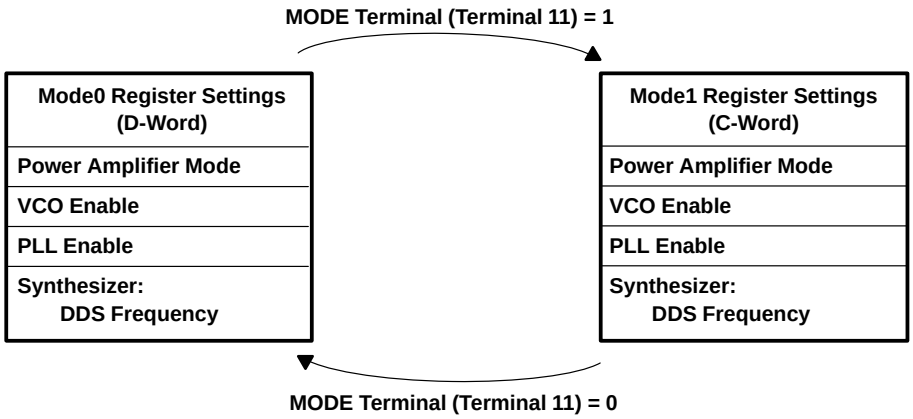


Figure 14. Interaction Between MODE Terminal and Preprogrammed Mode0 and Mode1 Control Registers

Table 6. Operating Mode Examples

FUNCTION/DESCRIPTION	MODE0	MODE1
Transmit on two different frequencies	Transmit on frequency 0	Transmit on frequency 1
Emulate FSK transmit operation using the MODE terminal for wideband FSK	Transmit on frequency 0	Transmit on frequency 0 + deviation

APPLICATION INFORMATION

A typical application schematic for an FSK system operating in the 433-MHz ISM band as shown in Figure 15.

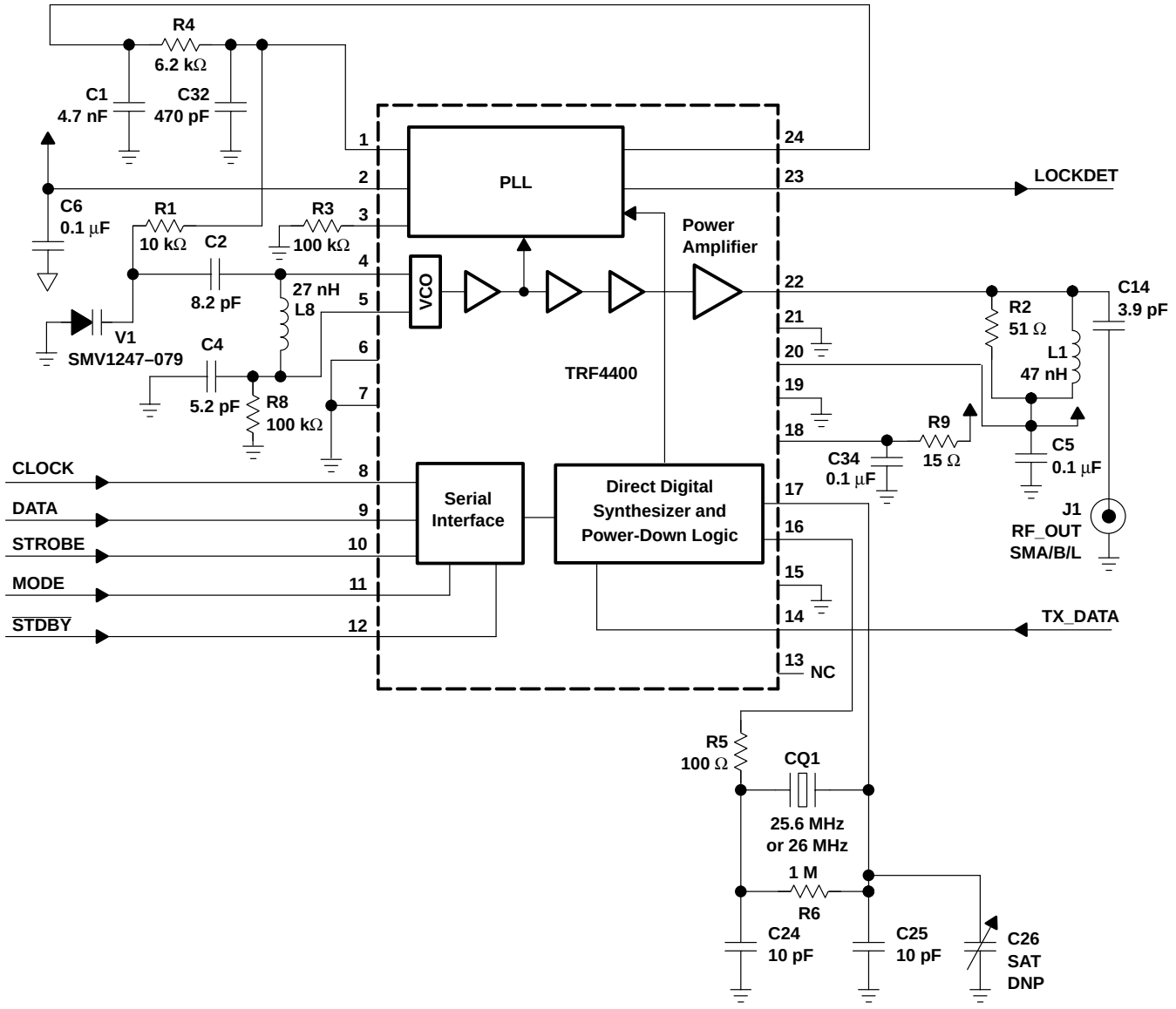


Figure 15. Typical Application Schematic for 433-MHz ISM Band

APPLICATION INFORMATION

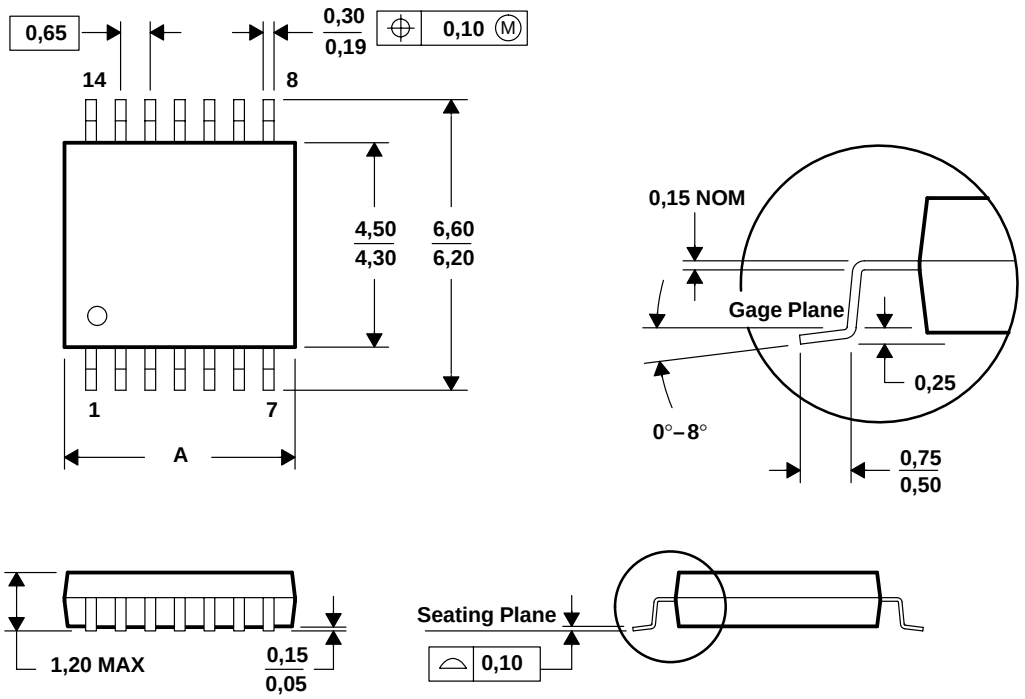
external component list for Figure 15 (5% tolerance unless otherwise noted)

DESIGNATOR	DESCRIPTION (SIZE)	VALUE	MANUFACTURER	PART NUMBER/COMMENTS
C1	Capacitor	4.7 nF		
C2	Capacitor	8.2 pF		
C4	Capacitor	5.2 pF		
C5	Capacitor	0.1 μF		
C6	Capacitor	0.1 μF		
C14	Capacitor	3.9 pF		
C24	Capacitor	10 pF		
C25	Capacitor	10 pF		
C26	Capacitor			Select at test (SAT), Do not place (DNP)
C32	Capacitor	470 pF		
C34	Capacitor	0.1 μF		
L1	Coil	47 nH	Murata	LQN21A6N8D04
L8	Coil	27 nH	Murata	LQW1608
R1	Resistor	10 kΩ		
R2	Resistor	51 Ω		
R3	Resistor	100 kΩ		
R4	Resistor	6.2 kΩ		
R5	Resistor	100 Ω		
R6	Resistor	1 MΩ		
R8	Resistor	100 kΩ		
R9	Resistor	15 Ω		
V1	Varactor diode	SMV1247-079	Alpha Industries	
CQ1	Crystal	25.6 MHz or 26 MHz	ICM (International Crystal Manufacturing, Incorporated)	865842: 25.6 MHz 865850: 26 MHz

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265