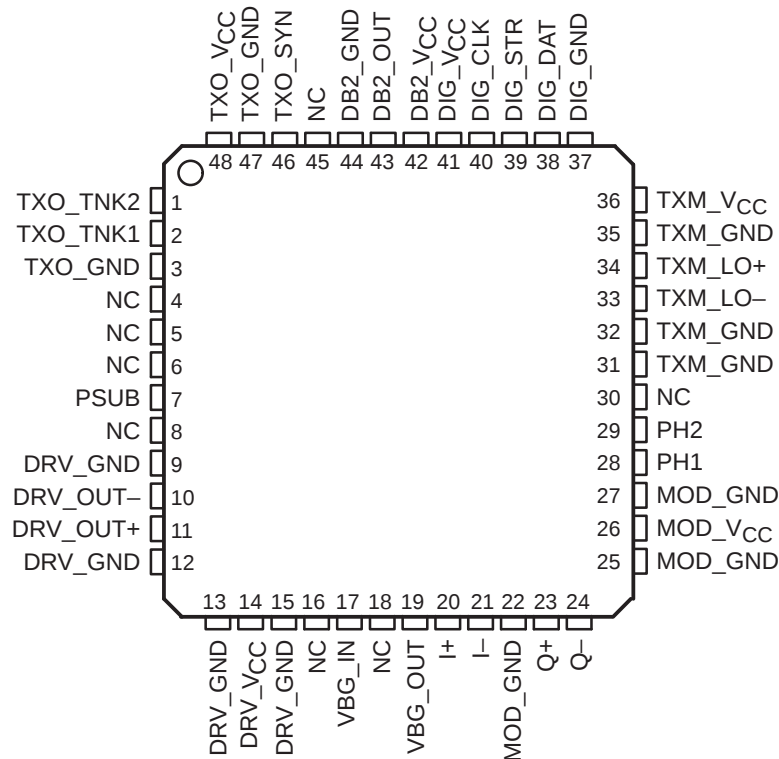


- Modulation and Upconversion from I/Q Baseband to RF on Single Chip
- Designed for GSM Portable Cellular Telephones
- Internal VCO and SSB Mixer for Transmit Carrier Generation
- Internal RF Filter for Minimal External Parts
- Power Amplifier Driver
- Independent Power-Up/-Down Functions
- 3.75-V Operation
- Low Current Consumption
- Serial Data Interface
- 48-Pin Plastic Quad Flatpack (PFB)

description

The TRF3520 radio frequency (RF) modulator/amplifier is a single-chip RF integrated circuit (IC) suitable for 900-MHz wireless global system for mobile communications (GSM) applications. It combines a direct conversion RF in-phase/quadrature-phase (I/Q) modulator, a single-sideband suppressed carrier (SSB) mixer, an RF filter, a power amplifier (PA) driver, a buffered voltage-controlled oscillator (VCO), and a serial interface into one small package. Very few external components are required. During idle operation, the individual functional elements may be selectively placed in standby mode for minimum power consumption.

PFB PACKAGE
(TOP VIEW)



NC – No internal connection



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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The TX1 transmitter block diagram illustrates the signal path from baseband inputs to the final output. The I/Q Modulator (dashed box) takes baseband inputs I+, I-, Q+, and Q- (pins 20, 21, 23, 24) and LO signals TXM_LO+ and TXM_LO- (pins 34, 33). It uses 0° and 90° phase shifters and mixers to generate the modulated signals. These signals pass through a Summing Junction (Σ) and a Power Amplifier Driver (pin 32) to produce DRV_OUT+ and DRV_OUT- (pins 11, 10). The output is then filtered by a Band-Pass Filter (BPF) and a Single-Sideband Transmit Mixer (pin 31) before being buffered (pin 30). The TXO_TNK1 and TXO_TNK2 pins (1, 2) are connected to an External Tank. The Transmit IF VCO (pin 45) is connected to a Buffer (pin 46) and a Divider (pin 43). The Divider output is connected to a Low-Pass Filter (LPF) and a Divide-by-Two Output (DB2_OUT). The Serial Interface (pins 41, 40, 39, 38, 37) provides control signals: DIG_VCC, DIG_CLK, DIG_STR, DIG_DAT, and DIG_GND.

The transmit intermediate frequency (IF) VCO generates a CW signal in the 200-MHz range. The IF VCO frequency is controlled by applying voltage to the required external tank varactors. Through on-chip buffers, the transmit IF VCO output is sent to the SSB transmit mixer and divide-by-two functional blocks, as well as to an external synthesizer where the transmit IF VCO frequency is controlled and phase locked. The error signal generated by the synthesizer is sent to the transmit IF VCO varactors' tuning port, completing the phase-locked loop (PLL) function. The VCO is characterized for operation in the 74-MHz to 494-MHz range.

This functional block halves the IF VCO frequency and provides a buffered amplitude-limited and low-pass filtered signal, which can become the LO signal for the TRF1020 GSM Receiver IC second down-conversion stage.

The SSB Tx mixer combines an external LO signal with the on-chip transmit IF VCO and performs a down-conversion function. The SSB Tx mixer suppresses the undesired upper sideband signal that is typically generated under the normal mixing process. An internal band-pass filter at the SSB Tx mixer output further reduces the undesired sideband and any spurious signals. This function eliminates the use of any external filtering. The LO is characterized for operation in the 990-MHz to 1400-MHz range.

The modulator provides direct I/Q modulation from baseband to RF. The differential baseband I/Q input signals also provide DC bias to the modulator. A nominal DC voltage of 1.35 V at the I and Q ports is required. Other types of complex I/Q modulations are possible with the TRF3520, but the device is optimized to meet GSM requirements.

power amplifier driver output

The I/Q modulator output is fed to the power amplifier driver, which is a high-gain, low-distortion, fixed gain amplifier. Its differential output can be converted to single-ended by a simple LC impedance-matching network and a 4:1 balun.

serial control interface

The serial control interface provides power-up and power-down capabilities for each of the functional blocks described in the previous paragraphs.

The TRF3520 device register is manipulated using a synchronous serial data port. The timing relationships are defined in Figure 1. One 17-bit word is clocked into a temporary holding register with the least significant bit clocked first. The operation register is loaded with the new data residing in the temporary registers using the rising edge of the strobe input.

The format of the control word is described in Table 1. Bits zero through two are reserved for future use. Bits three through seven are power conservation bits. Bits eight through 16 are reserved.

Table 1. Control Word Bit Assignments

BIT	FUNCTION	FUNCTIONAL IF
0	Reserved	—
1	Reserved	—
2	Reserved	—
3	Transmit oscillator and buffer amplifiers	1
4	Transmit mixer, LO buffer amplifier	1
5	Modulator	1
6	PA driver amplifier	1
7	Divide-by-two and limiter	1
8	Reserved	—
9	Reserved	—
10	Reserved	—
11	Reserved	—
12	Reserved	—
13	Reserved	—
14	Reserved	—
15	Reserved	—
16	Reserved	—

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Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DB2_GND	44	–	Divide-by-two circuitry ground
DB2_OUT	43	O	Divide-by-two frequency output
DB2_VCC	42	–	Divide-by-two circuitry bias supply
DIG_CLK	40	I	Digital clock input
DIG_DAT	38	I	Digital serial data input
DIG_GND	37	–	Digital ground
DIG_STR	39	I	Data strobe
DIG_VCC	41	–	Digital supply
DRV_GND	9, 12, 13, 15		PA driver ground
DRV_OUT+	11	O	PA driver noninverting output
DRV_OUT–	10	O	PA driver inverting output
DRV_VCC	14	–	PA driver bias supply
MOD_GND	22, 25, 27		Modulator ground
I+	20	I	Noninverting in-phase input
I–	21	I	Inverting in-phase input
Q+	23	I	Noninverting quadrature input
Q–	24	I	Inverting quadrature input
MOD_VCC	26	–	Modulator supply
NC	4, 5, 6, 8, 16, 18, 30, 45		No internal connection
PSUB	7		
TXO_GND	3, 47	–	Transmit VCO ground
TXO_SYN	46	O	Buffered transmit VCO output
TXO_TNK1	2	–	Transmit VCO tank connection 1
TXO_TNK2	1	–	Transmit VCO tank connection 2
TXO_VCC	48	–	Transmit VCO supply
TXM_GND	31	–	Transmit mixer ground
TXM_GND	32	–	Transmit mixer ground
TXM_GND	35	–	Transmit mixer ground
TXM_LO+	34	I	Transmit mixer LO noninverting input
TXM_LO–	33	I	Transmit mixer LO inverting input
TXM_VCC	36	–	Transmit mixer supply
PH1	28	–	Phase adjustment resistor 1
PH2	29	–	Phase adjustment resistor 2
VBG_IN	17		Band gap input
VBG_OUT	19		Band gap output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range: V_{CC}	–0.3 V to 5.5 V
Input voltage to any other pin: V_{IN}	–0.3 V to ($V_{CC} + 0.3$) V
Power dissipation, $T_A = 25^\circ\text{C}$, 48-pin PQFP	600 mW
Maximum operating junction temperature: T_{Jmax}	150°C
Operating ambient temperature range	–40°C to 85 °C
Storage temperature range	–65°C to 150 °C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	MAX	UNIT
High-level input voltage, V_{IH}	2.0	V_{CC}	V
Low-level input voltage, V_{IL}	–0.3	0.8	V
Supply voltage, V_{CC}	3.6	3.9	V
Operating free-air temperature, T_A	–40	85	°C

typical power consumption at 3.75 V (continuous operation)

MODULE	OPERATING CURRENT	STANDBY CURRENT	OPERATING POWER	STANDBY POWER
Transmit oscillator	8 mA	<10 μA	30 mW	<38 μW
Transmit mixer (SSBM)	50 mA	<10 μA	188 mW	<38 μW
Modulator	18 mA			
PA driver amplifier	45 mA	<10 μA	169 mW	<38 μW
Divide-by-two + LPF	10 mA	<10 μA	38 mW	<38 μW
Control logic	50 μA			
Total	131 mA	<50 μA	492 mW	<152 μW

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

transmit IF VCO $V_{CC} = 3.75$ V, $T_A = 25^\circ\text{C}$, $Z_O = 100\ \Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		141	194	247	MHz
Output power (See Note 1)	$Z_{load} = 100\ \Omega$	-20	-15		dBm
Phase noise	200-kHz offset		-110		dBc/Hz
DC current	Active mode		8		mA
	Standby mode			10	μA
Power-up time (See Note 2)			10		μs
Power-down time			10		μs

NOTES: 1. Measured at buffer output pin labeled TXO_SYN
 2. Includes oscillator starting time. This time is measured starting at strobe transition to high; there is additional time after a reset, i.e., applying V_{CC} to the circuit.



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transmit mixer, I/Q modulator and PA driver $P_{LO} = -10$ dBm, $V_{CC} = 3.75$ V, $T_A = 25^\circ\text{C}$, $Z_O = 50\ \Omega$ (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LO input frequency range			1070		1110	MHz
LO input power level			-12	-10	-8	dBm
PA driver RF output			880		915	MHz
PA driver RF output power level		See Note 7		6		dBm
Unwanted TX mixer sideband suppression at 1462 to 1497 MHz		LO = 1074 to 1109 MHz	35	45		dBc
DSB IM suppression	Third order	See Note 3	20			dBc
Carrier suppression		See Note 4	30	35		dBc
Sideband suppression		See Note 4	35	45		dBc
Modulator and PA driver spurious outputs	100 kHz to 500 MHz	See Note 5		35		dBc
	500 to 850 MHz	See Note 5	30	32		
	880 to 915 MHz	Offset ≥ 600 kHz (see Note 5)		69		
	925 to 935 MHz	See Note 5		85		
	935 to 960 MHz	See Note 5		82		
	960 to 1000 MHz	See Note 5		49		
	1000 to 1350 MHz	See Note 5	30	39		
	1350 to 1500 MHz	See Note 5		38		
	1500 to 1805 MHz	See Note 5		23		
	1805 to 1880 MHz	See Note 5		54		
	1880 to 12000 MHz	See Note 5		36		
I/Q input voltage range (differential)		Each differential line	0.0		1.80	V _{pp}
I/Q offset				5		mV
I/Q common mode voltage		See Note 6	1.25	1.35	1.45	V
I/Q input impedance (differential)		See Note 8	10			k Ω
I/Q input impedance (single-ended)		See Note 8	10			k Ω
I/Q input frequency range			0		2	MHz
Power-up time				10		μs
Power-down time				10		μs
PA driver output broadband noise		± 10 MHz, PA driver output ± 6 dBm		-131		dBc/Hz

- NOTES:
- $F_{out} = 880$ to 915 MHz, $V_{I/Q} = 1.40$ V_{pp}, 67.7 kHz sine wave. I & Q in-phase. Intermodulation suppression with respect to desired sideband level
 - $F_{out} = 880$ to 915 MHz, $V_{I/Q} = 1.40$ V_{pp}, 67.7 kHz sine wave. I & Q in quadrature-phase. Carrier and undesired sideband suppression with respect to desired sideband level
 - $V_{I/Q} = 1.40$ V_{pp}, 67.7 kHz sinewave. I & Q in quadrature-phase.
 - The TCM4400 provides for a common-mode voltage of 1.35 ± 0.1 V or $V_{CC}/2$ (software selectable)
 - Includes 1-dB loss associated with external balun
 - Specified by design.



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transmit mixer, I/Q modulator and PA driver $P_{LO} = -10$ dBm, $V_{CC} = 3.75$ V, $T_A = 25^\circ\text{C}$, $Z_O = 50\ \Omega$ (unless otherwise specified) (continued)

divide-by-two $V_{CC} = 3.75$ V, $T_A = 25^\circ\text{C}$, $Z_O = 50\ \Omega$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input frequency range		141	194	247	MHz
Output frequency		$F_{DB2_IN}/2$			
Output power (see Note 8)	$Z_{load} = 100\ \Omega$	-25	-20	-10	dBm
DC current	Active mode	10			mA
DC current	Standby mode	10			μA

NOTE 9: Measured at buffer output pin labeled DB2_OUT

serial interface timing requirements with $V_{CC} = 3.75$ V, $T_A = 25^\circ\text{C}$, $Z_O = 50\ \Omega$ (unless otherwise specified) (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_i CLOCK, DATA and STROBE input resistance		10			k Ω
f_{clock} CLOCK frequency		0		20	MHz
$t_{(r)}\ t_{(f)}$ CLOCK input rise and fall time				8	ns
$t_{w(High)}$ Pulse duration, CLOCK high		20			ns
$t_{w(Low)}$ Pulse duration, CLOCK low		20			ns
t_{su}	Data setup time before CLOCK high	20			ns
	Strobe setup time before CLOCK high	20			ns
t_h	Data hold time after CLOCK high	20			ns
	Strobe hold time after CLOCK high	20			ns
$t_{w(pulse)}$ Strobe pulse width duration		$\frac{2}{REF_IN}$			ns

PARAMETER MEASUREMENT INFORMATION

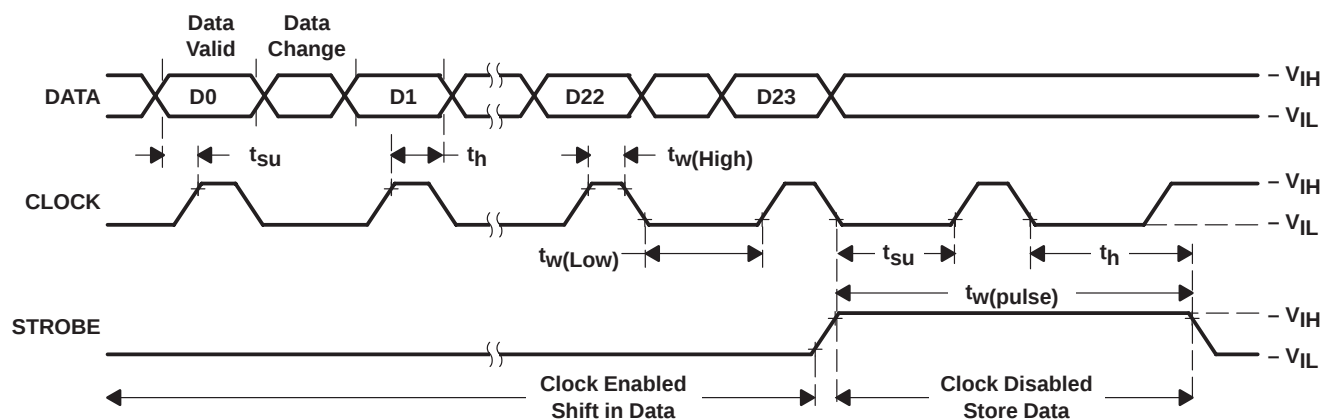


Figure 1. TRF3520 Timing Relationships

TYPICAL CHARACTERISTICS

Typical GSM RF modulator characteristics were evaluated using a VCO frequency of 194 MHz and LO frequency of 1094 MHz. The range of operation is specified in the document and is therefore customer specific.

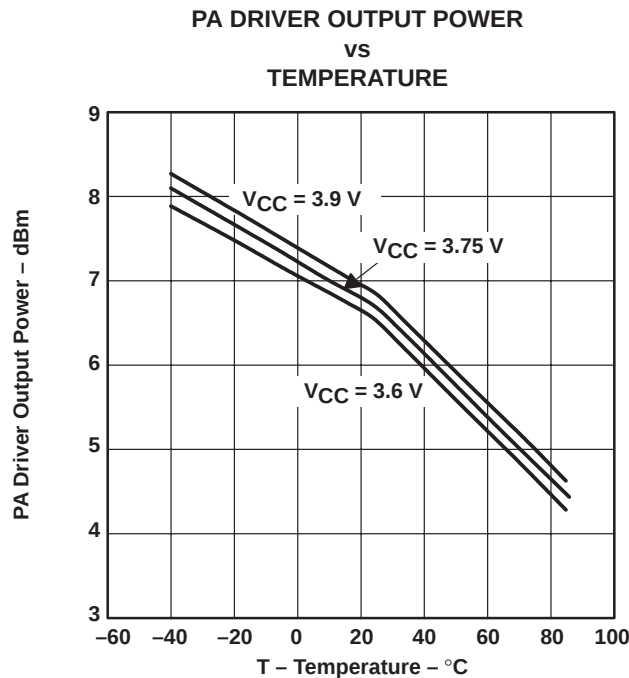


Figure 2

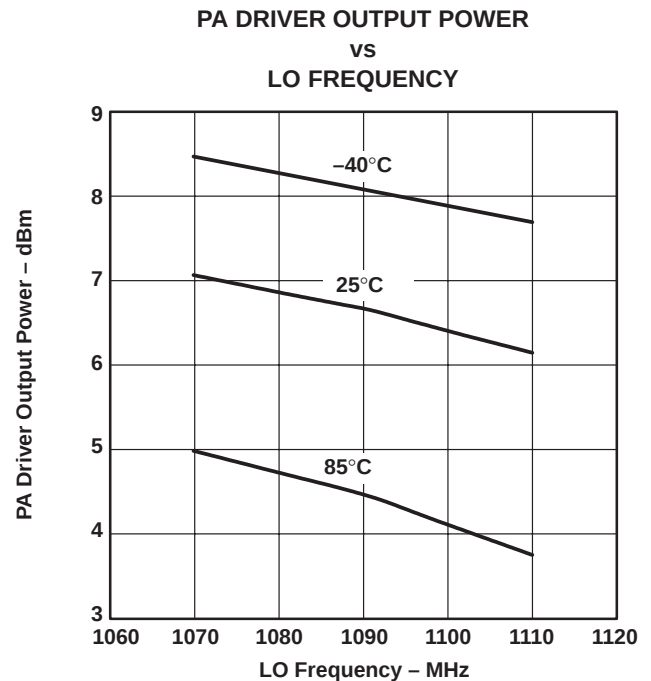


Figure 3

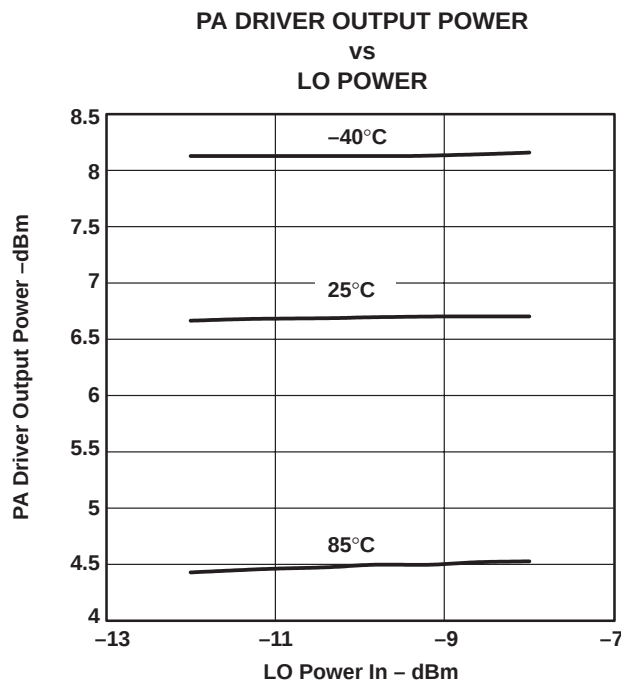


Figure 4

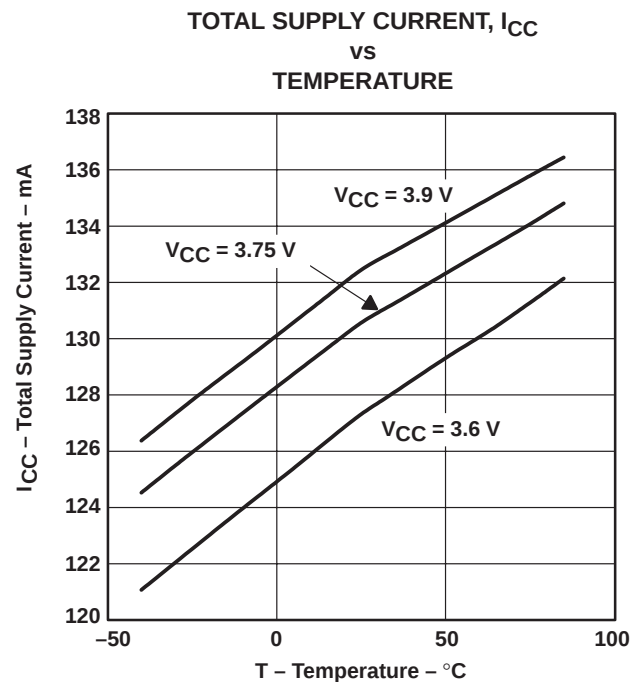


Figure 5

TYPICAL CHARACTERISTICS

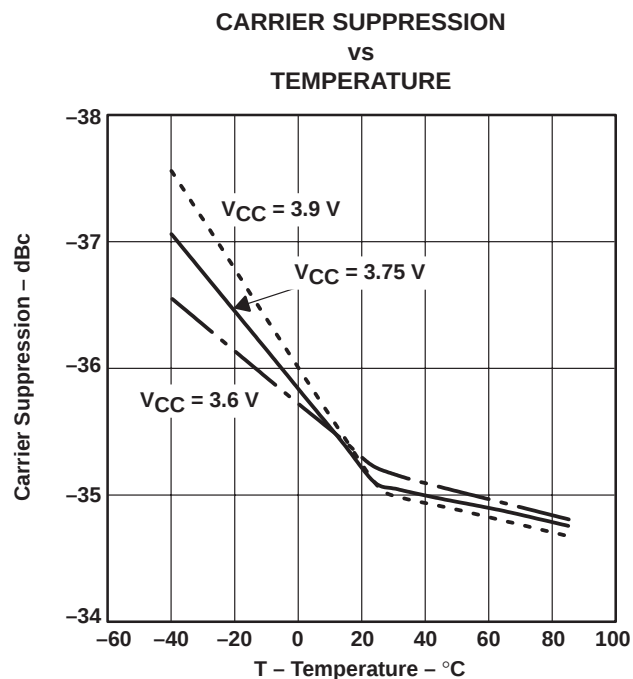


Figure 6

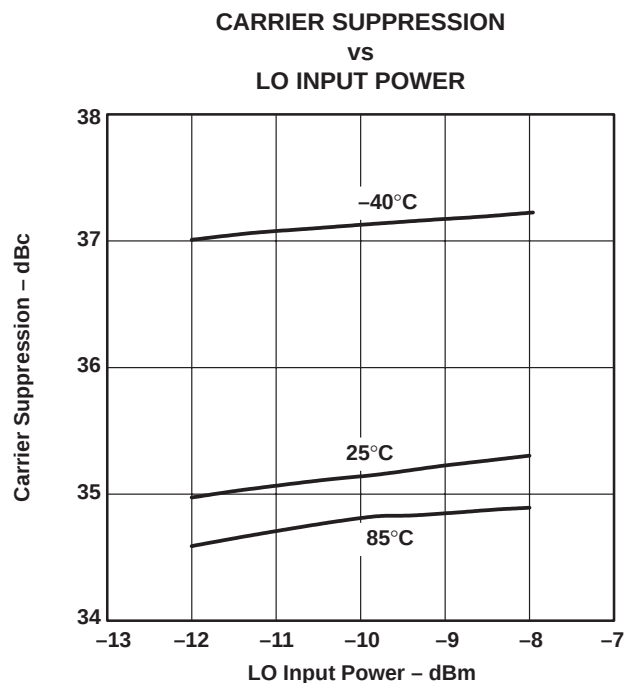


Figure 7

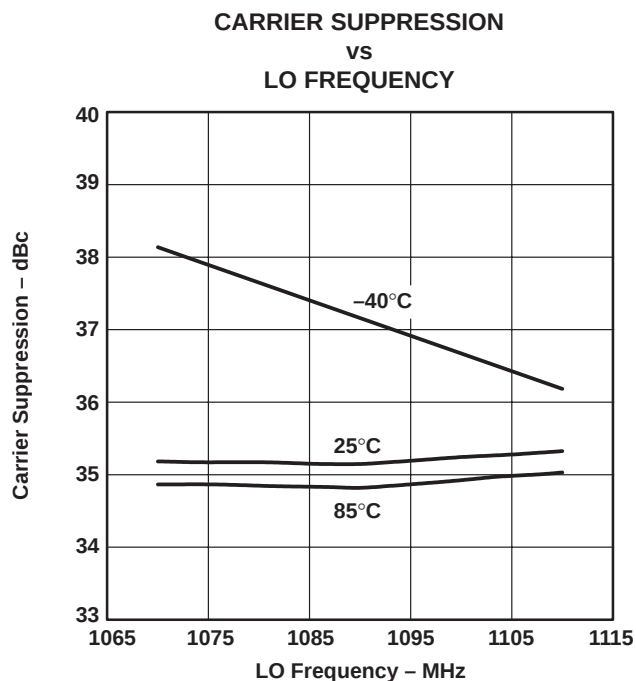


Figure 8

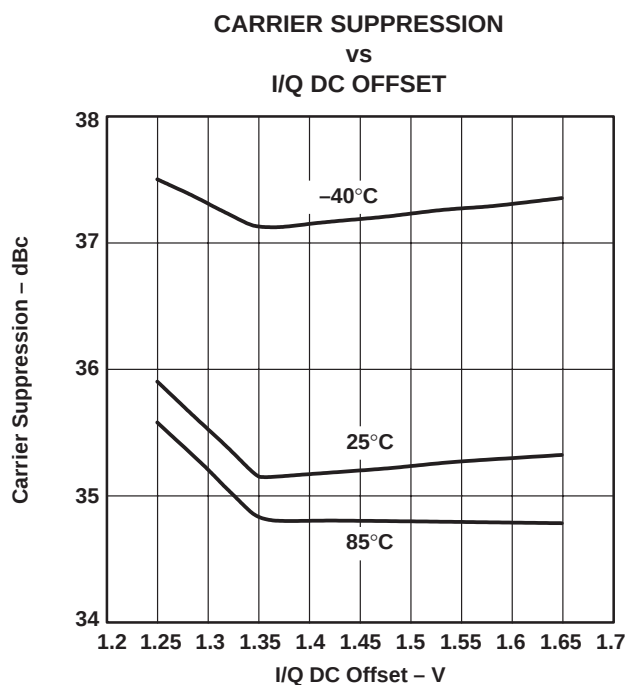


Figure 9

TYPICAL CHARACTERISTICS

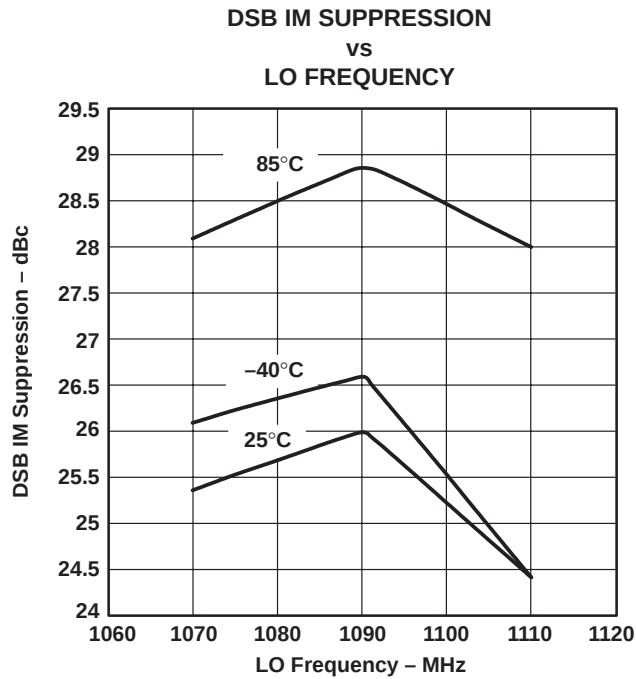


Figure 10

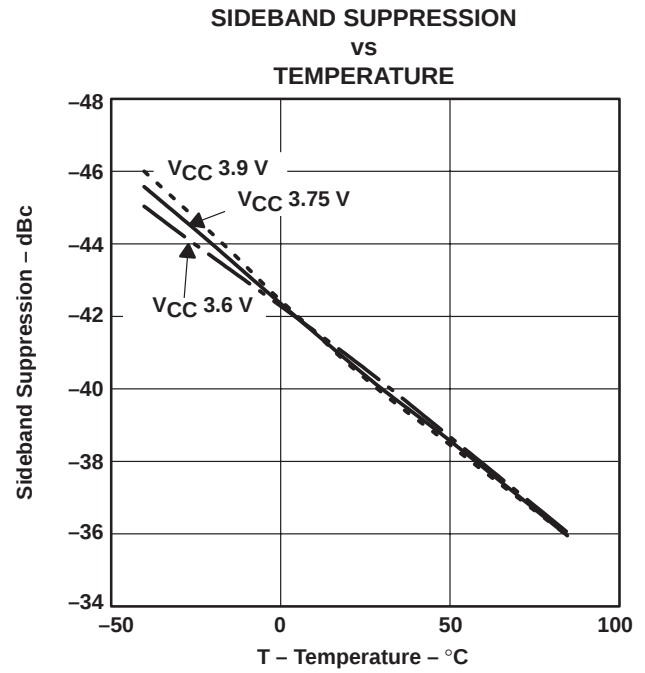


Figure 11

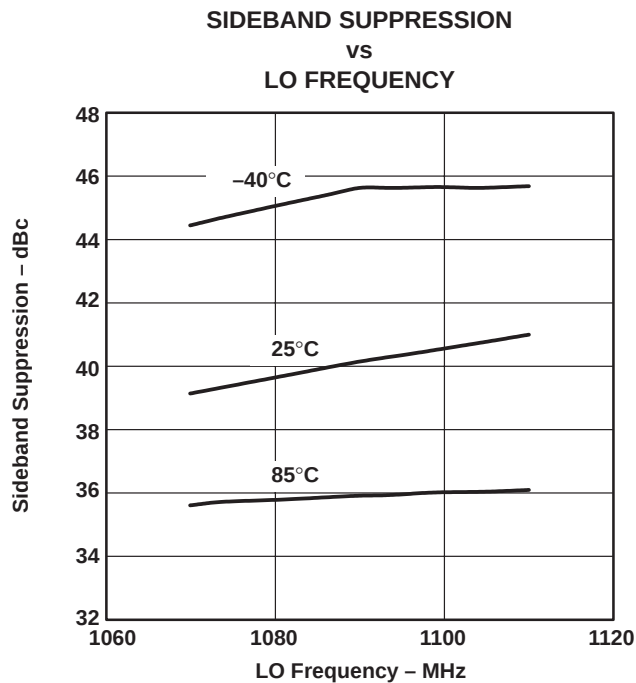


Figure 12

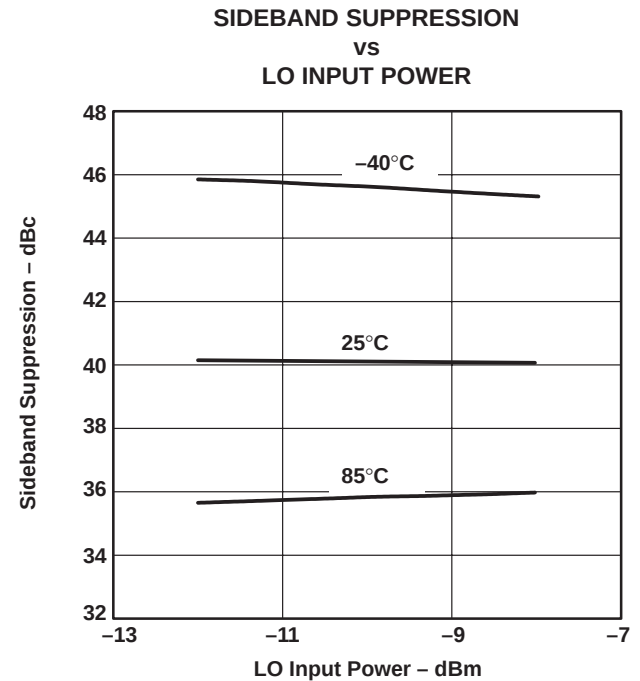


Figure 13

TYPICAL CHARACTERISTICS

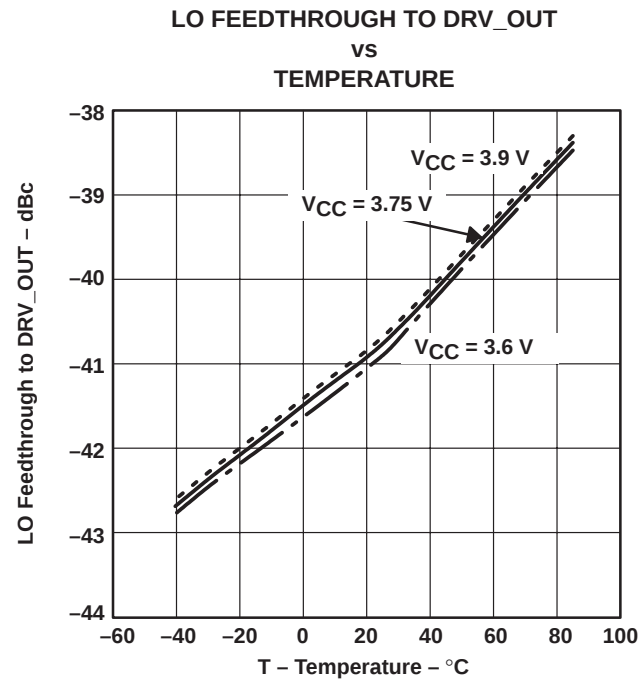


Figure 14

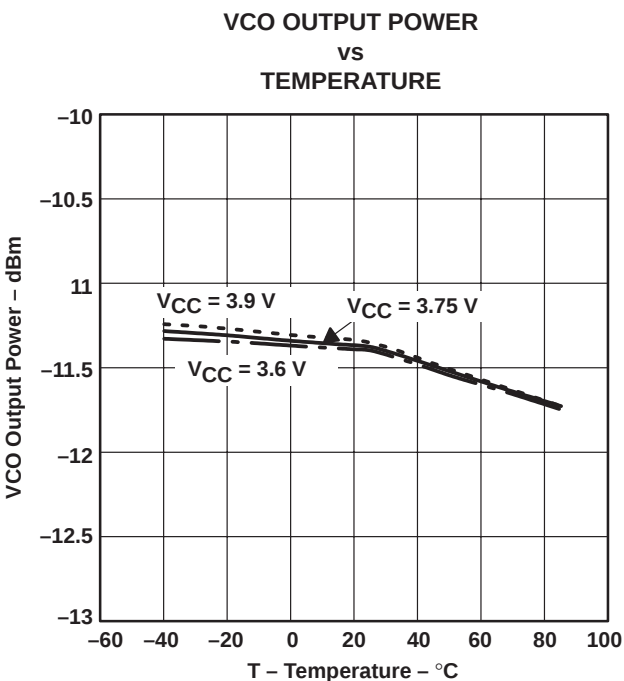


Figure 15

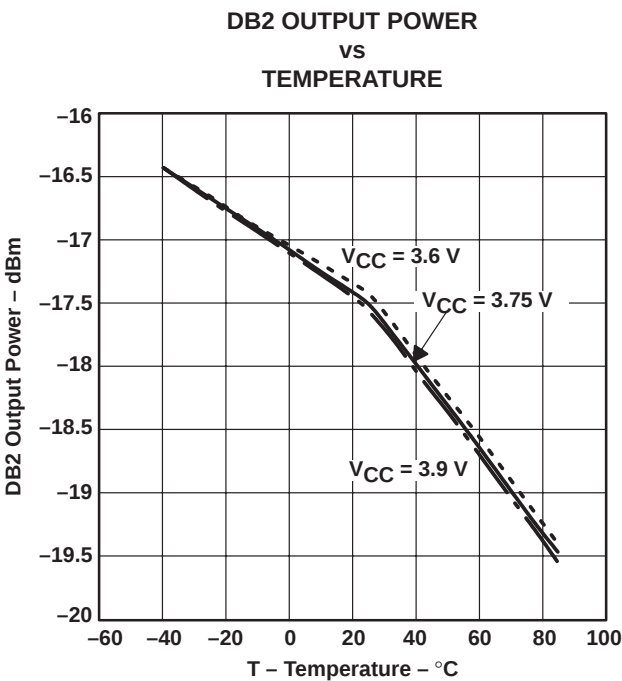


Figure 16

APPLICATION INFORMATION

Table 2. TRF3520 Application Board Parts List

DESIGNATORS	DESCRIPTION	VALUE	QTY	SIZE	MANUFACTURER	MANUFACTURER P/N
C1, 2, 3, 15	Capacitor	10 pF	4	0603	Murata	GRM39COG Series
C4, 5, 8, 10, 12, 14, 19, 32, 36, 37	Capacitor	.01 μ F	10	0603	Murata	GRM39COG Series
C6, 23, 26, 30, 35	Capacitor	1000 pF	5	0603	Murata	GRMX7R Series
C7, 9, 11, 25, 28, 29, 33, 34, 38	Capacitor	100 pF	9	0603	Murata	GRM1R8X7R Series
C13, 31	Capacitor	10 μ F	2	C	Panasonic	ECS–T1DC106R
C16	Capacitor	22 pF	1	0603	Murata	GRM39COG Series
C17	Capacitor	8 pF	1	0603	Murata	GRM39COG Series
C18	Capacitor	7 pF	1	0603	Murata	GRM39COG Series
C20, 22	Capacitor	15 pF	2	0603	Murata	GRM39COG Series
C21	Capacitor	4.7 pF	1	0603	Murata	GRM39COG Series
C24, 27	Capacitor	1.8 pF	2	0603	Murata	GRM39COG Series
C39	Capacitor	1.5 pF	1	0603	Murata	GRM39COG Series
L1	Inductor	100 nH	1	0603	Toko	LL1608–FR10K
L2	Inductor	47 nH	1	0603	Toko	LL1608–F47NK
L3	Inductor	56 nH	1	0603	Toko	LL1608–F56NK
L4, 5	Inductor	6.8 nH	2	0603	Toko	LL1608–F6N8K
J1, 3, 5, 6, 11	SMA connector		5		EF Johnson	142–0701–801
J2	Connector		1		Amp	747250–4
P1, P2, P3	Connector		3		Molex	46F522
J7, 8, 9, 10	BNC connector		4		Amp	413631–1
R2, 4, 6	Resistor	1.0 k Ω	3	0603	Panasonic	P1.0KGCT–ND
R3, 5, 7	Resistor	1.5 k Ω	3	0603	Panasonic	P1.5KGCT–ND
R8, 9, 10, 12, 18, 20	Resistor	0	6	0603	Panasonic	P0.0GCT–ND
R13, 14	Resistor	220	2	0603	Panasonic	P220GCT–ND
R15, 16	Resistor	47 k Ω	2	0603	Panasonic	P47KGCT–ND
R22	Resistor	2 k Ω	1	0603	Digikey	P2.0KGCT–ND
U1	IC		1		TI	TRF3520
Varactor	Varactor		2		Motorola	MMBV2109LT1
T1	4:1 Balun		1		MA/COM	ETC1.6–4–2–3

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Figure 17. TRF3520 Application Board Schematic

APPLICATION INFORMATION

The TRF3520 combines RF, IF, and digital signals. In order to obtain maximum performance, follow correct RFpwb layout procedures.

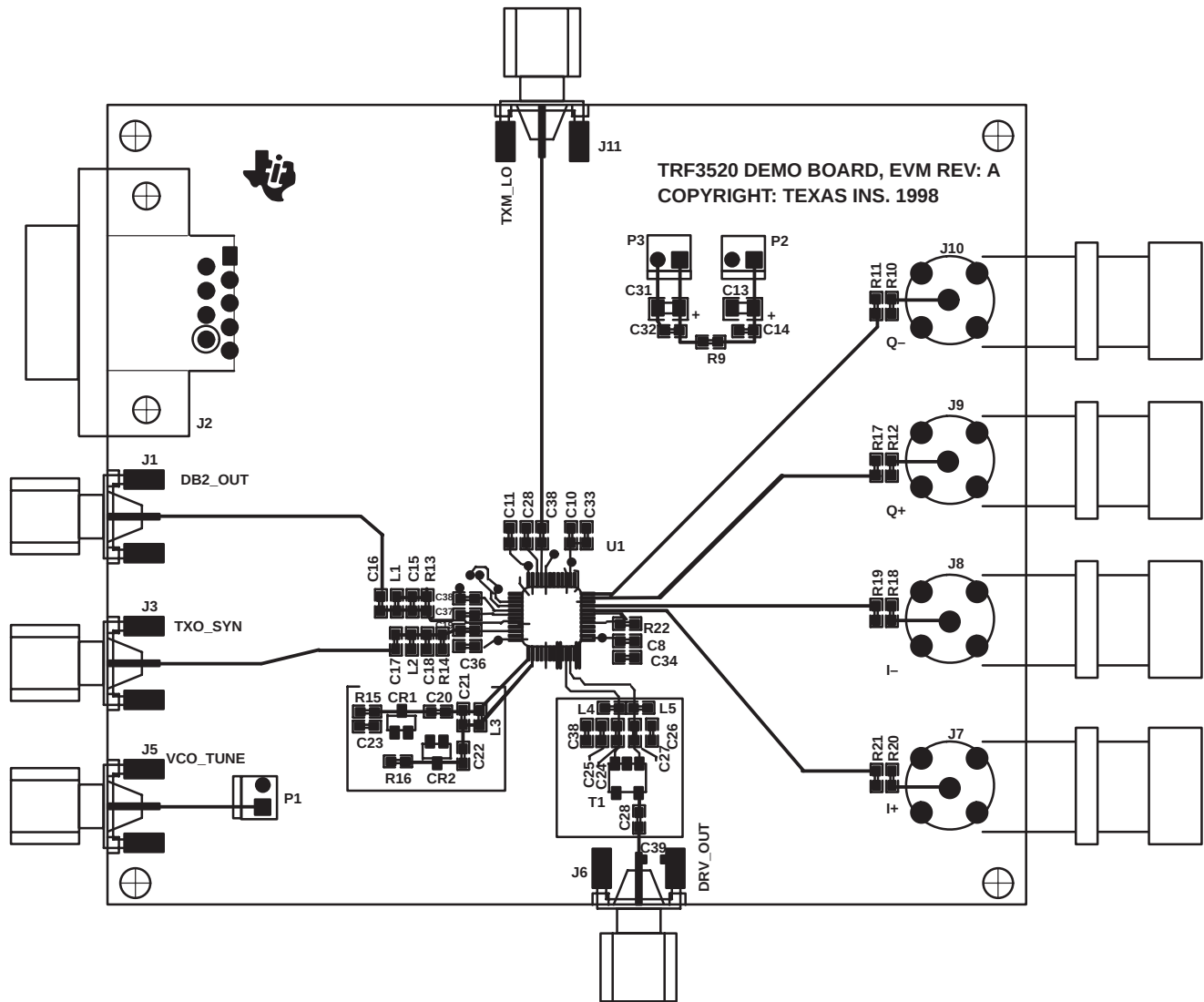


Figure 18. TRF3520 Application Board Layout

TRF3520

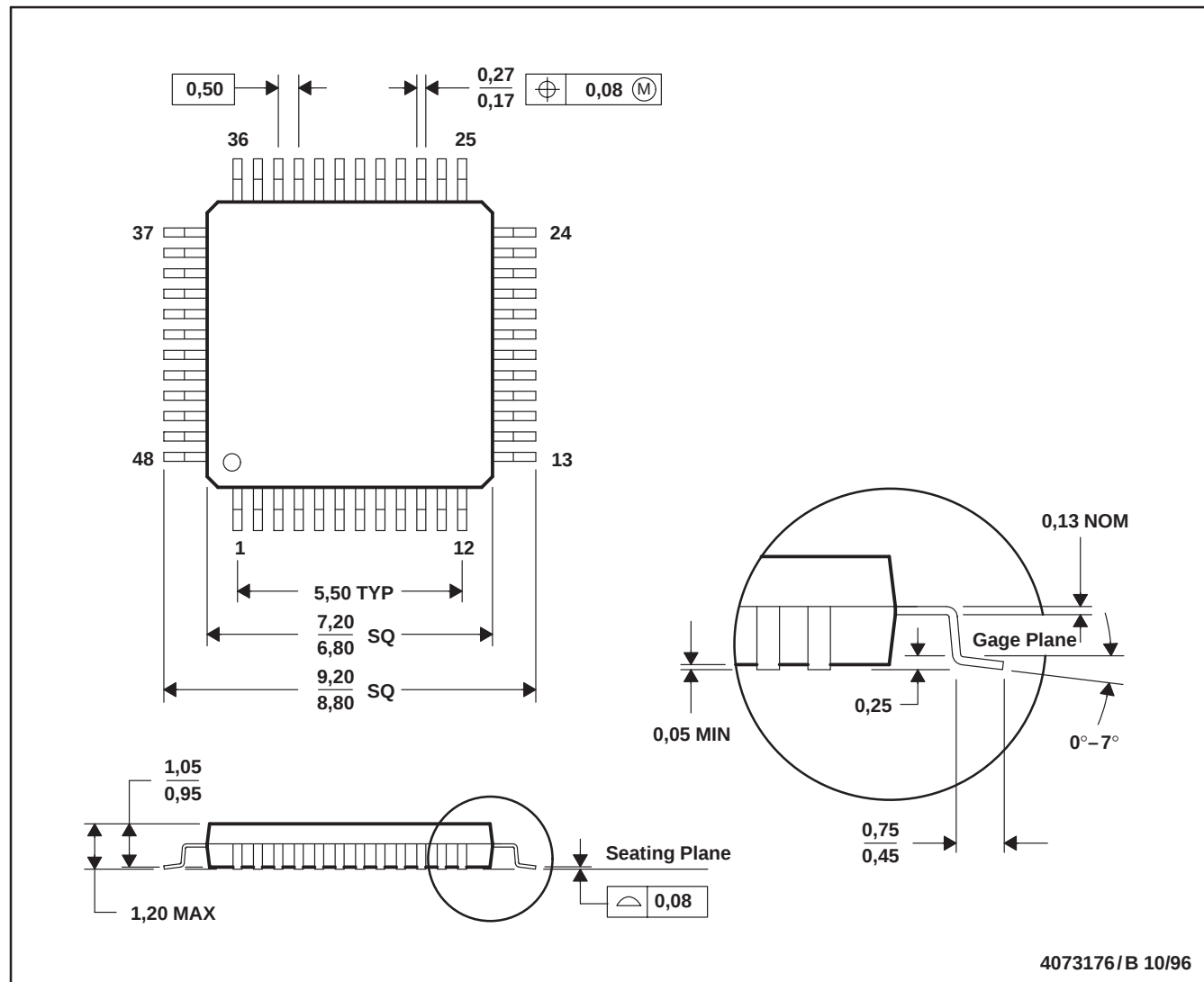
GSM RF MODULATOR/DRIVER AMPLIFIER

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MECHANICAL DATA

PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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