APEX

APEX SCIENCE & ENGINEERING CORP

（OPTOELECTRONIC DIV.）

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TQV1270MQTR20N

ROHS

DATA SHEET

Acceptance	

ISSUE	VERSION	APPROVER	CHECKER	ENGINEER
奉典 3/12 Jy-Hao	**A**	奉典 3/12 Edward		奉典 3/12 Alan

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Record of Revision

Rev	Issued Date	Description	Editor
A	2014-03-12	Preliminary Specification Release	

1 General Specifications

Feature		Spec
Display Spec.	Size	2.7 inch
	Resolution	960×240
	Interface	8-bit RGB /8-bit Dummy RGB /CCIR656/601/YUV
	Color Depth	16.7M (dithering)
	Technology Type	a-Si
	Pixel Pitch (mm)	0.16875x0.16875
	Pixel Configuration	RGB Delta
	Display Mode	Transmissive and Normally White
	Surface Treatment(Up Polarizer)	AG Type
	Viewing Direction	12 o'clock
	Gray Scale Inversion Direction	6 o'clock
Mechanical Characteristics	LCM (W x H x D) (mm)	63.50×46.60×3.20
	Active Area(mm)	54.00×40.50
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	2 LEDs serial
Electronic	Driver IC	HX8268-C

Note 1:Viewing direction for best image quality is different from TFT definition, there is a 180 degree shift.

Note 2 : Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

2 Input/Output Terminals

2.1 TFT LCD Panel

No	Symbol	I/O	Description	Comment
1	VCOM	I	Panel common voltage	
2	SPENB	I	SPI enable	
3	SPDA	I/O	SPI data input/output	
4	SPCK	I	SPI clock input	
5	HSD	I	Horizontal sync input	
6	VSD	I	Vertical sync input	
7	CLKIN	I	Data clock input	
8	DB7	I	Data input; MSB	
9	DB6	I	Data input	
10	DB5	I	Data input	
11	DB4	I	Data input	
12	DB3	I	Data input	
13	DB2	I	Data input	
14	DB1	I	Data input	
15	DB0	I	Data input; LSB	
16	GND	P	Power ground	
17	VDD	P	Supple power	
18	DVDD	C	Power setting capacitor connect pin	
19	C1P	C	Capacitor for charge pump	
20	C1M	C	Capacitor for charge pump	
21	C2P	C	Capacitor for charge pump	
22	C2M	C	Capacitor for charge pump	
23	VINT1	C	Power setting capacitor connect pin	
24	C3P	C	Capacitor for charge pump	
25	C3M	C	Capacitor for charge pump	
26	NC	-	No connection	
27	NC	-	No connection	
28	C4P	C	Capacitor for charge pump	
29	C4M	C	Capacitor for charge pump	
30	VGH	C	Power setting capacitor connect pin	
31	VGL	C	Power setting capacitor connect pin	
32	AGND	P	Power ground	
33	FRP	O	Frame Polarity output for VCOM	
34	COMDC	O	VCOM DC output in	

35	VCAC	C	Power setting capacitor connect pin	
36	DRV	O	VLED boost driving signal	
37	VLED	P	LED power anode	
38	FB	P	LED power cathode	
39	VCOM	I	Panel common voltage	

Note 1: I/O definition：

I-----Input O---Output P----Power(Ground) NC---No connection

3 Absolute Maximum Ratings

3.1 Driving TFT LCD Panel

Ta = 25°C

Item	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	VDD	-0.3	5	V	
Input signal voltage	V_t	-0.3	VDD +0.3	V	
Back Light Forward Current	I_F	-	25	mA	One LED
Operating Temperature	T_{op}	-20	70	℃	
Storage Temperature	T_{st}	-30	80	℃	

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

GND=0V, Ta=25℃

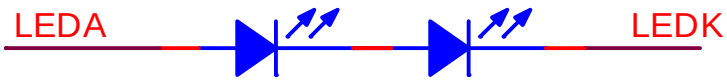
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Signal Voltage	High Level	V_{IH}	0.7×VDD	-	VDD	V	
	Low Level	V_{IL}	GND	-	0.3×VDD	V	
Output Signal Voltage	High Level	VOH	VDD-0.4	-	VDD	V	
	Low Level	VOL	GND	-	0.4	V	
(Panel+ LSI) Power Consumption		Normal Mode	-	6.78	-	mA	CLK 27MHz
		Standby Mode	-	22	-	uA	

4.2 Driving Backlight

Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Current	I_F	-	20	-	mA	2 LEDs
Forward Voltage	V_F	2.9	3.2	3.5	V	-
Backlight Power Consumption	W_{BL}	-	128	-	mW	-
Operating Life Time	--	10000	20000	--	Hrs	

Note1: Figure below shows the connection of backlight LED.



Note 2: One LED : I_F =20 mA, V_F =3.2V

Note 3: I_F is defined for one channel LED.

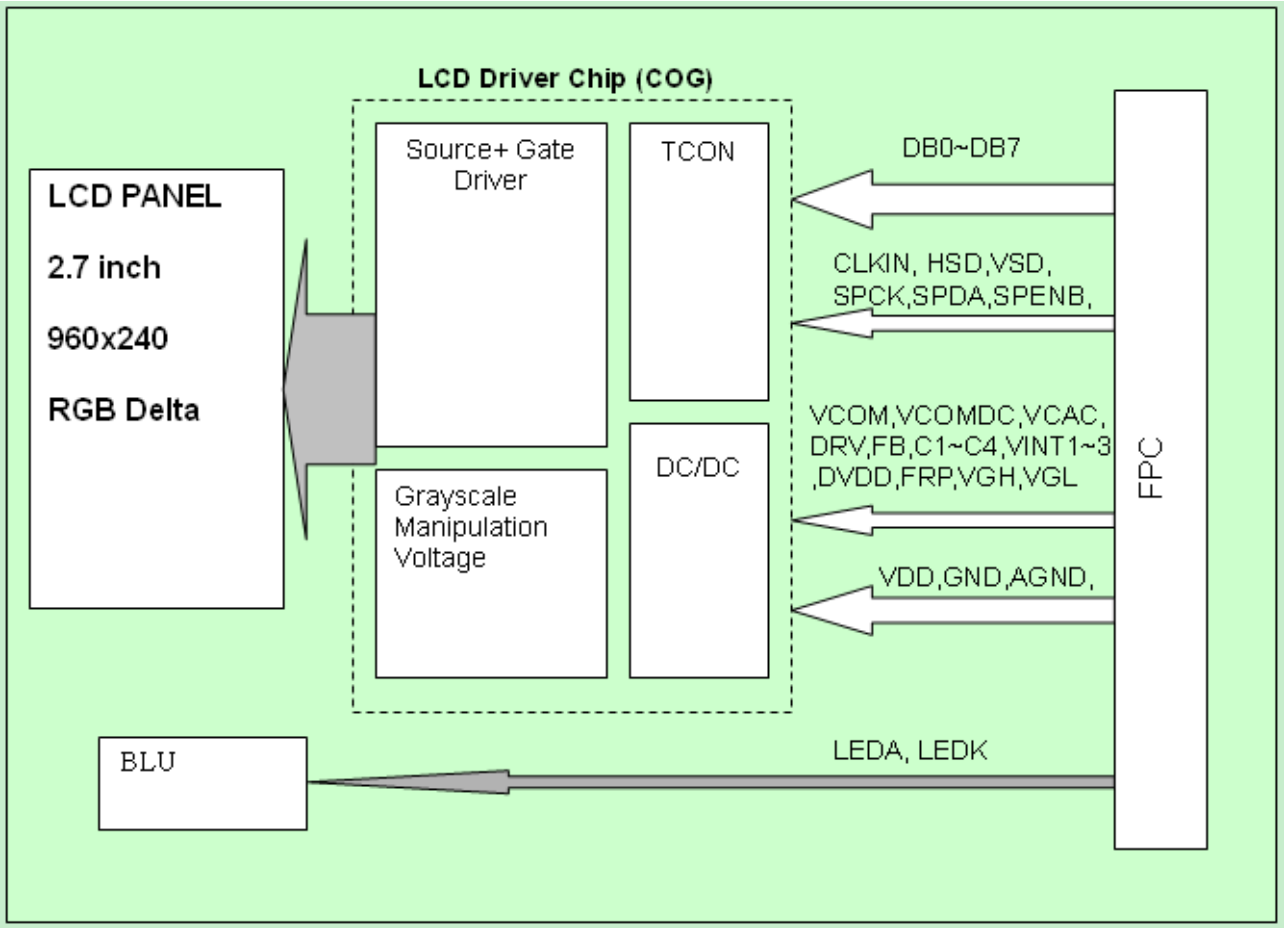
Optical performance should be evaluated at Ta=25℃ only.

If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced.

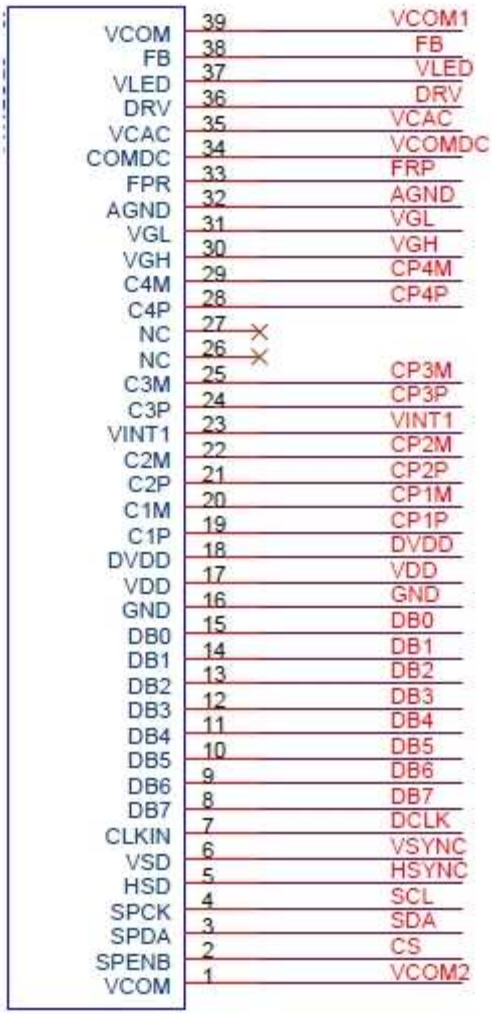
Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

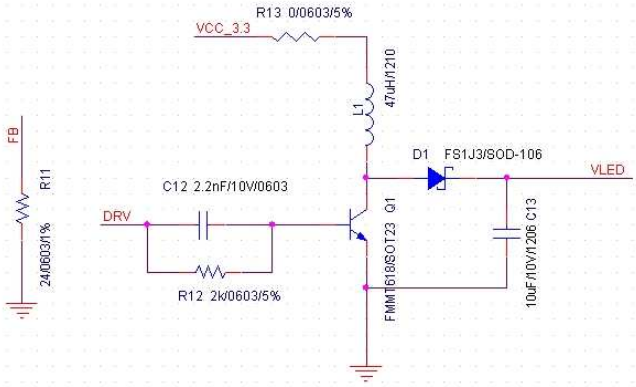
4.3 Block Diagram

LCD module diagram



4.4 APPLICATION CIRCUIT





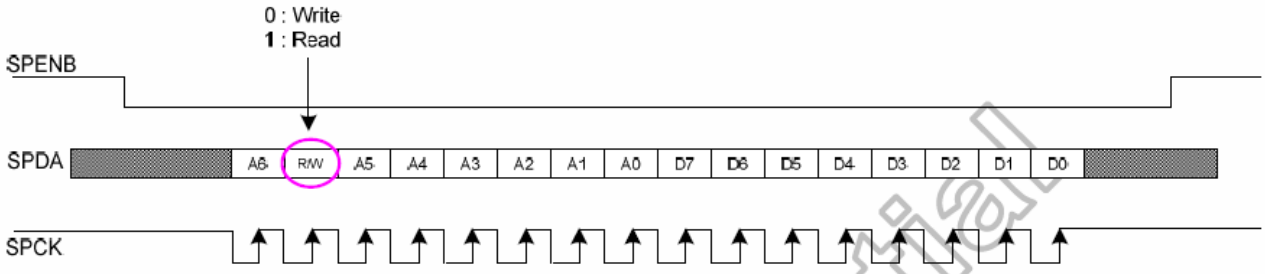
Recommend value of capacitor

Pad name	CAP (μF)	Pad name	CAP (μF)
C1P	1~2.2uF/6.3V	VDD	1uF/6.3V
C1M		DVDD	1uF/6.3V
C2P	1uF/6.3V	VINT	2.2uF/10V
C2M		VGH	2.2uF/25V
C3P	1uF/10V	VGL	2.2uF/16V
C3M		VCAC	2.2uF/6.3V
C4P	1uF/16v	FRP-VCOMDC	2.2uF/6.3V
C4M			

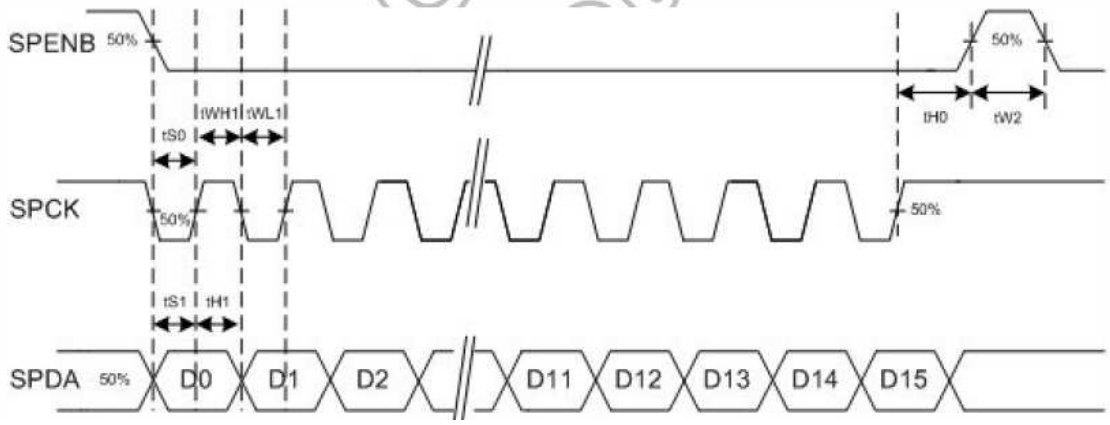
Note: Must use internal LED driver circuit to drive BackLight and must set R05h[1](PWM_EN)='1'

5 Timing Chart

5.1 3-WIRE SERIAL CONTROL INTERFACE



- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset, but commands are established by the VSD signal. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- If 16 bits or more of SPCK are input while SPENB is low, the last 16 bits of transferred data before the rising edge of SPENB pulse are valid data.
- Serial block operates with the SPCK clock
- Serial data can be accepted in the power save mode.



PARAMETER	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
SPENB input setup time	tS0	50			ns
SPDA input setup time	tS1	50			ns
SPENB input hold time	tH0	50			ns
SPDA input hold time	tH1	50			ns
SPCK pulse high width	tWH1	50			ns
SPCK pulse low width	tWL1	50			ns
SPENB pulse high width	tW2	400			ns

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5.2 3-WIRE REGISTER TABLE

Register	Register Address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R00h	0	0	0	0	0	0	0	0	Y CbCr	CCIR601			VCOM AC			
									0	0	x		1	0	1	1
R01h	0	0	0	0	0	0	0	1	VCDCEN		VCOM DC					
									1	x	0	1	1	1	0	0
R03h	0	0	0	0	0	0	1	1	Brightness							
									0	1	0	0	0	0	0	0
R04h	0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
									0	0	0	0	1	0	1	1
R05h	0	0	0	0	0	1	0	1	DRV FREQ	GRB	PWM DUTY			VGH/L EN	LED EN	
									0	1	0	1	1	1	1	x
R06h	0	0	0	0	0	1	1	0	HBLK EN	LED Current			VBLK			
									0	0	0	1	0	1	0	1
R07h	0	0	0	0	0	1	1	1	HBLK							
									0	1	0	0	0	1	1	0
R08h	0	0	0	0	1	0	0	0	BL DRV							
									0	0	x					
R0Bh	0	0	0	0	1	0	1	1	REGSEL							
									0	x						
R0Ch	0	0	0	0	1	1	0	0	PAIR		DESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
									0	0	0	0	0	1	1	0
R0Dh	0	0	0	0	1	1	0	1	CONTRAST							
									0	1	0	0	0	0	0	0
R0Eh	0	0	0	0	1	1	1	0	SUB-CONTRAST R							
									x	1	0	0	0	0	0	0
R0Fh	0	0	0	0	1	1	1	1	SUB-BRIGHTNESS R							
									x	1	0	0	0	0	0	0
R10h	0	0	0	1	0	0	0	0	SUB-CONTRAST B							
									x	1	0	0	0	0	0	0
R11h	0	0	0	1	0	0	0	1	SUB- BRIGHTNESS B							
									x	1	0	0	0	0	0	0
R12h	0	0	0	1	0	0	1	0	TRMEN							
									0	0	0	0	0	0	0	0
R13h	0	0	0	1	0	0	1	1								ENTRY EN
											x					0
R16h	0	0	0	1	0	1	1	0						GAMMA2.2		
											x			1	x	
R17h	0	0	0	1	0	1	1	1		GMA VP16				GMA VP8		
									x	1	0	0	x	1	0	0
R18h	0	0	0	1	1	0	0	0		GMA VP50				GMA VP32		
									x	1	0	1	x	1	0	0
R19h	0	0	0	1	1	0	0	1		GMA VP96				GMA VP72		
									x	1	0	0	x	0	1	1
R1Ah	0	0	0	1	1	0	1	0		GMA VP120				GMA VP110		
									x	1	0	1	x	1	0	0
R2Bh	0	0	1	0	1	0	1	1								STB
											x					0
R2Fh	0	0	1	0	1	1	1	1		VGH SEL		CF SEL	LC TYPE		SOPC	
									0	1	1	0	1	1	0	1
R3Ch	0	0	0	1	0	1	1	1	x	GMA VP127			x	GMA VP0		
										0	1	1		1	0	0
R3Dh	0	0	0	1	1	0	0	0		GMA VPN127				GMA VN0		
									x	0	1	0	x	1	0	1
R3Eh	0	0	0	1	1	0	0	1		GMA VN16				GMA VN8		
									x	1	0	0	x	1	0	0
R3Fh	0	0	0	1	1	0	1	0		GMA VN50				GMA VN32		
									x	1	0	1	x	1	0	0
R40h	0	0	0	1	1	0	0	0		GMA VN96				GMA VN72		
									x	1	0	0	x	0	1	1
R41h	0	0	0	1	1	0	0	1		GMA VN120				GMA VN110		
									x	1	0	1	x	1	0	0
R4Fh	0	0	0	1	1	1	1	1				ID				
									x	0	0	0	1	0	0	1
R55h	1	0	0	1	0	1	0	1	INV SEL	DAT INV						
									x	0	0			x		
R57h	1	0	0	1	0	1	1	1	VGHL ENB							
									x	0				x		
R5Ah	1	0	0	1	1	0	1	0							VGL SEL	
										x				0	1	0

Preliminary

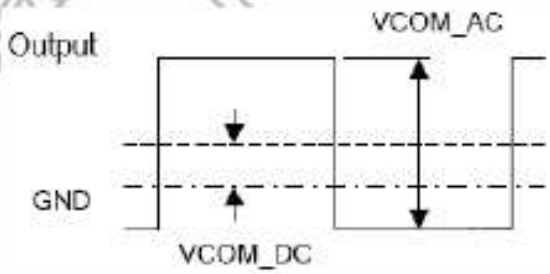
5.3 3-WIRE REGISTER DESCRIPTION

R00h : Data Format & VCOM AC Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	Y_CbCr	CCIRsel	-	-	VCOM_AC			
Initial setting value (default)								0	0	-	-	1	0	1	1

VCOM_AC : Common voltage AC level selection

D3	D2	D1	D0	LV LC (V)	NV LC-1 (V)	NV LC-2 (V)
0	0	0	0	3.7	4.0	5.0
0	0	0	1	3.8	4.1	5.1
0	0	1	0	3.9	4.2	5.2
0	0	1	1	4.0	4.3	5.3
0	1	0	0	4.1	4.4	5.4
0	1	0	1	4.2	4.5	5.5
0	1	1	0	4.3	4.6	5.6
0	1	1	1	4.4	4.7	5.7
1	0	0	0	4.5	4.8	5.8
1	0	0	1	4.6	4.9	5.9
1	0	1	0	4.7	5.0	6.0
1	0	1	1	4.8 (default)	5.1 (default)	6.1 (default)
1	1	0	0	4.9	5.2	6.2
1	1	0	1	5.0	5.2	6.2
1	1	1	0	5.1	5.2	6.2
1	1	1	1	5.2	5.2	6.2



CCIR601 : CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601. (Default)
1	Enable CCIR601. (please refer to the table of R4(SEL) for detail description)

Y_CbCr : Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

Y_CbCr	CbCr (R12[4])															
	0								1							
0	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
1	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

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R01h : VCOM DC Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	VCDCE	-	VCOM_DC					
Initial setting value (default)								1	-	1	0	1	1	0	0

VCOM_DC: Common voltage DC level selection (20mV/step)

D[5:0]	VCOM DC offset
00h	0.24
:	:
1Ch	0.8 (default)
3Fh	1.5

VCDCE : VCOM DC enable control

VCDCE	Function
0	VCOM_DC function disabled. The VCOMDC pin is disabled
1	VCOM_DC function enabled. The VCOMDC voltage follows VCOM_DC setting. (default)

R03h : Whole Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	1	Brightness							
Initial setting value (default)								0	1	0	0	0	0	0	0

Brightness : Adjust RGB Brightness

D7~D0	Brightness gain
00h	Dark(-64)
40h	Center(0)(default)
FFh	Bright(+191)

Setting accuracy 1bit/step

R04h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	Narrow	YUV	SEL		NTSC/PAL		VDIR	HDIR
Initial setting value (default)								0	0	0	0	1	0	1	1

HDIR : Shift registers of source driver direction selection

D0	HDIR Function
0	Shift from right to left. Y0 Y1 ... Yn-1 Yn
1	Shift from left to right. Y0 Y1 ... Yn-1 Yn (Default)

VDIR : Gate driver output direction selection

D1	VDIR Function
0	Shift from down to up. L0 L1 ... L239 L240
1	Shift from up to down. L0 L1 ... L239 L240 (Default)

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NTSC/ PAL : NTSC or PAL input mode selection

D3	D2	NTSC/PAL Mode
0	0	PAL.
0	1	NTSC.
1	x	Auto detection. (Default)

SEL : Input data timing format selection

CCIR601	YUV	SEL		Input Timing format
		D5	D4	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320 x 240.
0	0	1	x	8-bit Dummy RGB 360 x 240.
0	1	x	x	CCIR656.
1	1	0	x	YUV 640.
1	1	1	0	YUV 720.

YUV : YUV(CCIR656) or RGB input selection

D6	Data format
0	RGB input. (Default)
1	CCIR656/YUV640/YUV720 input.

Narrow : Normal display and Narrow display selection

D7	Function
0	Normal display. (Default)
1	Narrow display

Note: Narrow function was not supporting 8-bit RGB and 24-bit RGB input mode.

Narrow = 0 Narrow = 1

Figure 6.1 The Narrow function

R05h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1	DRV FREQ	GRB	PWM_DUTY			VGH/L EN	LED EN	-
Initial setting value (default)								0	1	0	1	1	1	1	-

LED_EN : Shut down for back light power converter

D1	LED_EN Function
0	The back light power converter is off.
1	The back light power converter is controlled by STB's power on/off sequence. (Default)

D1	VGH/L_EN Function
0	VGH/VGL charge pump is off.
1	VGH/VGL charge pump is controlled by STB's power on/off sequence. (Default)

PWM_DUTY : PWM duty cycle selection for back light power convert

PWM_DUTY			Function
D5	D4	D3	PWM duty cycle
0	0	0	20%
0	0	1	26%
0	1	0	32%
0	1	1	38% (Default)
1	0	0	44%
1	0	1	50%
1	1	0	56%
1	1	1	62%

GRB : Global reset

D6	GRB Function
0	Reset all registers to default value.
1	Normal operation. (Default)

DRV_FREQ : DRV signal frequency setting

D7	GRB Function
0	High frequency (Default)
1	Low frequency

R06h :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	0	HBLK_EN	LED_Current		VBLK				
Initial setting value (default)								0	0	0	1	0	1	0	1

VBLK : Vertical blanking setting for 8-bit RGB , 8-bit Dummy RGB & CCIR656

For 8-bit RGB, 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 NTSC mode, parallel RGB mode(PSEL=0)

D[4:0]	Function	Unit
00h~03h	3	H(Line)
04h	4	
15h	21(Default)	
1Fh	31	

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For 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 PAL mode. (Vertical blanking+3)

D[4:0]	Function	Unit
00h	3	H(Line)
04h	7	
15h	24(Default)	
1Fh	34	

LED_CURRENT : LED current adjustable for DC-DC feedback threshold voltage

D[6:5]	Feedback Threshold Voltage
00	0.6 V. (default)
01	0.75V.
10	0.45V.
11	0.3V.

HBLK_EN : HBLK function enable

D[7]	HBLK EN Function
0	Disable (default)
1	Enable

R07h : Horizontal Blanking Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	1	HBLK							
Initial setting value (default)								0	1	0	0	0	1	1	0

HBLK : Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	Unit	NTSC/PAL Mode
X	32h~45h	50~69	CLKIN	8-bit RGB.
X	46h	70		
X	47h~FFh	71~255		
0	X	241		8-bit Dummy RGB.
1	00h~03h	3		
	04h~FFh	4~255		
0	XXh	240		YUV640, YUV720.
1	00h~03h	3		
	04h~FFh	4~255		
0	X	61		Parallel RGB
1	04h~3Fh~	4~63		

R08h : Backlight Driving Capacity Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	BL_DRV		-	-	-	-	-	-
Initial setting value (default)								0	0	-	-	-	-	-	-

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BL_DRV : Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability. (Default)
0	1	2 times the Normal capability.
1	0	4 times the Normal capability.
1	1	8 times the Normal capability.

R0Bh : MTP

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	1	REGSEL	-	-	-	-	-	-	-
Initial setting value (default)								0	-	-	-	-	-	-	-

REGSEL : MTP function control register

D7	REGSEL Function
0	VCOM_DC[5:0] is read from MTP memory. (Default)
1	VCOM_DC[5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test

R0Ch :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	0	PAIR		SESEL	CbCr	DEpol	VDpol	HDpol	CLKINpol
Initial setting value (default)								0	0	0	0	0	1	1	0

CLKINpol : CLKIN polarity selection

D0	CLKINpol Function
0	Positive polarity. (Default)
1	Negative polarity

HDpol : HSD polarity selection

D1	HDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

VDpol : VSD polarity selection

D2	VDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

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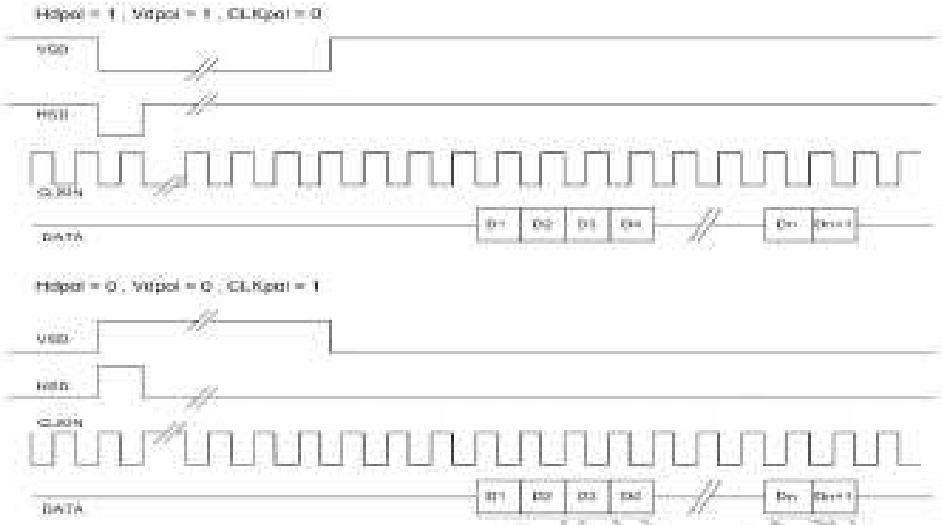


DEpol : DEN polarity selection

D3	DEpol Function
0	Positive polarity (Default)
1	Negative polarity

CbCr : Cb & Cr exchange position (valid for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb Y Cr. (Default)
1	Cr Y Cb

DESEL : DE Mode selection

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

DESEL only controls the HV and DE mode at 8-bit RGB, 8-bit Dummy RGB and Parallel Mode.

PAIR : Vertical start time of Odd/Even Frame

PAIR D7	PAIR D6	VBLK ODD/EVEN	Unit
-	0	21/21. (Default)	H (Line)
-	1	21/20.	

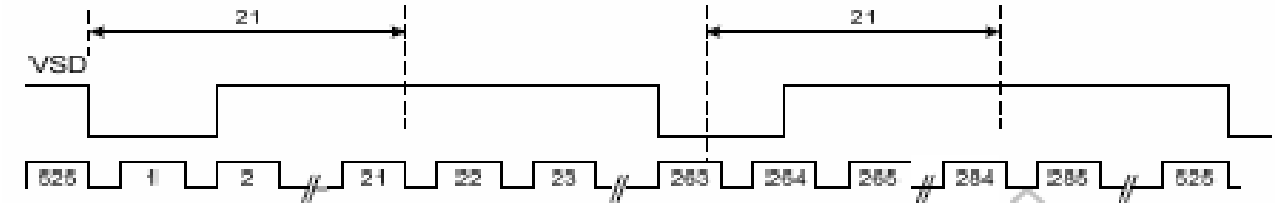
For 8-bit RGB / 8-bit Dummy RGB NTSC / 8-bit Dummy RGB PAL, parallel RGB mode(PSEL=0)
The typical value of VBLK of 8-bit Dummy RGB PAL(24 H) is different than 8-bit RGB/8-bit Dummy RGB NTSC(21H)

PAIR D7	PAIR D6	VBLK ODD/EVEN	Unit
0	0	21/21. (Default)	H (Line)
0	1	21/22.	
1	0	22/21.	
1	1	22/22.	

For CCIR656/YUV640/YUV720 NTSC/PAL
The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(21H).

Note: Vertical blanking must be adjusted base on the input data.

For example:



R0Dh : Whole Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	0	1	CONTRAST							
Initial setting value (default)								0	1	0	0	0	0	0	0

CONTRAST : RGB contrast level setting , the gain changes (1/64) / bit

D[7:0]	Contrast gain
00h	0
40h	1 (Default)
FFh	3.984

R0Eh : R Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	0	-	SUB-CONTRAST_R						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-CONTRAST_R : Red sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	R Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R0Fh : R Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	1	-	SUB-BRIGHTNESS_R						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-BRIGHTNESS_R : Red sub-pixel brightness level setting, setting accuracy:1 step/bit

D[6:0]	R Brightness gain
00h	DARK (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

R10h : B Contrast Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	0	-	SUB-CONTRAST_B						
Initial setting value (default)								-	1	0	0	0	0	0	0

SUB-CONTRAST_B : Blue sub-pixel contrast level setting, the gain changes (1/256)/bit

D[6:0]	B Contrast gain
00h	0.75
40h	1 (Default)
7Fh	1.246

R11h : B Brightness Adjustment

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	1	SUB-BRIGHTNESS_B							
Initial setting value (default)									1	0	0	0	0	0	0

SUB-BRIGHTNESS_B : Blue sub-pixel brightness level setting, setting accuracy:1 step/bit

D6~D0	B Brightness gain
00h	DARK (-64)
40h	Center(0) (Default)
7Fh	Bright (+63)

R12h : Instruction for OTP

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0	TRMEN							
Initial setting value (default)								0	0	0	0	0	0	0	0

TRMEN : VCOM DC Trim Function Control Register

VCOMDC Trim function control register, this IC have build-in MTP memory, at Power-on, IC will auto load the MTP memory to set the VCOMDC level to prevent flick issue.

Operation condition:
1. CLKIN frequency range 26Mhz ~ 31Mhz
2. Apply 7.5V to VPPMTP pin.

Programming procedure:
1. Set REGSEL = 1
2. Adjustment VCOM_DC(R1[5:0]) value, select proper VCOM_DC value
3. Set TRMEN[7:0] as following sequence : A0h 5Fh EEh 00h.
4. Hold 1s for MTP control block operation.
5. Set global reset (set R5[6] = 1) and restart the display operation.
6. Check the VCOMDC value.

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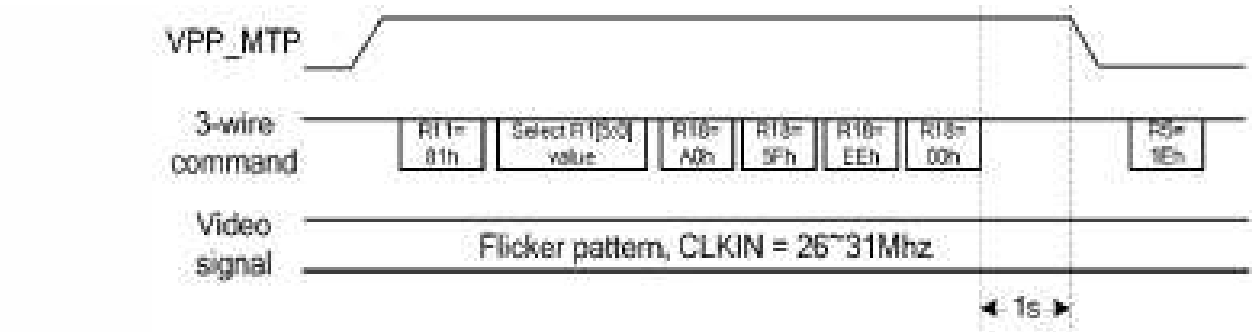


Note:(1) The Trim Block can be writing only for "3" times.
(2) After finishing TRMEN command do not power off within 1 second.
(3) Trim command exceed the limit may cause the VCOMDC output unknown value.

R13h : Entry Function Control

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	-	-	-	-	-	-	-	ENTRY_EN
Initial setting value (default)								-	-	-	-	-	-	-	0

ENTRY_EN : Entry function control

ENTRY_EN	Function
0	Through mode: Input data must be aligned with the color filter arrangement (default).
1	Alignment mode: Input data must always be the R1, G1, B1,R2, G2,

R16h : Gamma 2.2

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	0	-	-	-	-	-	GAMMA2.2	-	-
Initial setting value (default)								-	-	-	-	-	1	-	-

GAMMA2.2 : Select auto or manual gamma setting

D2	Function
0	Manual set gamma by R17h~R1Ah and R3Ch~R41h.
1	Auto set to gamma2.2. (default)

R17h、R18h、R19h、R1Ah : Gamma Point Setting

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	1	-	GMA_VP16			-	GMA_VP8		
Initial setting value (default)								-	1	0	0	-	1	0	0
0	0	0	1	1	0	0	0	-	GMA_VP50			-	GMA_VP32		
Initial setting value (default)								-	1	0	1	-	1	0	0
0	0	0	1	1	0	0	1	-	GMA_VP96			-	GMA_VP72		

Initial setting value (default)								-	1	0	0	-	0	1	1
0	0	0	1	1	0	1	0	-	GMA_VP120			-	GMA_VP110		
Initial setting value (default)								-	1	0	1	-	1	0	0

GMA_VP8 : Gamma reference voltage VP8;
GMA_VP16 : Gamma reference voltage VP16;
GMA_VP32 : Gamma reference voltage VP32;
GMA_VP50 : Gamma reference voltage VP50;
GMA_VP72 : Gamma reference voltage VP72;
GMA_VP96 : Gamma reference voltage VP96;
GMA_VP110 : Gamma reference voltage VP110;
GMA_VP120 : Gamma reference voltage VP120;

Reference point	000	001	010	011	8	101	110	111
VP0	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V
VP8	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V
VP16	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP32	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP50	-5 V	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V
VP72	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V	+4 V
VP96	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP110	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VP120	-10 V	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V
VP127	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V	+8 V
VN0	-10 V	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V
VN8	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V	+6 V
VN16	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN32	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN50	-5 V	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V
VN72	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V	+4 V
VN96	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN110	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V
VN120	-10 V	-8 V	-6 V	-4 V	-2 V	Default	+2 V	+4 V
VN127	-4 V	-3 V	-2 V	- V	Default	+ V	+2 V	+3 V

Note: (1) For low voltage LC V=25mV ,For Normal voltage LC V=40mV

R2Bh : Standby Mode

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	-	-	-	-	-	-	-	STB
Initial setting value (default)								-	-	-	-	-	-	-	0

STB : Standby (Power saving) mode

STB	Function
0	Standby Mode. (Default)
1	Normal operation.

R2Fh :

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	1	1	VGH_SEL			CF_SEL	LC_TYPE		SOPC	
Initial setting value (default)								0	1	1	0	0	0	0	1

VGH_SEL			VGH Voltage
D7	D6	D5	
0	0	0	13V
0	0	1	14V
0	1	0	15V
0	1	1	16V
1	0	0	17V
1	0	1	18V
1	1	0	18V
1	1	1	18V

SOPC : Source output driving capability selection

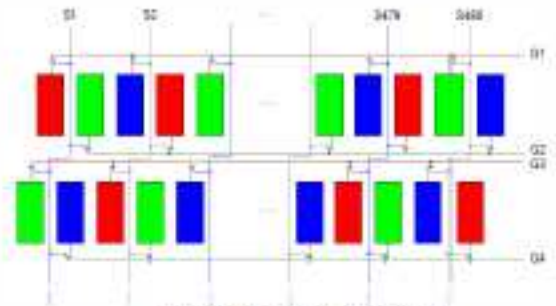
SOPC	Source driver capability
0	-25%
1	Normal. (default)
2	+25%
3	+50%

LC_TYPE : LC type select

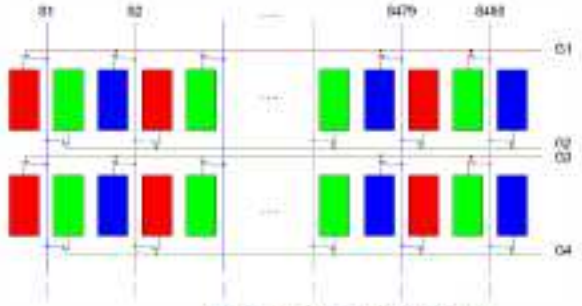
D5	D4	LC_TYPE Function
0	0	Low voltage LC(Default)
0	1	Reserved
1	0	Reserved
1	1	Normal LC

CF_SEL : Color filter selection register

CF_SEL	Function
0	Delta color filter. (Default)
1	Stripe color filter.



Delta color filter@960x240



Stripe color filter@960x240

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R55h : Inversion selection

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	1	-	INV_SEL	DAT_INV	-	-	-	-	-
Initial setting value (default)								-	0	0	-	-	-	-	-

DAT_INV	Inversion
0	Normal data output. (Default)
1	Inversion data output

INV_SEL	Inversion
0	One line inversion. (Default)
1	Column inversion.

R57h : VGHL_ENB

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	1	1	VGHL_ENB	-	-	-	-	-	-	-
Initial setting value (default)								0	-	-	-	-	-	-	-

VGHL_ENB	Inversion
0	VGH/VGL charge pump enable (Default)
1	For external VGH/VGL application

R5Ah : VGL_SEL

Address								Data setting							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	-	0	1	1	0	1	0	-	-	-	-	-	VGL_SEL		
Initial setting value (default)								-	-	-	-	-	0		

VGL_SEL			VGL Voltage
D2	D1	D0	
0	0	0	-8V
0	0	1	-9V
0	1	0	-10V(default)
0	1	1	-11V
1	0	0	-7V
1	0	1	-7V
1	1	0	-11V
1	1	1	-11V

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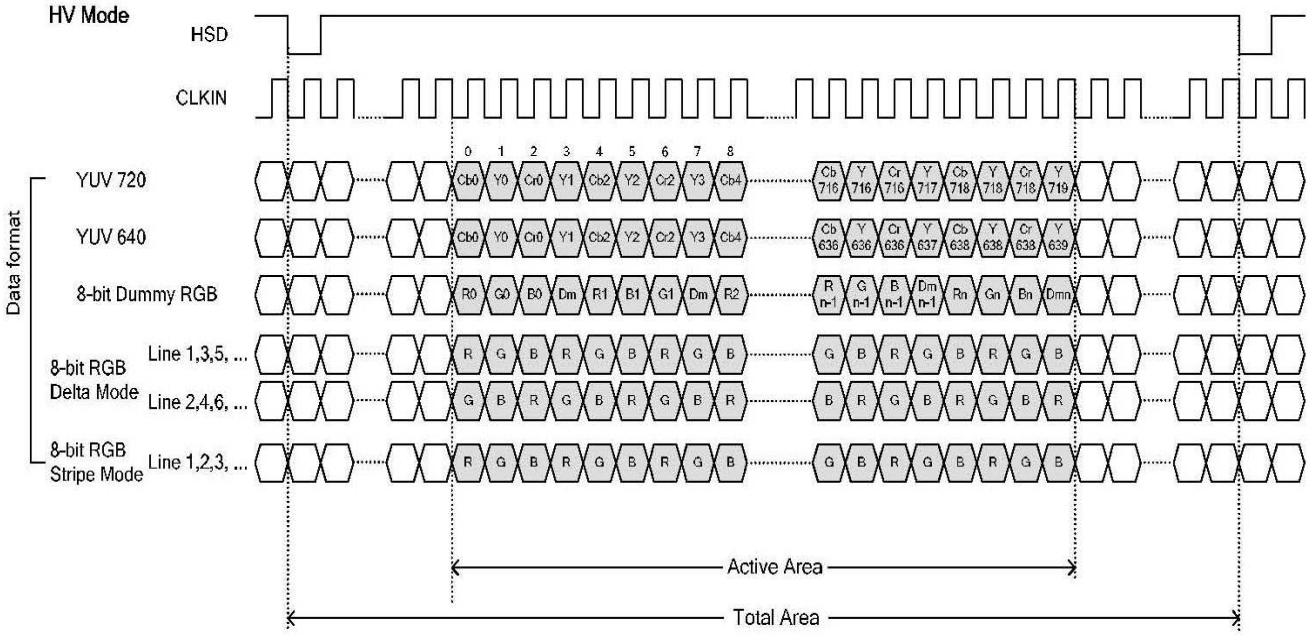
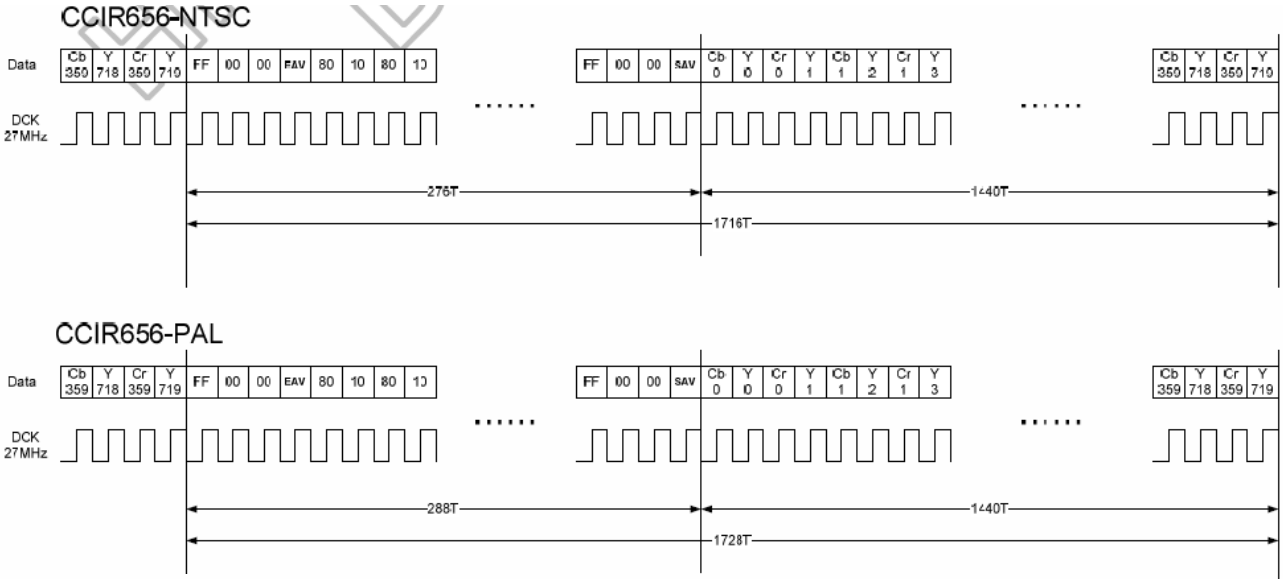
5.4 DATA INPUT FORMAT

Serial 8-bit RGB / 8-bit Dummy RGB / YUV Mode Data format



CCIR_656 Mode Data Format



XY							
D7	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

CCIR656/YUV640/YUV720 to RGB Conversion Formula

$$Rn = 1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 1.596 \times (Cr_n - 128)$$

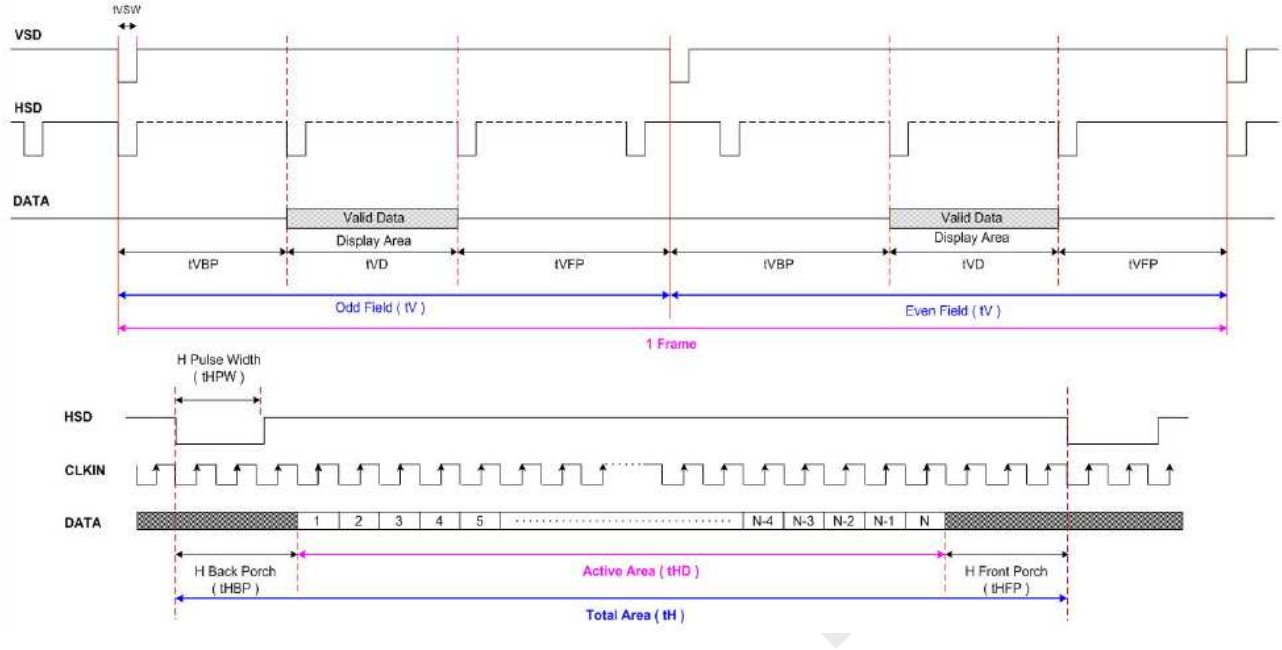
$$Gn = 1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] - 0.813 \times (Cr_n - 128) - 0.392 \times (Cb_n - 128)$$

$$Bn = 1.164 \times [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 2.017 \times (Cb_n - 128)$$

Where Y : 16~235 Cr : 16~240 Cb : 16~240

5.5 INPUT TIMING FORMAT

Serial 8-bit RGB / 8-bit Dummy RGB / YUV / Parallel RGB Input Timing Chart



8-bit RGB input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	13.5	27	27.19	MHz
HSD period		tH	1024	1716	1728	CLKIN
HSD display period		tHD		960		CLKIN
HSD back porch		tHBP	50	70	255	CLKIN
HSD front porch		tHFP	14	686	718	CLKIN
HSD pulse width		tHSW	1	1	tHBP-1	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1 CLKIN	1CLKIN	6H	
1 Frame			485	525	901	H

8-bit Dummy RGB input timing

8-bit Dummy RGB (320 mode/NTSC/24.535Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.535	30	MHz
HSD period		tH	1306	1560	1907	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	372	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (320 mode/PAL/24.375Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	20.45	24.375	30	MHz
HSD period		tH	1306	1560	1920	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	39	385	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

8-bit Dummy RGB (360 mode/NTSC/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1716	1907	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	35	212	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	242.5	262.5	450.5	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	3	21	31	H
	Even field		3.5	21.5	31.5	
VSD front porch	Odd field	tVFP	1.5	1.5	179.5	H
	Even field		1	1	179	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			485	525	901	H

8-bit Dummy RGB (360 mode/PAL/27Mhz) input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	23	27	30	MHz
HSD period		tH	1466	1728	1920	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	3	241	255	CLKIN
HSD front porch		tHFP	25	47	225	CLKIN
HSD pulse width		tHSW	1	1	200	CLKIN
VSD period time		tV	292.5	312.5	450.5	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	3	23	34	H
	Even field		3.5	23.5	34.5	
VSD Front porch	Odd field	tVFP	1.5	1.5	128.5	H
	Even field		1	1	128	
VSD pulse width		tVSW	1	1	200	CLKIN
1 Frame			585	625	901	H

YUV720 and YUV640 input timing

YUV 720 mode/NTSC input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1716	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	36	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

YUV 720 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	27	-	MHz
HSD period		tH	-	1728	-	CLKIN
HSD display period		tHD		1440		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	48	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

YUV 640 mode/NTSC input timing

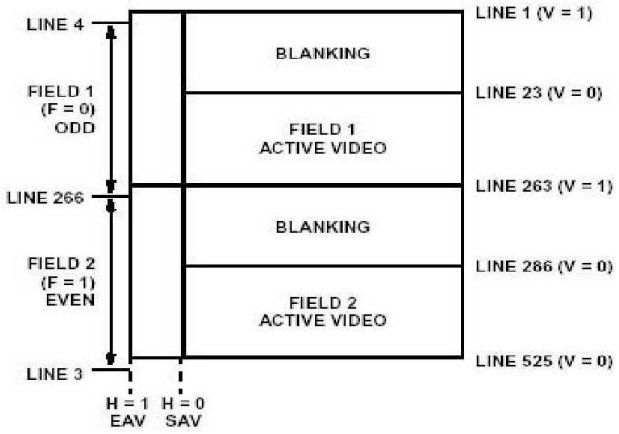
Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.535	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	262.5	-	H
Vertical display area		tVD		240		H
VSD back porch	Odd field	tVBP	-	21	-	H
	Even field		-	21.5	-	
VSD front porch	Odd field	tVFP	-	1.5	-	H
	Even field		-	1	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	525	-	H

YUV 640 mode/PAL input timing

Parameter		Symbol	Interlace			Unit
			Min.	Typ.	Max.	
CLKIN frequency		fCLKIN	-	24.375	-	MHz
HSD period		tH	-	1560	-	CLKIN
HSD display period		tHD		1280		CLKIN
HSD back porch		tHBP	-	240	-	CLKIN
HSD front porch		tHFP	-	40	-	CLKIN
HSD pulse width		tHSW	-	1	-	CLKIN
VSD period time		tV	-	312.5	-	H
Vertical display area		tVD		288		H
VSD back porch	Odd field	tVBP	-	24	-	H
	Even field		-	24.5	-	
VSD front porch	Odd field	tVFP	-	0.5	-	H
	Even field		-	0	-	
VSD pulse width		tVSW	-	1	-	CLKIN
1 Frame			-	625	-	H

CCIR656 input timing

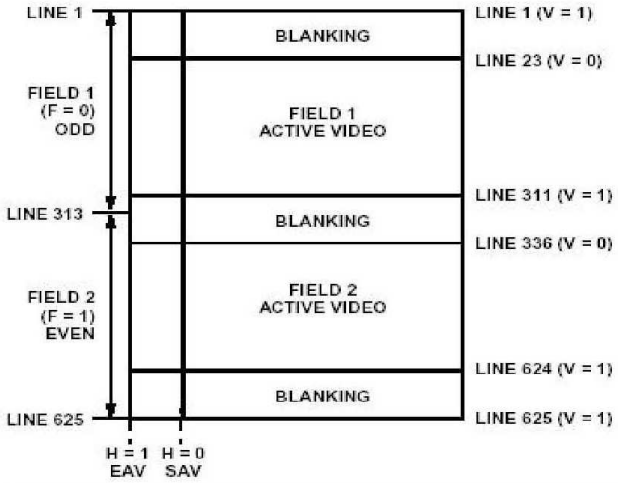
NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

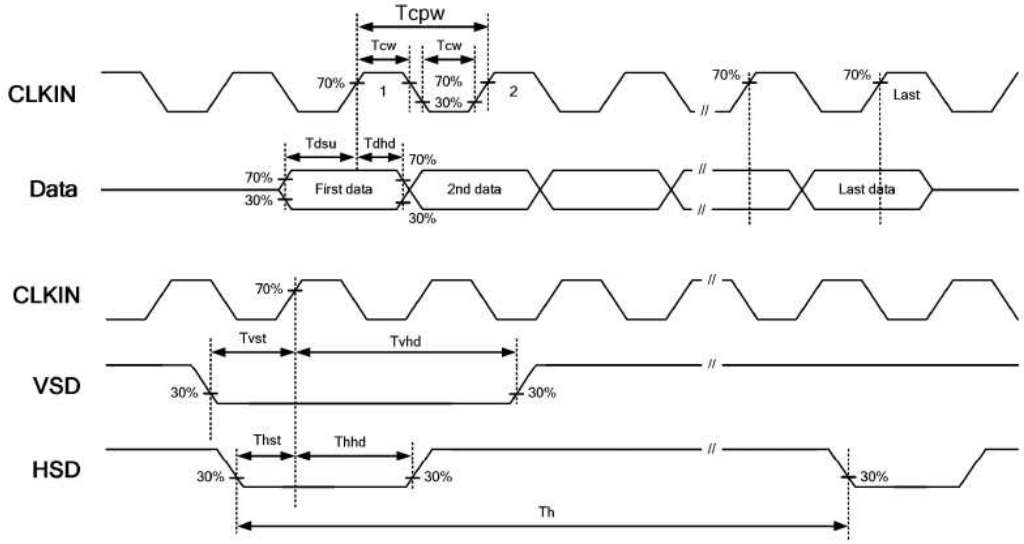
PAL mode

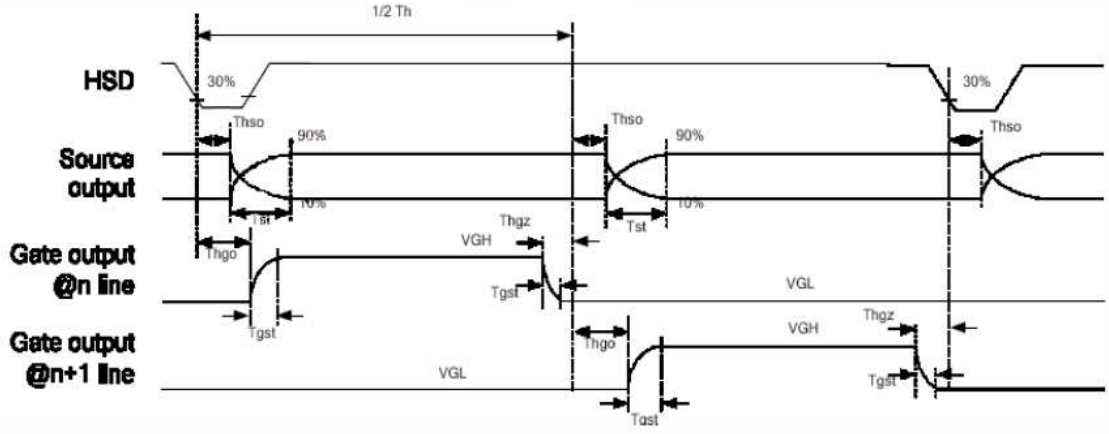


LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACTIVE VIDEO

5.6 AC ELECTRICAL CHARACTERISTICS



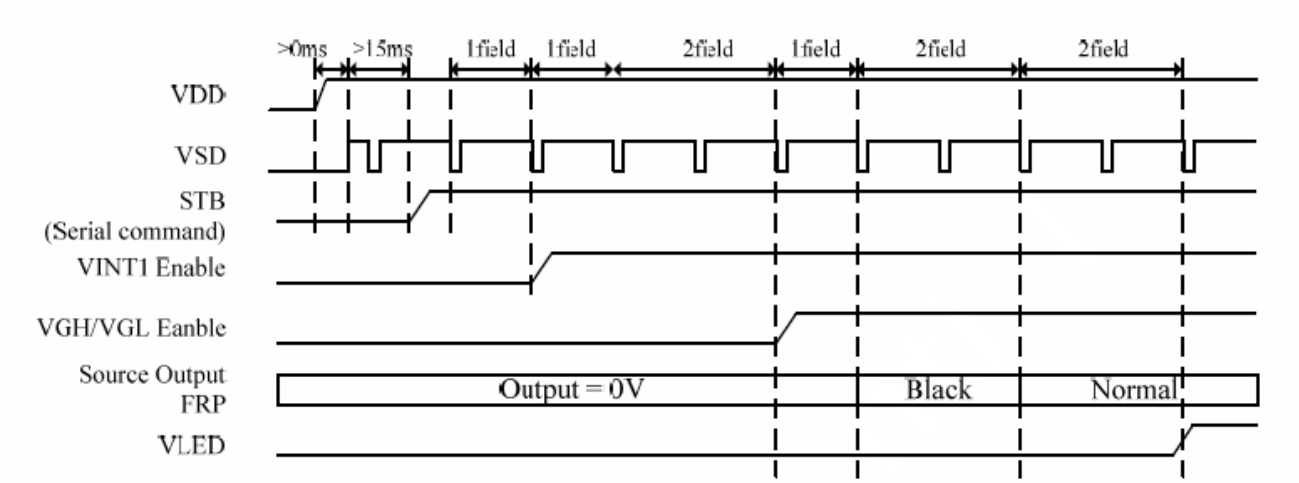


(VDD=3.0~3.6V,VDDIO=AVDD=VDD,GND=AGND=0V, TA=25℃)

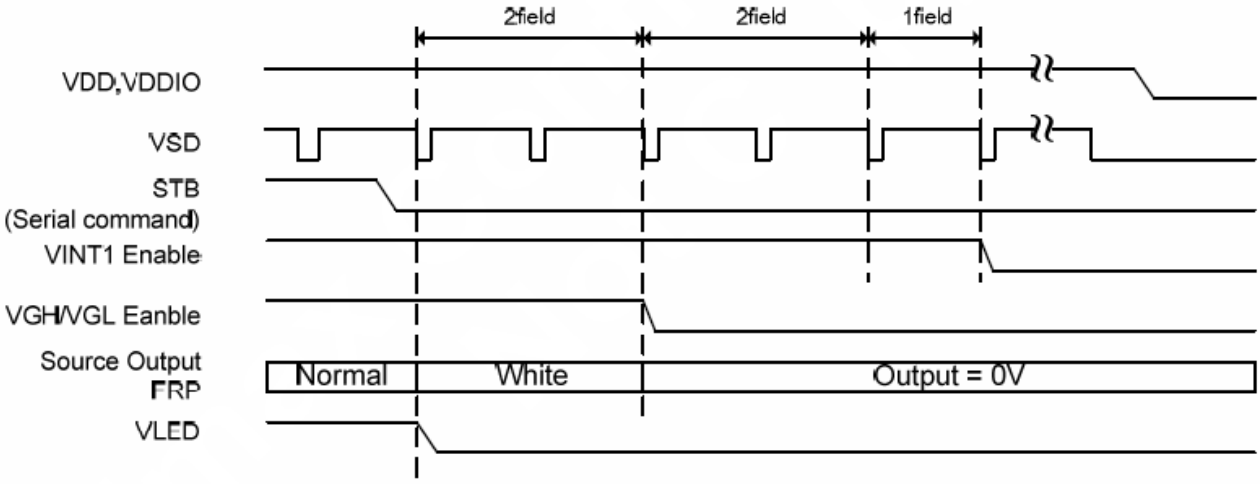
PARAMETER	Symbol	Spec.			Unit	Conditions
		Min.	Typ.	Max.		
HSD period time	Th	60	63.56	67	us	
HSD setup time	T_{hst}	12	-	-	ns	
HSD hold time	T_{hhd}	12	-	-	ns	
VSD setup time	T_{vst}	12	-	-	ns	
VSD hold time	T_{vhd}	12	-	-	ns	
Data setup time	T_{dsu}	12	-	-	ns	
Data hold time	T_{dhd}	12	-	-	ns	
Source output settling time	T_{ST}	-	-	8	us	R=5Kohm , C=30pF
Gate output settling time	Tgst	-	0.5	1	us	R=3Kohm , C=25pF
VCOM setting time	$T_{ST,vcom}$	-	-	9	us	R=200ohm , C=5nF

6 Power On/Off Sequence

6.1 POWER ON SEQUENCE



6.2 POWER OFF SEQUENCE



7 Optical Characteristics

Ta=25℃

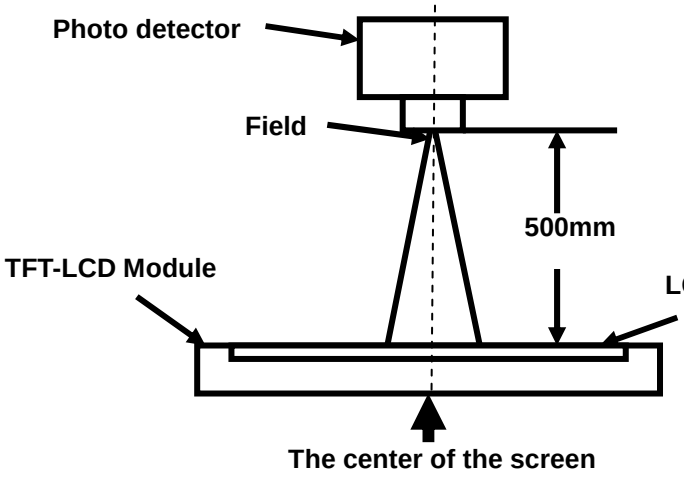
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
View Angles		θT	CR≧10	50	60	-	Degree	Note 2
		θB		60	70	-		
		θL		60	70	-		
		θR		60	70	-		
Contrast Ratio		CR	θ=0°	400	500	-		Note1 Note3
Response Time		T_{ON}	25℃	-	30	40	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.260	0.310	0.360		Note5, Note1
		y		0.280	0.330	0.380		
	Red	x		0.518	0.568	0.618		
		y		0.287	0.337	0.387		
	Green	x		0.300	0.350	0.400		
		y		0.494	0.544	0.594		
	Blue	x		0.106	0.156	0.206		
		y		0.059	0.109	0.159		
Uniformity		U		75	80	-	%	Note1 Note6
NTSC				-	40	-	%	Note 5
Luminance		L		200	250	-	cd/m^2	Note1 Note7

Test Conditions:

1. V_F =3.2V, I_F =20mA(Backlight current for each LED), the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。

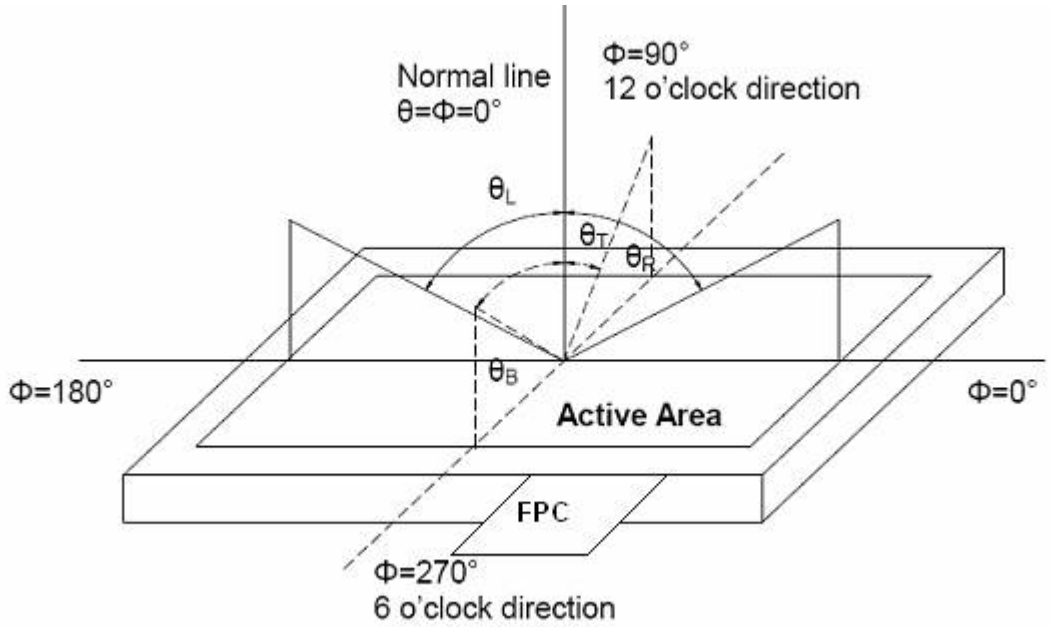


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

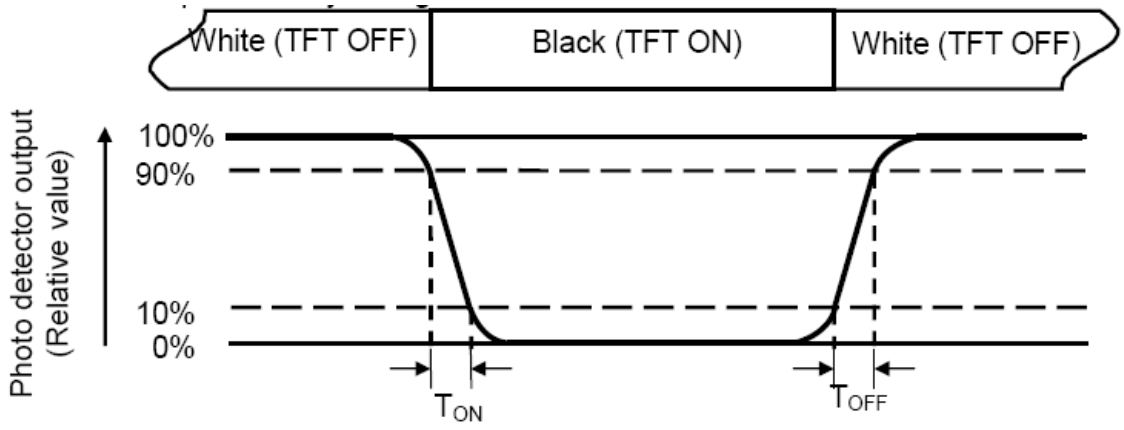
“White state “:The state is that the LCD should be driven by Vwhite.

“Black state”: The state is that the LCD should be driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length W----- Active area width

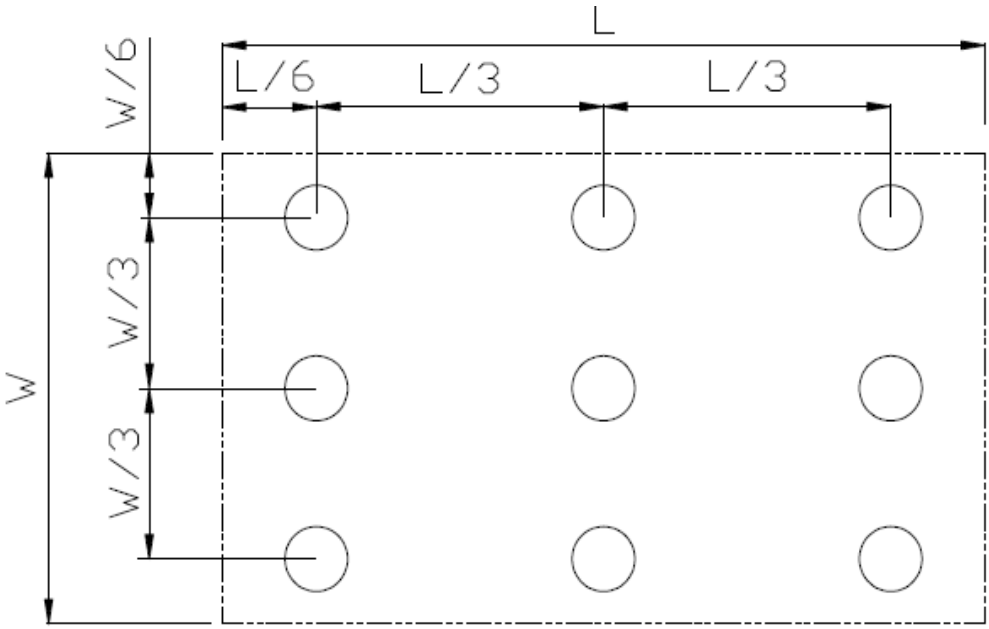


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

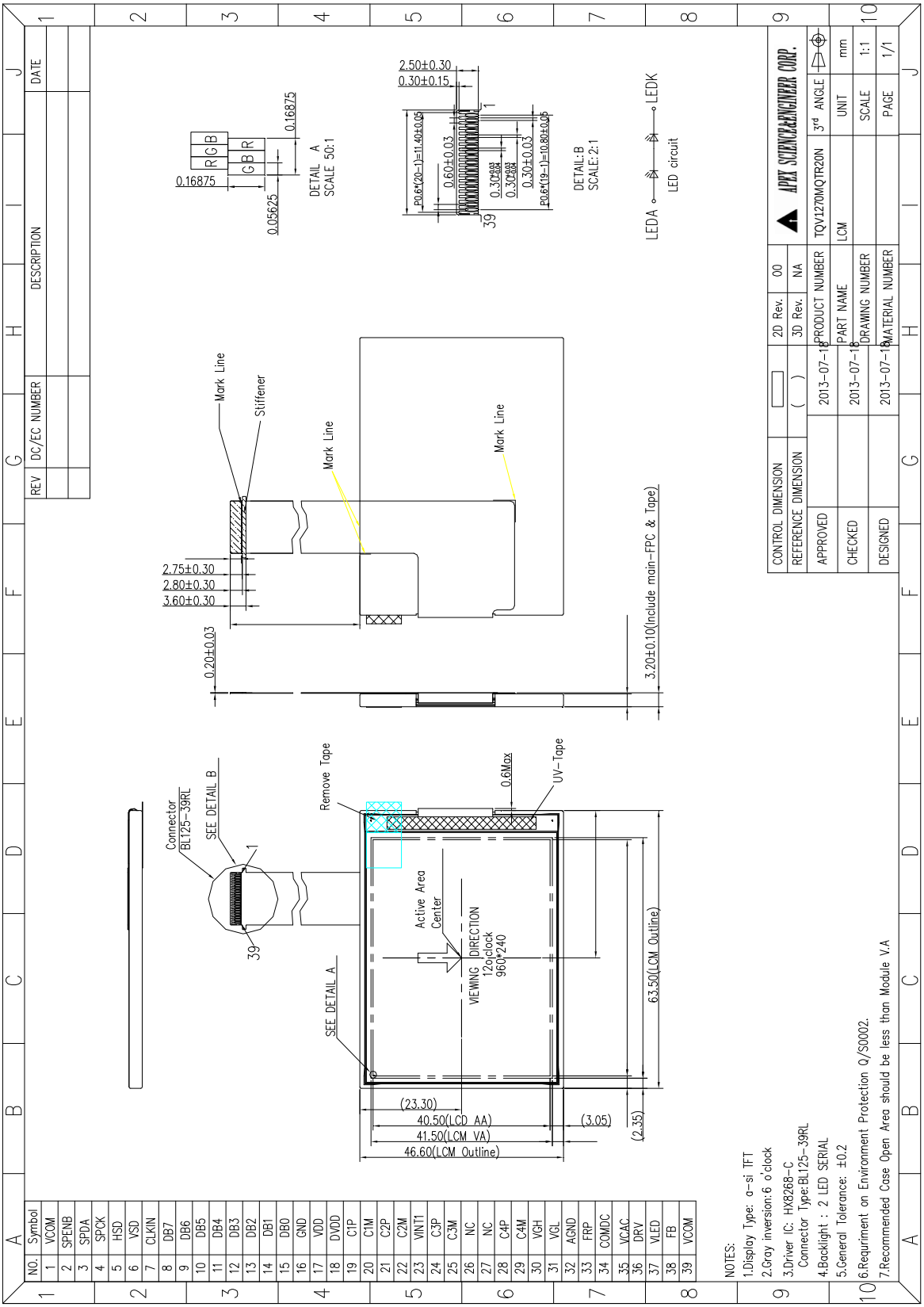
8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts=+70℃, 240hrs	Note1 IEC60068-2-1,GB2423.2
2	Low Temperature Operation	Ta=-20℃, 240hrs	IEC60068-2-1 GB2423.1
3	High Temperature Storage	Ta=+80℃, 240hrs	IEC60068-2-1 GB2423.2
4	Low Temperature Storage	Ta=-30℃, 240hrs	IEC60068-2-1 GB2423.1
5	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH 240 hours	Note2 IEC60068-2-78 GB/T2423.3
6	Thermal Shock (Non-operation)	-30℃ 30 min~+70℃ 30 min, Change time:5min, 20 Cycles	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22
7	Electro Static Discharge (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）	IEC61000-4-2 GB/T17626.2
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)(Package condition)	IEC60068-2-6 GB/T2423.10
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	IEC60068-2-27 GB/T2423.5
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample

9 Mechanical Drawing



10 Packing Drawing

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TQV1270MQTR20N	63.50x46.60x3.0	TBD	378	
2	Tray	PET(Transmit)	485x330x13.8	0.159	24	
3	Dust-proof bag	PE	700x545	0.046	1	
4	BOX	Corrugated paper	520x345x74	0.40	3	
6	Desiccant	Desiccant	45x35	0.002	6	
6	Carton	Corrugated paper	544x365x250	1.01	1	
7	Total Weight(Kg)	TBD Kg				

Packaging Specification and Quantity

(1) LCM quantity per tray: 3row×6column = 18
(2) Total LCM quantity in Carton: No. of PET trays 21 × quantity per tray 18 = 378
Note: Please refer to the data from “estimated report about the dimension and stack of Carton “ about stacking carton

Desiccant * 2

+

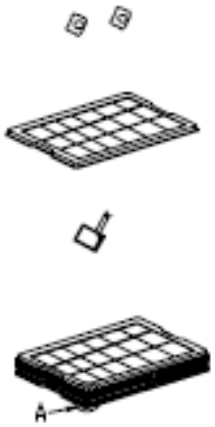
Use empty tray

+

LCM

+

Put products into the 7 trays * 18 LCMS per tray



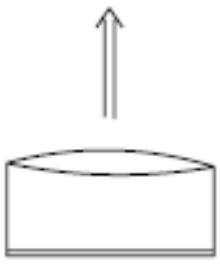
Tie up adhesive tape Tray

Box

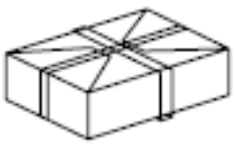
126 LCMS per Box

3 Box

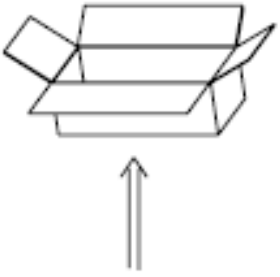
Use package bag 700 * 545mm



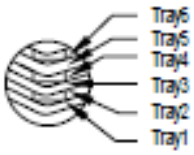
Use packaging tapes to seal the big packing



Put into carton 3*7*18=378 LCMs per carton



The tapes to seal carton



Rotate tray 180 degrees and place on top of stack.
Check the tray using Fig.A.

11 Precautions for Use of LCD Modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1 Be sure to ground the body when handling the LCD Modules.

11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions:

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.