

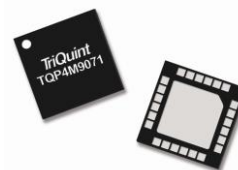
# TQP4M9071

High Linearity 6-Bit, 31.5dB Digital Step Attenuator



## Applications

- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE
- Test Equipments and Sensors
- IF and RF Applications
- General Purpose Wireless

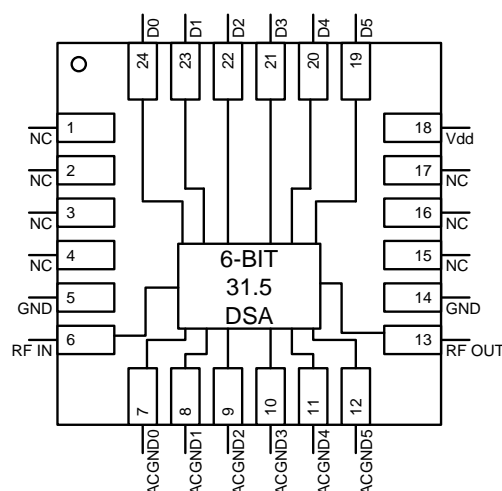


24-pin 4x4mm leadless QFN package

## Product Features

- DC - 4 GHz
- 0.5 dB LSB Steps to 31.5 dB
- +57 dBm Input IP3
- 1.7 dB Insertion Loss @ 2.2 GHz
- TTL / CMOS Compatible Parallel Control Interface
- No requirement for external bypass capacitors for operation above 700 MHz
- 50  $\Omega$  Impedance
- +3.3V or +5V Supply Voltage

## Functional Block Diagram



## General Description

The TQP4M9071 is a high linearity, low insertion loss, 6-bit, 31.5 dB Digital Step Attenuator (DSA) operating over the DC-4 GHz frequency range. The digital step attenuator uses a single positive 3.3V or 5V supply and has a parallel control interface for changing attenuation states. This product maintains high attenuation accuracy over frequency and temperature. No external matching components are needed for the DSA. The product has an added feature of not requiring external AC ground capacitors for operation above 700 MHz.

The TQP4M9071 is available in a standard lead-free /green/RoHS-compliant 24-pin 4x4mm QFN package.

## Pin Configuration

Pin #	Symbol
6	RF_ Input
7, 8, 9, 10, 11, 12	ACGND0-ACGND5
13	RF_Output
18	Vdd
19, 20, 21, 22, 23, 24	Attenuation Control Bits D0-D5
5, 14	Ground
Backside Paddle	Ground
All other pins are N/C	

## Ordering Information

Part No.	Description
TQP4M9071	6-Bit, 31.5 dB DSA
TQP4M9071-PCB_IF	0.04-0.5 GHz Evaluation Board
TQP4M9071-PCB_RF	0.7-3.5GHz Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

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High Linearity 6-Bit, 31.5dB Digital Step Attenuator



## Specifications

### Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power, 50Ω, T = 85°C	+28 dBm
V <sub>dd</sub> , Power Supply Voltage	+7.0 V
V <sub>ctrl</sub> , Control Bit Input Voltage	V <sub>dd</sub> +1V

Operation of this device outside the parameter ranges given above may cause permanent damage.

### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V <sub>dd</sub>	4.75	5	5.25	V
T (case)	-40		85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions: 25°C, V<sub>dd</sub> = +5V, 50Ω system, Mode 1, No external bypass capacitors used on pins 7-12.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range	See Note 1 and 2.	DC		4000	MHz
Insertion Loss	1.0 GHz		1.3		dB
	2.0 GHz		1.6		dB
	2.2 GHz		1.7	2.2	dB
	3.5 GHz		2.1		dB
Return Loss	All States		17		dB
Accuracy Error	0.04-2.7 GHz, All States, Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	0.7-2.7 GHz, All States, Mode 1 or Mode 2	± (0.3 + 3% of Atten. Setting) Max			dB
	2.7-3.5 GHz, All States, Mode 1 or Mode 2	± (0.4 + 4% of Atten. Setting) Max			dB
Attenuation Step	To be monotonic (Step Attenuation ≥ 0)	0	0.5		dB
Input IP3	Input = +15dBm / tone, All States		+57		dBm
Input P0.1dB	All States, DC-4 GHz		+30		dBm
Time <sub>rise / fall</sub>	10% / 90% RF		90		ns
Time <sub>On</sub> , Time <sub>Off</sub>	50% CTL to 10% / 90% RF		100		ns
Supply Voltage, V <sub>dd</sub>	See Note 3.		+5		V
Supply Current, I <sub>dd</sub>			1.4		mA

Notes:

1. In Mode 1 no external bypass capacitors are used and operating frequency is 0.7-4GHz. See page 5 for details.
2. In Mode 2 external bypass capacitors are used and operating frequency may be extended to 0.04-4GHz. See page 6 for details.
3. The product can be operated at lower V<sub>dd</sub> of +3.3V with reduced performance.

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## High Linearity 6-Bit, 31.5dB Digital Step Attenuator



### Control Logic Truth Table

Test conditions: 25°C,  $V_{dd} = +5V$

Control Bits						Attenuation State
D0	D1	D2	D3	D4	D5	
1	1	1	1	1	1	Reference : IL
0	1	1	1	1	1	0.5 dB
1	0	1	1	1	1	1 dB
1	1	0	1	1	1	2 dB
1	1	1	0	1	1	4 dB
1	1	1	1	0	1	8 dB
1	1	1	1	1	0	16 dB
0	0	0	0	0	0	31.5 dB
Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected						

### Control Logic Requirements

Device has six TTL/CMOS compatible parallel control inputs to select attenuation states. Test conditions: 25°C,  $V_{dd} = +5V$ .

Parameter	Conditions	Min	Typical	Max	Units
Low State Input Voltage		0		0.8	V
High State Input Voltage		2		Vdd	V
Low State Current @ 0.8V			5		uA
High State Current @ 5V			50		uA

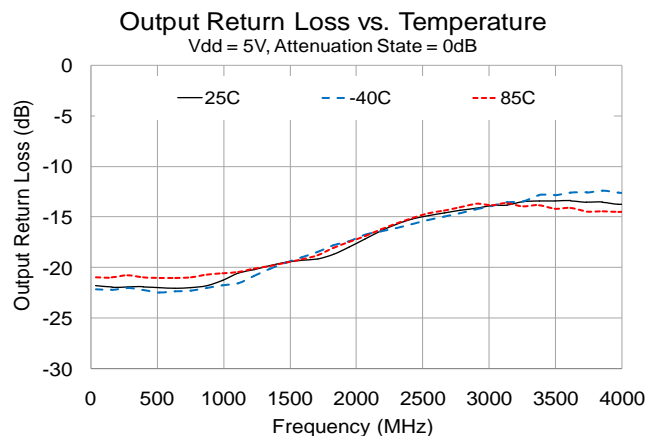
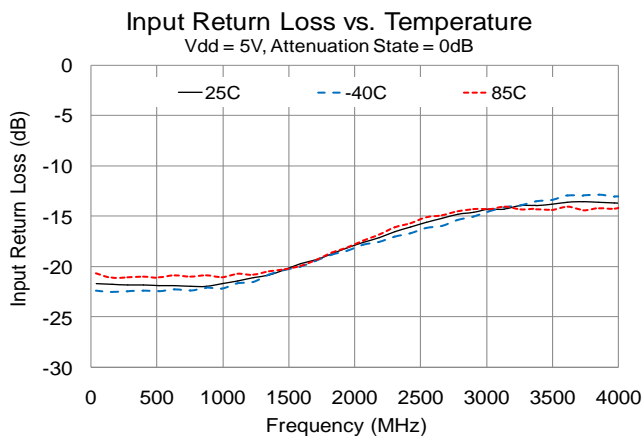
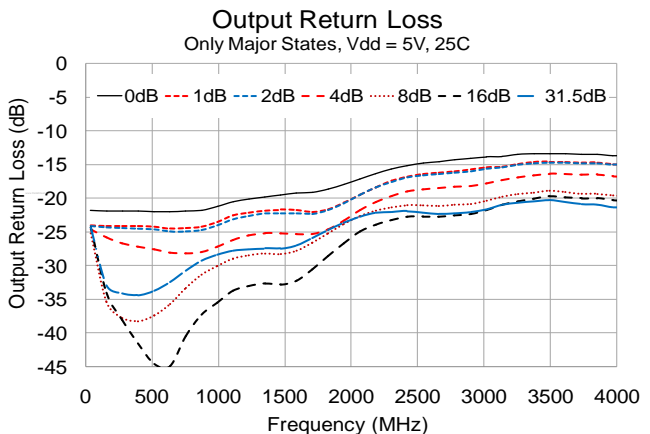
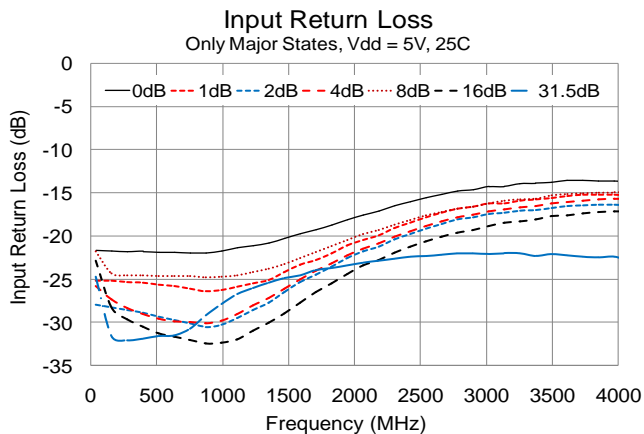
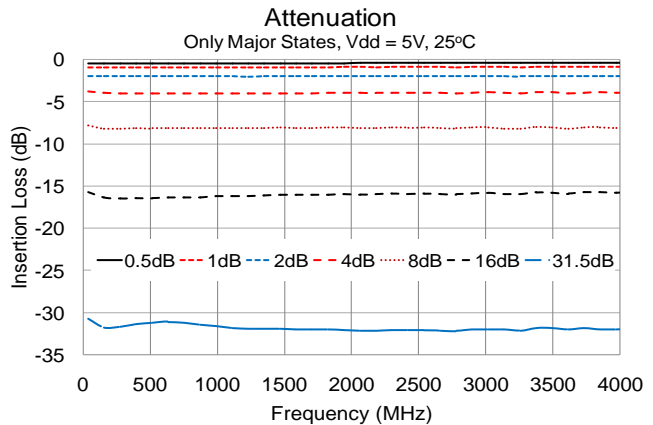
# TQP4M9071

## High Linearity 6-Bit, 31.5dB Digital Step Attenuator



### Typical Performance Data

Performance plots data is measured using Bias Tee on RF ports in Mode 2 configuration. Mode 2 operation is required to obtain performance at frequencies lower than 0.7 GHz. For frequency range 0.7 - 4.0 GHz, data is identical in Mode 1 and Mode 2.

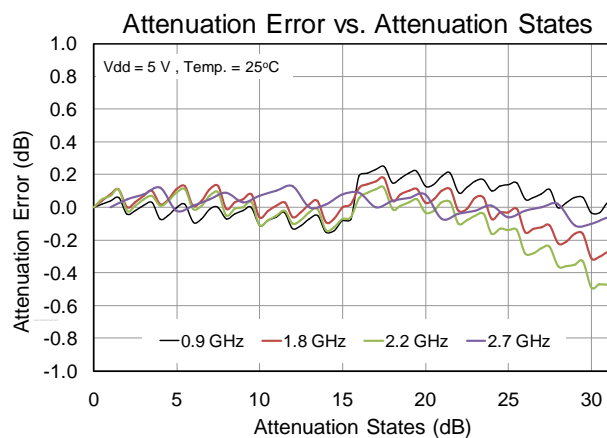
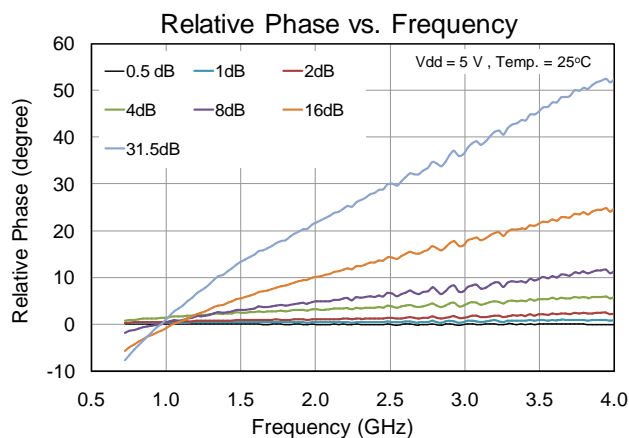
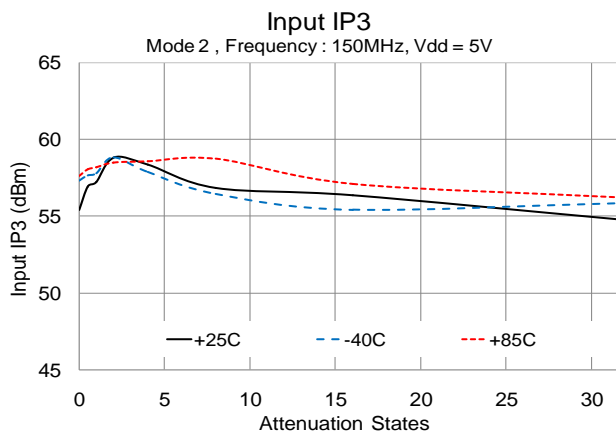
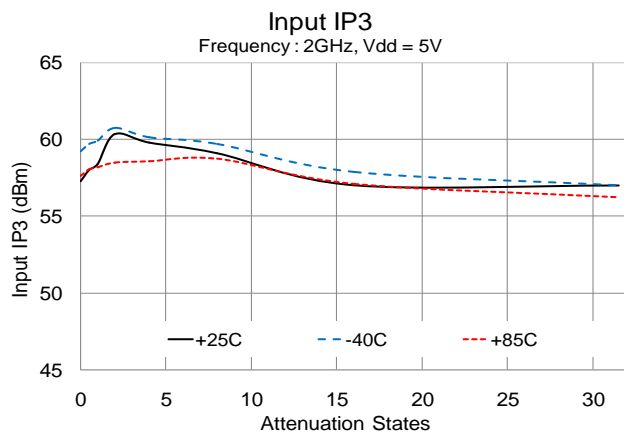


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High Linearity 6-Bit, 31.5dB Digital Step Attenuator



## Typical Performance Data

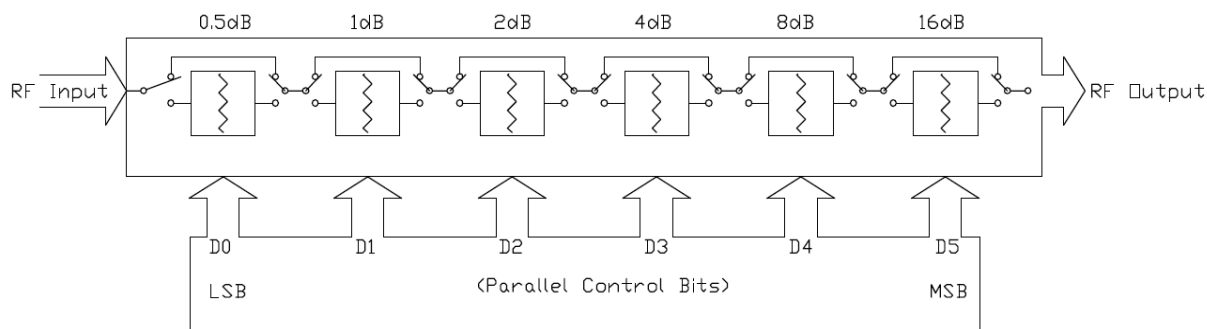


## Detailed Device Description

The TQP4M9071 is a high linearity, low insertion loss, wideband, 6-bit, 31.5 dB digital step attenuator. The digital step attenuator uses a single 3.3V or 5V supply and has a parallel control interface for changing attenuation states. This product maintains high attenuation accuracy over frequency and temperature. The product does not require any external bypass capacitors on AC ground pins for operation above 700 MHz. The DSA performance remains unchanged for frequency range 0.7 – 4 GHz in either Mode 1 or Mode 2. The operating frequency may be extended to low frequency range (0.04 – 0.7 GHz) with external bypass capacitors on AC ground pins (ACGND0-ACGND5).

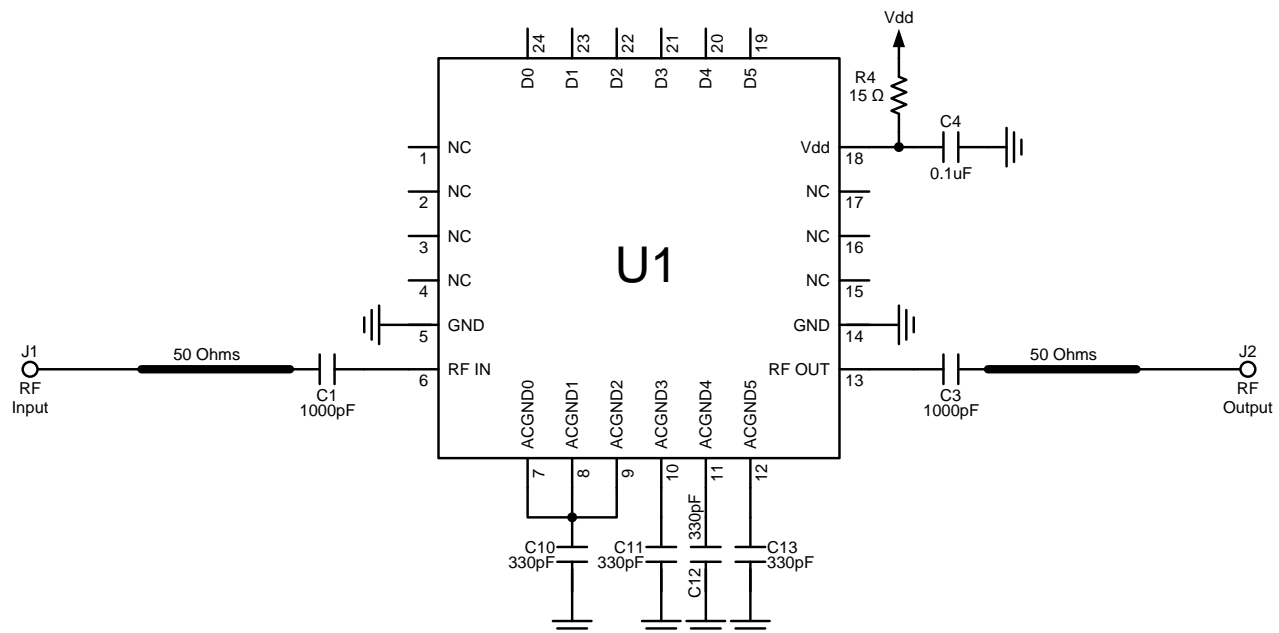
Further assistance may be requested from TriQuint Applications Engineering, [sjapplications.engineering@tqs.com](mailto:sjapplications.engineering@tqs.com).

## Functional Schematic Diagram



## Mode 1: 0.7 – 3.5 GHz Operation (TQP4M9071-PCB\_RF)

No external bypass capacitors required.



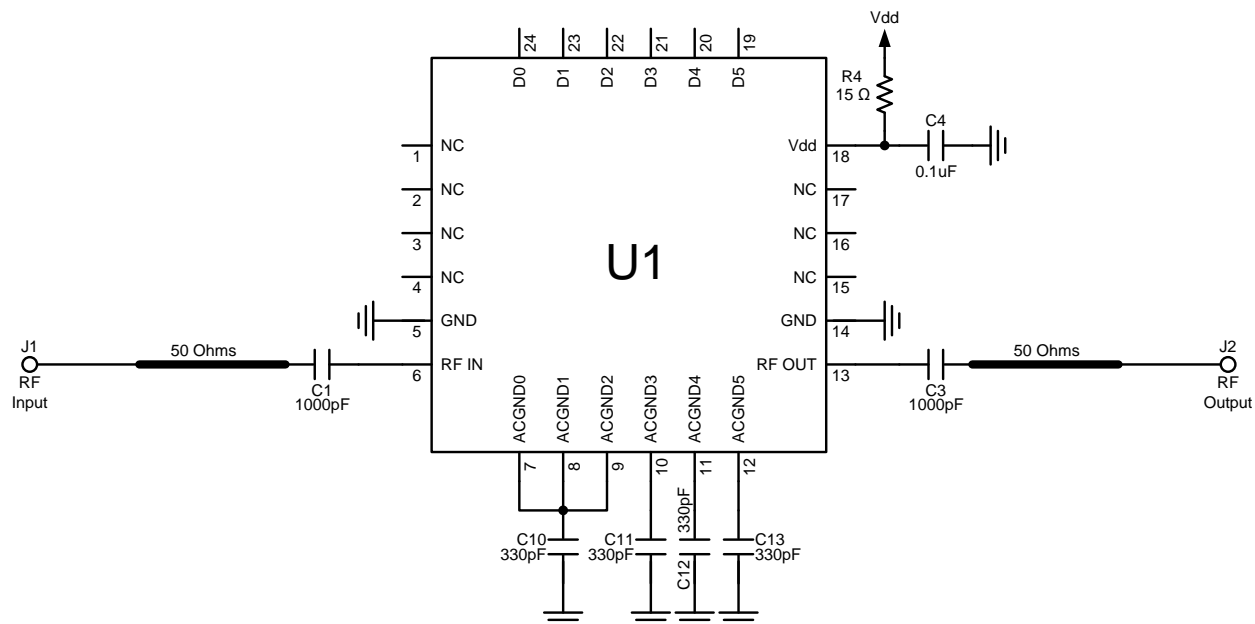
# TQP4M9071

**High Linearity 6-Bit, 31.5dB Digital Step Attenuator**



## Mode 2: 0.04 – 3.5 GHz Operation (TQP4M9071-PCB\_IF)

External bypass capacitors required on ACGND0 - ACGND5 pins. For improved operation below 0.1 GHz, blocking and bypass capacitors values can be increased to 10 nF. This circuit configuration can also be used for operation up to 4 GHz. The DSA performance remains unchanged for frequency range 0.7 – 3.5 GHz in either Mode 1 or Mode 2.

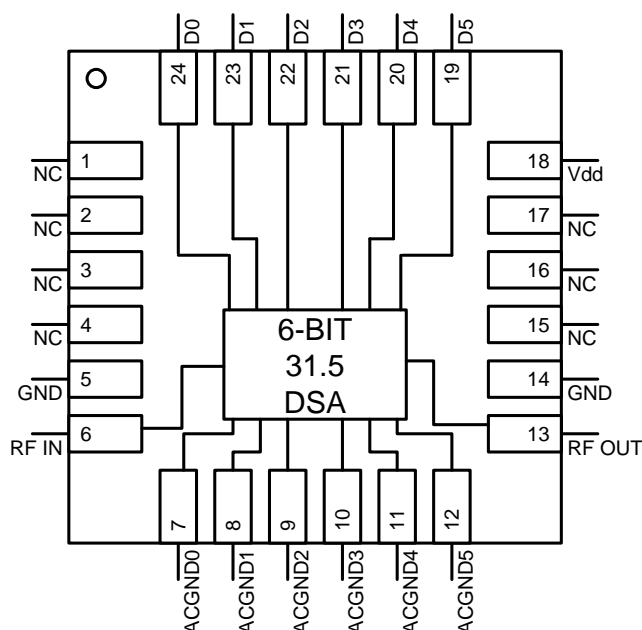


# TQP4M9071

High Linearity 6-Bit, 31.5dB Digital Step Attenuator



## Pin Description



Pin	Symbol	Description
6	RF_IN	RF Input , DC voltage present, blocking capacitor required
7	ACGND0	AC ground for extended low frequency operation option
8	ACGND1	AC ground for extended low frequency operation option
9	ACGND2	AC ground for extended low frequency operation option
10	ACGND3	AC ground for extended low frequency operation option
11	ACGND4	AC ground for extended low frequency operation option
12	ACGND5	AC ground for extended low frequency operation option
13	RF_OUT	RF Output , DC voltage present, blocking capacitor required
18	V <sub>dd</sub>	Supply Voltage, bypass capacitor required close to the pin
19	D5	16 dB attenuation control bit
20	D4	8 dB attenuation control bit
21	D3	4 dB attenuation control bit
22	D2	2 dB attenuation control bit
23	D1	1 dB attenuation control bit
24	D0	0.5 dB attenuation control bit
1, 2, 3, 4, 15, 16, 17	N/C	These pins are not connected internally but can be grounded on the PCB
5, 14	GND	These pins must be connected to RF/DC ground
Backside Paddle	GND	Multiple vias should be employed for proper performance; see page 10 for suggested footprint



# TQP4M9071

## High Linearity 6-Bit, 31.5dB Digital Step Attenuator



### Applications Information

#### PC Board Layout

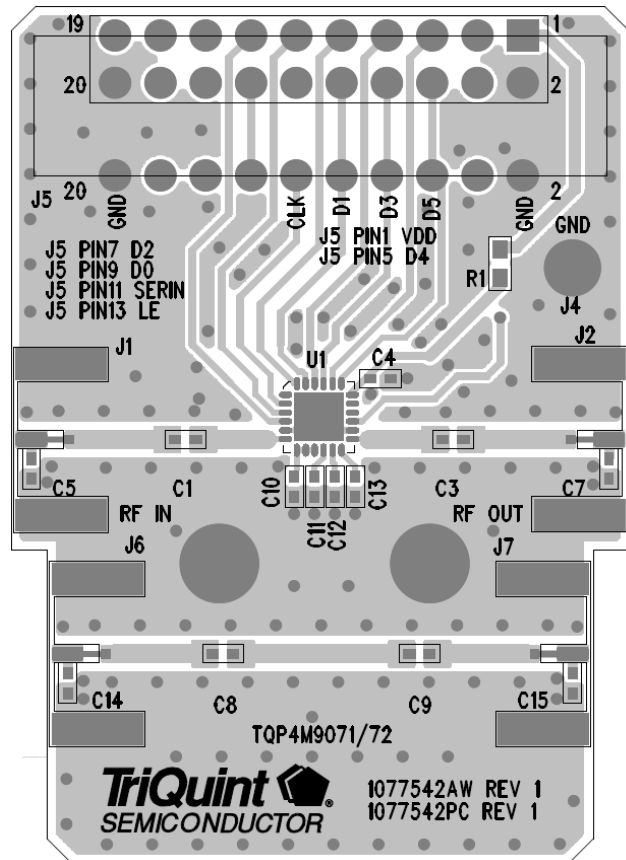
Top RF layer is .020" Rogers-4003,  $\epsilon_r = 3.45$ , 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .040", spacing = .020".

External DC blocking capacitors are required on RFin and RFout pins of the device. The supply voltage for the DSA is supplied externally through pin Vdd. Frequency bypassing for this pin is supplied by surface mount capacitor 0.1 uF (C4). This capacitor is placed close to the device pin in the board layout. To ensure application circuit is compatible with different standard power supplies, 15  $\Omega$  (R1) dropping resistor is highly recommended on Vdd supply line.

RF layout is critical for getting the best performance RF trace impedance needs to be 50 ohm. For measuring the actual device performance on connectorized PC board, input losses due to RF traces need to be subtracted from the data measured through SMA connectors. The calibration microstrip line J6-J7 estimates the PCB insertion loss for removal from the evaluation board measured data. All data shown on the datasheet are de-embedded up to the device input/output pins.

The PC board is designed to test using USB control interface board, Evaluation Board Host (EVH). Each TQP4M9071 evaluation board is supplied with the EVH board, USB cable and EVH graphical user interface (EVH GUI) to change attenuation states. Manual for using EVH and Application note describing the EVH are also available. Refer to TriQuint's website for more information

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



# TQP4M9071

**High Linearity 6-Bit, 31.5dB Digital Step Attenuator**



## Bill of Material: TQP4M9071-PCB\_RF

Reference Desg.	Value	Description	Manufacturer	Part Number
U1		High Linearity 6-Bit, 31.5dB, DSA	TriQuint	TQP4M9071
C4	0.1 uF	Cap, Chip, 0402, 16V, 20%	various	
C1,C3,C8, C9	1000 pF	Cap, Chip, 0402, 50V, 10%	various	
R1	15 $\Omega$	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	DNP	Do Not Place	various	

## Bill of Material: TQP4M9071-PCB\_IF

Reference Desg.	Value	Description	Manufacturer	Part Number
U1		High Linearity 6-Bit, 31.5dB, DSA	TriQuint	TQP4M9071
C4	0.1 uF	Cap, Chip, 0402, 16V, 20%	various	
C1,C3,C8, C9	1000 pF	Cap, Chip, 0402, 50V, 10%	various	
R1	15 $\Omega$	Res, Chip, 0402, 1/16W, 5%	various	
C10, C11, C12, C13	330 pF	Cap, Chip, 0402, 50V, 10%	various	

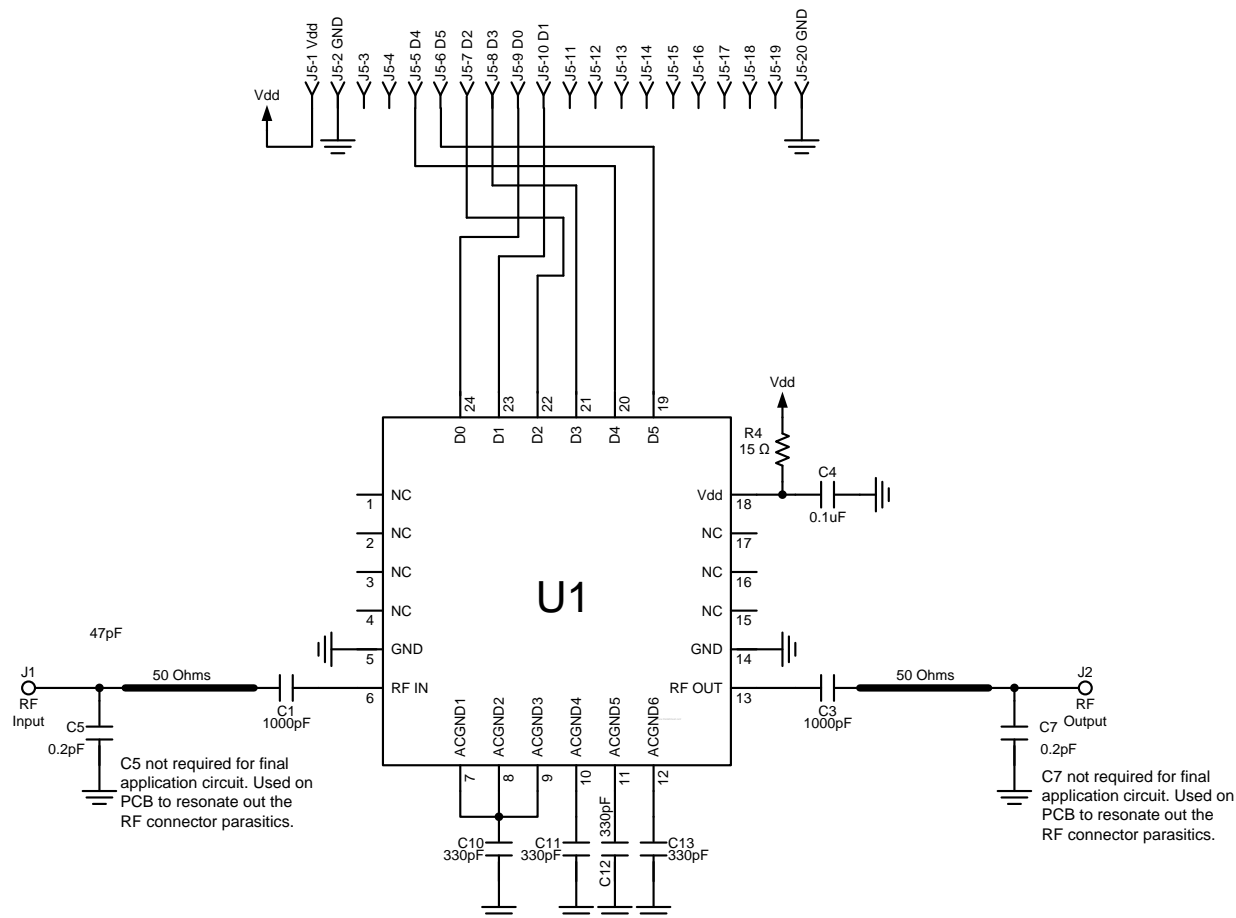
# TQP4M9071

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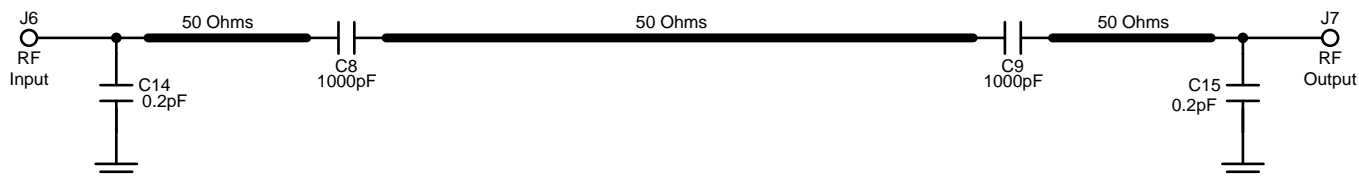


## Applications Information

### PC Board Schematic



### Thru Calibration Line



# TQP4M9071

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## Mechanical Information

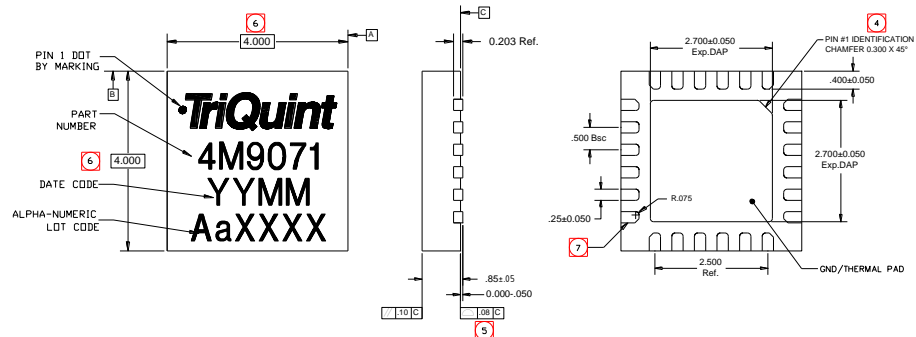
### Package Information and Dimensions

The component will be laser marked with "4M9071" product label with an alphanumeric lot code on the top surface of the package.

#### NOTES:

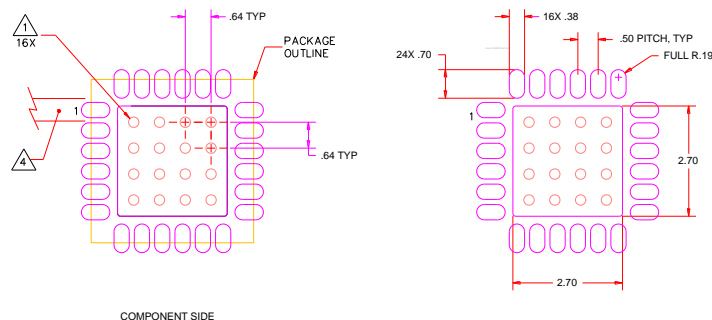
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VGGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JEDEC 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PACKAGE BODY LENGTH/WIDTH DOES NOT INCLUDE PLASTIC FLASH PROTRUSION ACROSS MOLD PARTING LINE.
7. DEVIATION FROM JEDEC STANDARD MO-229, ISSUE C, 12 LEAD COUNT NOT I



### Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



#### NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
5. USE 1 OZ. COPPER MINIMUM.
6. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

#### Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

### Product Compliance Information

#### ESD Information



#### Caution! ESD-Sensitive Device

ESD Rating: Class 1B  
Value: Passes  $\geq 500V$  to  $\leq 1000V$   
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV  
Value: Passes  $\geq 1000 V$   
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101

#### MSL Rating

The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

#### Solderability

This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ( $C_{15}H_{12}Br_4O_2$ ) Free
- PFOS Free
- SVHC Free

### Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: [www.triquint.com](http://www.triquint.com)  
Email: [info-sales@tqs.com](mailto:info-sales@tqs.com)

Tel: +1.503.615.9000  
Fax: +1.503.615.8902

For technical questions and application information:

Email: [sicapplications.engineering@tqs.com](mailto:sicapplications.engineering@tqs.com)

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